Model 1739-Z1D/Z2D/Z3D

U-Port Adapter

INSTRUCTION MANUAL

September, 1994

Model 1739-Z1D/Z2D/Z3D

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KineticSystems Corporation

Standardized Data Acquisition and Control Systems **1730-Series**

Serial Highway Driver Port Options

(Rev. Aug. 89)

FEATURES

- **Bit-serial and byte-serial modes to five megahertz**
- **Conforms to IEEE Standard 595**

APPLICATION

- **Interfaces the 2050-88 and 2160-88 Serial Highway Drivers to the CAMAC Serial Highway via D-Port or U-Port**

GENERAL DESCRIPTION

The 1730-Series of Port Options provides the Models 2050-2088 and 2160-2188 Serial Highway Drivers (SHDs) with a variety of serial transmission schemes. The Defined Port (D-Port) option is generally used for bit-serial or byte-serial data transmission when the transmission distance is relatively short and the common-mode voltage is relatively low. When increased distance, speed, and/or highway isolation is required, a suitable U-Port adapter should be used.

1730 D-PORT ADAPTER

The Model 1730 D-Port Adapter provides for bit-serial or byte-serial operation of the Serial Highway Driver. The clock and data signals conform to those specified for the defined ports in IEEE Standard 595. The D-Port signal levels follow EIA Standard RS-422 and exhibit a 12-volt, common-mode noise immunity. The data rate can be set from 100 kilobits per second to five megabytes per second.

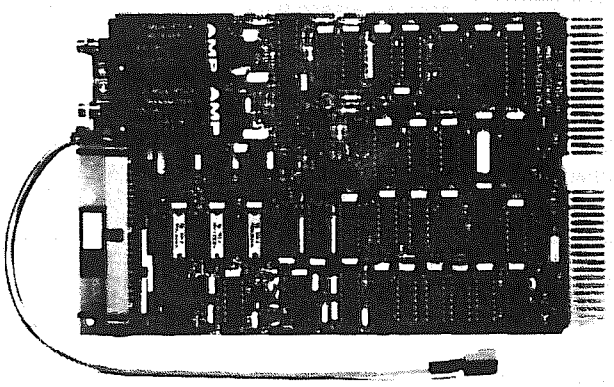
1733 AND 1736 TRANSFORMER-ISOLATED U-PORT ADAPTERS

The Models 1733 and 1736 are bit-serial U-Port Adapters (UPAs) providing a 500-volt, galvanic isolation through transformer coupling and using biphase signal encoding of clock and data over a single twisted pair. In addition to the high common-mode performance, these UPAs generally provide a 60% increase in acceptable loop distance for the same cable conditions and operating speed as a D-Port highway. The operating speed for these UPAs can range from 100 kilobits per second to five megabits per second. The 1733-B1A is arranged for dual-loop operation for systems that require redundant highways. This UPA can be used in the 2050-2088 Serial Highway Drivers. Appropriate versions of the 1736 are used in the 2050-88 Series as well as the 2160-88 Serial Highway Drivers. The companion UPA modules for the 1733 and 1736 are the 3933 and 3936, respectively.

1735 and 1738 FIBER OPTIC U-PORT ADAPTERS

The Models 1735 and 1738 U-Port Adapters (UPAs) use fiber optic cables to provide signal transmission that is immune to electromagnetic interference and does not cause signal radiation. Being a nearly perfect insulator, the fiber optic cable allows operation with a high voltage potential difference between the Serial Highway Driver and the crates on the highway. These UPAs convert the clock and data to a biphase signal that is transmitted optically through the cable.

The 1735 and 1738 are similar bit-serial units that operate at data rates from 100 kilobits per second to five megabits per second, using an optical wavelength of 820 nanometers. The maximum fiber optic cable length from the 1735 or 1738 is two kilometers. Since the limiting factor is optical loss and not data rate, a five megabit per second rate can be achieved up to the two kilometer limit. The 1735 is used in the 2050-2088 SHDs, while the 1738 is used in the 2160-88 SHDs. The companion UPA module for both the 1735 and 1738 is the 3938.



The 1739 U-Port Adapter shown which mounts in the Serial Highway backplane.

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1739 FIBER OPTIC U-PORT ADAPTERS

The 1739 operates in byte-serial mode at highway rates from one to five megabytes per second. This transmission is accomplished over a single fiber by converting each byte to a bit-serial, biphase, signal at a 10X rate (50 megabits/sec for a 5 megabyte/sec highway rate). Options of the 1739, operating at an 820 nanometer wavelength, are available for both the 2050-88 and the 2160-88 Series Serial Highway Drivers. With the appropriate fiber optic cable, each link on the highway can extend to one kilometer (approximately 3,300 feet). Versions of the 1739, operating at a 1300 nanometer wavelength, provide extended performance to three kilometers (approximately 10,000 feet) per link. *These extended-length UPAs are available for the 2160-88 Series only.* Since the distance is limited by the relatively frequency-independent optical loss, the full five megabyte/sec highway rate can be achieved for the one- or three-kilometer limits just discussed.

COMPATIBLE CABLE/UPAs (for 2160-2188 Serial Highway Drivers)

Model	Description	Mating Cable Assembly	Compatible UPA Module
1730	Bit/Byte D-Port	5800-Axyz/5800-Bxyz	None (See Note 1)
1736	Bit-serial cable UPA	5800-Cxyz/5800-Dxyz	3936
1738	Bit-serial FO UPA	5802-Cxyz/5802-Dxyz (See Note 2)	3938, 3954
1739-ZyD	Byte-serial FO UPA (820 nm)	(See Note 3)	3939-Z1A, 3939-Z2A
1739-ZyC	Byte-serial FO UPA (1300 nm)	5802-Exyz/5802-Fxyz (See Note 4)	3939-Z1C

Notes: 1. The 1730 is used for configuring a D-Port highway. It can also be used with other D-Port devices, such as the 2800 Highway Switch
2. The 1738 uses 100 micrometer fiber optic highway cable.
3. The 1739-ZyD operates with 100 micrometer fiber optic highway cable (5802-Cxyz/5802-Dxyz) and all options of the 3939 UPA module. When used with the 3939-Z2A, the following cables can be used: 50 (5802-Exyz), 62.5, 85, and 100 micrometer (provided that the optical loss is less than 5 dB/km).
4. The 1739-ZyC uses 50 or 62.5 micrometer cable with a loss of less than 1.5 dB/km to achieve the bandwidth required for a three kilometer link.

ORDERING INFORMATION (for 2160-2188 Serial Highway Drivers)

Weight: 0.45 kg. (1 lb.)

Description	2160 (Note 2)	2165	2170	2185	2188
Bit/Byte D-Port Adapter	1730-D1B	1730-D2B	1730-D2B	1730-D2B	1730-D1B
Bit-serial U-Port Adapter Twisted-pair cable	1736-B1B	1736-B2B	1736-B2B	1736-B2B	1736-B1B
Bit-serial U-Port Adapter Fiber optic cable, 820 nm	1738-Z1B	1738-Z2B	1738-Z2B	1738-Z2B	1738-Z1B
Byte-serial U-Port Adapter Fiber optic cable, 820 nm	1739-Z1D	1739-Z2D	1739-Z2D	1739-Z2D	1739-Z3D
Byte-serial U-Port Adapter Fiber optic cable, 1300 nm	1739-Z1C	1739-Z2C	1739-Z2C	1739-Z2C	1739-Z3C

Notes: 1. **Caution: Refer to the COMPATIBLE CABLE/UPAs chart above to assure proper system compatibility.**
2. The 2160-Z1A/-Z1B card sets accept a cable from the 1730 D-Port Adapter. The 1736 and 1738 UPAs each include a dual-height card for the Q-bus™ backplane. The 1739 UPA includes two dual-height cards. The +5V current rating is 0.5A for the 1736 and 1738 cards and 2.4A total for the 1739.

ORDERING INFORMATION (for 2050-2088 Serial Highway Drivers)

Weight: 0.45 kg. (1 lb.)

Model	Description	Mating Cable Assembly	Compatible UPA Module
1730-D1A	D-Port interface	5800-Axyz/5800-Bxyz	None (See Note 1)
1733-B1A	Bit-serial U-Port, dual loop	5800-Cxyz/5800-Dxyz	3933
1735-Z1A	Bit-serial U-Port, fiber optic (820 nm)	5802-Cxyz	3938, 3954
1736-B1A	Bit-serial U-Port, transformer	5800-Cxyz/5800-Dxyz	3936
1739-Z1A	Byte-serial U-Port, fiber optic (820 nm)	5802-Cxyz	3939-Z1A, 3939-Z2A

Notes: 1. The 1730 is used for configuring a D-Port highway. It can also be used with other D-Port devices, such as the 2800 Highway Switch
2. The 1730 can operate at strap-selectable rates from 100 kilobits/sec to 5 megabytes/sec; the 1733, 1735, and 1736 can operate from 100 kilobits/sec to 5 megabits/sec; the 1739 can operate from 1 to 5 megabits/sec.

Accessories — Refer to charts above.

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Model 1739-Z1D/Z2D/Z3D

MODEL SUFFIX EXPLANATION

Z1D The Model 1739-Z1D U-Port Adapter is an 820 nm wavelength fiber optic port for the Model 2160 Serial Highway Driver. The 1739-Z1D consists of the D1662 U-Port card, 1739-100 DC-to-DC converter and a 50-pin ribbon cable.

Z2D The Model 1739-Z2D U-Port Adapter is an 820 nm wavelength fiber optic port for the Model 2165, Model 2170 and Model 2185 Serial Highway Drivers. The 1739-Z2D consists of the D1661 U-Port card and a 50-pin ribbon cable which is split on one end and terminated with 26-pin ribbon connectors.

Z3D The Model 1739-Z3D U-Port Adapter is an 820 nm wavelength fiber optic port for the Model 2188 Serial Highway Driver. The 1739-Z3D consists of the D1661 U-Port card and a 50-pin ribbon cable.

INSTALLATION OF MODEL 1739-Z1D

1. The D1662 U-Port card and the 1739-100 DC-to-DC converter card have "GRANT" pass capability and may be inserted into any Q-Bus slot.

2. Connect D-Port cable P3 (50-pin ribbon cable) from the D1662 to the D149 Highway Driver card.

3. Connect power cable P1 (3 conductor cable) which is attached to the D1662 to power card 1739-100.

4. When the Model 1739-Z1D is installed in an equipment box which is external to the host computer, the Fiber-In and Fiber-Out cables are channelled through a slotted panel at the rear of the box.

5. Connect the Fiber-Out cable to the MFBR-1404 Transmitter (marked OUT) and connect the other end of the cable to the FO-IN of the first Model 3939 in the system.

6. Connect the Fiber-In cable to the HFBR-2406 Receiver (marked IN) and connect the other end of this cable to the FO-OUT of the last Model 3939 in the system.

INSTALLATION OF MODEL 1739-Z2D

1. The D1661 may be inserted into any backplane slot.

2. Connect D-Port cable P3 (50/26-pin ribbon cable) with the 50-pin end to the D1661 and the 26-pin connector, which is connected to pin 1 of the 50-pin connector, to the D161 Transmitter card. Connect the other 26-pin connector to the D160 Receiver card.

3. Connect the Fiber Optic cables as in Steps 5 and 6 of the Z1D installation instructions.

INSTALLATION OF MODEL 1739-Z3D

1. The D1661 may be inserted into any backplane slot.

2. Connect D-Port cable P3 (50-pin ribbon cable) from the D1661 to the D164 Highway Driver card.

3. Connect the Fiber Optic cables as in Steps 5 and 6 of the Z1D installation instructions.

POWER REQUIREMENTS

D1661	+5V	1250mA		
1739-100	+5V	1550mA		
D1662	+5V	1250mA	-5V	950mA

PERFORMANCE SPECIFICATIONS

Parameter	Conditions	Min	Typ	Max	Units
Optical Output	50 μm/.21 NA Fiber	-21		-14	dBm
Optical Output	62.5 μm/.29 NA Fiber	-16		-09	dBm
Optical Output	100 μm/.3 NA Fiber	-11		-04	dBm
Output Wavelength			820		
Optical Input	50-100 μm Core Dia. .2 - .3 NA Fiber BER = 10^{-9}	-29		-08	dBm
Dynamic Range		21			dBm
Input Wavelength			820		nm

STRAP OPTIONS

1. Transmitter Data Rate: Selects 1, 2.5 or 5 MHz byte D-Port IN rate.

2. Receiver Data Rate: Selects 1, 2.5 or 5 MHz byte D-Port OUT rate (Normally set the same as Transmitter Data Rate).

3. Transmitter Symmetry: Compensates for transmitter circuit delay variations. This strap is set at the factory and should not need to be moved.

TEST POINTS

TP1	TTL level byte clock in
TP2	DC voltage into the VCO
TP3	TTL level 50 MHz VCO clock
TP4	ECL level data separator clock
TP5	ECL level Manchester data into separator latch
TP6	ECL level Manchester data into transmitter
TP8	Transmitter current amplifier output

Model 1739-Z1D/Z2D/Z3D

ADJUSTMENT PROCEDURE

EQUIPMENT REQUIRED

Tektronix 100 MHz oscilloscope, Model 465B or equivalent
Digital voltmeter
Short length of 5802-E fiber-optic cable

VCO ADJUSTMENT

1. Strap the 1739 for 5 MHz operation.

2. Measure the voltage difference from TP2 to Ground.

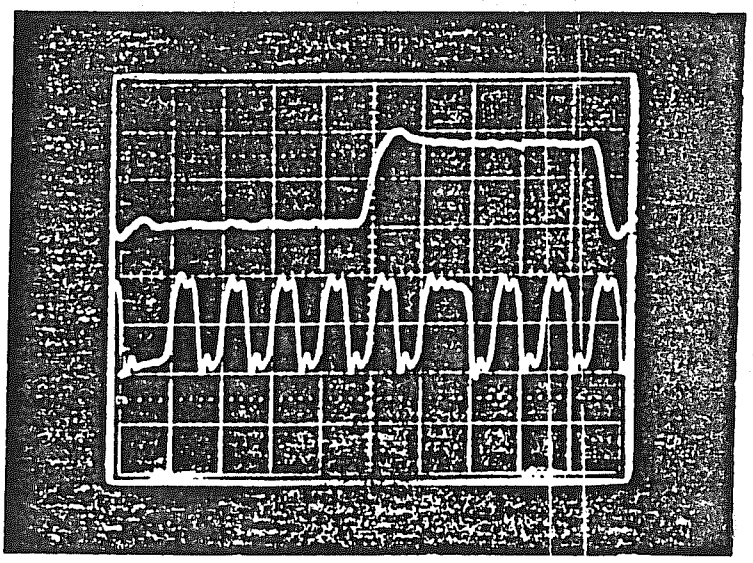
3. Adjust C6 for 2.25 volts ±.05V.

TRANSMITTER SYMMETRY

1. Sync scope on Channel A connected to TP1.

2. With scope Channel B, look at TP6 (transmitter input). See Photo 1.

3. Strap TSYM for equal positive and negative pulses.



BYTE CLOCK
TP1

WAIT BYTE
TP6

20NS/CM
PHOTO 1: WAIT BYTE AT TP6

RECEIVER ADJUSTMENT

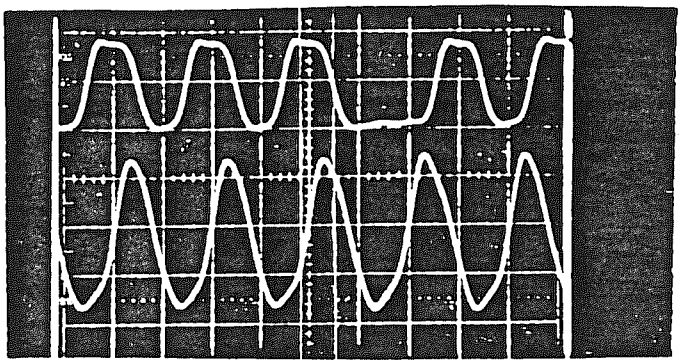
1. Connect FO OUT to FO IN using three (3) meters of 5802E fiber-optic cable.

2. Synchronize the scope EXT input to TP1 (Byte clock).

3. Attach scope Channel A to TP5 (Biphase data).

4. Attach scope Channel B to TP4 (Clock).

5. With the 1739 strapped for 5M byte operation and the scope time-base set at .1 μS x 10, adjust C52 to center the positive transition of the clock within the second half of the data cell time (See Photo 2).

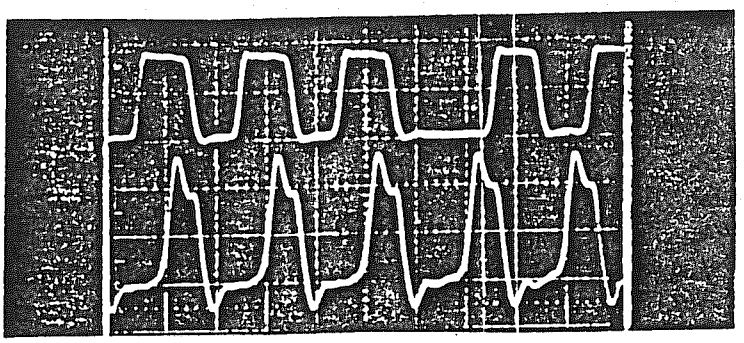


BIPHASE DATA
TP5

CLOCK
TP4

10NS/CM
PHOTO 2: 5M BYTE OPERATION

6. Strap the 1739 and Highway Driver for 2.5M byte and check that the positive clock transition is approximately centered within the second half of the data cell (See Photo 3). C52 may be adjusted slightly but 5M byte operation must then be rechecked.



BIPHASE DATA
TP5

CLOCK
TP4

20NS/CM
PHOTO 3: 2.5M BYTE OPERATION

7. Strap the 1739 and Driver for 1M byte and again check for proper clock alignment. Do not adjust C52.

The 1739 is now adjusted for proper operation at all three (3) of its operating frequencies.

TRANSMITTER SECTION

The transmitter section of the 1739 Fiber-Optic U-Port converts the 8-bit byte data from the D-Port IN, to 10-bit serial biphase data, and outputs this data through the FO OUT connector at ten times the byte clock frequency.

The transmitter section consists of four main parts:

1. The clock/counter.
2. The parallel to serial converter.
3. The NRZ to Manchester (Biphase) encoder.
4. The Fiber-Optic transmitter.

CLOCK/COUNTER

The fiber-optic transmitter clock is required to be ten times the frequency of the D-Port IN byte clock and must be locked to the D-Port clock. A basic phase-locked loop (Figure 1) is used in the 1739 to fulfill this requirement. When operating properly, it will acquire lock-on to the incoming byte clock, track it in frequency, and exhibit a fixed-phase relationship relative to the byte clock.

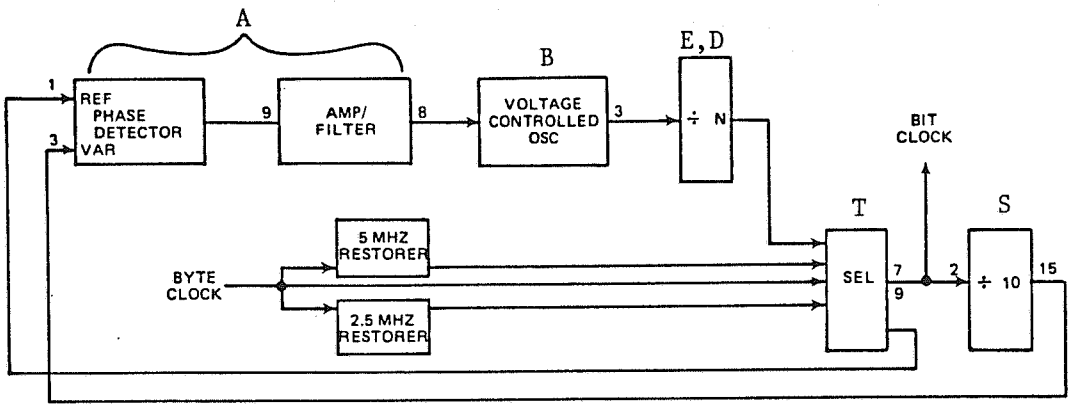


Figure 1

The loop consists of a phase detector, amplifier/filter (chip "A"), voltage-controlled oscillator (chip "B"), and counters (chips "D", "E", "S") which reduce the VCO 50 MHz to the byte clock frequency. This circuitry appears and acts like a unity gain feedback loop. The controlled variable is phase; any error between byte clock frequency and bit clock frequency ÷ N is amplified and applied to the VCO in a corrective direction.

Clock selector "T" selects one of three (3) operating frequencies. Chip"T" pin 7 outputs the bit clock which is 10X the byte frequency. The output of decade counter "S" and differential amplifier "K" pin 11 are fed into phase-detector "A". Chip "A" MC4044 consist of a phase-detector, a charge pump, and an amplifier. When all the negative transitions on R, the reference input, and V, the feedback input coincide, phase lockup occurs. When lockup occurs, both outputs U1 and D1 remain high. The circuit responds only to transitions and not to input waveform duty cycle. If R leads V, output U1 pulses while output D1 remains high. When PU is low (pulsing) and PD is high, the DC voltage, at the amplifier output pin 8, will rise. If V leads R, the reverse is true.

The phase detector amplifier output is fed into varactor diode CR3. CR3, a .22 μH choke and trimmer capacitor C6 form a resonant tank which controls the output frequency of oscillator "B". As the phase detector increases its DC output voltage, the capacitance of varactor diode CR3 decreases resulting in an increase in the resonant tank and VCO output frequency. Ship "C" MC10125 converts the ECL output of oscillator "B" to TTL levels for clocking the ÷ N counters.

PARALLEL TO SERIAL CONVERTER

When decade counter "S" overflows, pin 15 goes to a high logic level which produces the feedback signal to the phase detector and also the load signal to the parallel to serial converter chip "U". When "U" pin 19 is high, byte data from the D-Port receivers is loaded into "U" on the positive edge of the bit clock pin 12. With the load pulse high the same clock pulse which loads "U" also clears "H". The clearing of "H" produces the start-bit for the next byte of data to be shifted out. During the next 9 bit clocks, the 8 bits of data previously loaded into "U", and a stop-bit shifted into "U" because pin 11 is held high, are shifted through "H" and into TTL to ECL level converter "Q".

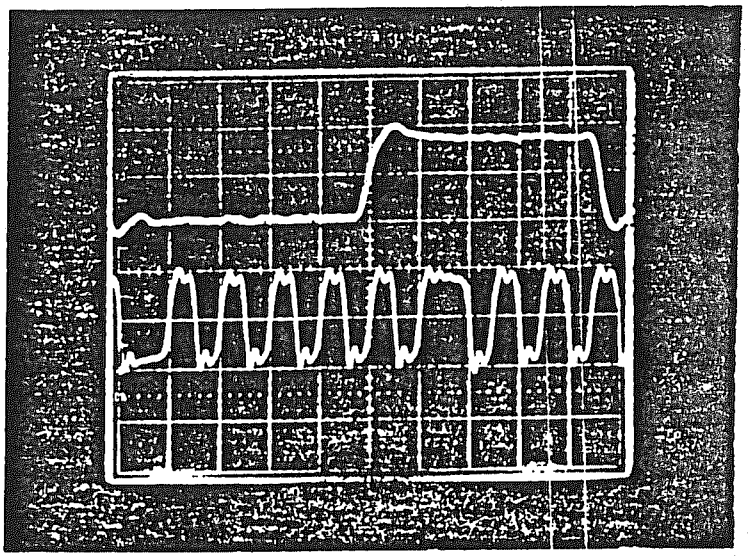
NRZ TO MANCHESTER ENCODER

NRZ data from converter "Q" goes directly to the data inputs of storage register chip "P". The data on the inputs to "P" is transferred to the Q outputs on the positive edge of the bit clock signal from level converter "Q". During the low portion of the clock signal, the state of register "P" is reversed by the outputs of gates "N".

TRANSMITTER

The output of storage register "P" through gate "Z" drives the differential inputs of the fiber-optic transmitter. The transmitter is capable of outputing approximately 10 μW (-20dBm) into a 50 μm cable and 100 μW (-10dBm) into a 100 μm cable.

TP6 TRANSMITTER INPUT



20NS/CM
PHOTO 4: WAIT BYTE AT TP6

A zero-bit at TP6, the transmitter input test point, has a positive transition in the center of the bit cell time. A one-bit has a negative transition at the center of its cell time; therefore, the second half of a zero-bit cell time is always positive and the second half of a one-bit cell time is always negative (See Photo 4).

RECEIVER SECTION

The receiver section of the Model 1739 Fiber Optic U-Port converts light impulses received at the FO IN connector to a biphase voltage signal, separates this signal into 10-bit NRZ data an clock signals, frames it into 8-bit data bytes, and along with a byte clock, outputs it to the D-Port OUT connector P3.

The receiver section consists of four main parts:

1. Fiber-Optic Receiver.
2. The data separator.
3. The sync circuitry.
4. The serial to parallel converter.

FIBER OPTIC RECEIVER

Light from the optical fiber is converted to a differential ECL voltage by the receiver module. The receiver has an input sensitivity range of 1.2 μW (-29 dBm) to 150 μW (-8 dBm).

DATA SEPARATOR

The biphase data from the receiver module goes to dual-edge detector chip "AG" which produces approximately 5 nanosecond pulses into "AND" gate "AH". The output of "AND" gate "AH" triggers monostable multivibrator "AF". Capacitor C52 is used to adjust the timing of one-shot "AF. Capacitor C52 is used to adjust the timing of one-shot "AF" to give the correct clock/data phase relationship at the input to latch "AA". The ECL output of latch "AA" (separated NRZ data) and one-shop "AE" (NRZ clock) are converted to TTL levels by chip "AJ".

SYNC CIRCUITRY

The sync circuitry will be explained with the use of schematic D5541, the 1739 byte sync timing diagram shown on page 11, and the listing for PROM "AD" (See page 12) of this manual.

Chips "AE", "AK", "AD", and associated gates, form a state machine which controls the framing of bit-serial data into byte-serial data. This state machine also produces a byte clock and a no-sync signal. The state machine may power up at any address (0-31). When clocks are produced as a result of incoming data, the sequencer will find a sync error and go to address 0. Chip "AK" is then cleared (pin 9 low) and further clocking is inhibited. The sequencer now waits for a "START" bit. A "START" bit follows the only negative transition in an NRZ wait-byte. Upon receiving this transition, "AK" pin 9 is set high and "AK" pin 6, along with gate "AB", produce half frequency sequencer clocks (B1-B5). Keeping in mind a wait-byte consists of six zeros followed by four ones, the sequencer must now find this pattern before byte sync can be established. As address register "AE" is clocked, incoming NRZ data is used as address bit 0 of PROM "AD". One can see from the PROM listing and byte sync timing diagram that if incoming data is in the wrong state for a given clock pulse the sequencer goes to address 0 and the process begins anew.

Once byte sync has been established, it is maintained by checking only the "STOP" bit.

If sync is maintained, a byte clock is produced at ship "AE" pin 10 and the no-sync signal to timer chip "J" goes away.

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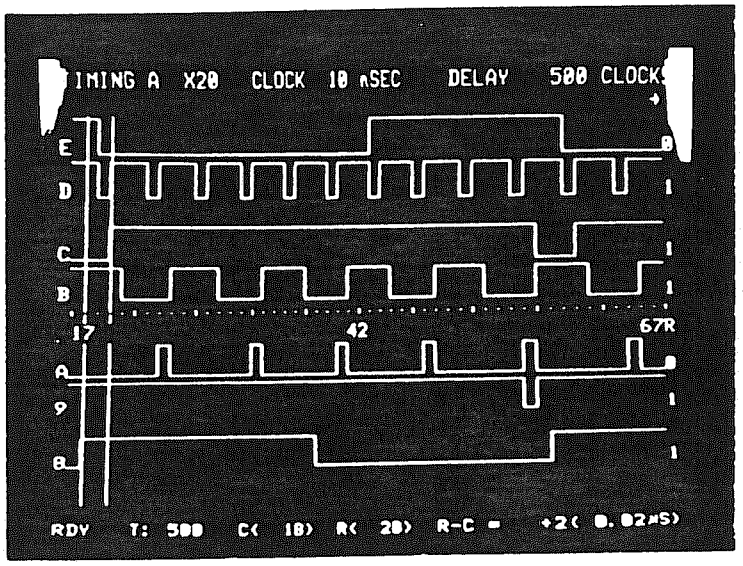
SERIAL TO PARALLEL CONVERTER

Shift register "AM" stores the incoming serial NRZ data stream. The sequencer PROM "AD" pin 9, and signal B5, clocks register "AN" when the 8 bits of byte data are positioned properly within shift register "AM". Data from register "AN" and the byte clock are presented at the D-OUT connector P3 by differential drivers "W", "X", and "Y".

1739 BYTE SYNC TIMING DIAGRAM



E NRZ wait-byte at "AE" pin 6.

D Clock at "AL pin 2.

C "AK" pin 9.

B "AK" pin 6.

A B1 through B5 at "AE" pin 9.

9 Clear to chip "AK".

8 Byte clock out a "Y" pin 1.

Model 1739-Z1D/Z2D/Z3D

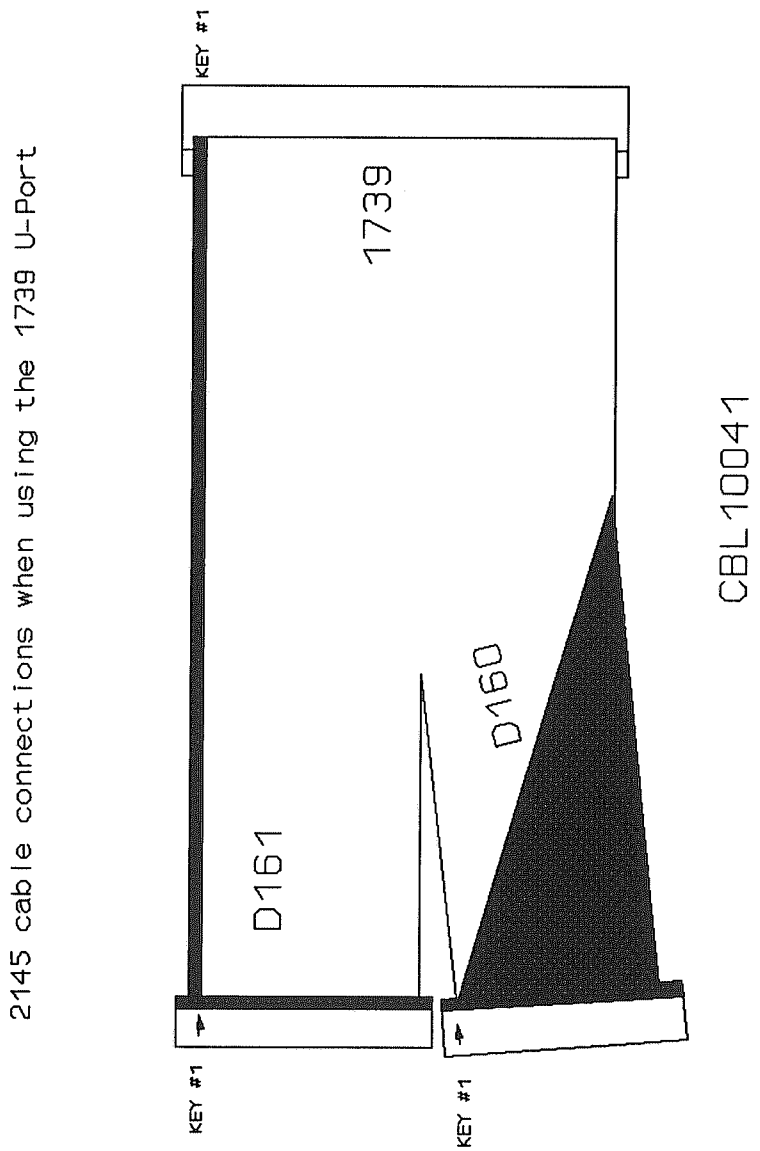
Files copied:
DX1:PROM39.DAT to TT:

1739 BYTE SYNC PROM

I.C. LOCATION "AD" 10-JAN-85

AAAAA 43210	HEX	QQQQQQQQ 76543210	COMMENT	B-SIG.
0-00000	01	00000001	START WAIT	B1
1-00001	01	00000001	BYTE SEQ	B1
2-00010	02	00000010	1ST "0"	B2
3-00011	C0	11000000	RETURN	B2
4-00100	03	00000011	2ND "0"	B3
5-00101	C0	11000000	RETURN	B3
6-00110	04	00000100	3RD "0"	B4
7-00111	C0	11000000	RETURN	B4
8-01000	C0	11000000	RETURN	B5
9-01001	85	10000101	1ST "1"	B5
10-01010	C0	11000000	RETURN	B1
11-01011	06	00000110	2ND "1"	B1
12-01100	37	00110111	NORMAL	B2
13-01101	37	00110111	SYNC	B2
14-01110	38	00111000	OPERATING	B3
15-01111	38	00111000	RANGE	B3
16-10000	39	00111001	"	B4
17-10001	39	00111001	"	B4
18-10010	AA	10101010	"	B5
19-10011	AA	10101010	"	B5
20-10100	E0	11100000	RET.STOP=0	B1
21-10101	26	00100110	NEXT BYTE	B1
22-10110	C0	11000000	NOT USED GO TO START	
23-10111	C0	11000000	"	
24-11000	C0	11000000	"	
25-11001	C0	11000000	"	
26-11010	C0	11000000	"	
27-11011	C0	11000000	"	
28-11100	C0	11000000	"	
29-11101	C0	11000000	"	
30-11110	C0	11000000	"	
31-11111	C0	11000000	"	

```
        !        !!!!!!!!
NRZ DATA         !!!!!!!A1
                 !!!!!!A2
                 !!!!!A3
                 !!!!A4
                 !!!BYTE CLOCK
                 !!NO-SYNC
                 !CLEAR "M"
                 CLEAR "C"
    ACTIVE:---HHLLHHHH
```


2145 cable connections when using the 1739 U-Port
KEY #1
1739
D161
D160
CBL10041
KEY #1
KEY #1