Model 2140-Z1A

Enhanced Serial Highway Driver for
VMEbus Systems

INSTRUCTION MANUAL

November, 2002

CONTENTS

FIGURES

CHARTS

VME bus Enhanced Serial Highway Driver

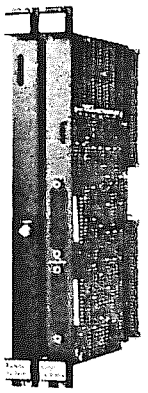
Allows a computer VME bus to host a Serial Highway — 2140

Features

- **Provides a dedicated VME bus interface to the CAMAC serial highway**
- **Supports the Enhanced highway mode with throughput of 3 Mbytes/s**
- **Conforms to VMEbus specification (IEEE Standard 1014)**
- **High-speed hardware list processing**
- **Available with software-selectable byte-packing between 24-bit CAMAC and 32-bit VME words**
- **Available with CAMAC-standard D-port connectors or fiber optic adapter**
- **Up to three kilometers between highway nodes at full throughput using fiber-optic transmission**
- **Supports up to 62 nodes**

Typical Applications

- **Distributed data acquisition and control**
- **Systems requiring high throughput with minimum software overhead**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 2140 Serial Highway Driver (SHD) is implemented on two double-Eurocard form-factor printed circuit boards. As a VMEbus master, the 2140 is capable of VME burst transfer rates of greater than four Mbytes/s. Two data FIFOs, one for read data and one for write data, are used to buffer burst transfers between the 2140 and the VMEbus back plane. The size of the transfer burst is programmable up to 256 transfers.

As a slave, the 2140 uses VME short (16-bit) I/O address space for on-board register access. The base address is switch-selectable on 256-byte boundaries. Interrupts for "Operation Complete" and "CAMAC Demand Message" sources are provided. The interrupt levels and vectors used with these sources are fully programmable from the VMEbus.

The 2140 SHD operates with Serial Highway clock rates to five megahertz and supports up to 62 remote CAMAC crates for distributed data acquisition and control. It includes a block-data "enhancement" to the Serial Highway that provides DMA data throughput at rates up to three Mbytes/s.

The CAMAC Serial Highway protocol, as specified by IEEE Standard 595, provides for one CAMAC 24-bit Dataway operation per Serial Highway message. The highway block-mode enhancement contained in the 2140 uses a pipeline approach and allows multiple Dataway operations to occur within one highway message, giving a DMA data throughput rate that is greater than five 5 times the rate of non-enhanced SHDs.

Highway Options

The 2140 operates in bit-serial mode to five megabits per second or byte-serial mode to five Mbytes/s. It is available with the standard D-Port highway connectors or self-contained fiber optic U-Port adapters. Regardless of the port option chosen, the 2140 maintains the two-card VME profile. The 1740 D-Port or 1749 U-Port adapters are provided on separate PC card assemblies and must be ordered to form a complete Serial Highway Driver. When ordered together, the SHD with port adapter is assembled as a unit at the factory.

List Processing

Full three megabyte data throughput is obtained for single-NAF block transfers between the VME backplane and a single CAMAC module. Operation can be extended to multi-NAF scan operations by using the 3830 List Sequencer module in remote crates. This module stores up to four NAF lists and operates with the enhanced highway protocol. A Command List Processor is included in the 2140 Highway Driver. This List Processor contains an 8K x 32 RAM memory and supports a large number of lists. Multiple block transfers can be included in a list.

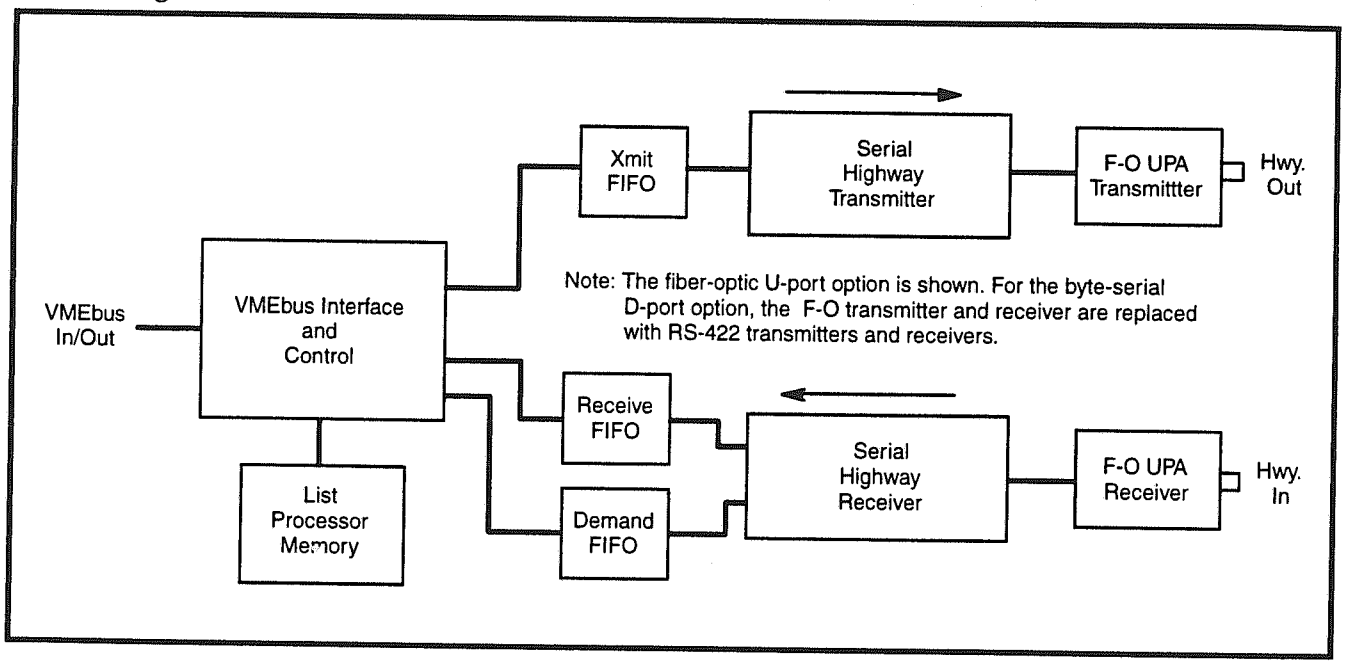
Byte Packing

The 2140 contains two software-selected byte-packing modes: Standard and Special. In "Standard" mode, each 24-bit CAMAC transfer is packed into a 32-bit VME word with the most-significant byte filled with ones. Also in this mode, two 16-bit CAMAC transfers are packed into one 32-bit VME word. "Special" mode supports only 24-bit CAMAC transfers, with four 24-bit CAMAC words packed into three 32-bit VME words. This mode supports certain CAMAC modules that are byte packed to increase highway throughput, such as the 3195-E1A DAC module and the 3595-E1A ADC module. Standard or Special mode is selected on a command-by-command basis in the Command Memory.

Highway Compatibility

In addition to the Enhanced Mode, the 2140 includes software-selected operating modes for Q-Stop, Ignore Q, and Wait-until-Q block transfers, making it usable with any Type L-2 serial crate controller (SCC) meeting the specifications of IEEE-595. Enhanced-mode messages require use of the 3952-Z1E or 3952-Z1F Enhanced L-2 SCCs. The compatibility of the enhanced protocol allows "Standard" and "Enhanced" L-2 SCCs to be mixed on the same highway, provided that the software directs enhanced block messages only to the "Enhanced" SCCs.

Block Diagram



Ordering Information

Model 2140-Z1A Enhanced Serial Highway Driver, for VMEbus host

Note: A 1740 D-port or 1749 U-port Adapter must also be ordered to form a complete Serial Highway Driver.

Associated Products

Model 1740-D1A	D-port Interface, bit-serial & byte-serial, for model 2140
Model 1749-Z1A	U-port Adapter, byte-serial, fiber optic, 820 nm, for model 2140
Model 3830-Z1A	List Sequencer for 3952 Serial Crate Controllers
Model 3939-Z1C	U-port Adapter, byte-serial, fiberoptic, 1300 nm operation
Model 3939-Z2A	U-port Adapter, byte-serial, fiberoptic, 1300 nm operation
Model 3952-Z1G	Enhanced Serial Crate Controller, type L-2, with standard relays
Model 3952-Z1H	Enhanced Serial Crate Controller, type L-2, with high-gauss relays

UNPACKING AND INSTALLATION

The Model 2140 Serial Highway Driver (SHD) is implemented on two VME "B" size modules and shipped in antistatic bags within styrofoam packing containers. Carefully remove the modules from their static-proof bags and set the various options to conform to the operating environment. The default settings on the 2140 are as follows:

1. Base address is set of $80000000 HEX
2. VME Bus Request is set to level three.
3. Highway speed is 5 MHz, byte.
4. Q-Repeat timeout is set to 15 seconds.
5. Spare byte is set to variable.

Refer to the section on Switch and Strap Selection (page 3) for more details of the various option settings.

The 2140 requires both P1 and P2 VME backplane connectors. The VME slot in which the 2140 Receiver module will reside, requires the Bus Request (BR) and Interrupt Acknowledge (IACK) straps to be removed for proper VMEbus operation. Any empty slots between the 2140 Receiver card and slot one should have their BR and IACK straps loaded. The 2140 Receiver and Transmitter cards are connected through Row A and Row C pins of the P2 connector. A jumper cable is provided for this connection. Install the jumper cable on the VME card cage backplane. Note that the Receiver and Transmitter card must occupy adjacent slots.

SWITCH AND STRAP SELECTIONS

Device Address Selection

The 2140 is shipped from the factory to reside in the extended address space of the VMEbus and responds to Address Modifier Codes (09, 0A, 0D, 0E HEX). The switches SA31 through SA08 determine the base address of the 2140. The 2140 must allocate 256 byte locations in the VMEbus.

WHEN SELECTING A BASE ADDRESS, CARE SHOULD BE TAKEN TO AVOID ADDRESSES ASSIGNED TO OTHER DEVICES.

The bit pattern for the base address is shown below:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SA31	SA30	SA29	SA28	SA27	SA26	SA25	SA24	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SA15	SA14	SA13	SA12	SA11	SA10	SA09	SA08	0	0	0	0	0	0	0	0

Bits 31 through 08 are user selectable via the address switches SA31-SA08.
Bits 07 through 00 are set to "0" to indicate a block of 256 bytes.
Refer to Figure 1 (page 5) for switch location and switch settings.

Upon request the 2140 can be used in the standard (A24) or short I/O (A16) address space of the VMEbus. A PROM in location U35 must be changed to recognize the proper Address Modifier Codes. For standard addressing, the 2140 will respond to 39, 3A, 3D, 3E HEX; while

in short I/O addressing, the 2140 will respond to 29 and 2D HEX. Strap positions C, D, E and F change settings. In standard addressing mode, switch SW4 is not used, while in short I/O addressing, switches SW4 and SW3 are not used.

VMEbus Grant Selection

The 2140 can be selected for all four Bus Request (BR) settings. The 2140 uses the BR signals to become a VME master for DMA operations. The BR straps on the VME backplane need to be removed from the slot that the 2140 Receiver occupies. The default setting is BR #3. Refer to Figure 1 (page 5) for location of Bus Request straps and settings.

Figure 1 (page 5) shows the 2140 Receiver card strap locations for Bus Grant In, Bus Grant Out, Q-Repeat timeout and Auto-Trigger timer speed selections.

Bus Request is shown at level 3. BGI0 through BGI2 are shown jumpered to BGO0 through BGO2. Q-Repeat timeout is strapped to 15 seconds. The Auto-Trigger straps are removed. See the Auto-Trigger Speed Chart for trigger speed selection. Figure 1 (page 5) also shows the Base Address switches SW1, SW3 and SW4 set to $80000000 HEX.

Highway Speed Selection (D-Port Only)

The 2140 can transmit serial highway bytes of information in either the bit-serial or byte-serial mode. In bit-serial mode, the bytes are transmitted using one data signal and an accompanying bit-clock signal. The eight-bit byte is transmitted with the least significant bit first. It is preceded by a Start bit (logic 0) and followed by a Stop bit (logic 1).

In the byte-serial mode, the bytes are transmitted using eight data signals and an accompanying byte-clock signal. The byte-serial mode increases serial highway data throughput by a factor of ten. A front panel switch selection, on the D-Port option, allows the user to select either bit-serial or byte-serial highway modes. The user also has the ability to select a clock frequency at which the serial highway is to operate. Five D-Port highway frequencies are front-panel switch selectable.

The following chart shows the positions of the switches necessary to obtain the desired serial highway operating mode and speed.

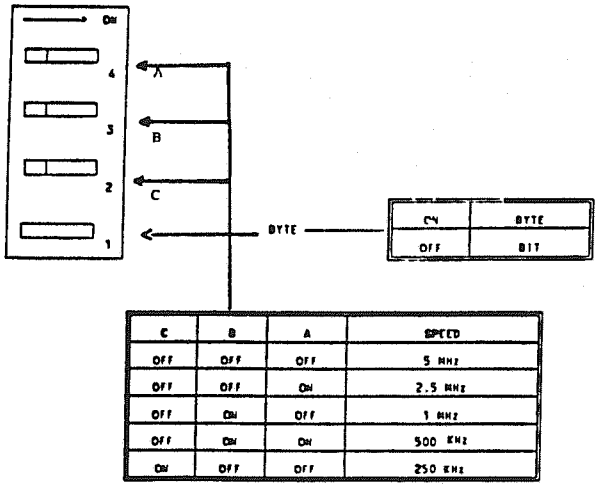


CHART I 2140 Highway Model and Speed Selection

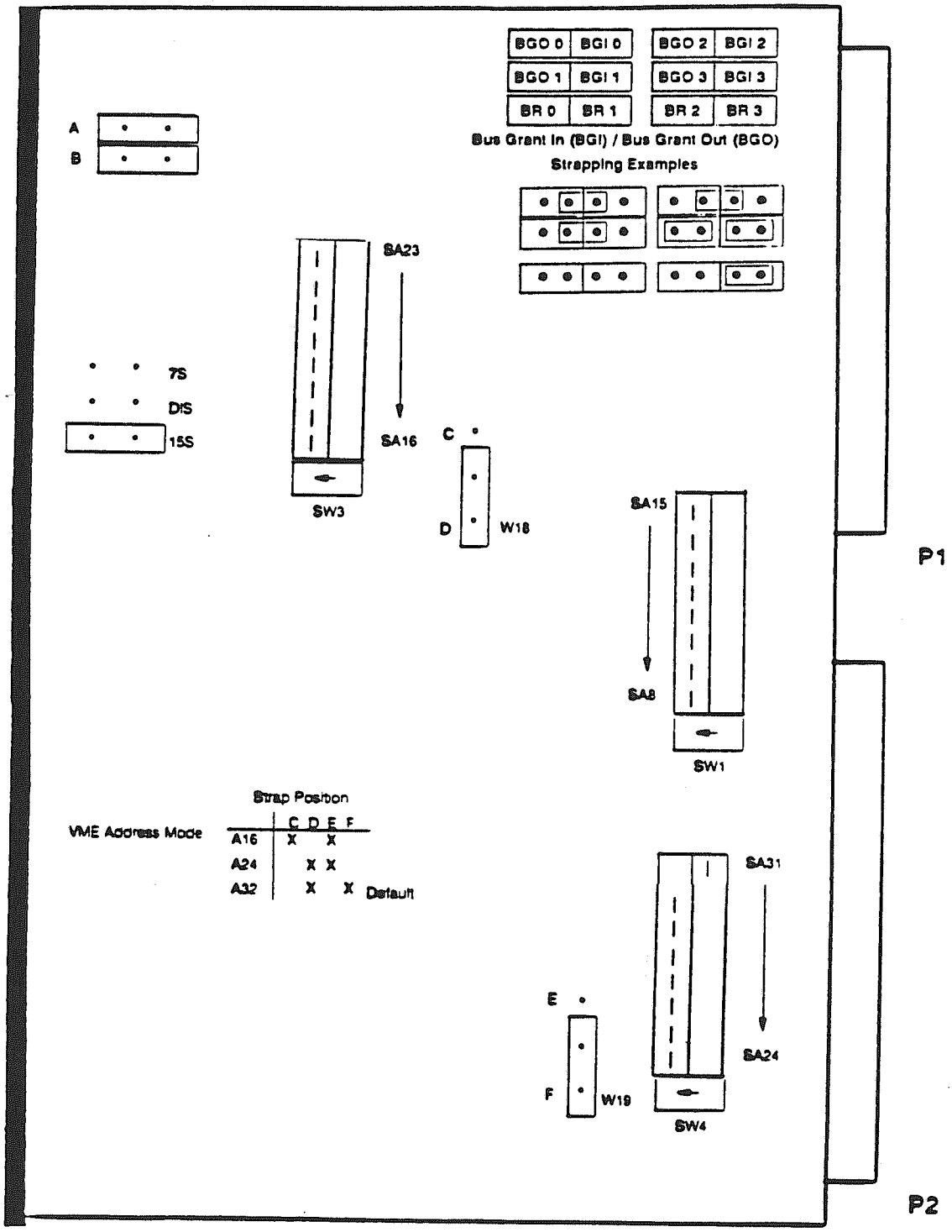


Figure 1 2140 Receiver Switch and Strap Locations

SOFTWARE DRIVER

Software support is available in the form of device drivers and subroutine libraries. Consult the factory for available versions.

I/O THROUGHPUT

The estimated DMA I/O throughput for the 2140 Serial Highway Driver is as follows:

Transfer Type in List	Operation Rate (per transfer)
Single CAMAC Transfer	4.5 microseconds
Inline Write Transfer	5.5 microseconds
Normal Highway Mode Block Transfer	4.5 microseconds
Enhanced Highway Mode Block Transfer	1.0 microsecond

This data assumes that the 2140 is operating in byte-serial mode at a 5 MHz clock rate and the VMEbus is not limiting the rate. The rate per CAMAC Dataway operation is the same for 16-bit and 24-bit transfers. Setup and software overhead are not included.

FRONT-PANEL INDICATORS

RUN — Is a one-shot extended indication of the Command List being executed. RUN is turned on when the Command List is triggered. RUN is turned off when a Command List HALT instruction is executed or an Abort List condition occurs. RUN is also turned off on power-up.

LAM — This LED is turned on when the Demand Message FIFO is not empty. LAM is turned off on power-up, when the Demand FIFO is cleared and when the FIFO is read empty.

NO SYNC — This LED is normally off. It is on when the Serial Highway In Clock is not received (open highway) or when the receiver circuitry is not able to establish bit synchronization.

E3,E2,E1 — These three LEDs indicate the priority encoded result of the last attempt to execute a Command List.

Code	
7	NO SYNC
6	ADNR (Crate-Address not recognized)
5	TMO (Highway Time Out)
4	STE (Highway Transmission Error)
3	Not Used
2	NO X
1	NO Q
0	NO ERROR

See the Control Status Register for an explanation of each code. An ERROR code of zero is the normal power-up state.

NO X NO X indicates that the last CAMAC operation executed resulted in an X response of zero.

NO Q NO Q indicates that the last CAMAC operation executed resulted in a Q response of zero.

2140 REGISTER LAYOUT

Registers with OFFSET = $00 through $4E must be read and written with D16 (Word Data). Registers with OFFSET = $60 through $7C must be read and written with D32 (Longword Data).

Channel Status/Error Register (CSE) D16 OFFSET = $00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
COC 0=NO 1=YES	N/U 0	NDT 0=NO 1=YES	ERR 0=NO 1=YES	ACT 0=NO 1=YES	N/U 0	N/U 0	RDY 1	N/U 0	N/U 0	N/U 0	ERROR CODE				

Device/Operation Control Register (DOC) D16 OFFSET = $04

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXT REQ MODE	N/U 0	N/U 1	N/U 1	OCR BITS (5:4)	N/U 0	N/U 0	N/U 0	DIR	N/U 0	OPERAND SIZE		N/U 0	N/U 0	N/U 1	N/U 0

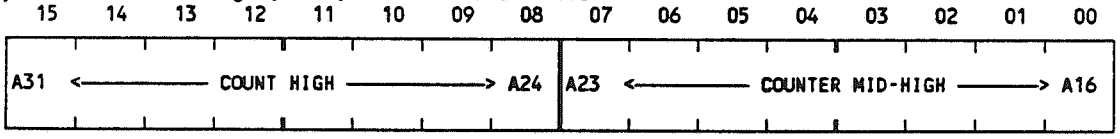
Sequence/Channel Control Register (SCC) D16 OFFSET = $06

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NOT USED								START	N/U 0	N/U 0	SOFT ABORT	INT ENA	N/U 0	N/U 0	N/U 0
0	0	0	0	0	1	0	0								

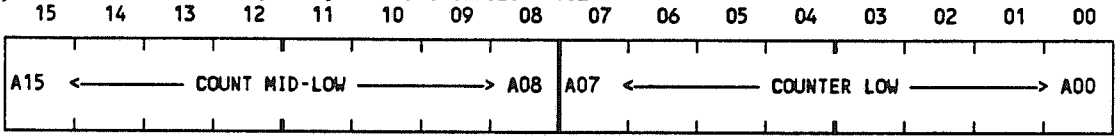
Memory Transfer Count Register (MTC) D16 OFFSET = $0A

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bit 15 <— COUNT HIGH —> Bit 08								Bit 07 <— COUNT LOW —> Bit 00							

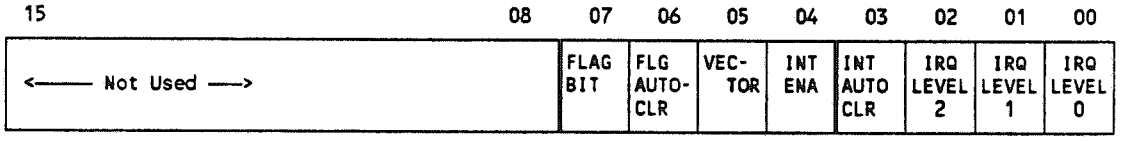
Memory Address Counter High (MACHI) **D16 OFFSET = $0C**



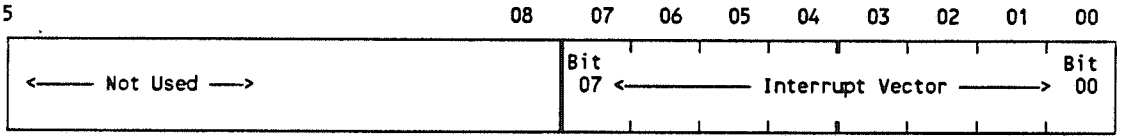
Memory Address Counter Low (MACLO) **D16 OFFSET = $0E**



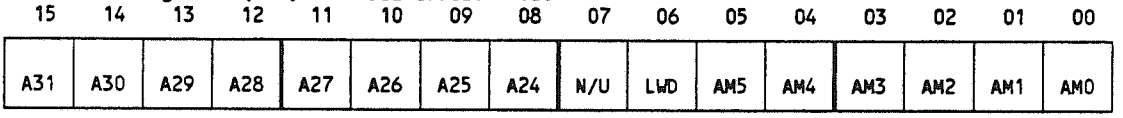
LAM Interrupt Control Register **D16 OFFSET = $40**
Done Interrupt Control Register **D16 OFFSET = $42**
DMA Buffer Empty Interrupt Control Register **D16 OFFSET = $44**
List Abort Interrupt Control Register **D16 OFFSET = $46**



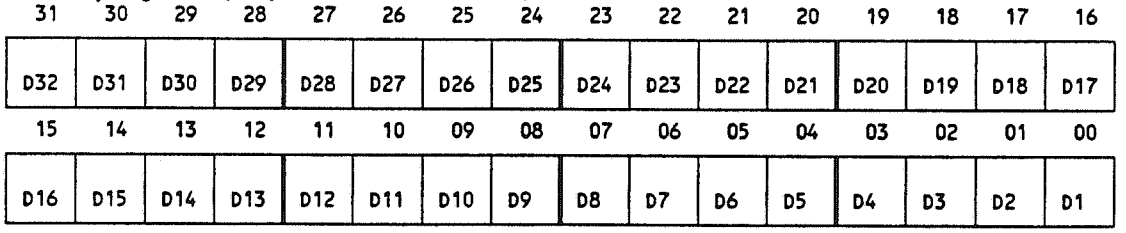
LAM Interrupt Vector Register **D16 OFFSET = $48**
Done Interrupt Vector Register **D16 OFFSET = $4A**
DMA Buffer Empty Interrupt Vector Register **D16 OFFSET = $4C**
List Abort Interrupt Vector Register **D16 OFFSET = $4E**



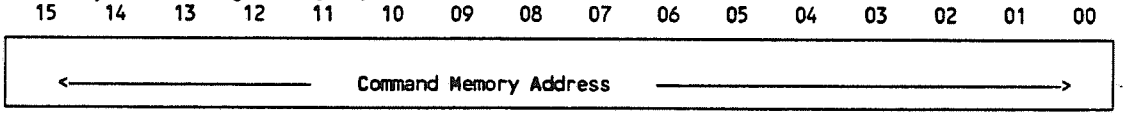
Address Modifier Register (AMR) **D32 OFFSET = $60**



Command Memory Register (CMR) **D32 OFFSET = $64**



Command Memory Address Register (CMA) **D32 OFFSET = $68**



Command Word Count Register (CWC) **D32 OFFSET = $6C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Word Count High															

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Word Count Low 2's Complement of the number of 16/24-bit CAMAC data words															

Demand Request Register (DRR) **D32 OFFSET = $70**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	5	4	3	2	1	0	0	C32	C16	C8	C4	C2	C1

CAMAC Data Register (CDR) **D32 OFFSET = $74**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
D32	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1

Data Burst Register (DBR) **D32 OFFSET = $78**

15	08	07	00
<—— Don't Care ——>		Burst Size 0 —— 255	

Control Status Register (CSR) **D32 OFFSET = $7C**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ABT	0	0	N>23	STE	DLY ERR	TMO	NO SYNC	RPY ERR	0	LPE	TPE	ADNR	DIR	NO X	NO Q

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DMD Pend	DMD OVER RUN	CLEAR DMD FIFO	SHD Reset	DONE	ERROR CODE			Burst	Append	Timer				Trigger	

DMA Controller Register

The DMA Controller has twelve 8-bit registers that need to be programmed prior to any DMA transfer on the VMEbus. These twelve registers can be grouped as six 16-bit word registers for ease of programming. Programming information on the DMA controller can be found below in the register descriptions and also in the Technical Specifications included in APPENDIX B of this manual.

Channel Status/Error Register

The Channel Status/Error Register (SCER) is used to monitor current status and error conditions of the DMA controller. Prior to starting a DMA transfer, bits #15, #13, and #12 must be cleared to zero. A register layout and description of the Channel Status/Error Register is given below:

Channel Status Register (CSR) — Channel Error Register (CER)

15	14	13	12	11	10	09	08	07	06	05	04 03 02 01 00
COC 0=NO 1=YES	N/U 0	NTD 0=NO 1=YES	ERR 0=NO 1=YES	ACT 0=NO 1=YES	N/U 0	N/U 0	RDY 1	N/U 0	N/U 0	N/U 0	ERROR CODE

D08(EO) OFFSET = $00 — D08(EO) OFFSET = $01

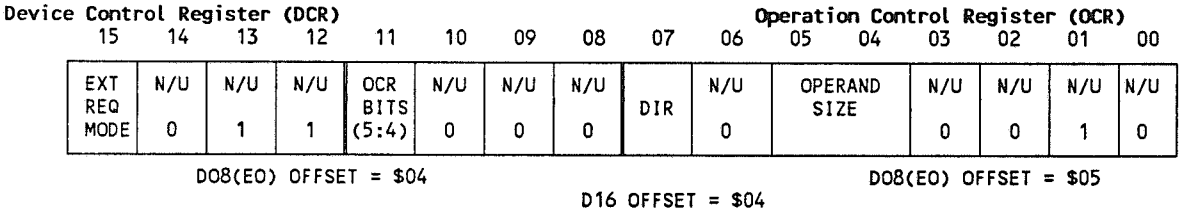
D16 OFFSET = $00

BIT #	MNEMONIC	DESCRIPTION
15	COC	**Channel Operation Complete.** When this bit is set, a DMA transfer has completed whether successful or not. This bit must be cleared before another transfer is started.
14	N/U	**Not used.** Read as zero.
13	NDT	**Normal Device Terminate.** When this bit is set, the command list has aborted. Check the 2140 on-board CSR register for the abort condition. This bit must be cleared before another transfer is started.
12	ERR	**Error.** Error is set when the transfer termination was due to an error. Read the Channel Error Register to determine the cause. This bit must be cleared before another transfer is started.
11	ACT	**Channel Active.** This bit is set when the channel has been started and remains set until the operation is terminated.
10,9	N/U	**Not used.** Read as zeros.
8	RDY	**Ready Input State.** This bit indicates the 2140 is ready. This bit is always read as a one.
7,6,5	N/U	**Not used.** Read as zeros.
4 - 0	ERR CODE	**Error Code.** This Error Code indicates the source of the error when indicated by CSR #12. These Error Code bits are clear when the CSR #12 is cleared.

ERROR CODES
00000 = No Error
01001 = Bus Error
10001 = Software Abort

Device/Operation Control Register

The Device/Operation Control Register (DOCR) isused to select operating conditions of the DMA Controller. This register must be written to, before a transfer is started. A register layout and description of the Device/Operation Control Register is given below:



BIT #	MNEMONIC	DESCRIPTION
15	**EXT REQ MODE**	**External Request Mode.** This bit is written with a one in Cycle Steal mode. A value of zero equals Burst mode.
14	**N/U**	**Not used.** Read as zero.
13,12	**N/U**	**Not used.** Read as zero.
11	**OCR (5:4)**	This bit is set if either bit **#4 or #5 in the Operation Control Register** is set to one.
10 - 8	**N/U**	**Not used.** Read as zeros.
7	**DIR**	**Direction** 0 = Memory to 2140 (CAMAC writes) 1 = 2140 to Memory (CAMAC reads)
6	**N/U**	**Not used.** Read as zero.
5,4	**SIZE**	**Operand Size.** Operand size must be set to 11. The 2140 transfers 32-bit data words.

Bits 5, 4	Size
0 0 =	Byte
0 1 =	Word
1 0 =	Long Word
1 1 =	Double Word

3,2	**N/U**	**Not used.** Read as zeros.
1	**N/U**	**Not used.** Read as one.
0	**N/U**	**Not used.** Read as zero.

Sequence/Channel Control Register

The Sequence/Channel Control Register (SCCR) is used to initiate the start of a DMA operation or to abort a DMA operation. A register layout and description of the Sequence/Channel Control Register is given below:

SEQUENCE CONTROL REGISTER (SCR) — CHANNEL CONTROL REGISTER (CCR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
NOT USED								START	N/U	N/U	SOFT ABORT	INT ENA	N/U	N/U	N/U
0	0	0	0	0	1	0	0		0	0			0	0	0

D08(EO) OFFSET = $06 — D08(EO) OFFSET = $07

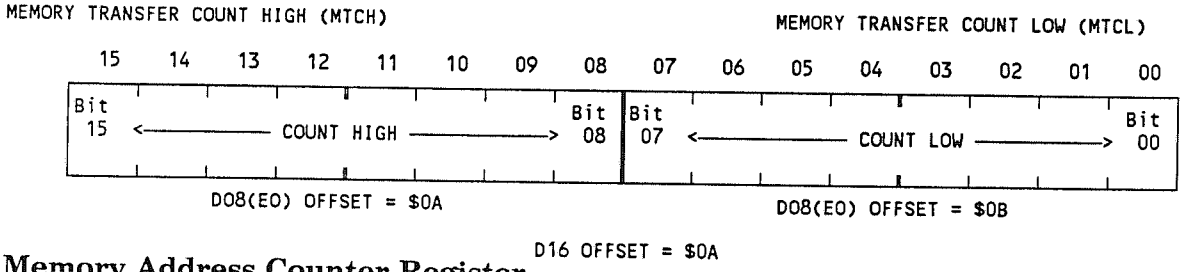
D16 OFFSET = $06

BIT #	MNEMONIC	DESCRIPTION
15-11	**N/U**	**Not used.** Read as zeros.
10	**N/U**	**Not used.** Read as one.
9, 8	**N/U**	**Not used.** Read as zeros.
7	**START**	**Start operation.** Setting this bit to a one will initiate the DMA controller and set the Active bit in the CSR. A pending start can only be reset by a software abort being set in the CCR.
6 ,5	**N/U**	**Not used.** Read as zero.
4	**SOFT ABORT**	**Software Abort.** Setting this bit stops a DMA transfer.

3	**INT ENA**	**Interrupt Enable.** This bit must be set to zero. The 2140 Bus Interrupter is used for BUFFER EMPTY interrupts.
2-0	**N/U**	**Not used.** Read as zeros.

Memory Transfer Count Register

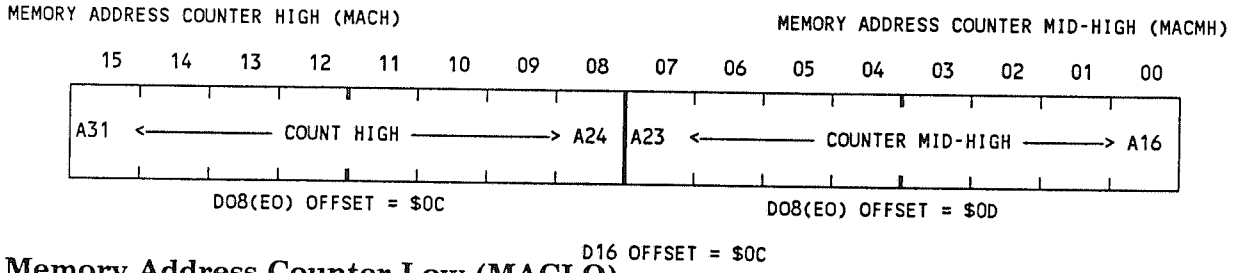
The Memory Transfer Count (MTC) Register is a 16-bit counter which counts the number of words transferred by the DMA controller. A register layout of the Memory Transfer Count Register is given below:



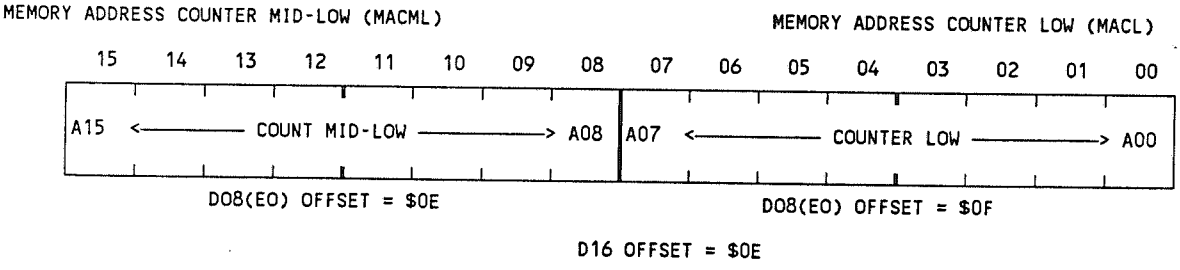
Memory Address Counter Register

The Memory Address Counter Register is a 32-bit register which programs the starting address of a DMA transfer. Only the least significant 24-bits of the counter are implemented in the DMA controller. If 32 operations are desired, the upper eight address bits can be programmed in the 2140 Address Modifier Register. Two 16-bit Memory Address Counters must be loaded before the start of a DMA transfer. A register layout of the Memory Address Counter Register is given below:

Memory Address Counter High (MACHI)



Memory Address Counter Low (MACLO)

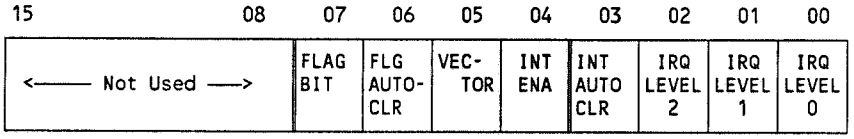


BUS INTERRUPT REGISTERS

The Model 2140 uses the MC68153 Bus Interrupter to generate four separate interrupts. The four conditions that can cause an interrupt are: 1) a LAM, 2) DONE bit in the CSR set, 3) DMA Buffer Empty and 4) List Abort condition. If any two or more interrupts are set to the same interrupt request level, MC68153 gives preference to the highest number requester; that is, List Abort has the highest priority and LAM has the lowest. Programming information on the Bus Interrupter can be found below in the register descriptions and also in the Technical Specifications included in APPENDIX A of this manual.

Interrupt Control Registers

The Interrupt Control Registers are used to enable and select the interrupt request level. A register layout and description of the Interrupt Control register is given below:



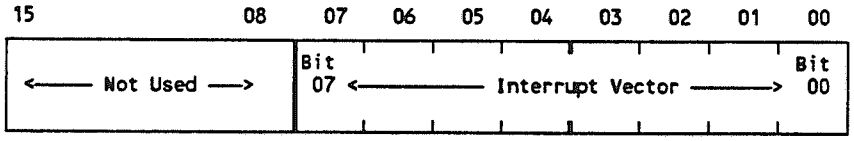
Interrupt Control Register		OFFSET
LAM	D16 = $40	D08(EO) = $41
DONE	D16 = $42	D08(EO) = $43
DMA BUFFER EMPTY	D16 = $44	D08(EO) = $45
LIST ABORT	D16 = $46	D08(EO) = $47

BIT #	MNEMONIC	DESCRIPTION
15-8	N/U	**Not used.** These bits are shown only for clarity when D16 operations are preformed. These bits are read as ones.
7	FLAG	**FLAG.** This bit can be used by software in conjunction with test and set instructions.
6	FLG AUTO-CLR	**Flag Auto-Clear.** When this bit is set, the FLAG bit is automatically cleared during an interrupt acknowledge cycle.
5	VECTOR	**Vector.** This bit must be set to zero, the 2140 uses internal vectors.
4	INT ENA	**Interrupt Enable.** Setting this bit to a one will enable interrupts.
3	INT AUTO-CLR	**Interrupt Auto-Clear.** Setting this bit to a one will clear bit #4 (INT ENA) during an interrupt acknowledge cycle responding to this request. To re-enable, bit #4 must be written with a one.

2-0	**IRQ LEVEL**	**Interrupt Request Level.** This three bit field determines the interrupt level, one through seven, to be generated. A value of zero disables the interrupt.

Interrupt Vector Registers

Each Interrupt Control Register has its own associated Interrupt Vector Register. Each register is 8-bits wide and supplies a data byte during an interrupt acknowledge cycle. A register layout of the Interrupt Vector Register is given below:



Interrupt Vector Register	OFFSET	
LAM	D16 = $48	D08(EO) = $49
DONE	D16 = $4A	D08(EO) = $4B
DMA BUFFER EMPTY	D16 = $4C	D08(EO) = $4D
LIST ABORT	D16 = $4E	D08(EO) = $4F

2140 ON-BOARD REGISTERS

Address Modifier Register

The Address Modifier Register (AMR) is a D16 write only register. Information written into the AMR is used to provide the VMEbus Address Modifier signals and the upper eight address signals (A31-A24) when the 2140 transfers data as a VMEbus master. The upper eight address signals cannot increment during a DMA transfer. This is only an 8-bit latch register that is enabled when the 2140 becomes a VMEbus master. A register layout and a description of the AMR is given below:

ADDRESS MODIFIER REGISTER

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A31	A30	A29	A28	A27	A26	A25	A24	N/U	LWD	AM5	AM4	AM3	AM2	AM1	AM0

D32 OFFSET = $60

BIT #	MNEMONIC	DESCRIPTION
15-8	**A31-A24**	**VME Address Lines.** These added address bits are to make use of the full VME address range when the 2140 becomes a VMEbus master. These bits do not increment during a DMA transfer.
7	**N/U**	**Not used.** Read as a one.

6	**LWD**	**Longword.** This bit must be clear because the 2140 only transfers 32-bit data words.
5-0	**AM5-AM0**	**Address Modifier Codes.** These bits must be written with the proper AM Code before a DMA transfer is started.

Command Memory Register

The 2140 Command Memory is an 8K x 32-bit RAM memory. All CAMAC commands are executed from this memory. Data for one or more command lists is written or read as if the memory was a single 32-bit register. The Memory Address is incremented automatically after each write or read operation. If multiple lists are present, the list to be executed is selected by first setting the Command Memory Address to that list. All lists **must** be CAMAC **"Read"** or **"Write"**, with the following exceptions:

1. Read or write lists can contain dataless CAMAC commands, using Function Codes F(8) through F(15) and F(24) through F(31).
2. Read lists can contain Inline Write operations.

The instructions for the Command List (written as MEM DATA) can be selected from the following:

(a) **Single CAMAC Transfer** -- Read, Write, or Control

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W(1)	0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(2)	0	0	C32	C16	C8	C4	C2	C1	CM 0	TM2 0	TM1 0	QM2 0	QM1 0	WS2	WS1	AD

D32 OFFSET = $64

(b) **Single CAMAC Transfer** -- Inline Write (usually in Read list)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W(1)	0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(2)	0	0	C32	C16	C8	C4	C2	C1	CM 0	TM2 1	TM1 1	QM2 0	QM1 0	WS2	WS1	AD
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W(3)	X	X	X	X	X	X	X	X	W24	W23	W22	W21	W20	W19	W18	W17

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(4)	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1

Note: Word #4 is a dummy word for 16-bit Inline Write operation.

D32 OFFSET = $64

(c) **Block CAMAC Transfer**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W(1)	0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(2)	0	0	C32	C16	C8	C4	C2	C1	CM 0	TM2 0	TM1 1	QM2 X	QM1 X	WS2	WS1	AD

	31	16
W(3)	WORD COUNT HIGH	

	15	00
W(4)	WORD COUNT LOW (The 2's Complement of the number of 16-bit or 24-bit CAMAC transfers)	

D32 OFFSET = $64

(d) **JUMP instruction** -- Jump to another command list.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(1)	0	0	0	0	0	0	0	0	CM 1	TM2 1	TM1 0	0	0	0	0	0

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(2)	0	0	0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

D32 OFFSET = $64

(e) **HALT instruction** -- End of Command list.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W(1)	0	0	0	0	0	0	0	0	CM 1	TM2 0	TM1 0	0	0	0	0	0

D32 OFFSET = $64

Any list can contain a combination of the above instructions, terminated by the HALT instruction.

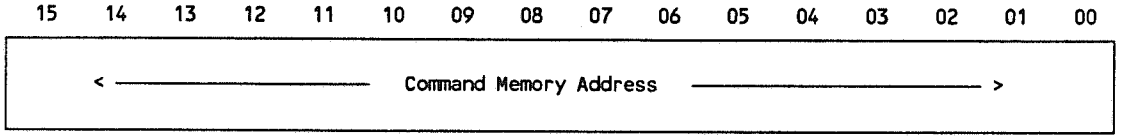
The Mode word (word #1) in the list instructions is partitioned as follows:

BIT #	MNEMONIC	DESCRIPTION
15-14	**N/U**	**Not Used.** Don't care.
13-8	**C32,C16,C8 C4,C2,C1**	**Crate.** This 6-bit field selects one of sixty-two 3952 Crate Controllers.
7	**CM**	**Command Mode:** 0 = CAMAC transfer 1 = Non-CAMAC instruction. (HALT, etc.)
6,5	**TM2,TM1**	**Transfer Mode: CM = 0** 0 0 = Single CAMAC transfer 0 1 = Normal Highway Mode Block Transfer 1 0 = Enhanced Highway Mode Block Transfer 1 1 = Single Inline write transfer **Transfer Mode: CM = 1** 0 0 = HALT instruction 0 1 = Not Used 1 0 = JUMP instruction 1 1 = Not Used
4,3	**QM2,QM1**	**Q-Mode Transfer Type:** Normal: 0 0 = Q-Stop; 0 1 = Q-Ignore; 1 0 = Q-Repeat; 1 1 = Q-Scan Enhanced: 0 0 = Q-Stop; 0 1 = Q-Ignore (Single NAF); 1 0 = Q-Repeat; 1 1 = Q-Ignore (3830 LSM)
2,1	**WS2,WS1**	**Word Size:** 0 0 = 24-bit CAMAC transfer 0 1 = 16-bit CAMAC transfer 1 0 = 24-bit Byte Packing **(Enhanced only)** 1 1 = 16-bit Word Reversed
0	**AD**	**Abort Disable.** Data of zero will Abort a transfer on an error (refer to the Operation Section of this manual for a description of error for each mode). Data of one disables Abort.

Command Memory Address Register

The Command Memory Address (CMA) Register is a 16-bit Write/Read Counter. When loading a new list, this register is loaded with an address that points to the initial word location for that command list. When writing or reading the Command Memory, the address register is auto-incremented after each read or write operation. After a HALT instruction is encountered

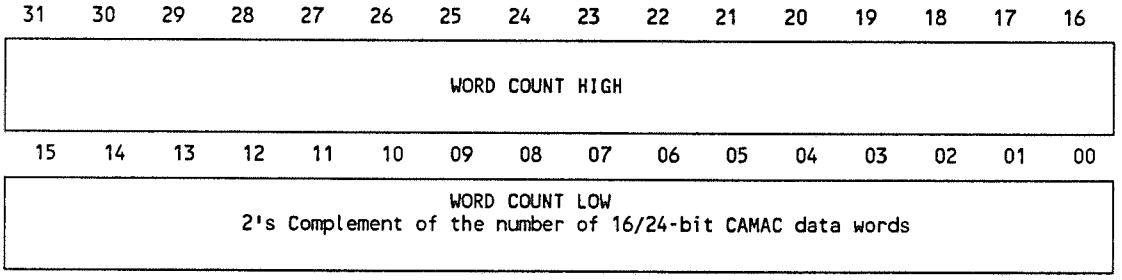
or the list is aborted, the Command Memory Address Register points to the next list address. A layout of the Command Memory Address Register is given below:



D32 OFFSET = $68

Command Word Count Register

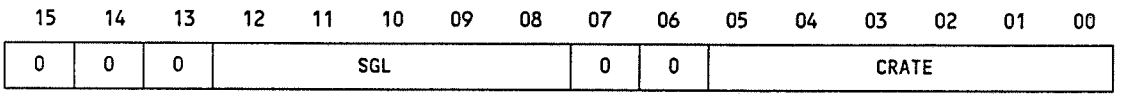
The Command Word Count (CWC) Register is a 32-bit read-only counter which contains the 2's complement of the number of words not yet executed in a CAMAC block transfer read or write operation. When a CAMAC block transfer is executed, this register is loaded by the Command Memory Sequencer with the initial word count from the command list and incremented as transfers occur for that block. When a block transfer is aborted, the "current" word count can be determined by reading this register. Note that the data in this register monitors the last block operation executed not the total word count for all the list operations. A register layout for the Command Word Count Register is given below:



D32 OFFSET = $6C

Demand Request Register

The Demand Request Register (DRR) provides read-only access to Serial Highway Demand messages. This register is the read port of a FIFO capable of "holding" up to 512 Demand messages. After a Demand word is read, the next Demand word (if present) is available for reading. The DEMAND PENDING bit is set in the CSR as long as this FIFO is not empty. If the Demand FIFO is full with 512 Demands and another Demand is received, the DEMAND OVERRUN bit is set in the CSR. The Demand FIFO can be cleared without reading it by the CLEAR DEMAND FIFO bit in the CSR.

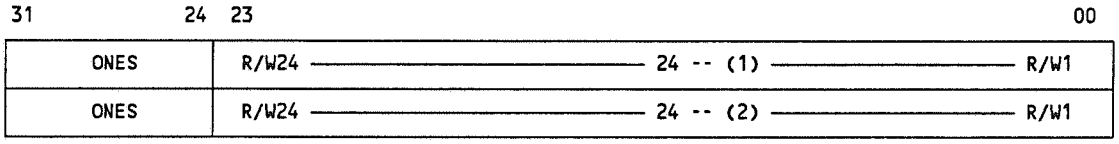


D32 OFFSET = $70

CAMAC Data Register

The CAMAC Data Register provides the port for data transfer (read or write data) over the Serial Highway. The 2140 SHD contains two first-in, first-out (FIFO) buffers, one for write data and one for read data. If the Command List contains write commands, this register is written to transfer data over the Serial Highway via the Transmit FIFO. If the Command List contains read commands, this register is read to transfer data from the Serial Hgihway via the Reply FIFO.

Single and block CAMAC data words are packed into one block for the entire transfer block as selected by a write or read Command List. This list can contain a mixture of 16-bit and 24-bit CAMAC transfers. The following diagrams show FIFO data packing when a Command List contains mixtures of 16-bit and 24-bit commands.



WS2, WS1 = 0 0 24-bit Normal
D32 OFFSET = $74

31 — 24	23 — 16	15 — 08	07 — 00
24 -- (1) HI	24 -- (1) MID	24 -- (1) LO	24 -- (2) HI
24 -- (2) MID	24 -- (2) LO	24 -- (2) HI	24 -- (3) MID
24 -- (3) LO	24 -- (3) HI	24 -- (3) MID	24 -- (4) LO

WS2, WS1 = 1 0 24-bit Packed
D32 OFFSET = $74

The 24-bit packed data transfer can only be used with enhanced data transfer commands. During 24-bit packed transfers, four 24-bit CAMAC words are packed into three VME words. If the total number of CAMAC words in the block are not divisible by 4, and if the packed command being executed is followed by another type of command, one, two, or three bytes of the FIFO are filled with ones.

31 — 24	23 — 16	15 — 08	07 — 00
16 -- (2) HI	16 -- (2) LO	16 -- (1) HI	16 -- (1) LO
16 -- (4) HI	16 -- (4) LO	16 -- (3) HI	16 -- (3) LO

WS2, WS1 = 0 1 16-bit Normal
D32 OFFSET = $74

31 — 24	23 — 16	15 — 08	07 — 00
16 -- (1) HI	16 -- (1) LO	16 -- (2) HI	16 -- (2) LO
16 -- (3) HI	16 -- (3) LO	16 -- (4) HI	16 -- (4) LO

WS2, WS1 = 1 1 16-bit Reversed
D32 OFFSET = $74

When an odd number of data words are transferred by 16-bit Normal or 16-bit Reversed commands and are followed by another type of command, two bytes of data in the FIFO are filled with ones.

31 24	23 16	15 08	07 00
ONES	R/W24 — 24 (1) — R/W1		
24 -- (1) HI	24 -- (1) MID	24 -- (1) LO	24 -- (2) HI
24 -- (2) MID	24 -- (2) LO	ONES	ONES
ONES	ONES	16 -- (1) HI	16 -- (1) LO
16 -- (1) HI	16 -- (1) LO	ONES	ONES
ONES	R/W24 — 24 (2) — R/W1		

D32 OFFSET = $74

The above diagram shows data for the following Command List:

Single 24-bit Normal transfers
Two 24-bit Packed transfers
One 16-bit Normal transfers
One 16-bit Reversed transfers
One 24-bit Normal transfers

Data Burst Register

The Data Burst Register is an 8-bit write-only counter, used to specify the 2s complement number of VME data transfers which will occur for each DMA controller VMEbus arbitration. The Data Burst Register retains its loaded value until a SHD Reset is preformed from the Control Status Register (CSR) or a power-up occurs. If Burst Mode is specified in the CSR and the Burst Register is zero, cycle steal VMEbus data transfers will occur.

DATA BURST REGISTER (DBR)

15 08	07 00
	2s Complement for Number of VME transfers per burst

D32 OFFSET = $78

Control Status Register

The Control Status Register (CSR) is used to set initial operating conditions, start operations and monitor the results of those operations. A layout and description of the CSR is given below:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ABT	DMA DONE	0	N>23	STE	DLY ERR	TMO	NO SYNC	RPY ERR	0	LPE	TPE	ADNR	DIR	NO X	NO Q

15	14	13	12	11	10 09 08	07	06	05 04 03 02	01 00
DMD Pend	DMD OVER RUN	CLEAR DMD FIFO	SHD Reset	DONE	ERROR CODE	Burst	Append	Timer	Trigger

D32 OFFFSET = $7C

BIT #	MNEMONIC	DESCRIPTION
1,0	**Trigger**	**Trigger** is used to arm or start a list operation. 0 0 No trigger 0 1 Start list immediately, stop list when Halt command occurs. 1 0 Arm a Command List. Execution commences when the next timer "tic" occurs. List is retriggered on each "tic". Operation is stopped by resetting to 0 0 or by SHD Reset. 1 1 Not valid.
05-02	**Timer**	This write/read field is used to select the timer "tic" rate. It is cleared by power-up or SHD Reset. All of the available rates are shown in the following chart.

Timer Field 05,04, 03,02	Straps A -- IN B -- IN	Straps A -- OUT B -- IN	Straps A -- IN B -- OUT	Straps A -- OUT B -- OUT
0	1 MEG	10K	100	1
1	100K	1K	10	.1
2	500K	5K	50	.5
3	333.3K	3.3K	33	.33
4	250K	2.5K	25	.25
5	200K	2K	20	.2
6	166.6K	1.6K	16	.16
7	83.3K	830	8.3	.083
8	100K	1K	10	.1
9	10K	100	1	.01
A	50K	500	5	.05
B	33.3K	330	3.3	.033
C	25K	250	2.5	.025
D	20K	200	2	.02
E	16.6K	160	1.6	.016
F	8.3K	83	.83	.0083

Note: All frequencies shown are in HERTZ. Frequency tolerance is ±.01%.

CHART II Internal Timer "TIC" Rate Selection

BIT #	MNEMONIC	DESCRIPTION
06	**Append**	When set, this write/read bit causes the 32-bit CSR to be placed at the end of a read block operation. In the event of an aborted operation, this word is inserted after the last valid 32-bit read word transferred. This bit has no effect on write block operations.
07	**Burst**	When set, this write/read bit will cause the DMA Controller to transfer the number of data words specified by the Burst Register per VMEbus arbitration.
10-08	**Error Code**	This three-bit read only field is the priority-encoded result of the last execution (or attempted execution) of a Command List. The errors are listed in the order of priority (highest priority first). The code represents the decimal value of these bits.

Code	Error Type
7	NO SYNC -- (See Bit 24)
6	ADNR -- (See Bit 19)
5	TMO -- (See Bit 25)
4	STE -- (See Bit 27)
3	NOT USED
2	NO X -- (See Bit 17)
1	NO Q -- (See Bit 16)
0	NO ERROR -- None of the errors defined above are present.

11	**DONE**	This read-only bit is set when the 2140 has completed or aborted a Command list. It is cleared while the SHD is executing a list. Read data may remain in the Reply FIFO after the assertion of SH DONE (if not already transferred to the VME memory).
12	**SHD Reset**	This write-only bit resets the 2140 to its power-up state. This bit is read as ZERO.
13	**Clear DMD FIFO**	This write-only bit clears the contents of the Demand FIFO. This bit is read as ZERO.

14	**DMD Overrun**	This read-only bit is set whenever the Demand FIFO overflows. This bit is cleared by power-up, RESET, or CLR DMD FIFO.
15	**DMD Pend**	This read-only bit is set whenever the Demand FIFO contains data. This bit is cleared by power-up, RESET, or CLR DMD FIFO.
16	**NO Q**	If set, the last CAMAC operation executed resulted in a Q response of ZERO (indicating data not accepted by a write operation, data not available for a read operation, or a FALSE response to a "test" command).
17	**NO X**	If set, the last CAMAC operation executed resulted in an X response of ZERO (indicating that the command was not executed by the target module). Note that the unique flag from the 3830 List Sequencer module, X=0 and Q=1, does not set the NO X bit.
18	**Dir**	Direction Bit - Set for Write lists, cleared for Read lists.
19	**ADNR**	**Address Not Recognized** is set to indicate that the Crate address in the last Command message was not recognized by any Serial Crate Controller. (The Command message returned to the SHD.)
20	**TPE**	If set, a transverse parity error was detected in the last incoming Reply message to the 2140.
21	**LPE**	If set, a longitudinal parity error was detected in the last incoming Reply message to the 2140.
22	**0**	Not used, read as zero.
23	**RPY ERR**	If set, the Error (ERR) bit was TRUE in the last Serial Highway message.
24	**NO SYNC**	If set, the Serial Highway receiver in the 2140 is not currently in synchronization.
25	**TMO**	Timeout is set when the 2140 initiates a Serial Highway message and a valid Reply is not received within a predefined time.
26	**DLY ERR**	If set, indicates that the RPY ERR bit was set in command prior to this one.

27	**STE**	A Serial transmission error occurred on the last Serial Highway transaction. **STE = ERR + LPE + TPE**
28	**N>23**	If set, a Q-mode address scan caused the CAMAC station number (N) to be incremented beyond 23.
29	**0**	Not Used, read as ZERO.
30	**DMA DONE**	Read only bit set upon the completion of the DMA operation. DMA Buffer has been transferred.
31	**ABT**	This read-only bit is set when the Command List is terminated by one or more of the following Abort Definitions. (Refer to the Operating Mode section of this manual for more information on the definition of this bit.)

- ADNR (Address not recognized)
- TMO (Highway timeout)
- N>23 (Attempt beyond Slot 23)
- STE (Serial Transmission Error) · AD
- $\overline{\text{QM3}}$ (NOT Q-Scan) · NOX · AD
- QMO (Q-Stop) · NO Q
- TM2 (Enhanced block) · QM2 (Q-Repeat) · NO X · NO Q · WCO

where:

AD (Abort Disable) is the LSB of the Command Mode byte (Bit 0 0 of a Command List word).

QMx is the decimal value of the Q Mode (Bits 04-03 of a Command List word).

TMx is the decimal value of the Transfer Mode (Bits 06-05 of a Command List word).

OPERATING MODES

The 2140 provides four types of operations based on the Q-Response received from the Serial Crate Controller (SCC). These four types Q-Stop, Q-Ignore, Q-Repeat and Q-Scan are specified in bits <04:03> of the Command Mode Byte.

Four transfer modes, Single, Normal (Standard) Block, Enhanced Block and Single Inline Write are provided by the 2140. These four transfer modes are specified in bits <06:05> of the Command Mode Byte.

The following is a detailed description of the transfer modes and the Q-types associated with each.

Q-Stop Single Transfer (TM2=0:TM1=0, QM2=0:QM1=0)

When using the Q-Stop Single Transfer mode of operation, bits <06:03> of the Command Mode byte are set to zero. Only one CAMAC/Serial Highway operation takes place for each Single Transfer Command. If a NO Q condition exists after the execution of a Q-Stop Command, the Command List is aborted, and the "ABORT", "DONE", and "ERROR" bits of the CSR are set.

$$ABORT = NO{\cdot}Q + \overline{[AD}(ERR + NO{\cdot}X + TPE + LPE)]$$

Q-Ignore Single Transfer (TM2=0:TM1=0, QM2=0:QM1=1)

To select the Q-Ignore Single Transfer mode of operation, set Command Mode Bits <06:05> to 00 and <04:03> to 01. Only one CAMAC/Serial Highway operation takes place per command. The following is the definition of "ABORT" when using Q-Ignore Single Transfer:

$$ABORT = \overline{AD}(ERR + NO{\cdot}X + TPE + LPE)$$

Q-Repeat Single Transfer (TM2=0:TM1=0, QM2=1:QM1=0)

To select the Q-Repeat Single Transfer mode of operation, set command Mode bits <06:05> to 00 and <04:03> to 10. Multiple CAMAC/Serial Highway operations may occur depending on the returned CAMAC Q-Response. The highway driver repeats the operation until a Q-Response of one is obtained or a timeout occurs. A timeout Strap Option on the REC circuit card (see Strap Option section of this manual) selects 15 seconds, 7 seconds or disable as the time before a timeout ABORT takes place. When timeout is disabled, the driver will repeat a command indefinitely if a Q=1 response is not received. In this case it is necessary to set the "Reset Driver" bit in the CSR. The following is the definition of "Abort" when using Q-Repeat Single transfer.

$$ABORT = TMO + \overline{[AD}(ERR + NO{\cdot}X + TPE + LPE)]$$

Q-Scan Single Transfer (TM2=0:TM1=0, QM2=1:QM1=1)

To select the Q-Scan Single Transfer mode of operation, set the Command Mode Byte bits <06:05> to 00 and <04:03> to 11. Multiple CAMAC/Serial Highway operations may occur, depending on the returned CAMAC Q-Response. During Q-Scan operations, the highway driver uses the CAMAC Q-Response from the previous command to determine the station number and subaddress for the next command. Q-Scan type operations are usually associated with blocks of data as opposed to single words and is described in more detail under Normal Block Transfers. The following equation is the definition of "ABORT" when using Q-Scan Single Transfer:

$$\text{ABORT} = N > 23 + \overline{AD}(\text{ERR} + \text{TPE} + \text{LPE})$$

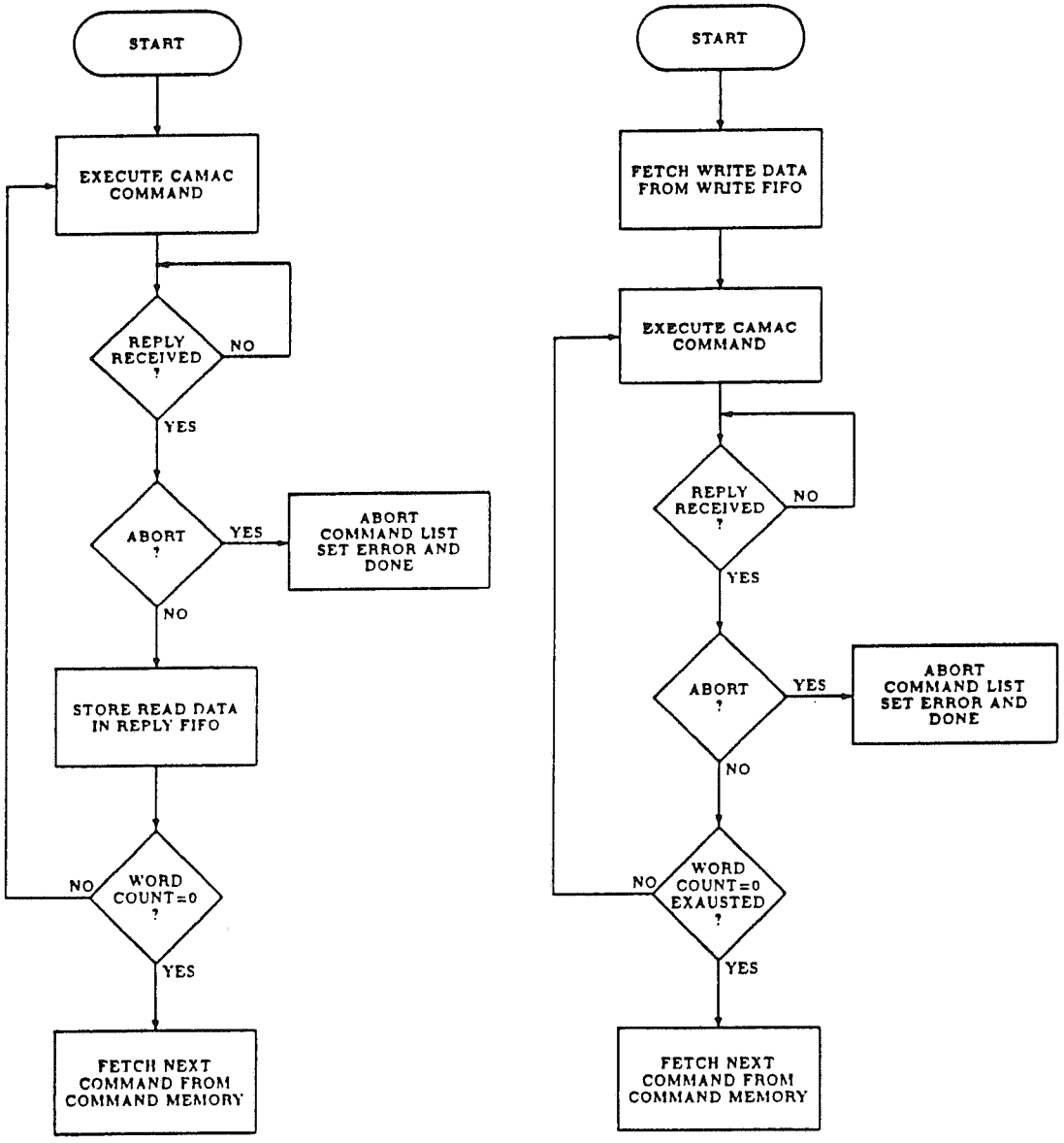
Normal Block Transfers

The 2140 supports four types of normal speed (standard) block transfers; these are Q-Stop, Q-Ignore, Q-Repeat and Q-Scan.

In the normal block transfer mode, transfers to/from the CAMAC crate are done in a conservative fashion. For CAMAC reads, a command message is sent down the serial highway and when the 2140 receives the Reply message, it determines if the data received is valid and should be stored in the Reply FIFO. Data validity depends on parameters such as the selected Q-Mode type, the CAMAC Q-and X- responses and also several other status indicators. After the data is stored in the Reply FIFO, the 2140 examines the word count to see if additional transfers are required. The 2140 then either fetches the next command from the Command List or continues the above sequence.

When executing CAMAC writes, the 2140 examines the Write FIFO for data. When data is present the command message is sent out on the serial highway. The 2140 then receives the Reply message and determines if additional CAMAC writes are required. If additional transfers are required, the above sequence continues until the word count is reached.

The following describes transfers in the Normal Block Mode:



IGNORE-Q READ COMMANDS

IGNORE-Q WRITE COMMANDS

Figure 2 Ignore Q-Block Commands

Q-Stop Normal Block Transfer (TM2=0:TM1=1, QM2=0:QM1=0)

To select the Q-Stop Normal Block Transfer Mode, set the Command Mode Byte bits <06:05> to 01 and <04:03> to 00. During the Q-Stop block transfer operations, the CAMAC command specified in the NAF is repeated until a Q-Response of zero is received or the word count is exhausted. The block transfer will also terminate if an "Abort" is generated. The following equation describes "Abort" when in the Q-Stop block transfer mode.

$$ABORT = N0\text{-}Q + \overline{AD}(NO\text{-}X + ERR + TPE + LPE)$$

Q-Ignore Normal Block Transfer (TM2=0:TM1=1, QM2=0:QM1=1)

Q-Ignore Normal Block Transfer is selected by setting the Command Mode bits <06:05> to 01 and bits <04:03> to 01. During a Q-Ignore block transfer operation, the CAMAC command specified in the NAF is repeated until the word count is exhausted. The block transfer will also terminate if an "Abort" is generated. The following equation describes "Abort" when in the Q-Ignore block transfer mode.

$$ABORT = \overline{AD}(NO\text{-}X + ERR + TPE + LPE)$$

Figure Figure 2 is a simplified flow diagram for Q-Ignore reads and writes.

Q-Repeat Normal Block Transfer (TM2=0:TM1=1, QM2=1:QM1=0)

To select Q-Repeat Normal Block Transfer mode, set Mode bits <06:05> to 01 and <04:03> to 10. During a Q-Repeat block transfer, the CAMAC command NAF is repeated for each data word until a Q-Response of one is obtained. A Q-Response of one causes either new write data to be fetched from the Write FIFO or Read Data to be stored into the Reply FIFO. The command is repeated for each data word until the word count is exhausted. The driver could repeat a command indefinitely if a Q=1 response is not received; therefore, a timeout strap option is provided on the REC circuit board which selects 15 seconds, 7 seconds or disable as the time before a timeout Abort takes place. When timeout is disabled and a Q=1 response is never received, it is necessary to set the "Reset Driver" bit in the CSR to abort the operation.

The following equation describes "Abort" when in the Q-Repeat block transfer mode:

$$ABORT = TMO + \overline{AD}(NO\text{-}X + ERR + TPE + LPE)$$

Figure Figure 3 is a simplified flow diagram for Q-Repeat reads and writes.

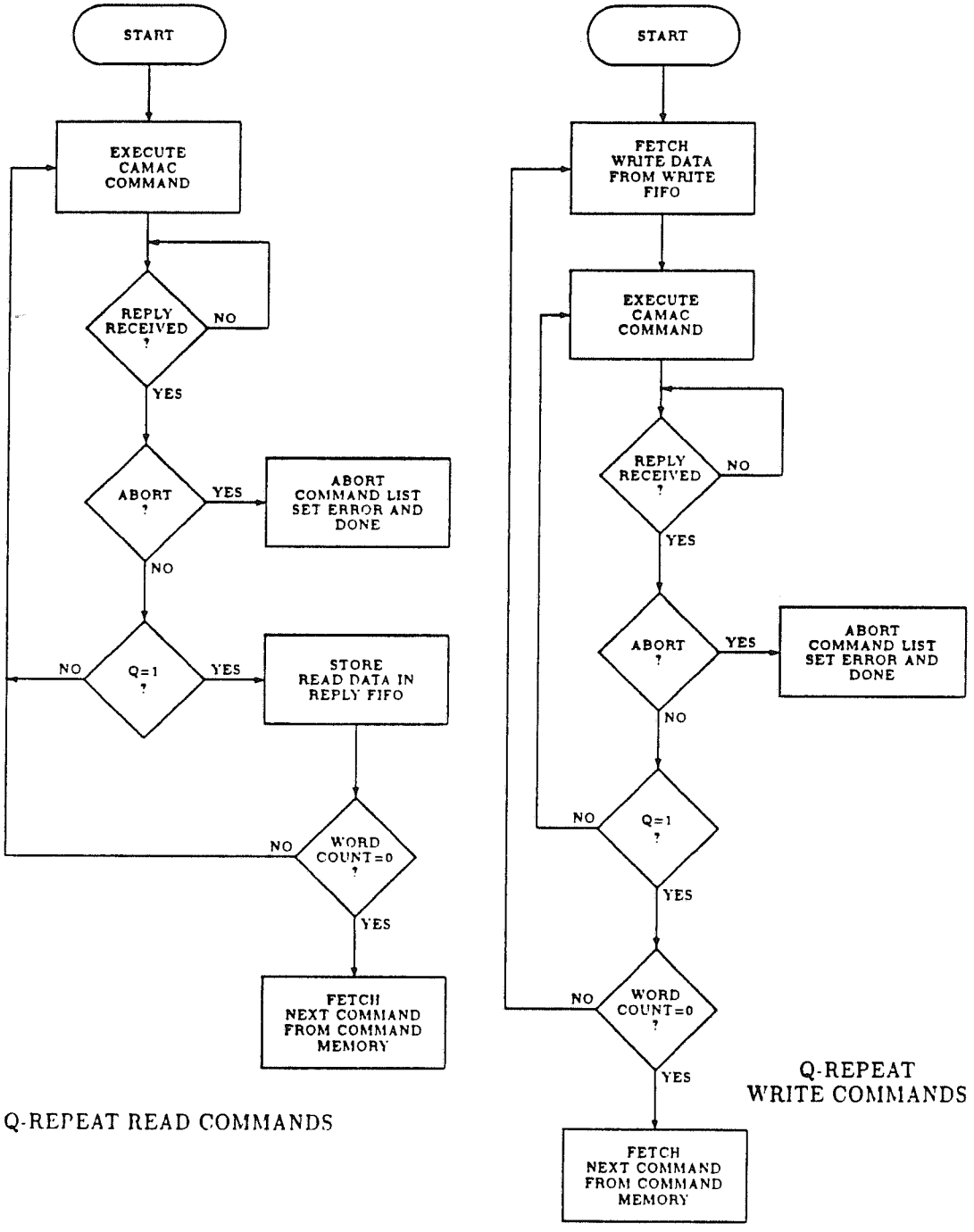


Figure 3 Q-Repeat Block Commands

Q-Scan Normal Block Transfer (TM2=0:TM1=1, QM2=1:QM1=1)

To select the Q-Scan block transfer mode, set Command Mode bits <06:05> to 01 and bits <04:03> to 11. During Q-Scan block transfer operations, the 2140 uses the Q-Response from the previous command to determine the station number and subaddress for the next command. A Q-Response of zero indicates that the last valid subaddress of the current station number has been accessed. The 2140 responds to a Q=0 by resetting the subaddress, incrementing the station number, and continuing the scan. A Q-Response of one indicates the last command was executed to a valid CAMAC address. The 2140 responds to a Q=1 by either storing the read data into the Reply FIFO or fetching new write data from the Write FIFO.

When a Q=1 is received, the 2140 updates the CAMAC address as follows: the subaddress is incremented or, if the subaddress was 15, it is reset to zero, and the station number is incremented. If, due to a programming error, the 2140 increments the station number beyond 23, the block transfer will terminate, the Command List will abort, and the "ERROR" bit will set.

The following equation is the definition of "Abort" when using Q-Scan block transfers:

$$ABORT = N > 23 + \overline{AD}(ERR + TPE + LPE)$$

Figures Figure 4 and Figure 5 are simplified flow diagrams for Q-Scan read and writes.

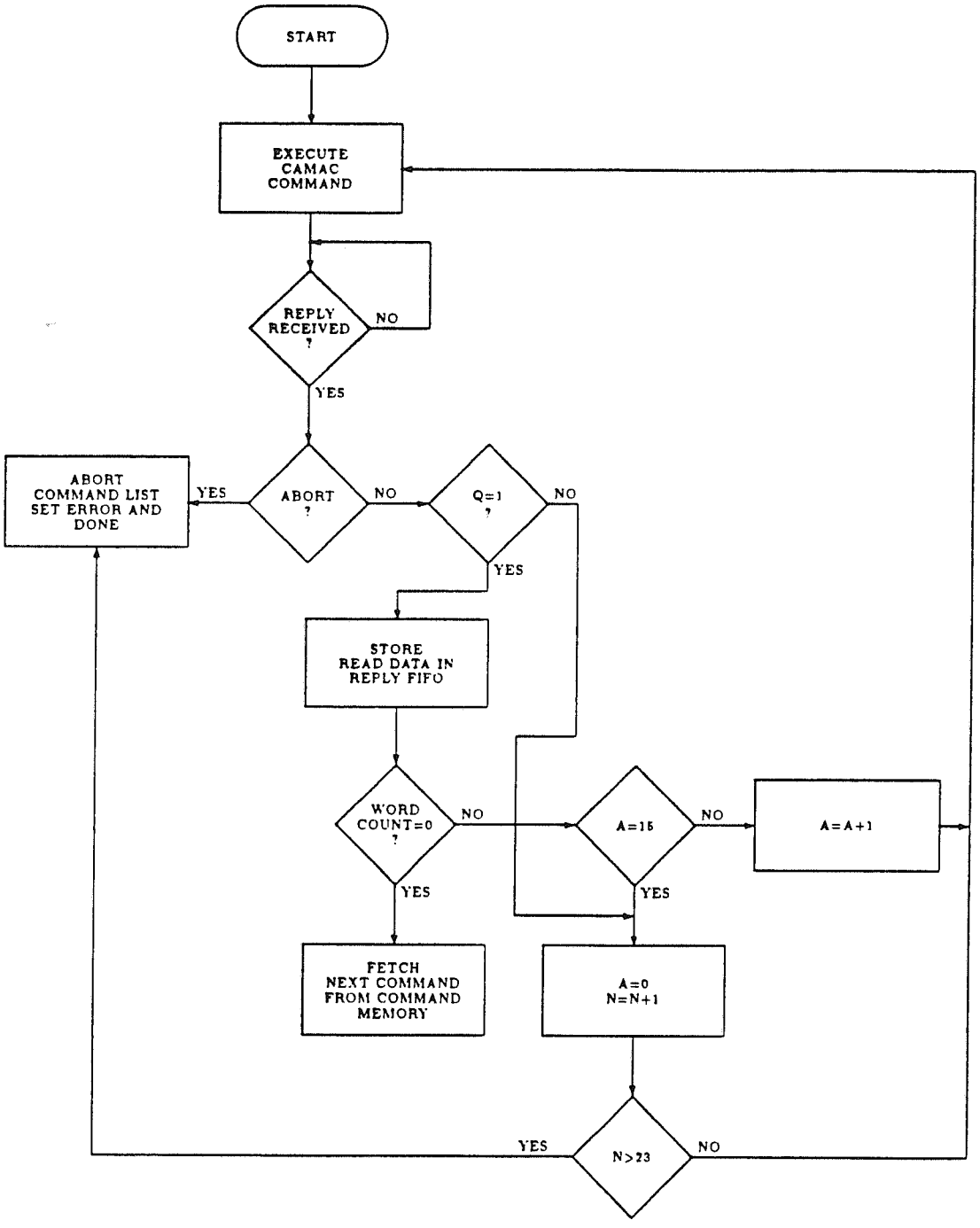


Figure 4 Q-Scan Read Commands

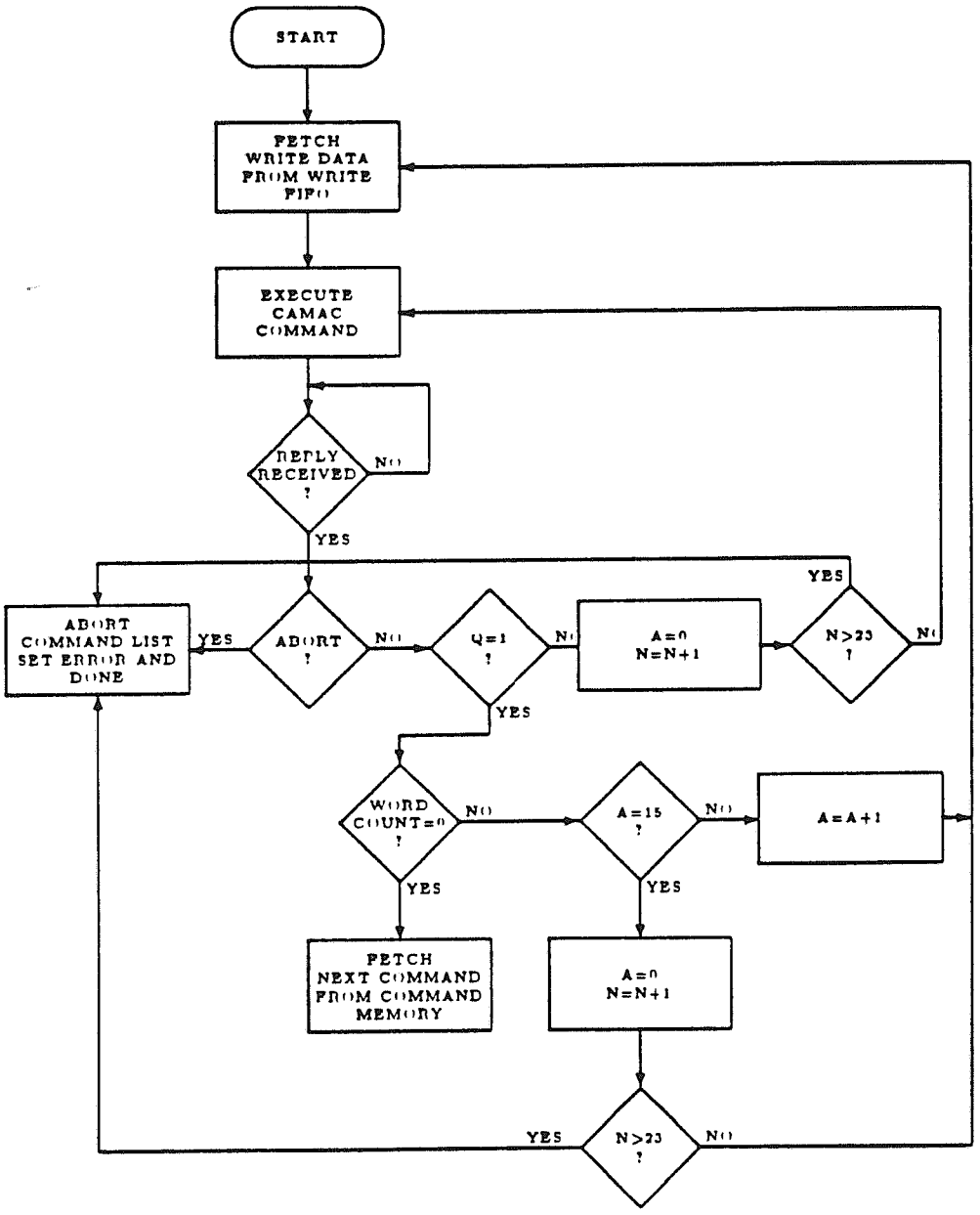


Figure 5 Q-Scan Write Commands

Fast Serial Highway Block Transfers

The 2140 provides five types of Fast (Enhanced Speed) Serial Highway Block Transfers: Single NAF Q-Stop, Single NAF Q-Ignore, Single NAF Q-Repeat (read only), List Sequence Q-Repeat (read only), and List Sequence Q-Ignore. The two List Sequence operation modes require the use of the KSC Model 3830-Z1A List Sequencer Module.

In the Fast Serial Highway mode of operation, transfers to (from) the CAMAC crate are done in a pipelined fashion. Data transmitted onto (or received from) the Serial Highway are FIFO buffered. The 2140 provides two FIFOs (one for write and one for read). When a fast block write command is executed, data for that command may already be in the Write FIFO. In this case, data is transmitted on the highway at maximum speed. If during long block transfers, the VME channel cannot maintain the 3 Mega-byte data rate required by the serial highway, the 2140 will insert "filler" words into the datastream to maintain data on the serial highway. The crate controllers are able to detect these "filler" words, discard them, and report this in the status byte of the Reply message. The 2140 receiver checks the status byte of each word. If the status byte returned indicates a "filler" word, both the status byte and the following data are discarded. If the status byte indicates a valid word, the status byte is stored in the status register and read data (if a read command) is stored in the read reply FIFO.

Fast Serial Highway Command/Reply Sequence

The Block Write Operation Figure 6 (page 36) shows the bytes associated with the Fast Serial Highway Command/Reply sequence for a CAMAC write operation. This byte stream is a logical extension of the CAMAC Standard for single-transactions. A key element in the sequence is the CONTROL byte. The two LSBs of this byte are decoded by the crate controller with the following meaning:

D1	D0	
0	0	The received word is not a "filler" word and it is <u>not</u> the last word in the block.
0	1	The received word is <u>not</u> a "filler" word and it <u>is</u> the last word in the block.
1	0	The received word <u>is</u> a "filler" word and it is <u>not</u> the last word in the block.
1	1	The received word <u>is</u> a "filler" word and it <u>is</u> the last word in the block.

During write operation, the 2140 inserts "filler" words whenever the transmit data FIFO is empty. As soon as additional CAMAC write data is loaded into the FIFO, the 2140 stops sending "filler" words and resumes sending the actual write data. Due to the pipelined nature of the transfer a word count of greater than 2 is needed for write operations.

During read operations, the 2140 inserts "filler" words whenever the reply FIFO exceeds the half-full indicator so that read reply data already on the highway is not lost. As soon as the

FIFO is less than half-full, the 2140 stops sending "filler" words and the actual read data is then accepted.

The status byte in the reply for each word provides an Q and X response from the module as well as error information. After the first word in a block is received, bit 5 of the status byte, normally set to a one to indicate a reply, is set to zero by the crate controller to indicate a "filler" word. If the receiver encounters a "filler" word, it discards the status byte and the following data:

2140-Z1A

COMMAND/REPLY SEQUENCE FOR BLOCK WRITE OPERATION

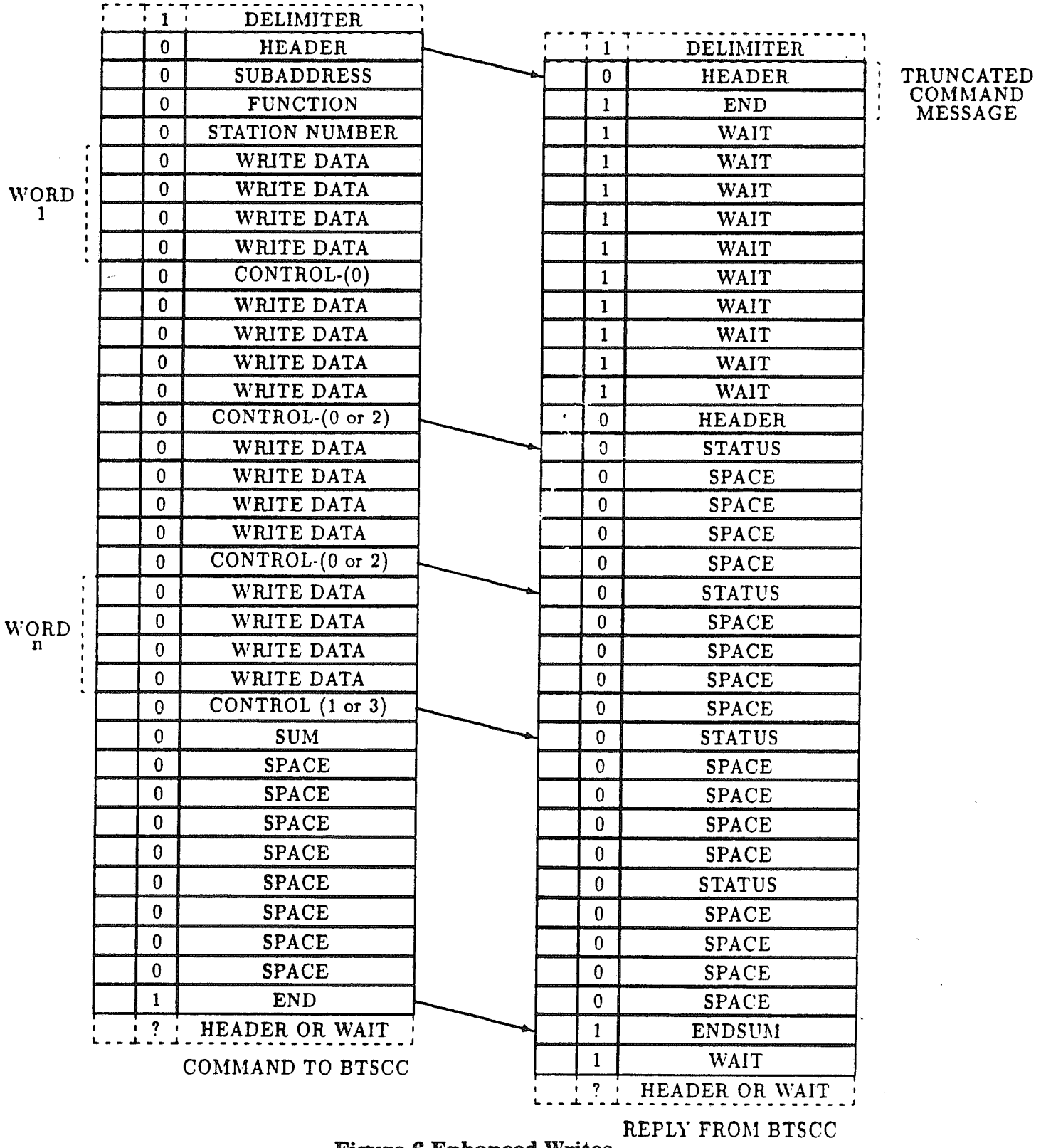


Figure 6 Enhanced Writes

The Block Read Operation, Figure 7 (page 38) shows a Fast Serial Highway Command/Reply sequence for a CAMAC read command. This block mode transaction is very similar to a write operation except that groups of four SPACE bytes are provided in the Command message to allow space for read data (6 bits per byte) in the Reply message.

2140-Z1A

COMMAND/REPLY SEQUENCE FOR BLOCK READ OPERATION

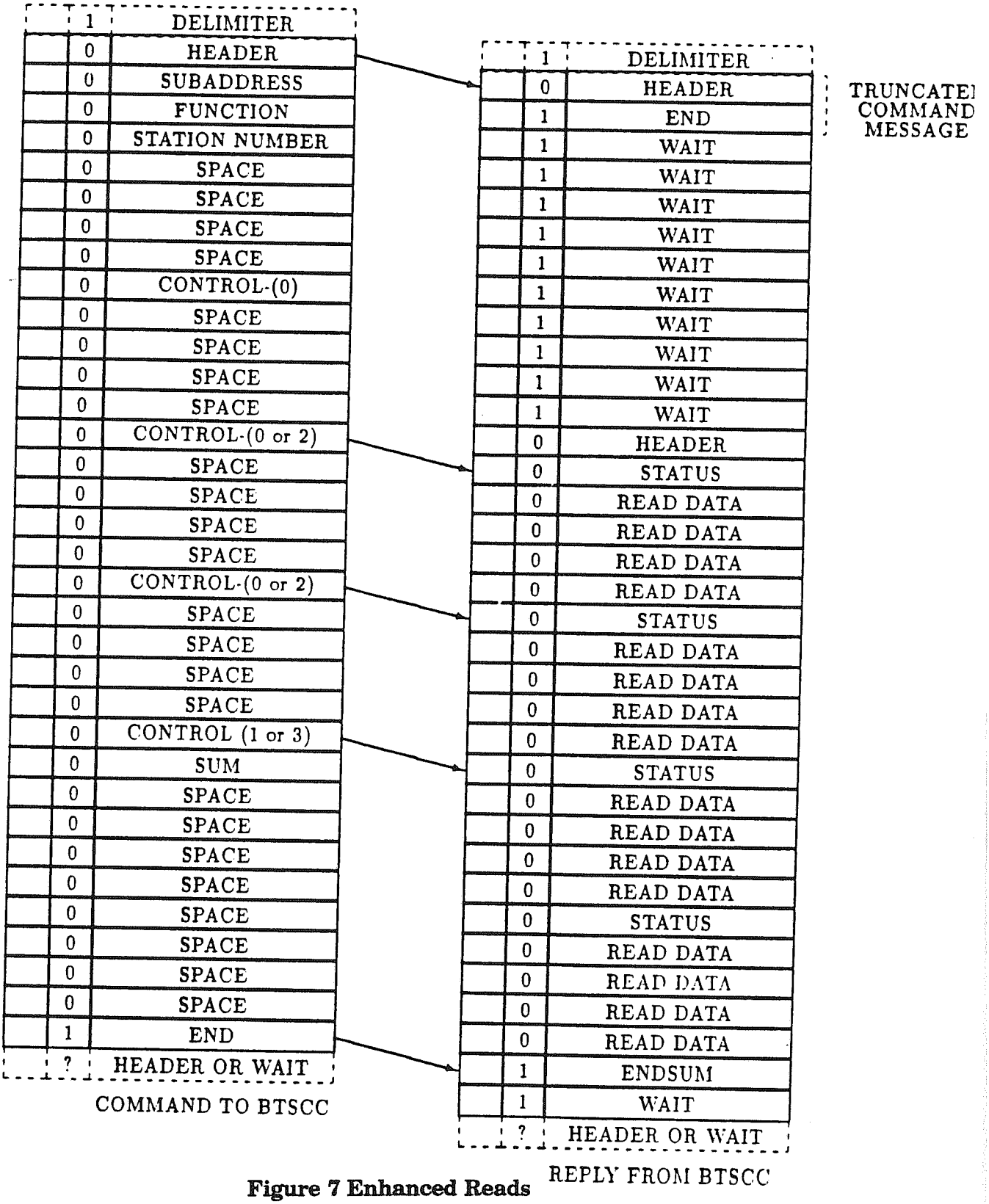


Figure 7 Enhanced Reads

The following is a description of the five Fast Serial Highway Block Transfer Modes:

Q-Stop Single NAF Fast Block Transfer (TM2=1:TM1=0, QM2=0:QM1=0)

To select the Q-Stop Single NAF Fast Block Mode of operation, set command Mode bits <06:05> to 10 and <04:03> to 00. During Q-Stop block transfers, the CAMAC command loaded in the NAF is repeated until a Q-Response of zero is received or the word count is exhausted. The block transfer will also terminate if an "Abort" is generated. The following equation describes "Abort" when in the Q-Stop block transfer mode:

$$\text{ABORT} = \text{NO-Q} + \overline{\text{AD}}(\text{NO-X} + \text{ERR} + \text{TPE} + \text{LPE})$$

Q-Ignore Single NAF Fast Block Transfer (TM2=1:TM1=0, QM2=0:QM1=1)

To select the Q-Ignore Single NAF Fast Block mode of operation, set command mode bits <06:05> to 10 and <04:03> to 01. During a Q-Ignore block transfer, the CAMAC command specified in the NAF is repeated until the word count is exhausted. The block transfer will also terminate if an "Abort" is generated. The following equation describes "Abort" when in the Q-Ignore block transfer mode:

$$\text{ABORT} = \overline{\text{AD}}(\text{NO-X} + \text{ERR} + \text{TPE} + \text{LPE})$$

Q-Repeat Single NAF Fast Block Transfer (TM2=1:TM1=0, QM2=1:QM1=0)

To select the Q-Repeat Single NAF Fast Block mode of operation, set command mode bits <06:05> to 10 and <04:03> to 10. Q-Repeat Fast Block is a read-only mode.

When executing Q-Repeat reads, the 2140 places valid read commands on the Serial Highway as long as the reply FIFO is not half-full. When valid read data with a Q=1 is returned to the 2140, it is stored into the reply FIFO and the Word Count Register is incremented. The block transfer is complete when the word count is exhausted. But, during this time the 2140 will have placed several extra reads onto the highway. Thus, care should be taken when using this mode for CAMAC reads since there is no control on the number of actual CAMAC read cycles performed. The driver will continue to place read commands onto the highway indefinitely if a Q=1 response is not received. Therefore, a strap-selectable hardware timeout (see Strap Option Section of this manual) has been implemented which will "Abort" the block. The following equation describes "Abort" when in the Q-Repeat transfer mode:

$$\text{ABORT} = \text{TMO} + \text{AD}(\text{NO-X} + \text{ERR} + \text{TPE} + \text{LPE})$$

Fast Serial Highway List Sequence Modes

List sequencing allows Fast Serial Highway operations to take place to a predefined list of CAMAC commands. This is accomplished with the use of the KSC Model 3830-Z1A List Sequencer Module. Each CAMAC data word transferred has a corresponding NAF loaded in the List Sequencer Module (LSM) must be loaded with the CAMAC commands used during the block transfer must contain either CAMAC write or CAMAC read commands, but not both.

Control commands may be present in either of the lists as long as data space is allocated to them during the DMA operation.

There are four lists available, two write and two read, in the LSM. Each of these lists can hold 512 CAMAC commands. It is also possible to load the LSM in such a way that only two lists are available, one for reads and one for writes. In this case, each list is 1024 commands long.

List 0 and List 1 of the LSM contain sets of CAMAC read NAFs to be performed. List 2 and List 3 contain sets of CAMAC write NAFs to be performed. When loading the 2140 to execute list sequencing, a special CAMAC command must be loaded in the NAF. This command informs the 3952 Block Transfer Serial Crate Controller (BTSCC)/LSM combination as to which list to use for the block transfer.

Command	NAF List	Data Type
N(30)F(12)A(0)	List 0	Read
N(30)F(12)A(1)	List 1	Read
N(30)F(12)A(2)	List 2	Write
N(30)F(12)A(3)	List 3	Write

When the 3952 BTSCC receives one of these commands, it enables the list-mode block transfer.

Before the list sequence block transfer can begin, the 3830 List Sequencer Module must be loaded. Refer to the 3830-Z1A Operating Manual for loading procedure. After all the NAFs have been loaded into the LSM, an additional word is loaded, which has bit 16 set, that indicates the end of the list. If the end-of-list flag is overrun during list sequencing the LSM will generate a Q=1 and X=0 response. This "special" Q and X response informs the 2140 that the list was overrun. The 2140 does not write this status byte to the status register.

When the 2140 receives the Q=1 X=0 response, it sets the "Abort" bit in the status register. At this time the block word count is checked and if it is not zero and the command list abort bit is set, the command list will abort. As seen before, the 2140 may execute more CAMAC reads than are actually necessary. This will cause the LSM to overrun its list and return the Q=1 X=0 response. Thus, the "Abort" bit is set upon completion of a Fast Serial Highway List Sequence CAMAC read block transfer operation.

Q-Repeat Fast SH List Sequence Block Transfer (TM2=1:TM1=0, QM2=1:QM1=0)

To select the Q-Repeat Fast Serial Highway List Sequence Block Transfer Mode, set command Mode bits <06:05> to 10 and <04:03> to 10.

This mode is only available for CAMAC read commands. During CAMAC reads, read reply data is stored in the reply FIFO whenever a Q=1 response is received in the status byte A Q=1 response also causes the LSM to increment to the next NAF in the list. A Q=0 response indicates to the LSM that valid data has not been received which causes the LSM to continue executing the current NAF. The block transfer continues until the word count is exhausted. The block transfer terminates if an "ABORT" is generated. This mode is not available for CAMAC writes since CAMAC write data words are sent in a pipeline fashion.

Before the block transfer read is initiated, the LSM must be enabled to operate in the Q-Repeat mode. To enable the LSM for Q-Repeat, execute an F(26)A(0) to N (LSM). To disable Q-Repeat, execute a F(24)A(0) to N (LSM).

The 2140/LSM repeats a command indefinitely if a Q=1 response is not obtained. In this case, the hardware timeout may be used to abort the operation.

The following equation is the definition of "ABORT" when using Q-Repeat Fast Serial Highway List Sequence block transfers.

$$\text{ABORT} = \overline{(\text{NO-Q} \cdot \text{NO-X})} + \overline{\text{AD}}(\text{ERR} + \text{NO-X} + \text{TPE} + \text{LPE})$$

NOTE: The "special" X=0 Q=1 response by the LSM is not loaded into the status register by the 2140.

Q-Ignore Fast SH List Sequencer Block Transfer (TM2=1:TM1=0, QM2=0:QM1=1)

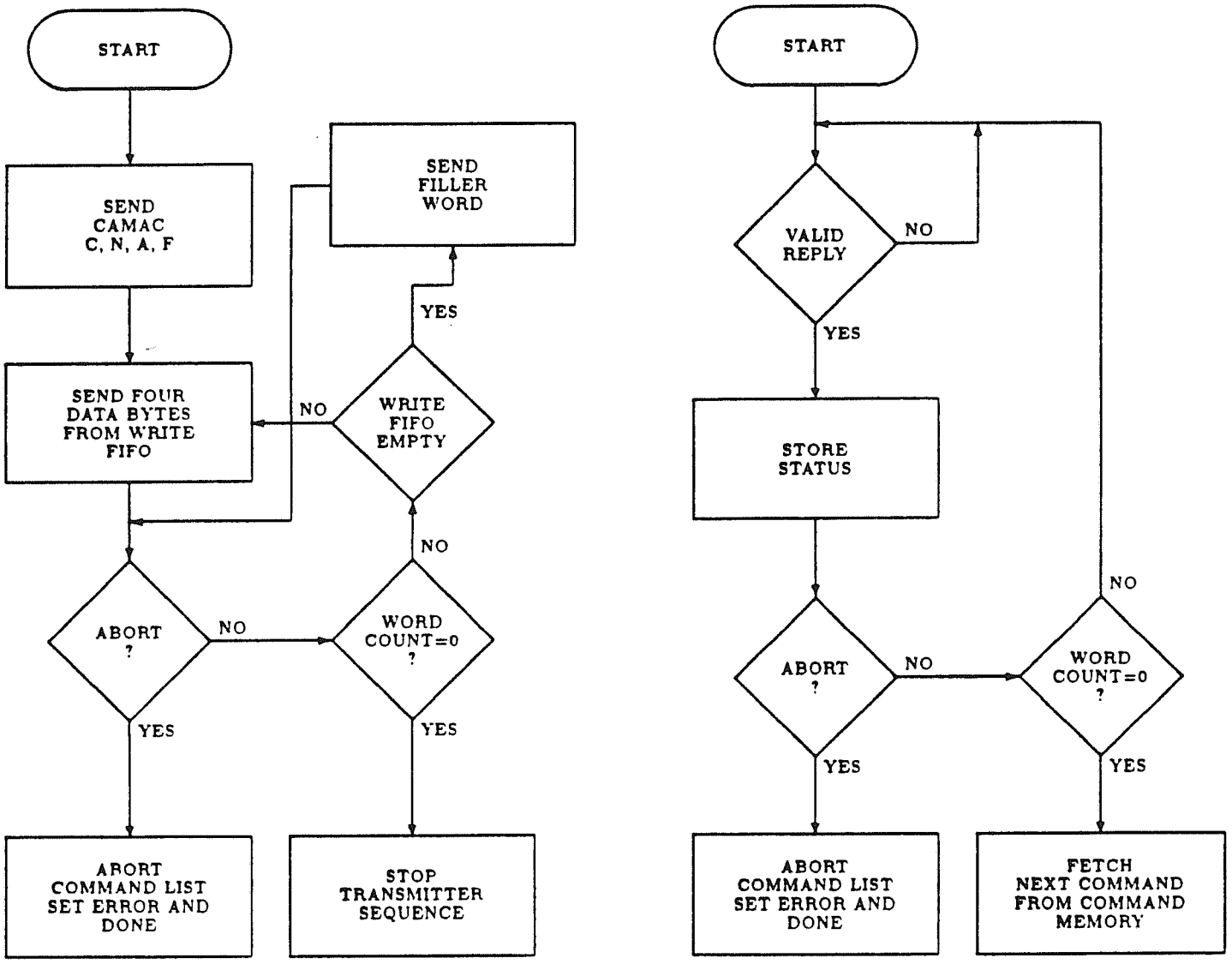
To select the Q-Ignore Fast Serial Highway List Sequence block transfer mode, set command mode bits <06:05> to 10 and <04:03> to 11. In this mode, the NAF pointer in the LSM is incremented after every CAMAC cycle. The block transfer continues until the word count is exhausted. The block transfer terminates if an "ABORT" is generated. The following equation is the definition of "ABORT" when using Q-Ignore Fast Serial Highway List Sequence block transfers.

$$\text{ABORT} = \overline{(\text{NO-Q} \cdot \text{NO-X})} + \overline{\text{AD}}(\text{NO-X} + \text{ERR} + \text{TPE} + \text{LPE})$$

Fast Serial Highway Flow Diagrams

Figures 8 and 9 (pages 42 and 43) are simplified flow diagrams for Fast Serial Highway writes and reads.

2140-Z1A

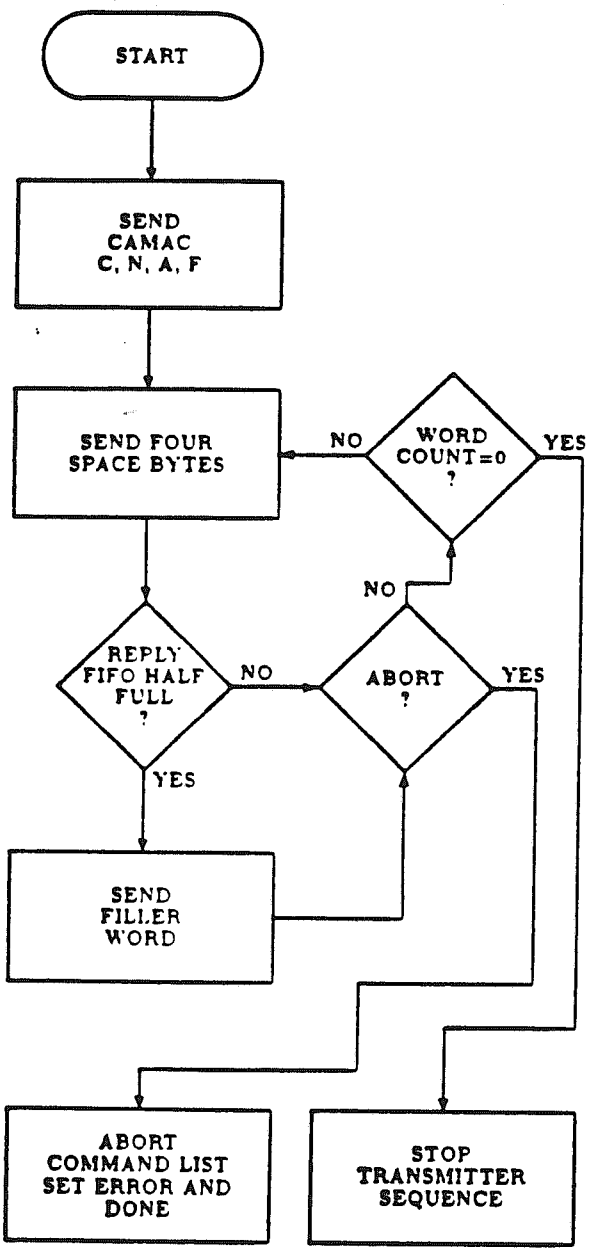


SERIAL HIGHWAY TRANSMITTER SEQUENCE

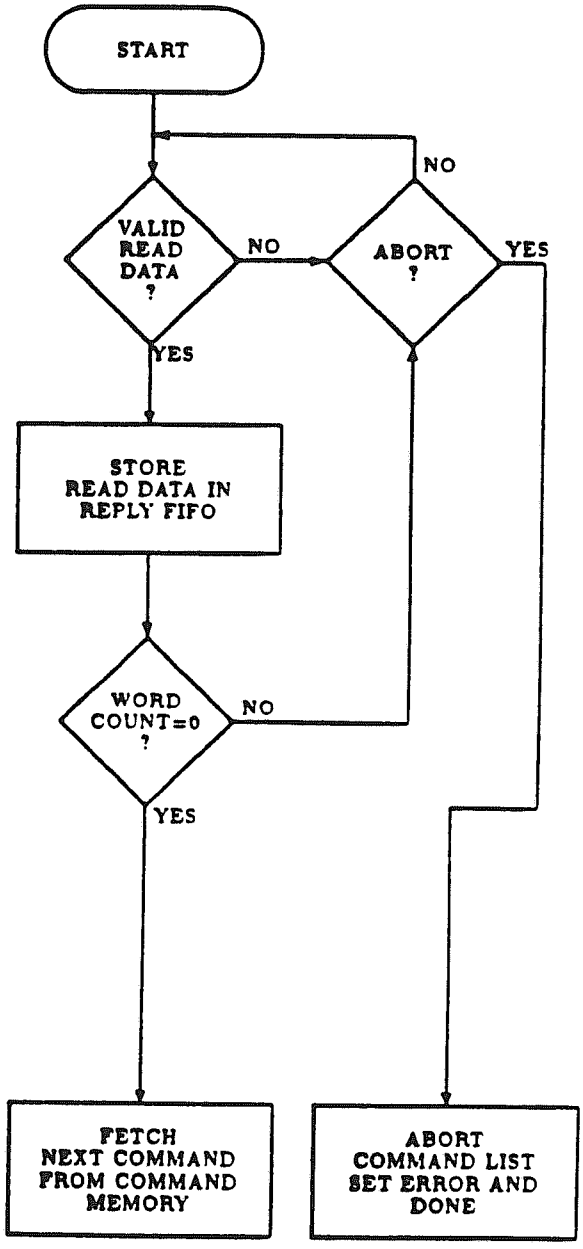
SERIAL HIGHWAY RECEIVER SEQUENCE

THESE SEQUENCES RUN SIMULTANEOUSLY

Figure 8 Enhanced Serial Highway Block Writes



SERIAL HIGHWAY
TRANSMITTER SEQUENCE



SERIAL HIGHWAY
RECEIVER SEQUENCE

THESE SEQUENCES RUN SIMULTANEOUSLY

Figure 9 Enhanced Serial Highway Block Reads

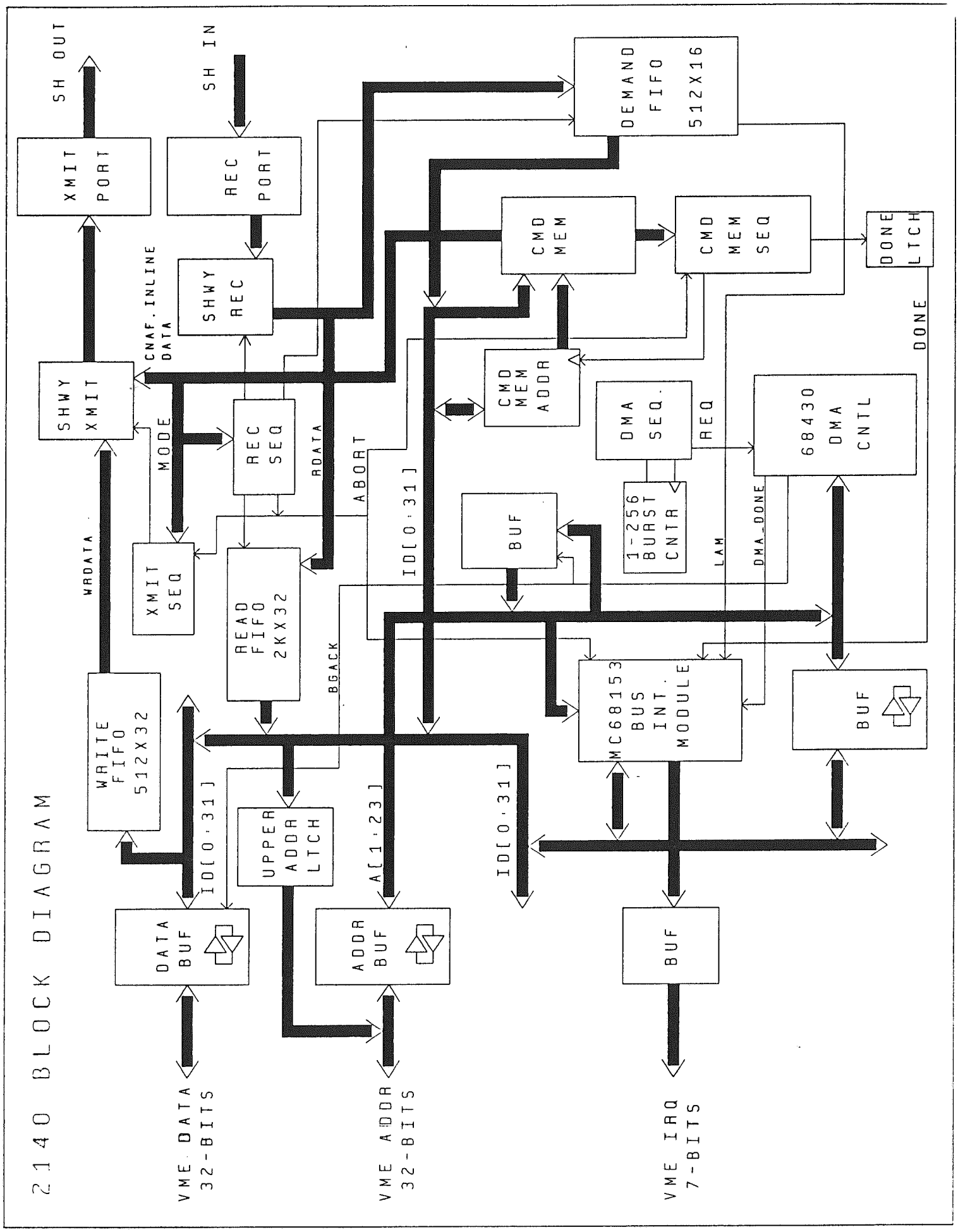
Demands

The Model 3952 Serial Crate Controller (SCC) has the ability to alert the 2140 Enhanced Serial Highway Driver (ESHD) that a CAMAC LAM is pending by asynchronously generating and transmitting a Demand message on the serial highway. The contents of this message are stored in the 2140 ESHD's Demand FIFO. The Demand FIFO allows the 2140 ESHD to store up to 512 Demand messages. If LAM Interrupt enable is set in the Interrupt Control Register, OFFSET $40, and interrupt will be sent to the VMEbus. An interrupt routine, which resets the LAM enable bit, reads one word from the Demand FIFO and then sets the LAM enable bit, will send an interrupt to the VMEbus for each word in the Demand FIFO.

Unbypass and Loop Collapse Operations

When executing a Unbypass or Loop Collapse operation to a 3952, special restrictions apply. These two commands to the 3952 cause the serial highway to be momentarily broken. While the highway if "broken", random data is received by the 2140's serial highway receiver circuitry. This causes erratic operation of the receiver sequencer which results in erroneous activity. To prevent this, the 2140 must know in advance that one of these operations is to occur. To execute these operations successfully, follow the procedure below:

UNBYPASS	Execute a selective-clear {F(23)} command to the 3952 with data = 4000_8.
LOOP COLLAPSE	Execute a selective-set {F(19)} command to the 3952 with data = 2000_8.


2140 BLOCK DIAGRAM
SH OUT
SH IN
XMIT PORT
REC PORT
DEMAND FIFO 512X16
CMD MEM
CMD MEM SEQ
DONE LTCH
SHWY REC
CNAF.INLINE DATA
SHWY XMIT
MODE
REC SEQ
RDATA
ABORT
CMD MEM ADDR
DMA SEQ.
REQ
68430 DMA CNTL
DONE
ID[0:31]
BUF
1-256 BURST CNTR
LAM
DMA_DONE
WRDATA
XMIT SEQ
READ FIFO 2KX32
BGACK
MC68153 BUS INT. MODULE
BUF
WRITE FIFO 512X32
ID[0:31]
UPPER ADDR LTCH
A[1:23]
ID[0:31]
DATA BUF
ADDR BUF
BUF
VME DATA 32-BITS
VME ADDR 32-BITS
VME IRQ 7-BITS

APPENDIX A

MOTOROLA MC68153 BUS INTERRUPTER CHIP

MOTOROLA

SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

MC68153

Advance Information

BUS INTERRUPTER MODULE

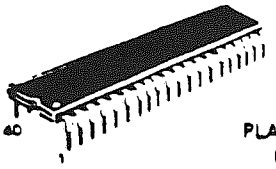
The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to 4 independent sources of interrupt requests and is fully programmable.

- VERSAbus/VMEbus Compatible
- MC68000 Compatible
- Handles 4 Independent Interrupt Sources
- 8 Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

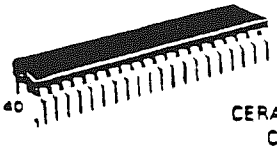
TTL

BUS INTERRUPTER MODULE

ADVANCED LOW POWER SCHOTTKY

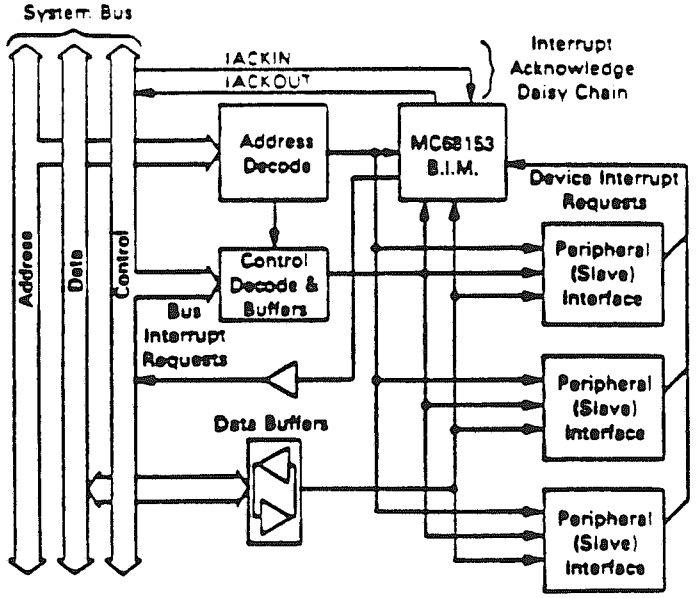


P SUFFIX
PLASTIC PACKAGE
CASE 711-03



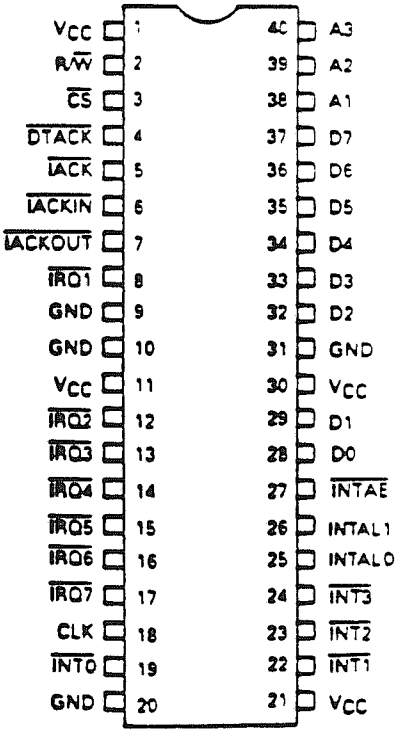
L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM



VERSAbus is a trademark of Motorola.

PIN ASSIGNMENTS



This document contains information on a new product. Specifications and information herein are subject to change without notice

ADI-1057
(Replacing NP-151)

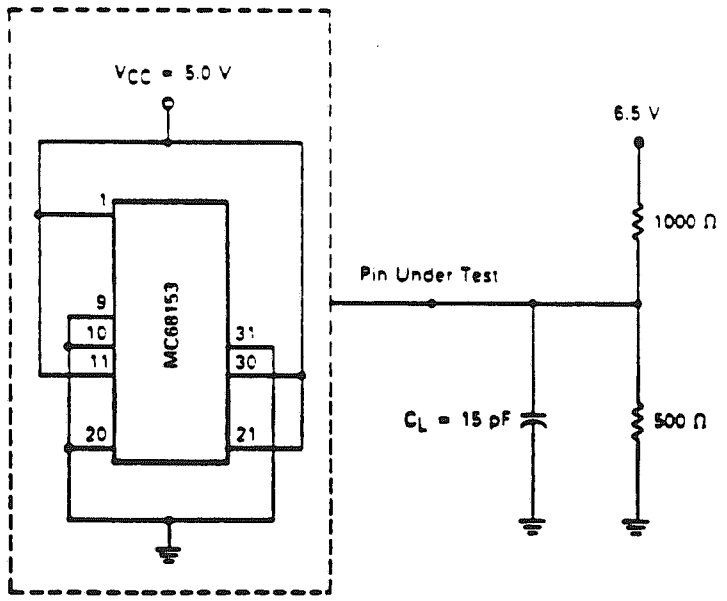
ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Input Current	I_{in}	−30 to +5.0	mA
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{OL}	Twice Rated I_{OL}	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Operating Temperature	T_J	−55 to +175	°C

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	—	V	
Low Level Input Voltage	V_{IL}	—	0.8	V	
Input Clamp Voltage	V_{IK}	—	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
High Level Output Voltage[1]	V_{OH}	2.7	—	V	V_{CC} = MIN, I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}	—	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Output Short Circuit Current[2]	I_{OS}	−15	−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
High Level Input Current	I_{IH}	—	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
Low Level Input Current	I_{IL}	—	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
Supply Current	I_{CC}	225	385	mA	V_{CC} = MAX
Output Off Current (High)	I_{OZH}	—	20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
Output Off Current (Low)	I_{OZL}	—	−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V

AC TEST CIRCUIT — AC Testing of All Outputs



NOTES:
1. Not applicable to open-collector outputs.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. $\overline{IACK}$ Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Test Number[5]	Max (ns)
CLK High to Data Out Valid (Delay)[3]	1	55
CLK High to $\overline{DTACK}$ Low (Delay)[3]	2	40
$\overline{CS}$ High to $\overline{DTACK}$ High (Delay)	3	35
CLK High to Data Out Valid (Delay)[4]	4	55
CLK High to $\overline{INTAE}$ Low (Delay)[4]	5	40
$\overline{IACK}$ High to Data Out High Impedance (Delay)	6	60
$\overline{IACK}$ High to $\overline{DTACK}$ High (Delay)	7	45
$\overline{CS}$ High to Data Out High (Delay)	8	45
$\overline{CS}$ High to $\overline{IRQ}$ High (Delay)	9	60
$\overline{IACK}$ High to $\overline{INTAE}$ High (Delay)	10	35

GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VERSAbus, VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{INT0}$ – $\overline{INT3}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{IRQ1}$ – $\overline{IRQ7}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to from the system bus. These are active high, 3-state pins.

ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

CHIP SELECT — $\overline{CS}$

$\overline{CS}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

READ/WRITE — R/$\overline{W}$

The R/$\overline{W}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

DATA TRANSFER ACKNOWLEDGE — $\overline{DTACK}$

$\overline{DTACK}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM

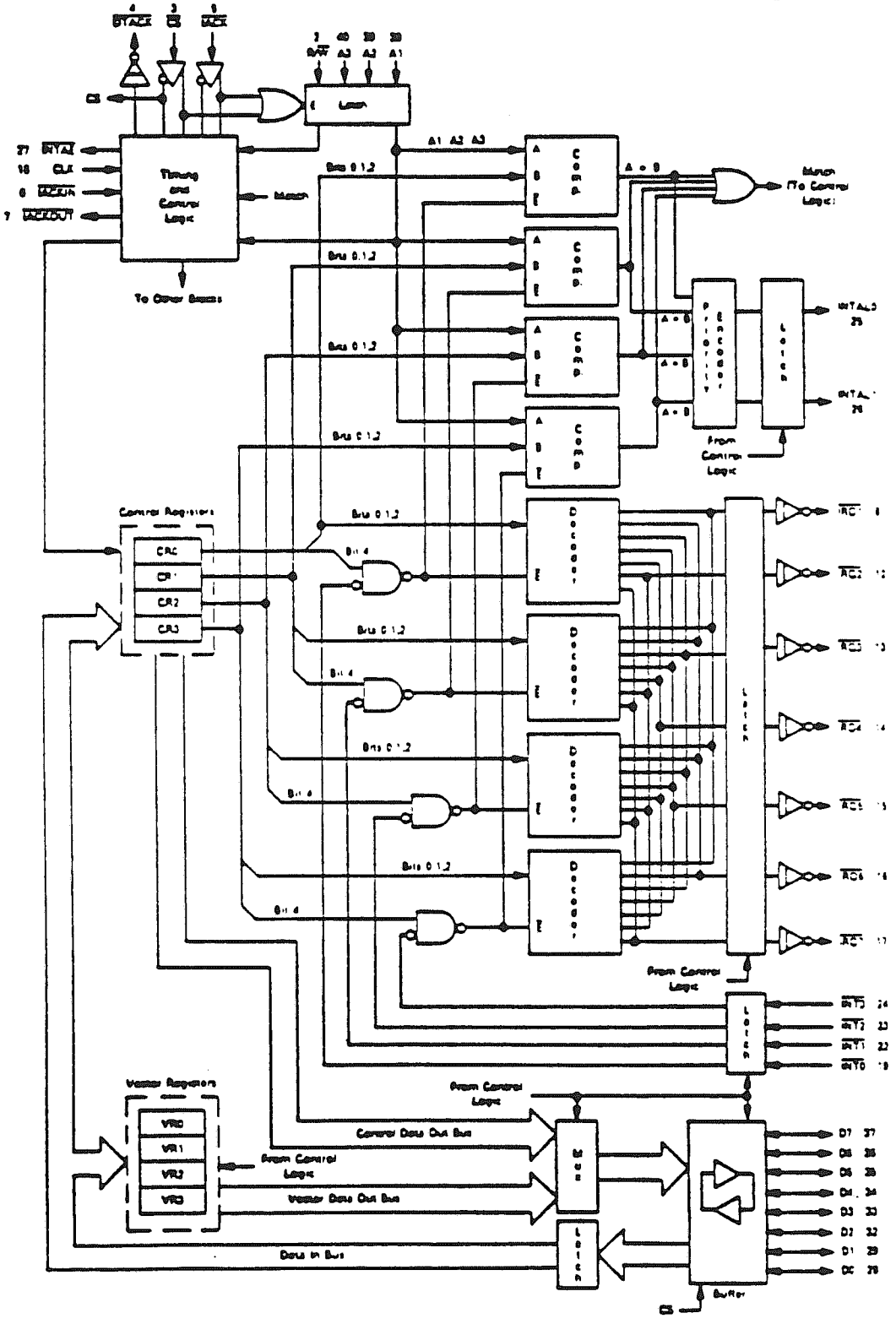
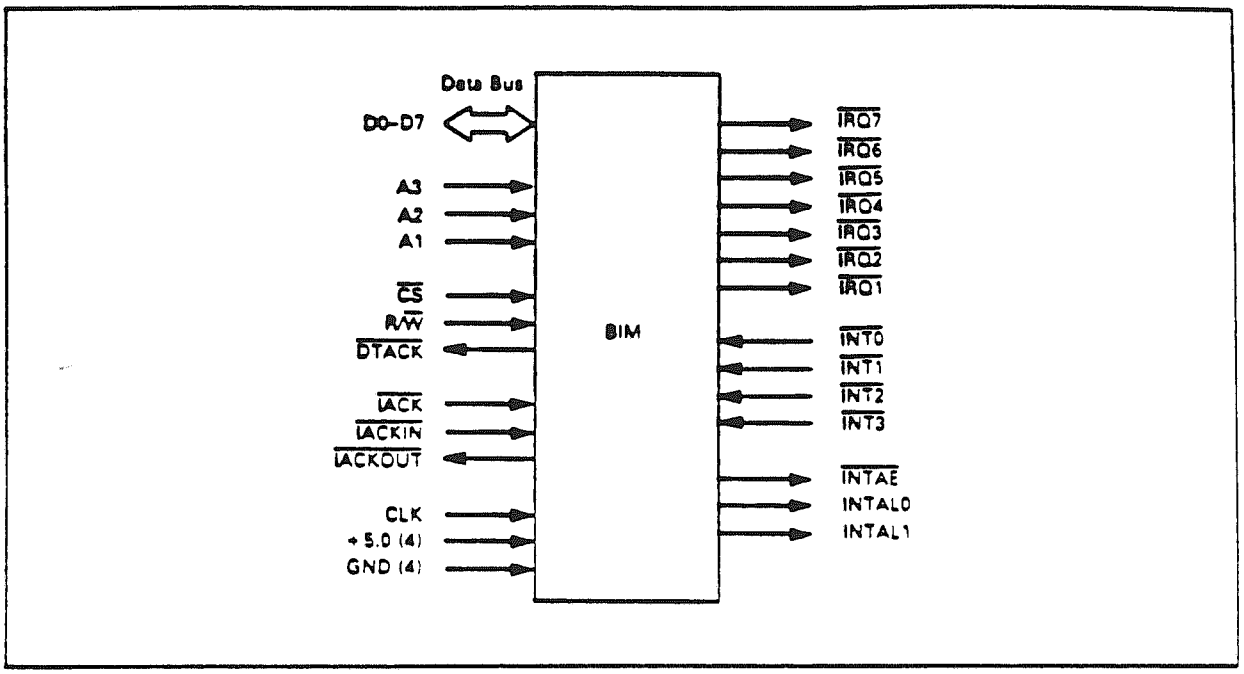


FIGURE 3 — LOGICAL PIN ASSIGNMENT



INTERRUPT ACKNOWLEDGE SIGNALS — $\overline{IACK}$, $\overline{IACKIN}$, $\overline{IACKOUT}$

These three pins support the interrupt acknowledge cycle. A low level on the $\overline{IACK}$ input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After $\overline{IACK}$ is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally and determines if a match exists. Then, if input $\overline{IACKIN}$ is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output $\overline{IACKOUT}$ if *no* match exists.

$\overline{IACKIN}$ and $\overline{IACKOUT}$ form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until $\overline{IACKIN}$ is asserted and not pass the signal on (assert $\overline{IACKOUT}$) if it is to complete the interrupt acknowledge cycle.

BUS INTERRUPT REQUEST SIGNALS — $\overline{IRQ1}$ - $\overline{IRQ7}$

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain $\overline{IRQ1}$ - $\overline{IRQ7}$ high between interrupt requests.

DEVICE INTERRUPT REQUEST SIGNALS — $\overline{INT0}$ - $\overline{INT3}$

$\overline{INT0}$ - $\overline{INT3}$ are active low inputs used to indicate to the BIM that a device wants a bus interrupt.

INTERRUPT ACKNOWLEDGE ENABLE — $\overline{INTAE}$

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt ($\overline{INTx}$) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a $\overline{DTACK}$ signal.

INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when $\overline{INTAE}$ is asserted low.

CLOCK — CLK

The CLK input is used to supply the clock for internal operations of the MC68153.

RESET — $\overline{CS}$, $\overline{IACK}$

Although a reset input is not supplied, an on-board reset is performed if $\overline{CS}$ and $\overline{IACK}$ are asserted simultaneously.

FIGURE 4 — MC68153 REGISTER MODEL

ADDRESS BIT A3	A2	A1	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME
0	0	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0
0	0	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1
0	1	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2
1	1	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3
1	0	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0
1	0	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1
1	1	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2
1	1	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3
			7	6	5	4	3	2	1	0	REGISTER NAME
			REGISTER BIT								

REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device. The other four (VR0 – VR3) are vector registers that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

A value of zero in the field disables the interrupt.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{INTX}$ line is asserted and IRE is cleared, no interrupt request ($\overline{IRQX}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{IN}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{IN}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{DTACK}$ signal, i.e., an internal response. If X/$\overline{IN}$ is set, the vector is not supplied and no $\overline{DTACK}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{IN}$) control register bit is clear. This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. The control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

The MC68153 is compatible with many system buses, however, it is primarily intended for VMEbus, VERSAbus and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to ask for an interrupt of other processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (such as the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritizes interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DSO* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

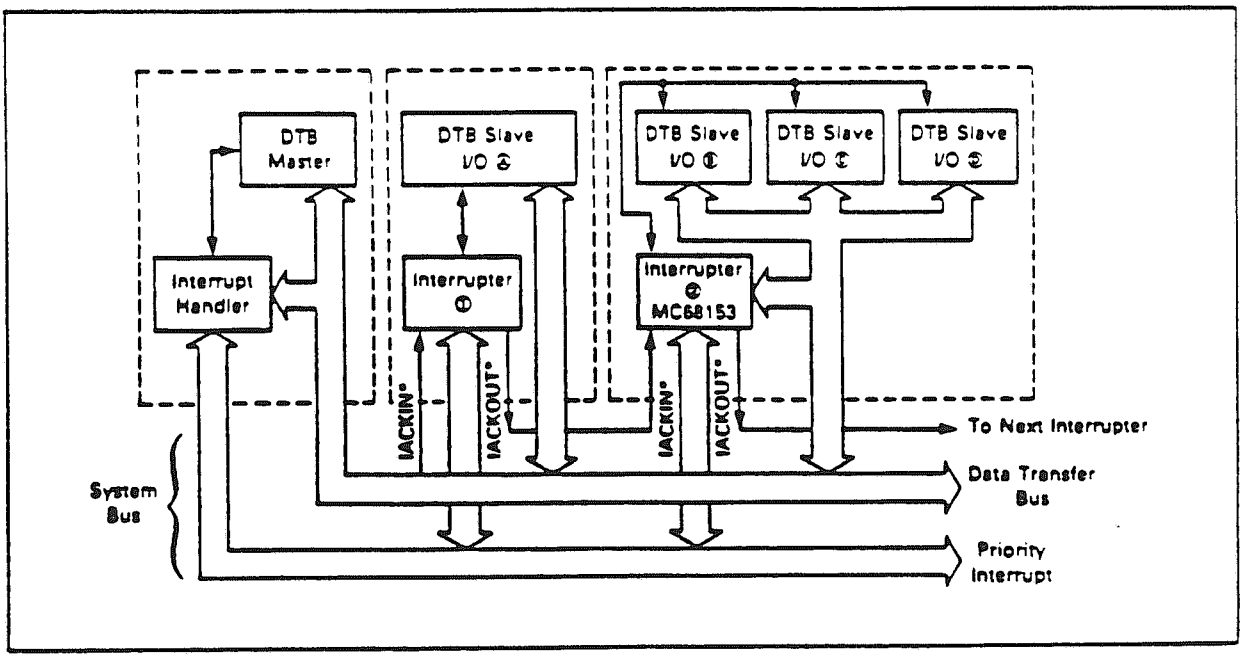
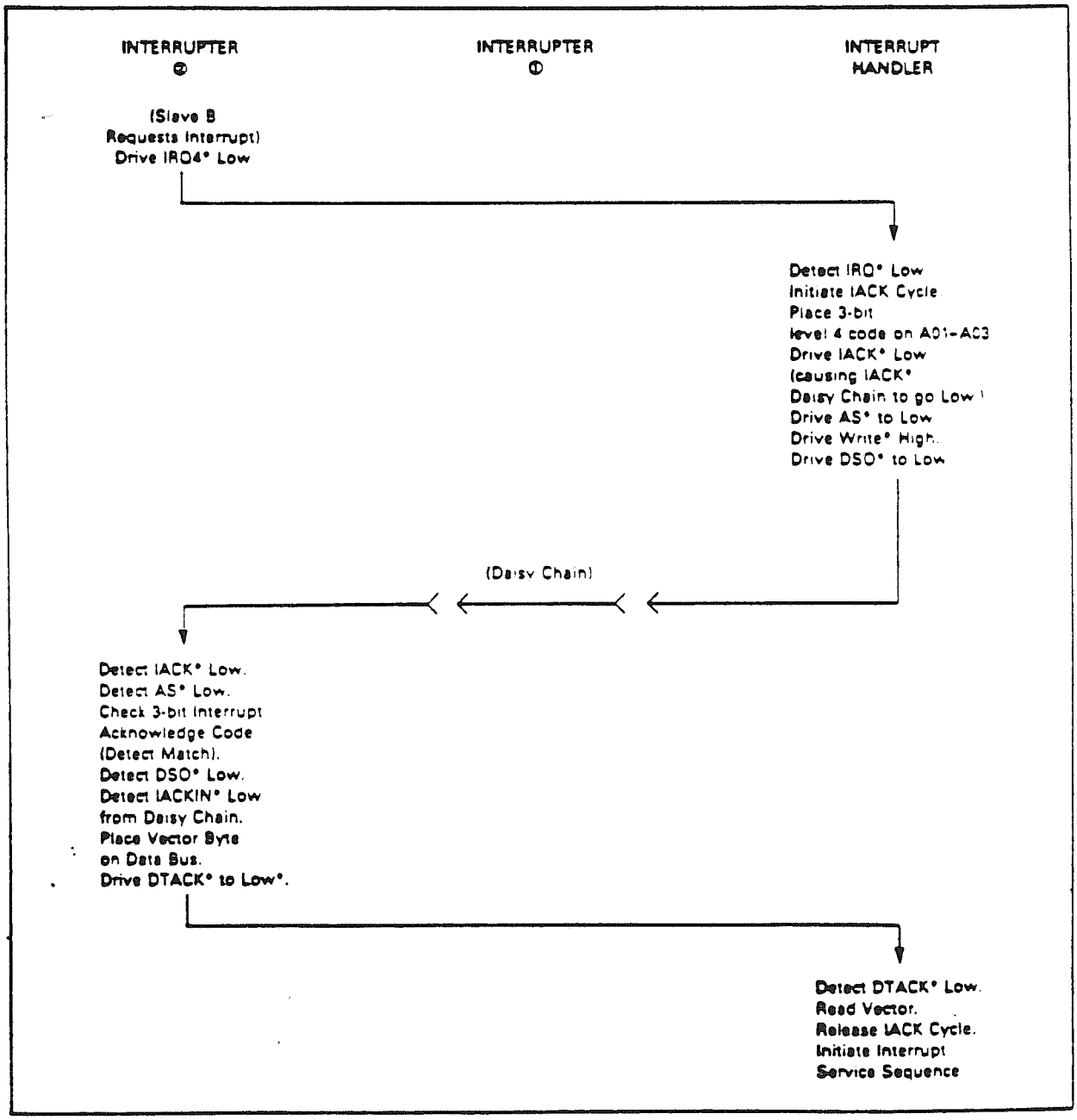


Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector points to its starting address.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM



This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification MVMEBS or VERSAbus Specification M68KVBS. Also, the MC68153 can be used with other buses having similar interrupt structures.

BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the MC68153 interface to VERSAbus or VMEbus. Address Decode and Control Decode are dependent on the application and must be designed to guarantee BIM ac specifications. It is possible in most cases that the decode logic can be shared with the slave devices. Buffers are provided where shown to comply with bus loading and drive specifications. It is also possible that buffers can be shared with the slave bus interface.

READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following signals generate read and write cycles: Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{DTACK}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{W}$ and A1–A3 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{DTACK}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{W}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for $\overline{DTACK}$ is dependent on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus/VERSAbus INTERFACE BLOCK DIAGRAM

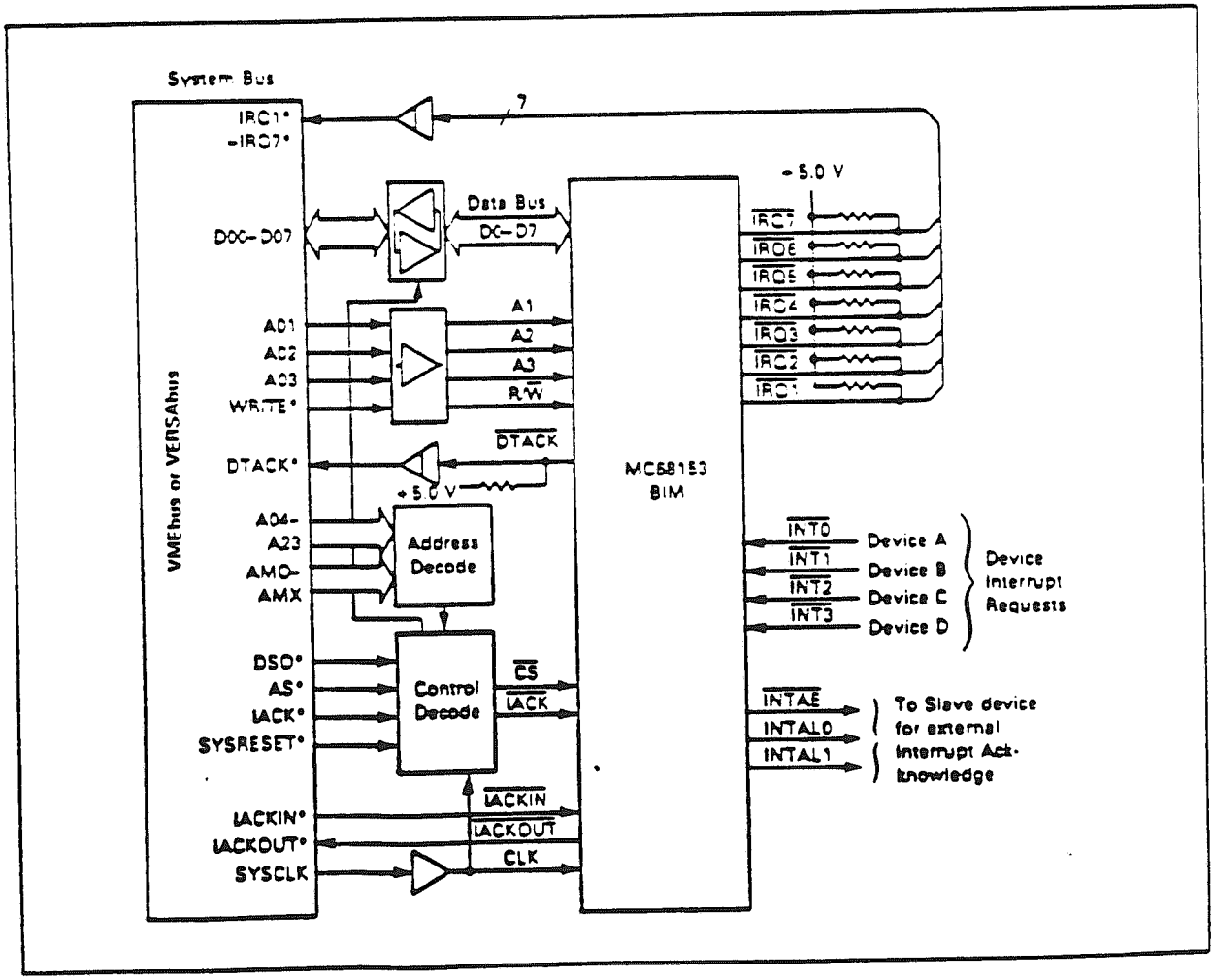


FIGURE 8 — READ CYCLE

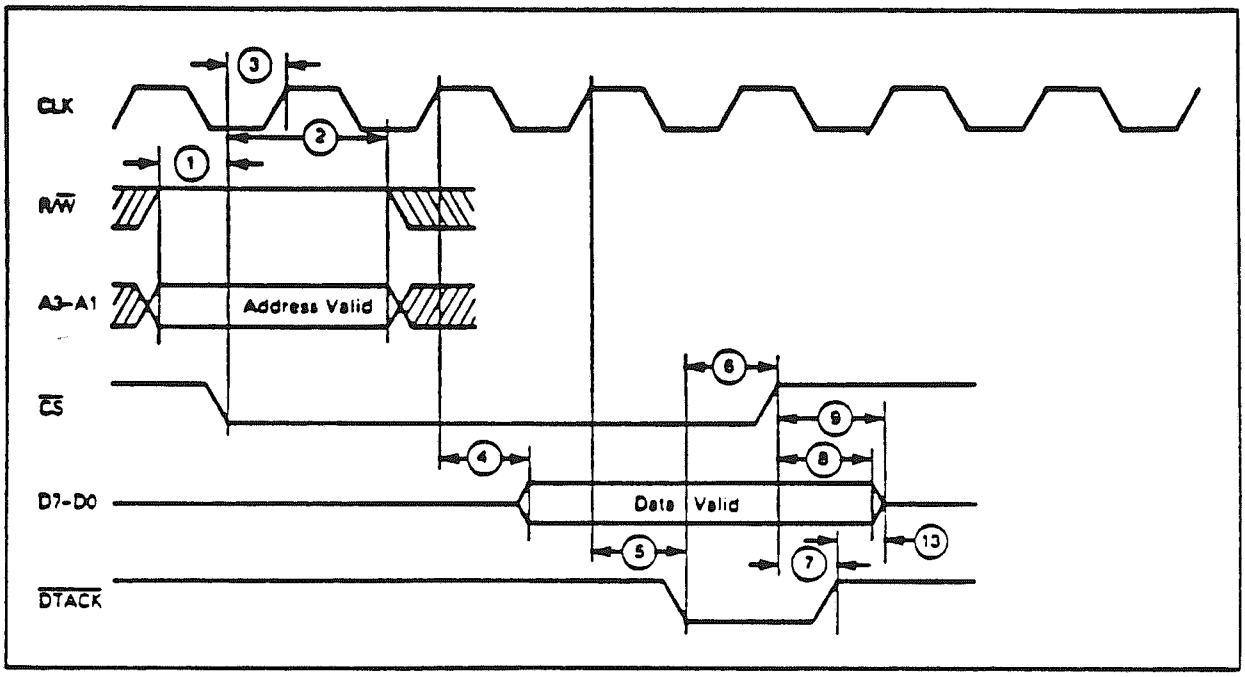
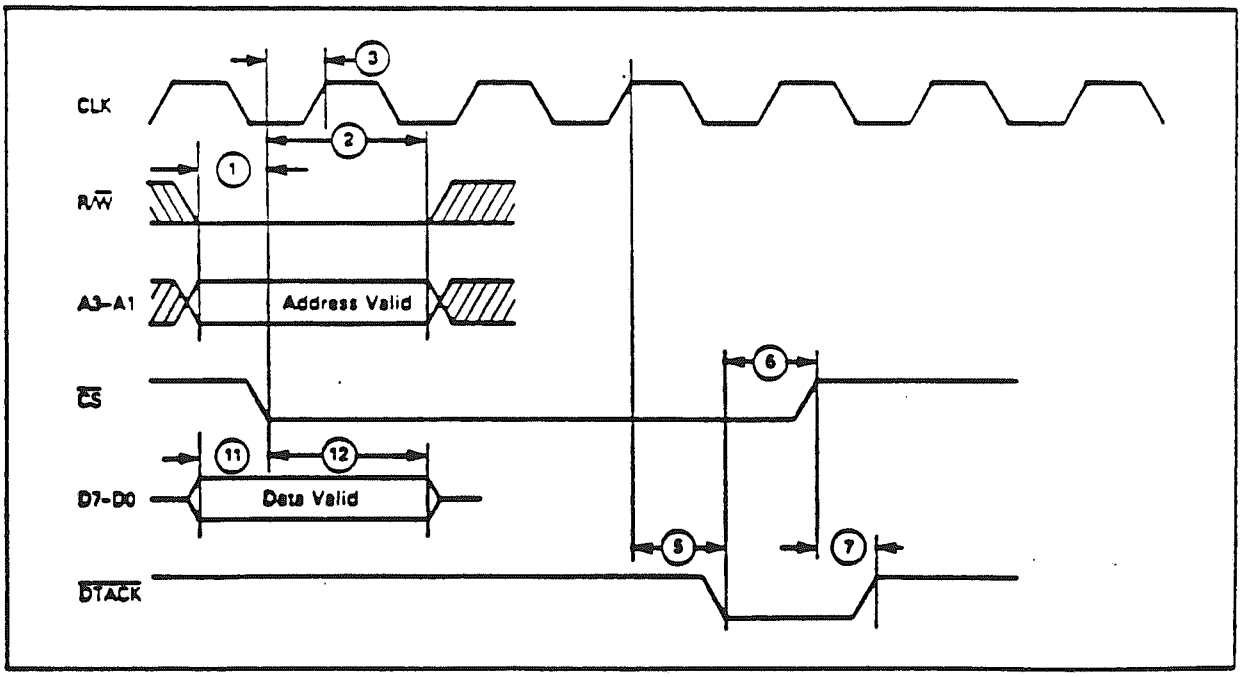


FIGURE 9 — WRITE CYCLE



INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, and $\overline{INT3}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{IRQ1}$–$\overline{IRQ7}$) is asserted. The asserted $\overline{IRQX}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. That $\overline{IRQX}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{IACK}$ low. R/$\overline{W}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{IACKIN}$ is not asserted. Asserting $\overline{IACK}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{IACKIN}$ is not asserted), another Interrupter has responded to the $\overline{IACK}$ cycle. The cycle will end, the chip $\overline{IACK}$ is negated, and no additional action is required.

2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{IACKIN}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{IACKOUT}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.

3. Respond internally — For this case, $\overline{IACKIN}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{DTACK}$ signal asserted. $\overline{IACKOUT}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{INTERNAL}$ control register bit (X/$\overline{IN}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{IN}$ bit sets this response either internally (X/$\overline{IN}$ = 0) or externally (X/$\overline{IN}$ = 1).

4. Respond externally — For the final case, $\overline{IACKIN}$ is also asserted, a match is found and the associated control register has X/$\overline{IN}$ bit set to one. The MC68153 does not assert $\overline{IACKOUT}$ and does assert $\overline{INTAE}$ low. $\overline{INTAE}$ signals that the requesting device must complete the IACK cycle (supplying a vector and $\overline{DTACK}$) and that the 2-bit code contained on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

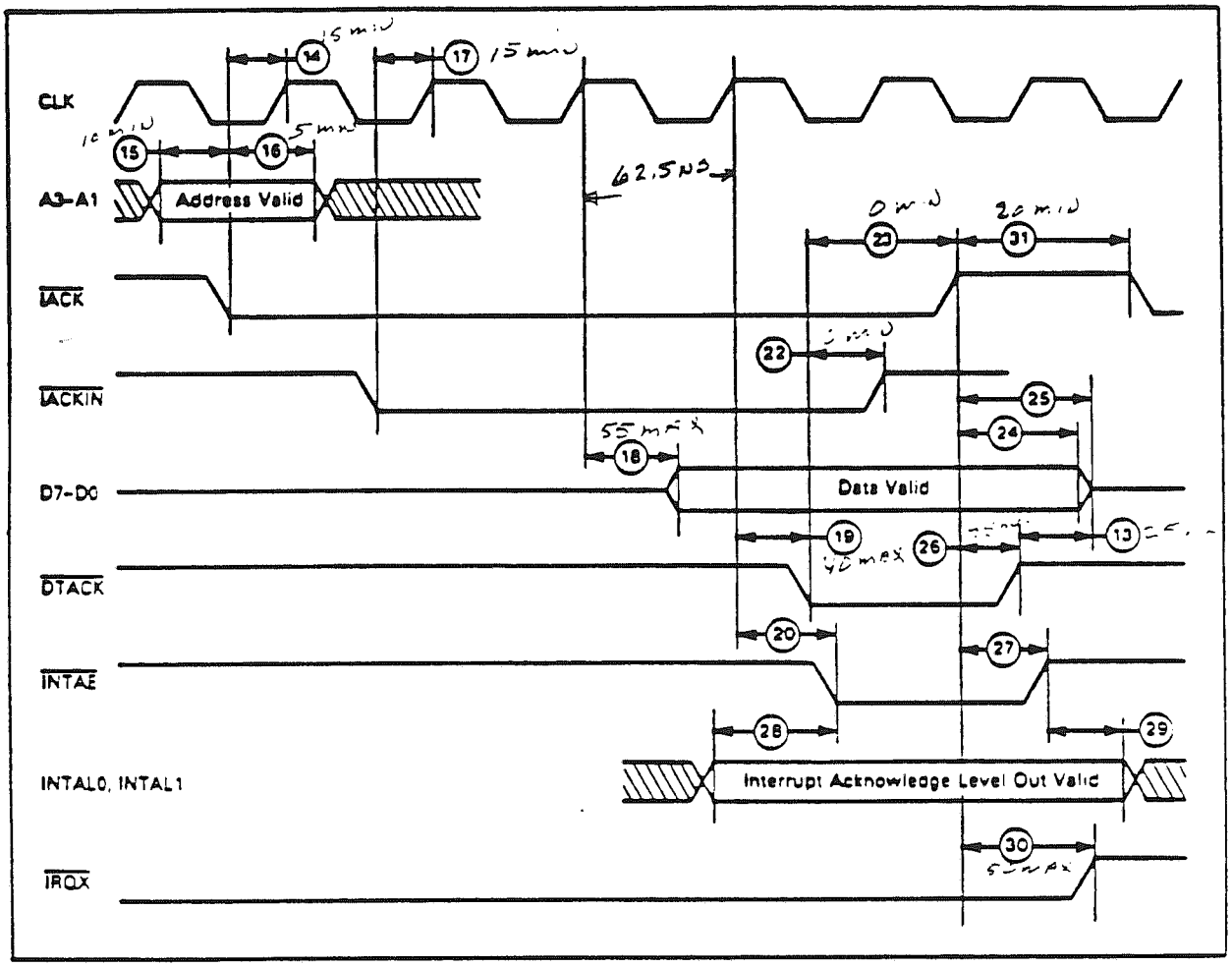
1. One or more device interrupt inputs ($\overline{INT0}$–$\overline{INT3}$) has been asserted and corresponding control bit IRE value is one.
2. $\overline{IACK}$ asserted.
3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the highest number requester, that is, $\overline{INT3}$ has highest priority and $\overline{INT0}$ has lowest.
4. Control register bit X/$\overline{IN}$ of matching interrupt source must be zero.
5. $\overline{IACKIN}$ asserted.

The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{DTACK}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{INTAE}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{DTACK}$ released) after $\overline{IACK}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{IRQX}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{IACKOUT}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{INT0}$–$\overline{INT3}$ after $\overline{IACK}$ is asserted are locked out to prevent any race conditions on the daisy chain.

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR



External Interrupt Acknowledge

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{IN}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{DTACK}$ must be supplied by an external device. $\overline{INTAE}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{DTACK}$. The cycle is terminated after $\overline{IACK}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{IACKOUT}$ is not asserted and new device interrupts are disabled for reasons discussed above.

Pass On IACK Daisy Chain

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{IACKIN}$ is asserted. The following conditions are thus met:

1. $\overline{IACK}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{IACKIN}$ is asserted.

$\overline{IACKOUT}$ is asserted if these conditions are valid. This output drives $\overline{IACKIN}$ of the next interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{IACKOUT}$ is negated after $\overline{IACK}$ is negated.

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

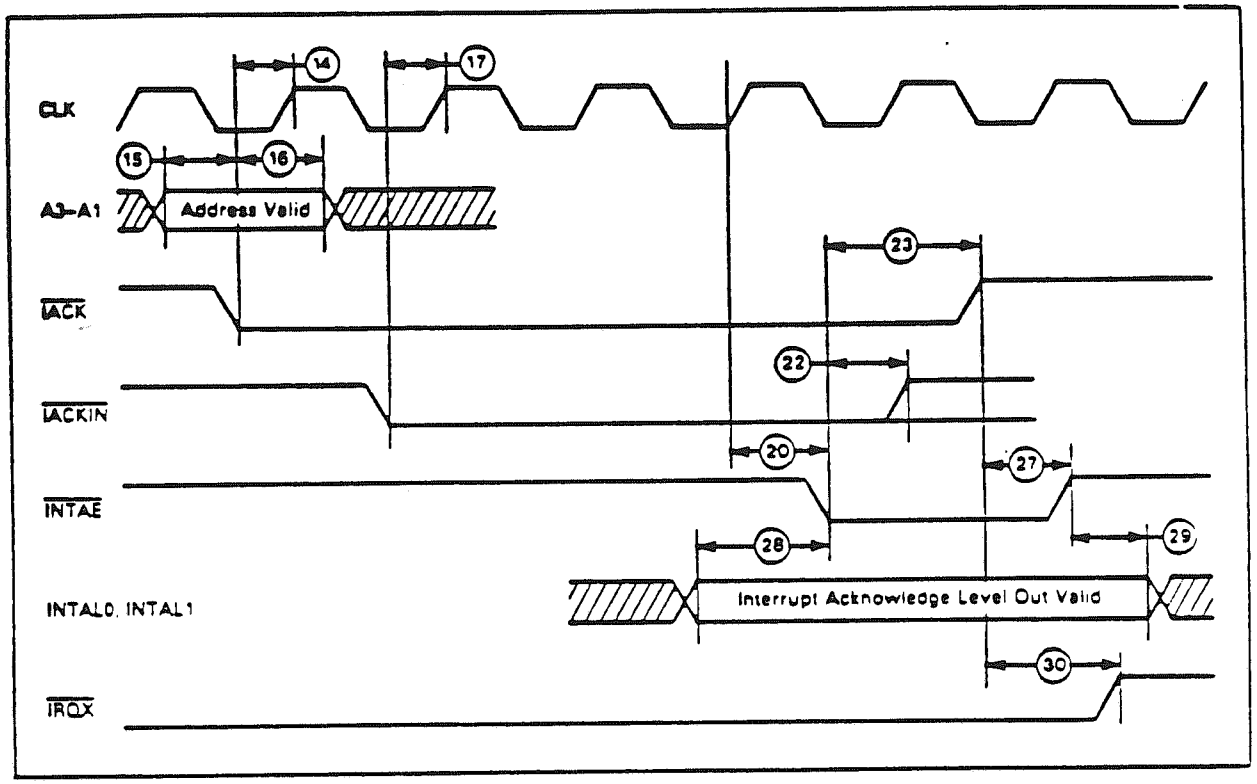
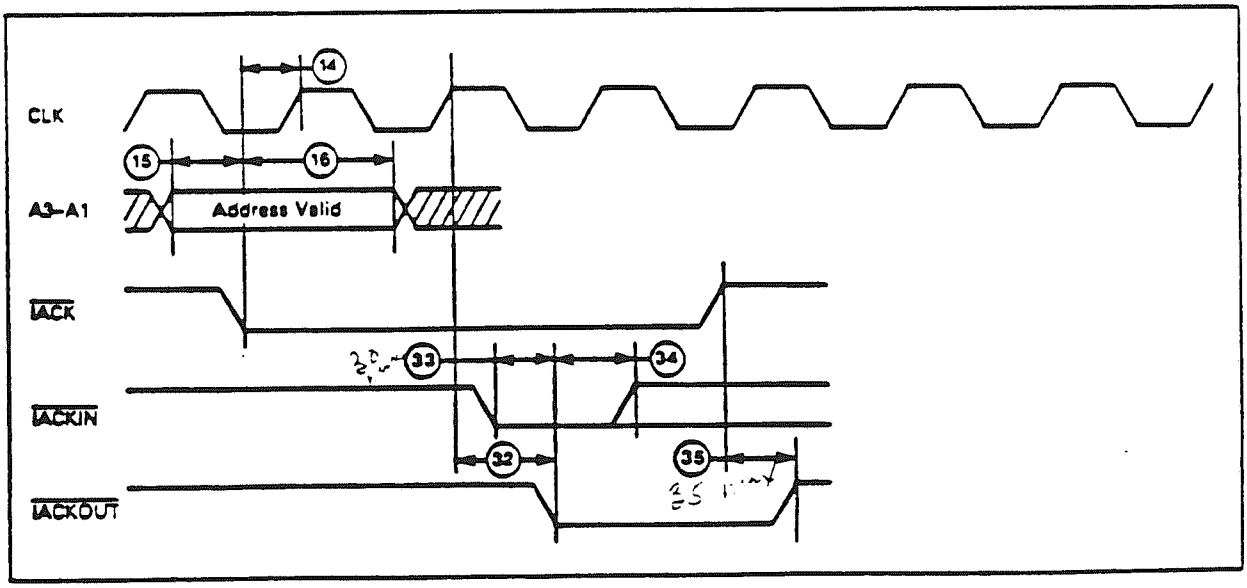


FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — IACKOUT



CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus and VERSAbus applications derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14).

FIGURE 13 — RESET

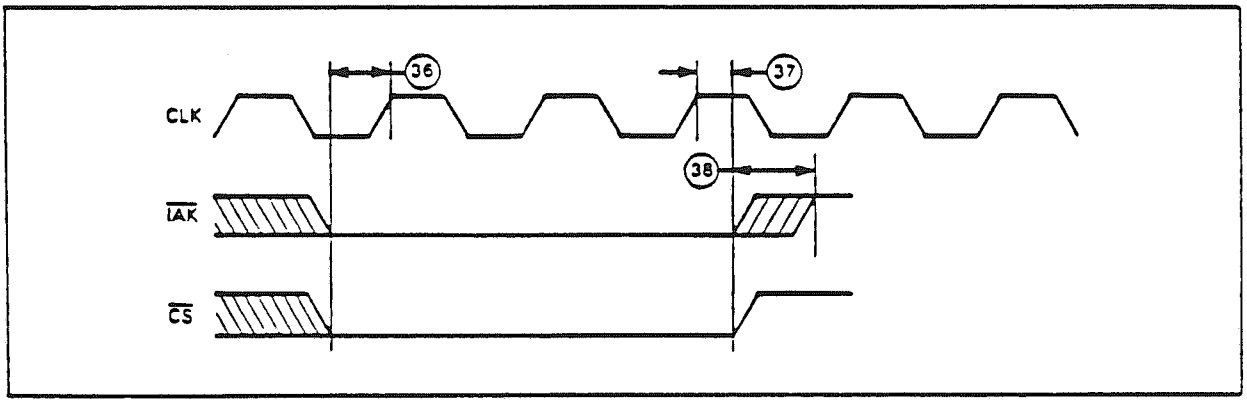


FIGURE 14 — CLOCK WAVEFORM

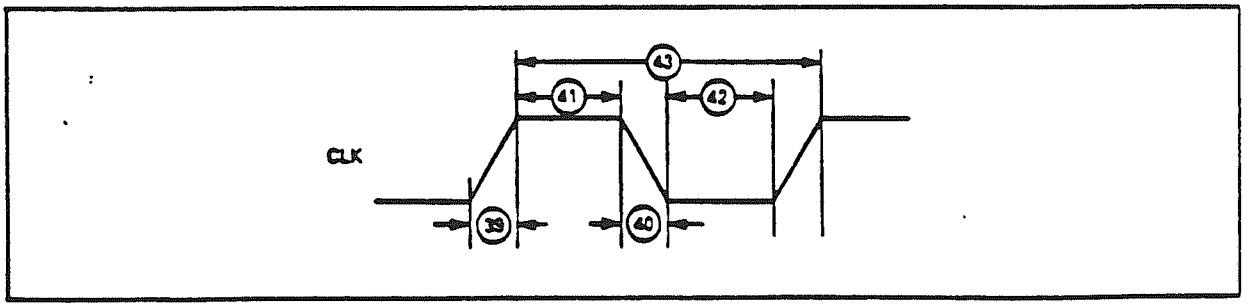


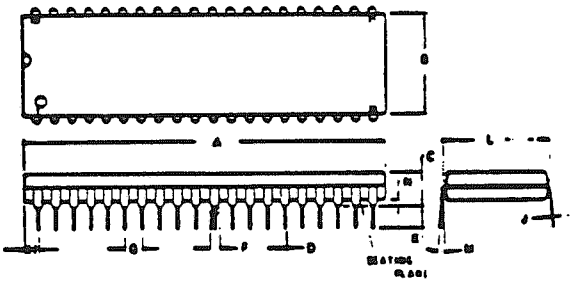
TABLE 1
AC PERFORMANCE SPECIFICATIONS
(V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Number	Characteristic	Min	Max	Units	Notes
1	R/W, A1–A3 Valid to CS Low (Setup Time)	10	—	ns	
2	CS Low to R/W, A1–A3 Invalid (Hold Time)	5.0	—	ns	
3	CS Low to CLK High (Setup Time)	15	—	ns	1
4	CLK High to Data Out Valid (Delay)	—	55	ns	2
5	CLK High to DTACK Low (Delay)	—	40	ns	2
6	DTACK Low to CS High	0		ns	
7	CS High to DTACK High (Delay)	—	35	ns	10
8	CS High to Data Out Invalid (Hold Time)	0	—	ns	
9	CS High to Data Out High-Impedance (Hold Time)	—	80	ns	
10	CS High to CS or IACK Low	20	—	ns	
11	Data In Valid to CS Low (Setup Time)	10	—	ns	
12	CS Low to Data In Invalid (Hold Time)	5.0	—	ns	
13	DTACK High to Data Out High-Impedance	—	25	ns	10
14	IACK Low to CLK High (Setup Time)	15	—	ns	1
15	A1–A3 Valid to IACK Low (Setup Time)	10	—	ns	
16	IACK Low to A1–A3 Invalid (Hold Time)	5.0	—	ns	
17	IACKIN Low to CLK High (Setup Time)	15	—	ns	1, 8
18	CLK High to Data Out Valid (Delay)	—	55	ns	3
19	CLK High to DTACK Low (Delay)	—	40	ns	3
20	CLK High to INTAE Low (Delay)	—	40	ns	3
22	DTACK Low to IACKIN High	0	—	ns	8
23	DTACK Low to IACK High	0	—	ns	
24	IACK High to Data Out Invalid (Hold Time)	0	—	ns	
25	IACK High to Data Out High Impedance (Delay)	—	60	ns	
26	IACK High to DTACK High (Delay)	—	45	ns	10
27	IACK High to INTAE High (Delay)	—	35	ns	
28	INTAL0, INTAL1 Valid to INTAE Low (Setup Time)	1.0	2.0	CLK Per	
29	INTAE High to INTAL0, INTAL1 Invalid (Hold Time)	1.0	2.0	CLK Per	
30	IACK High to IRQx High (Delay)	—	50	ns	7, 10
31	IACK High to IACK or CS Low	20	—	ns	
32	CLK High to IACKOUT Low (Delay)	—	40	ns	5
33	IACKIN Low to IACKOUT Low (Delay)	—	30	ns	4, 8
34	IACKOUT Low to IACKIN, IACK High	0	—	ns	8
35	IACK High to IACKOUT High (Delay)	—	35	ns	
36	IACK and CS both Low to CLK High (Setup Time)	15	—	ns	9
37	CLK High to IACK or CS High (Hold Time)	0	—	ns	
38	IACK or CS High to IACK and CS High (Skew)	—	1.0	CLK Per	6
39	Clock Rise Time	—	10	ns	
40	Clock Fall Time	—	10	ns	
41	Clock High Time	20	—	ns	
42	Clock Low Time	20	—	ns	
43	Clock Period	40	—	ns	

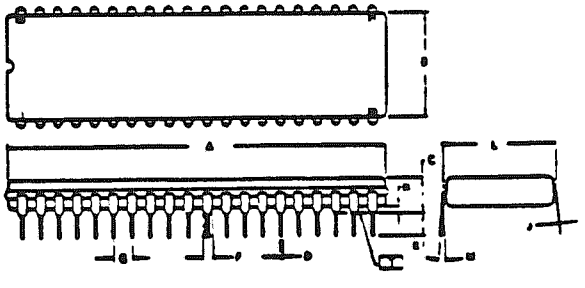
NOTES:

1. This specification only applies if the VBIM had completed all operations initiated by the previous bus cycle when CS or IACK was asserted. Following a normal bus cycle, all operations are completed within 2 clock cycles after CS or IACK have been negated. If IACK or CS is asserted prior to completion of these operations, the new cycle, and hence, DTACK is postponed.
   If the IACK, IACKIN or CS setup time is violated, DTACK may be asserted as shown, or may be asserted one clock cycle later (i.e. IACK will not be recognized until the next rising edge of the clock).
2. Assumes that 3 has been met.
3. Assumes that 14 and 17 have both been met.
4. Assumes that 14 has been met. (IACKOUT cannot go low prior to IACKIN going low).
5. Assumes that 14 has been met and IACKIN has been low for at least the amount of time specified by 33.
6. 38 is the minimum skew between the last moment when both IACK and CS are asserted to when both are negated, to insure that an access cycle is not unintentionally started.
7. Assumes no other INTx input is causing IRQx to be driven low.
8. In non-daisy chain systems, IACKIN may be tied low.
9. Failure to meet this spec. causes RESET to be ignored for 1 clock period. It is then necessary to keep these signals low for 3 clock periods instead of 2.
10. Delay time is specified from input signal to Open-Collector Output pulled High thru 1.0 kΩ resistor to +5.5 V.

OUTLINE DIMENSIONS



CASE 711-03
PLASTIC PACKAGE



CASE 734-04
CERAMIC PACKAGE

TYPICAL THERMAL CHARACTERISTICS

Package	θJA (Junction to Ambient) Still Air	Junction Temperature Still Air @ 70°C Ambient
L Suffix	40°C/W	147°C
P Suffix	35°C/W	137°C

MOTOROLA Semiconductor Products Inc.
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APPENDIX B

SIGNETICS SCB68430 DIRECT MEMORY ACCESS INTERFACE CHIP

Signetics

Microprocessor Products

SCB68430
Direct Memory Access Interface (DMAI)

Preliminary Specification

DESCRIPTION

The SCB68430 Direct Memory Access Interface (DMAI) is a single channel interface circuit which is intended to complement the performance and architectural capabilities of the SCN68000 microprocessor. The DMAI functions by transferring a series of operands (data) between memory and a device: operand sizes may be byte, word, or long word. A block is a sequence of operands: the number of operands in the block is determined by a transfer count stored within the DMAI. The SCB68430 can be programmed to utilize single cycle (cycle stealing) or burst data transfers.

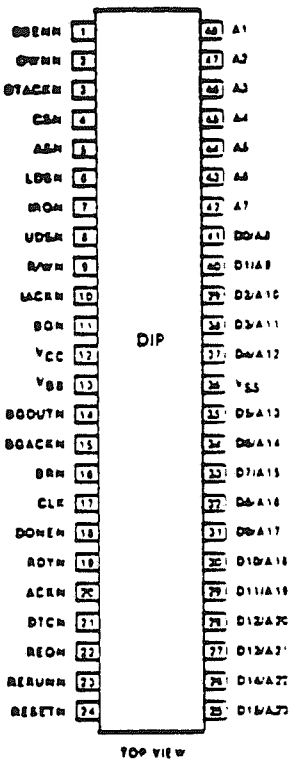
The DMAI provides two interfaces. The microprocessor interface is fully compatible with the SCN68000 microprocessor. The device interface includes lines for requesting, acknowledging, controlling, and timing the data transfers. The DMAI is a single-channel subset of the other 68000 family DMA controllers (68440 and 68450). It is software compatible with these devices and provides similar interfacing signals to both the system bus and the device.

The SCB68430 is constructed using Signetics ISL bipolar technology.

FEATURES

- Bus compatible with SCN68000 microprocessor
- Software compatible with other 68K family DMA controllers
- Single address transfers
- Cycle steal and burst mode operation
- Bus arbitration daisy chain
- Automatic rerun on bus error
- Supports 32-bit transfers for VME bus
- Supports SCN68000 vectored interrupts
- 24-bit address counter
- 16-bit transfer counter
- Maximum transfer rate of 5 Mbytes per second
- Signetics ISL bipolar technology

PIN CONFIGURATION



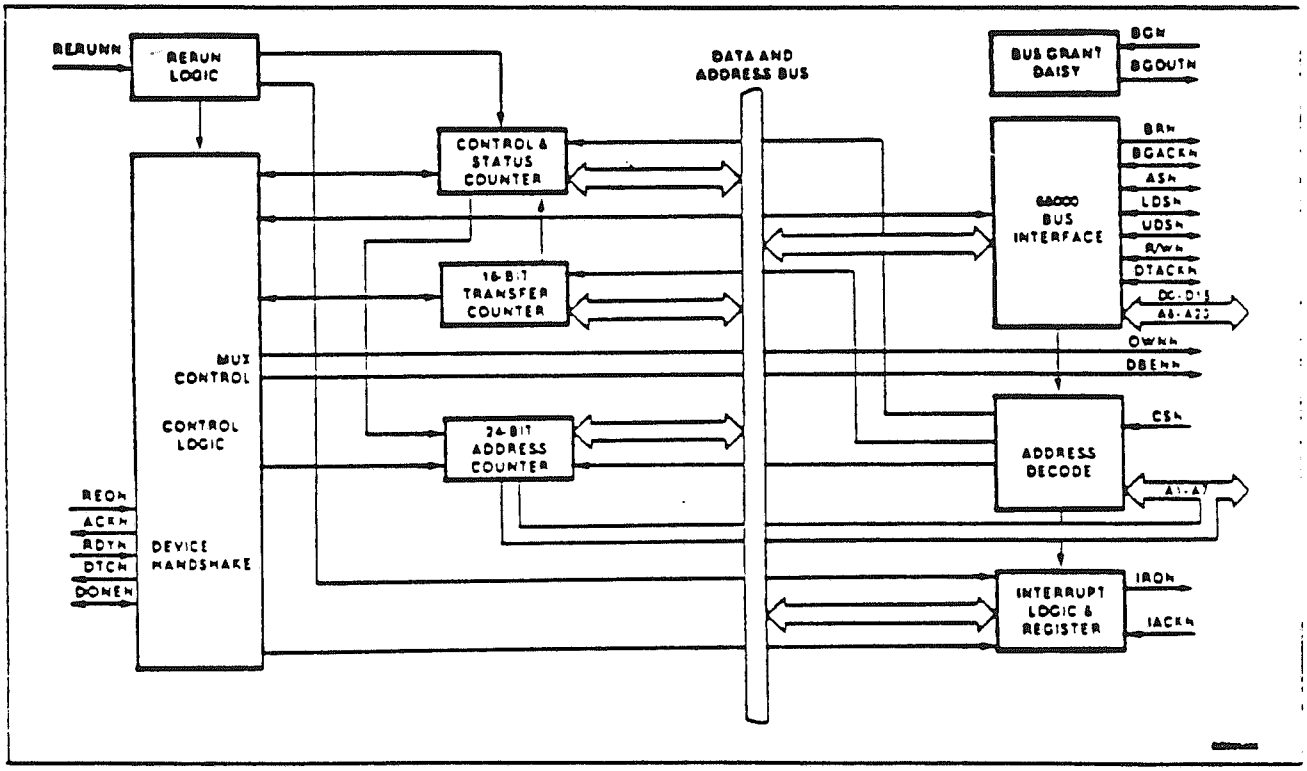
Pin	Function	Pin	Function	Pin	Function
1	NC	19	CLK	36	D7/A15
2	DBENN	20	DONEN	37	D6/A14
3	OWNN	21	RDYN	38	D5/A13
4	DTACKN	22	ACKN	39	V_{SS}
5	CSN	23	DTCN	40	NC
6	ASN	24	REQN	41	D4/A12
7	LDSN	25	RERUNN	42	D3/A11
8	RQN	26	RESETN	43	D2/A10
9	UDSN	27	NC	44	D1/A9
10	R/WN	28	D15/A23	45	D0/A8
11	LACKN	29	D14/A22	46	A7
12	BGN	30	D13/A21	47	A6
13	V_{CC}	31	D12/A20	48	A5
14	NC	32	D11/A19	49	A4
15	V_{SS}	33	D10/A18	50	A3
16	BGOUTN	34	D9/A17	51	A2
17	BGACKN	35	D8/A16	52	A1
18	BRN				

Direct Memory Access Interface (DMAI) SCB68430

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%, T_A = 0°C to 70°C	
	10MHz	12.5MHz
Ceramic DIP	SCB68430CAI48	SCB68430CCI48
Plastic DIP	SCB68430CAN48	SCB68430CCN48
Plastic LCC	SCB68430CAA52	SCB68430CCA52

BLOCK DIAGRAM



PIN DESCRIPTION

MNEMONIC	PIN NO.	TYPE	DESCRIPTION
A1 - A7	48 - 42	I/O	Address Lines: Active high, three-state. In the MPU mode, these low order address lines specify which internal register of the DMAI is being accessed. In DMA mode, A1 - A7 are ouputs which provide the low order address bits of the location being accessed. Three-stated in IDLE Mode.
A8 - A23/ D0 - D15	41 - 37 35 - 25	I/O	Address/Data Lines: Active high, three-state. These lines are time multiplexed for data and address leads. The lines OWNN, RWN, CSN, and DBENN are used to control the demultiplexing of the address and data using external circuitry. In MPU mode, the bidirectional data lines (D0 - D15) are used to transfer data between the MPU and the DMAI. In the DMA mode, A8 - A23 provide the high order address bits of the location being accessed. Three-stated in IDLE mode.
ASN	5	I/O	Address Strobe: Active low, three-state. In MPU and IDLE modes, ASN is an input which indicates that the current bus master has placed a valid address on the bus. It is monitored by the DMAI during bus arbitration to ascertain that the previous bus master has completed the current bus cycle. In DMA mode, it is an output indicating that the DMAI has placed a valid address on the bus
UDSN	8	I/O	Upper Data Stobe: Active low, three-state. In MPU and IDLE modes, UDSN is an input which indicates that the upper data byte of the addressed word is being addressed. In DMA mode, it is an output with the same meaning
LDSN	6	I/O	Lower Data Strobe: Active low, three-state. In MPU and IDLE modes, LDSN is an input which indicates that the lower data byte of the addressed word is being addressed. In DMA mode, it is an output with the same meaning
R/WN	9	I/O	Read/Write: Active high for read, low for write, three-state. In MPU mode, R/WN is an input which controls the direction of data flow through the DMAI's input/output data bus interface and, if required, through an external data bus buffer. R/WN high causes the DMAI to place the data from the addressed register on the data bus, while R/WN low causes the DMAI to accept data from the data bus. In DMA mode, R/WN is an output to memory and I/O controllers indicating the type of bus cycle. It is held three-stated during IDLE mode
CSN	4	I	Chip Select: Active low. When low, places the DMAI into the MPU mode. This input signal is used to select the DMAI for programmed data transfers. These transfers take place over D0 - D15 as controlled by the R/WN and A1 - A7 inputs. The DMAI is deselected when CSN is high. CSN is ignored during DMA mode
DTACKN	3	I/O	Data Transfer Acknowledge: Active low, three-state. In MPU mode, DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate that valid data is present on the bus. The signal is negated (driven high) when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive third state a short time after it is negated. In DMA Mode, DTACKN is an input monitored by the DMAI to determine when the addressed device (memory) has latched the data (write cycle) or put valid data on the bus (read cycle)
RESETN	24	I	Master Reset: Active low. Assertion of this pin clears internal control registers (See table 1), initializes the interrupt vector register to H'0F', and sets the status register to the default value B'0000 000X', where X is the state of RDYN. All bidirectional I/O lines are three-stated and the DMAI is placed in the IDLE mode.
CLK	17	I	Clock: Active high. Usually the system clock, but may be any clock meeting the electrical specifications. Used by the DMAI to synchronize device functions and external control lines, and may not be gated off at any time
IRQN	7	O	Interrupt Request: Active low, open collector. This output is asserted, if interrupts are enabled, upon end of transfer, on occurrence of a bus error, and on receipt of an abort from the MPU. The CPU can read the status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DMAI to output an interrupt vector on the data bus.
IACKN	10	I	Interrupt Acknowledge: Active low. When asserted, indicates that the current cycle is an interrupt acknowledge cycle. The DMAI normally responds by placing the contents of the interrupt vector register on the data bus and asserting DTACKN. IACKN is not serviced if the DMAI has not generated an interrupt request.
BRN	16	O	Bus Request: Active low, open collector. BRN is asserted by the DMAI to request ownership of the bus after a DMA request is sensed on the REQN input from the I/O device. It is negated when the bus has been granted (BGN low) and BGACKN has been asserted, or, in burst DMA request mode, if the I/O device negates its request at least one clock cycle before BGACKN is asserted
BGN	11	I	Bus Grant: Active low. BGN indicates to the DMAI that it is to be the next bus master. This signal is originated by the MPU and propagated via a daisy chain or other prioritization mechanism. After BGN is asserted, the DMAI waits until DTACKN, ASN, and BGACKN have become inactive before assuming ownership of the bus by asserting BGACKN

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO.	TYPE	DESCRIPTION
BGOUTN	14	O	Bus Grant Output: Active low. Daisy chain output which is asserted by the DMAI when BGN is asserted and the DMAI does not have a bus request pending.
BGACKN	15	I/O	Bus Grant Acknowledge: Active low, three-state. As an input, BGACKN is monitored by the DMAI during the bus arbitration cycle to determine when it can assume ownership of the bus (BGACKN negated). In DMA mode, it is asserted by the DMAI to indicate that it is the bus master. Three-stated in MPU and IDLE modes
RERUNN	23	I	Rerun: Active low. This input is asserted by external error detect logic to indicate a bus error. In DMA mode, the DMAI stops operation and three-states the data, address, and control lines, except BGACKN. It remains halted until RERUNN becomes inactive, and then re-tries the last bus cycle. If RERUNN is asserted again, the DMAI sets the ERR bit in the status register, stops DMA operation, releases the bus, and interrupts the CPU, if interrupts are enabled, responding with a special interrupt vector when IACKN is asserted. Not monitored in MPU and IDLE modes.
REQN	22	I	DMA Request: Active low. This input from the I/O device requests service from the DMAI and causes the DMAI to request control of the bus. In burst mode, the input is level sensitive, and the DMAI releases the bus after REQN is negated and the current DMA cycle is completed. In cycle steal mode, the REQN input is negative edge triggered. A negative going edge must occur at least one clock cycle before DTCN is asserted to accomplish continuous transfer cycles but not earlier than beginning of master cycle
ACKN	20	O	DMA Request Acknowledge: Active low. ACKN is asserted by the DMAI to indicate that it has gained the bus and the requested bus cycle is now beginning. It is asserted at the beginning of every bus cycle after ASN has been asserted, and is negated at the end of every bus cycle
RDYN	19	I	Device Ready: Active low. RDYN is asserted by the requesting device to indicate to the DMAI that valid data has either been stored or put on the bus. If negated, it indicates that the data has not been stored or presented, causing the DMAI to enter wait states. RDYN can be held low continuously if the device is fast enough so that wait states are not required
DTCN	21	O	Device Transfer Complete: Active low. In DMA mode, DTCN is asserted by the DMAI to indicate to the device that the requested data transfer is complete. On a write to memory operation, it indicates that the data provided by the device has been successfully stored. On a read from memory operation, it indicates to the device that the data from memory is present on the data bus and should be latched
DONEN	18	I/O	Done: Active low, open collector. As an output, DONEN is asserted by the DMAI concurrent with the ACKN output to indicate to the device that the transfer count is exhausted and that the DMAI's operation is completed as a result of that transfer. As an input, if asserted by the device before the transfer count became zero, it causes the DMAI to abort service and generate an interrupt request, if interrupts are enabled
OWNN	2	O	Own: Active low, open collector. This output is asserted by DMAI during the DMA mode to indicate bus mastership. It can be used to enable external address/data and control buffers. Inactive in MPU and IDLE modes
DBENN	1	O	Data Bus Enable: Active low, open collector. Asserted by the DMAI when CSN is asserted or when IACKN is asserted and the DMAI has an interrupt request pending. Can be used to enable bidirectional data buffers for D0 - D15. Inactive in IDLE and DMA mode.
V_{CC}	12	I	Power Supply: +5 volt power input.
V_{BB}	13	I	Power Supply: +1.5 volt power input.
V_{SS}	36	I	Ground: Signal and power ground input.

PIN DESCRIPTION

The Pin Description table describes the function of each of the pins of the DMAI. Signal names ending in 'N' are active low. All other signals are active high. In the descriptions, 'MPU mode' refers to the state when the DMAI is chip selected. The term 'DMA mode' refers to the state when the DMAI assumes ownership of the bus. The DMAI is in the 'IDLE mode' at all other times.

In this data sheet signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the high (logic one) state or the low (logic zero) state. Refer to the individual pin descriptions for the definition of the active level of each signal.

REGISTERS AND COUNTERS

Register Map

The internal accessible register organization of the DMAI is shown in table 1. The following rules apply to all registers:

1. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle but no write occurs.
2. Unused bits of a defined register are read as indicated in the register descriptions.
3. All registers are addressable as 8-bit quantities. To facilitate operation with the 68K MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DMAI is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control and status registers are initialized on RESET.

To provide compatibility with the other 68K family DMA controllers, control and status bits are mapped in bit positions equivalent to where they are located in the register map of the other devices. Bits which are used in the other devices but not in the DMAI are assigned default values. If upward compatibility to the other controllers is required, the programmer should use these default values when writing the control words to the registers, although they have no effect in the DMAI. When a register is read, the default value is returned regardless of the value used when the register is programmed. The default value is indicated by '(x)' in unused bit positions in the register formats, which are illustrated in table 2.

Table 1. DMAI ADDRESS MAP

ADDRESS BITS[1,2] 7 6 5 4 3 2 1 0	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
d d 0 0 0 0 0 0	CSR	Channel Status Register	R/W[3]	Yes
d d 0 0 0 0 0 1	CER	Channel Error Register	R	Yes
d d 0 0 0 0 1 0		Reserved		
d d 0 0 0 0 1 1		Reserved		
d d 0 0 0 1 0 0	DCR	Device Control Register	R/W	Yes
d d 0 0 0 1 0 1	OCR	Operation Control Register	R/W	Yes
d d 0 0 0 1 1 0	SCR	Sequence Control Register	R/W[4]	No
d d 0 0 0 1 1 1	CCR	Channel Control Register	R/W	Yes
d d 0 0 1 0 0 0		Reserved		
d d 0 0 1 0 0 1		Reserved		
d d 0 0 1 0 1 0	MTCH	Memory Transfer Counter High	R/W	No
d d 0 0 1 0 1 1	MTCL	Memory Transfer Counter Low	R/W	No
d d 0 0 1 1 0 0	MACH	Memory Address Counter High	R/W[4]	No
d d 0 0 1 1 0 1	MACMH	Memory Address Counter Middle High	R/W	No
d d 0 0 1 1 1 0	MACML	Memory Address Counter Middle Low	R/W	No
d d 0 0 1 1 1 1	MACL	Memory Address Counter Low	R/W	No
d d 0 1 d d d d		Reserved		
d d 1 0 0 0 d d		Reserved		
d d 1 0 0 1 0 0		Reserved		
d d 1 0 0 1 0 1	IVR	Interrupt Vector Register - Normal	R/W	Yes
d d 1 0 0 1 1 0		Reserved		
d d 1 0 0 1 1 1	IVR	Interrupt Vector Register - Error	R/W	Yes
d d 1 0 1 0 d d		Reserved		
d d 1 0 1 1 0 0		Reserved		
d d 1 0 1 1 0 1	CPR	Channel Priority Register	R/W[4]	No
d d 1 0 1 1 1 0		Reserved		
d d 1 0 1 1 1 1		Reserved		
d d 1 1 d d d d		Reserved		

NOTES:
1. A0 = 0 for UDSN asserted. A0 = 1 for LDSN asserted
2. 'd' designates don't care
3. A write to this register may perform a status resetting operation
4. This register is a dummy register present only to provide compatibility with other 68K family DMA controllers. A write to this register has no effect on the DMAI

Table 2. REGISTER BIT FORMATS

DEVICE CONTROL REGISTER

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
DCR	EXTERNAL REQUEST MODE 0 = BURST 1 = CYCLE STEAL	NOT USED (0)	NOT USED (1)	NOT USED (1)	NOT USED (*)	NOT USED (0)	NOT USED (0)	NOT USED (0)

*Should be programmed as '0' for SIZE (OCR[5:4]) = 00 and as '1' otherwise. When read, the value of this bit is OCR[5] .OR.OCR[4]

OPERATION CONTROL REGISTER (OCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
DCR	DIRECTION 0 = MEM TO DEV 1 = DEV TO MEM	NOT USED (0)	OPERAND SIZE 00 = BYTE 01 = WORD (16 BIT) 10 = LONG WORD* 11 = WORD (32-BIT)*		NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)

*Long word and 32-bit word modes are not supported by 68440. 32-bit word mode is not supported by 68450.

SEQUENCE CONTROL REGISTER (SCR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
SCR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (1)	NOT USED (0)	NOT USED (0)

CHANNEL CONTROL REGISTER (CCR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CCR	START 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	SOFTWARE ABORT 0 = NO 1 = YES	INTERRUPT ENABLE 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	NOT USED (0)

CHANNEL STATUS REGISTER (CSR)

	BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT09	BIT08
CSR	CHANNEL OPERATION COMPLETE 0 = NO 1 = YES	NOT USED (0)	NORMAL DEVICE TERMINATE 0 = NO 1 = YES	ERROR 0 = NO 1 = YES	CHANNEL ACTIVE 0 = NO 1 = YES	NOT USED (0)	NOT USED (0)	READY INPUT STATE 0 = LOW 1 = HIGH

CHANNEL ERROR REGISTER (CER)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CER	NOT USED (0)	NOT USED (0)	NOT USED (0)	ERROR CODE 00000 = NO ERROR 01001 = BUS ERROR 10001 = SOFTWARE ABORT				

CHANNEL PRIORITY REGISTER (CPR)

	BIT07	BIT06	BIT05	BIT04	BIT03	BIT02	BIT01	BIT00
CPR	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)	NOT USED (0)

Device Control Register (DCR)

[15] External Request Mode

This bit selects whether the DMAI operates in burst or cycle steal mode.

0 Burst mode. This mode allows a device to request the transfer of multiple operands using consecutive bus cycles. In this mode the request (REQN) line is an active low input which is asserted by the device to request an operand transfer. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. If the request line is active when the DMAI asserts ACKN, and remains active at least until the DMAI asserts device transfer complete (DTCN), the DMAI recognizes a valid request for another operand, which will be transferred during the next bus cycle. If the request line is negated before the DMAI asserts DTCN, the DMAI relinquishes the bus and waits for the next request, but the current transfer will be completed.

1 Cycle steal mode. In this mode, the device requests an operand transfer by generating a falling edge on the request (REQN) line. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN)

output. The request line must be in the inactive state for at least one clock cycle before a request is made. After a request has been asserted, it must remain at the assertion level for at least one clock cycle. If another request is received before the first operand part of a former request is acknowledged, the second request is not recognized. Normally, the DMAI will relinquish the bus after servicing a valid request. However, if the device generates a new request before the DMAI asserts DTCN for the last operand part, the DMAI will retain ownership of the bus and that request will be serviced before the bus is relinquished.

Operation Control Register (OCR)

[7] Direction
0 Transfer is from memory to device.
1 Transfer is from device to memory.

[5:4] Operand Size
The programming of these bits determine whether UDSN, LDSN, or both are generated during the transfer cycle and the increment by which the memory address counter (MAC) is changed in each transfer cycle.

00 Byte. The operand size is 8 bits. The MAC is incremented by one after each operand transfer. If the LSB of the MAC is a '0', UDSN is asserted during the transfer. If the LSB of a MAC is a '1', LDSN is asserted during the transfer. The transfer counter decrements by one before each byte is transferred.

01 Word. The operand size is 16 bits. The MAC is incremented by two after each operand transfer. The value of the LSB of the MAC is ignored and both UDSN and LDSN are asserted during the transfer. The transfer counter decrements by one before each word is transferred.

10 Long word. The operand size is 32 bits. The operand is transferred as two 16-bit words. The MAC is incremented by two after each 16-bit word is transferred. The value of the LSB of the MAC is ignored and both UDSN and LDSN are asserted during the transfer. The transfer counter decrements by one before the entire long word is transferred. Note that this mode is not implemented in the 68440.

11 Double word. The operand size is 32 bits. The operand is transferred as a single 32-bit word. The MAC is incremented by four after each operand transfer. The value of the two LSBs of the MAC is ignored (the A1 output will always be a zero in this mode) and both UDSN and LDSN are asserted during the transfer. The transfer counter decrements by one before the double word is transferred. Note that this mode is not implemented in the 68440 or 68450; it is included in the DMAI to support VME bus operations.

Sequence Control Register (SCR)

This register serves no function in the DMAI. It is included only to provide compatibility with the programming for the 68440 and 68450 DMA controllers.

Channel Control Register (CCR)

[7] Start Operation
0 No start pending.
1 Start operation. The start bit is set to initiate operation of the DMAI. The memory address counter and the memory transfer counter should have been previously initialized, and all bits of the channel status register (CSR) should have previously been reset. The DMAI initiates operation by clearing any pending requests, clearing the start bit, and setting the channel active bit in the CSR. The DMAI is then ready to receive requests for an operation. The channel cannot be started if any of the internal status bits in the CSR (CSR[15:11]) have not been cleared.
A pending start cannot be reset by a write to the register. START can be cleared only by the DMAI when it starts operation or by setting the software abort bit (CCR[4]).

[4] Software Abort
0 Do not abort.
1 Abort operation. Setting this bit terminates the current operation of the DMAI and places it in the IDLE state. The channel operation complete and error bits in the CSR are set, the channel active bit in the CSR is reset, and an ABORT ERROR condition is signaled in the CER. Setting this bit causes a pending start to be reset.

[3] Interrupt Enable
0 Interrupts not enabled.
1 Enable interrupts. An interrupt request is generated if the channel operation complete bit in the CSR is set. When the IACKN input is asserted, the DMAI returns the normal interrupt vector if the error bit in the CSR is not set, or the error interrupt vector if error is set.

Channel Status Register (CSR)

A read of this register provides the status of the DMAI. The COC, NDT, and ERR bits can be cleared by writing a '1' to the bit positions of the register which are to be cleared. Those bit positions which are written with a '0' remain unaffected.

[15] Channel Operation Complete
This bit is set following the termination, whether successful or not, of any DMAI operation and indicates that the DMA transfer has completed. This bit must be cleared to start another channel operation.

[13] Normal Device Termination
This bit is set when the device terminates the DMAI operation by asserting the DONEN line while the device was being acknowledged. This bit must be cleared to start another channel operation.

[12] Error
This bit is used to report that the DMAI's operation was terminated due to the occurrence of an error. The condition which caused the error can be determined by reading the channel error register (CER). This bit must be cleared to start another channel operation. When this bit is cleared, the CER is also cleared.

[11] Channel Active
This bit is set after the channel has been started and remains set until the channel operation terminates. It is then automatically cleared by the DMAI. The bit is unaffected by the write operations.

[8] Ready Input State
This bit reflects the state of the RDYN input at the time the CSR is read. The bit is a '0' if RDYN is low and a '1' if RDYN is high. This bit is unaffected by write or reset operations.

Channel Error Register (CER)

[4:0] Error Code
This field indicates the source of error when an error is indicated in CER[12]. The contents of this register are cleared when CER[12] is cleared.

00000 No error.

01001 Bus error. A bus error occurred during the last bus cycle generated by the DMAI. See rerun description in OPERATION section.

10001 Software abort. The channel operation was terminated by a software abort command. See CCR[4].

Channel Priority Register (CPR)

This register serves no function in the DMAI. It is included only to provide compatibility with the programming for the other 68K family DMA controllers.

Memory Address Counter (MACH, MACMH, MACML, MACL)

The 32-bit memory address counter is used to program the memory location where the first operand to be transferred is located or is to be transferred to, depending on the direction of transfer. The counter must be initialized prior to beginning the transfer of a block of data and then increments automatically depending on the operand length, as de-

scribed in the Operation Control Register description.

Only the least significant 24 bits of the counter (MACMH, MACML and MACL) are implemented in the DMAI. The most significant byte of the counter, MACH, is provided only to allow compatibility with programming of the 68440 and 68450. Writing to MACH has no effect on the DMAI operation. Reading MACH always returns H'00'.

Memory Transfer Counter (MTCH, MTCL)

The 16-bit memory transfer counter programs the number of operands to be transferred by the DMAI. The counter must be initialized prior to beginning the transfer of a block of data and then decrements once per operand transfer (regardless of operand size) until it reaches the terminal value of zero. Channel operation then terminates and the COC bit in the CSR will be asserted.

Interrupt Vector Register (IVR)

The IVR contains the value to be placed on the data bus upon receipt of an interrupt acknowledge from the MPU. Only the seven most significant bits of the programmed value are used by the DMAI. The output vector from the DMAI contains a zero in the least significant bit position if a normal termination occurred (error bit not set) and contains a one in the least significant bit position if termination was due to an error (error bit set).

The contents of this register are initialized to H'0F' by a reset. The value returned will be H'0F', regardless of the error state, until the register is programmed by the MPU.

To provide compatibility with the other 68K family DMA controllers, the IVR has two addresses (see table 1). If program compatibility is required, the value written at the normal IVR address should have a zero as its LSB, and the value written at the error IVR address should be the same but with the LSB equal to one.

OPERATION

A DMAI operation proceeds in three principal phases. During the initialization phase, the MPU configures the channel control registers, loads the initial memory address and transfer count, and starts the channel. During the transfer phase, the DMAI accepts requests for transfers from the device, arbitrates for and acquires ownership of the bus, and provides for addressing and bus controls for the transfers. The termination phase occurs after the operation is complete, when the DMAI reports the status of the operation.

Operation Initiation

After having programmed the control registers, the memory address counter, and the memory transfer counter, the MPU sets the start bit (CCR[7]). The DMAI initiates the operation by clearing any pending requests, clearing the start bit, and setting the channel active bit in the CSR. The DMAI is then ready to receive valid requests for an operation.

The channel cannot be started if any of the internal status bits in the CSR (CSR[15:11]) have not been cleared. An error is not signaled if this condition occurs. The only indication of this state is that the start bit remains set in the CCR. A pending start cannot be reset by a write to the register. START can be cleared only by the DMAI when it starts operation or by setting the software abort bit (CCR[4]).

Device/DMAI Communication

Communication between the peripheral device and the DMAI is accommodated by five signal lines.

Request (REQN)

The device makes a request for service by asserting the request line. The DMAI can operate in either the burst request mode or the cycle stealing request mode, as programmed by the external request mode bit (DCR[15]).

The burst mode allows a device to request the transfer of multiple operands using consecutive bus cycles. In this mode the request line is an active low input. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. If the request line is active when the DMAI asserts ACKN, and remains active at least until the DMAI asserts device transfer complete (DTCN), the DMAI recognizes a valid request for another operand, which will be transferred during the next bus cycle. If the request line is negated before the DMAI asserts DTCN, the DMAI relinquishes the bus and waits for the next request. For long word transfers (2 x 16), the request must be asserted at least until the acknowledge for the second part of the operand has been asserted.

In the cycle steal mode, the device requests an operand transfer by generating a falling edge on the request line. The DMAI services the request by arbitrating for the bus, obtaining the bus, and notifying the peripheral by asserting the acknowledge (ACKN) output. The request line must be in the inactive state for at least one clock cycle before a request is made. After a request has been asserted, it must remain at the assertion level for at least one clock cycle. If another request is received before the first operand part of a former request is acknowledged, the second request is not recognized. Normally, the DMAI will relinquish the bus after servicing a valid request. However, if the device generates a new request before the DMAI asserts DTCN for the last operand part, the DMAI will retain ownership of the bus and that request will be serviced before the bus is relinquished.

Acknowledge (ACKN)

The DMAI asserts the acknowledge line, which implicitly addresses the device making the request, during transfers to and from the device. The line may be used to control buffering circuits between the data bus and the MPU bus.

During burst mode, REQN must not be disasserted for less than one CLK period plus four RC time constants, where R is the value of the resistor used for the pullup on BRN and C has a typical value of 20pF.

Ready (RDYN)

Ready is an active low input which is asserted by the requesting device to indicate to the DMAI that valid data has either been stored or put on the bus. If negated, it indicates that the data has not been stored or presented, causing the DMAI to enter wait states until RDYN is asserted. RDYN can be held low continuously if the device is fast enough so that wait states are not required. The current state of the ready input is reflected in CSR[8].

Done (DONEN)

Done is a bidirectional active low signal. As an output, it is asserted and negated by the DMAI concurrent with the ACKN output of the last operand part to indicate to the device that the memory transfer count is exhausted and that the DMAI's operation is completed as a result of that transfer.

The DMAI also monitors the state of the line while acknowledging a device. If the device asserts DONEN, the DMAI will terminate operation after the transfer of the current operand. In this case the DMAI clears the channel active bit and sets the channel operation complete and normal device termination bits in the CSR. If both the DMAI and the device assert DONEN, the device termination is not recognized, but the operation does terminate.

Device Transfer Complete (DTCN)

DTCN is an active low output which is asserted by the DMAI to indicate to the device that the requested data transfer is complete. On a write to memory operation, it indicates that the data provided by the device has been successfully stored. On a read from memory operation, it indicates to the device that the data from memory is present on the data bus and should be latched. DTCN is not asserted if assertion of the RERUNN input terminates the bus cycle.

Bus Arbitration

Upon receiving a valid request for a transfer from the device, the DMAI will arbitrate for and obtain ownership of the system bus.

The DMAI indicates that it wishes to become the bus master by asserting its bus request (BRN) output. This is a wire-ORed signal that indicates to the MPU that some external device requires control of the bus. The processor is effectively at a lower priority level than external devices and will relinquish the bus after it has completed the last bus cycle it has started. The processor puts the bus up for external arbitration by asserting its bus grant (BGN) output. This signal may be routed through a daisy chain (such as provided by the DMAI) or through some other priority-encoded network. When the DMAI making the bus request receives the bus grant (indicated by its BGN input being asserted), it is to be the next bus master. It waits until address strobe (ASN), data transfer acknowledge (DTACKN) and bus grant acknowledge (BGACKN) become inactive and then assumes ownership of the bus by asserting its own BGACKN output. The DMAI then negates the BRN output and proceeds with the data transfer phase. After this phase is completed, the DMAI relinquishes bus ownership by negating the BGACKN output.

In burst DMA mode, detection of an active low request input after the DMAI operation has been started will begin the bus arbitration cycle. However, if the device negates its request at least one clock cycle before the DMAI asserts BGACKN, the DMAI will negate its bus request and will not assume ownership of the bus.

Data Transfers

The actual transfer of data between the memory and the device occurs during the data transfer phase. All transfers occur during a single cycle except in the case of long word operands, in which case two cycles are used to transfer the operand as two 16-bit words. The transfers take place using a 'single address' protocol: the DMAI addresses the memory via the bus address lines, while the device is implicitly addressed via the acknowledge output.

When a request is generated using the request method programmed in the control register, the DMAI obtains the bus and asserts acknowledge to notify the device that a transfer is to take place. The DMAI asserts all S68000 bus control signals needed for the transfer and holds them until the device responds with ready. The bus cycle then terminates normally. Ready may be tied low (asserted) if the device is fast enough.

When the transfer is from memory to the device, data is valid when DTACKN is asserted by the memory and remains valid until the data strobe(s) are negated. The assertion of DTCN from the DMAI can be used to latch the data, as the data strobes are not removed until one-half clock after the assertion of DTCN.

When the transfer is from device to memory, the data must be valid on the bus before the DMAI asserts the data strobe(s). The device indicates valid data by asserting ready. The DMAI then asserts the strobes and holds them asserted until the memory accepts the data, indicated by the assertion of DTACKN. The DMAI then asserts DTCN and negates the data strobes.

Flow charts for these operations are shown in figures 1 and 2. Refer to the timing section for the equivalent timing diagrams.

Operation Termination

Termination of the block transfer occurs under the conditions detailed below.

Terminal Count

As part of each transfer of an operand, the DMAI decrements the memory transfer counter. If this counter is decremented to zero, the operand is the last operand of the block. The DMAI operation is complete and it notifies the device of completion by asserting the DONEN output during the last operand transfer cycle. When the transfer has been completed, the channel active bit in the CSR is cleared and the COC bit is set, unless an error occurs.

Device Termination

The DMAI monitors the state of the DONEN line while acknowledging a device transfer request. If the device asserts DONEN, the DMAI will terminate operation after the transfer of the current operand. When the transfer has been completed, the DMAI clears the channel active bit and sets the COC and normal device termination bits in the CSR. If both the DMAI and the device assert DONEN, the device termination is not recognized, but the operation does terminate.

Software Abort

The software abort bit (CCR[4]) allows the MPU to abort the current operation of the DMAI. The COC and error bits in the CSR are set, the channel active bit in the CSR is cleared, and an abort error condition is signaled in the CER.

Rerun Error

The DMAI provides a rerun input (RERUNN) to indicate a bus exception condition. RERUNN must arrive prior to or in coincidence with DTACKN in order to be recognized, and the DMAI verifies that the line has been stable for two clock cycles before acting on it. The occurrence of a rerun during a DMAI bus cycle forces it to terminate the bus cycle in an orderly manner.

When the assertion of rerun is verified, the DMAI stops operation and three-states the data, address, and control lines, except BGACKN, so that it retains ownership of the bus. It remains halted until rerun becomes inactive, and then re-tries the last bus cycle. If rerun is asserted again, the DMAI stops DMA operation, releases the bus, sets the error and COC bits in the CSR, clears the active bit in the CSR, and sets the error code in the CER to indicate a bus error.

While stopped due to assertion of rerun, the DMAI does not generate any bus cycles and will not honor any requests until it is removed. However, the DMAI still recognizes requests.

Error Recovery Procedure

If an error occurs during a DMA transfer such that the DMAI stops the DMA operation, information is available to the operating system for an error recovery routine.

The information available to the operating system consists of the memory address counter, the memory transfer counter, and the control, status, and error registers. The DMAI decrements the memory transfer counter before attempting a DMA operation, so the register will contain the count minus one of the attempted transfer. The memory address counter will contain the address at which the DMA operation was attempted.

Reset

The reset input (RESETN) provides a means of resetting and initializing the DMAI from an external source. If the DMAI is a bus master when reset is received, the DMAI relinquishes the bus. Reset clears the control and error registers, sets all bits of the status register except CSR[8] to zero, and initializes the interrupt vector register to H'0F.

Interrupts

The interrupt enable bit (CCR[3]) determines whether the DMAI generates interrupt requests. When the bit is set, an interrupt request is generated if the channel operation complete bit in the CSR is set. When the IACKN input is asserted, and the DMAI has an interrupt request pending, the DMAI returns an interrupt vector on the data bus.

The interrupt vector issued is the contents of the IVR. Only the seven most significant bits of the programmed value are used by the DMAI. The vector from the DMAI contains a zero in the LSB position if a normal termination occurred (error bit not set) and contains a one in the LSB position if termination was due to an error (error bit set).

The contents of this register are initialized to H'0F' by a reset. The value returned will be H'0F', regardless of the error state, until the register is programmed by the MPU.

To provide compatibility with the other 68K family DMA controllers, the IVR has two addresses (see table 1). If program compatibility is required, the value written at the

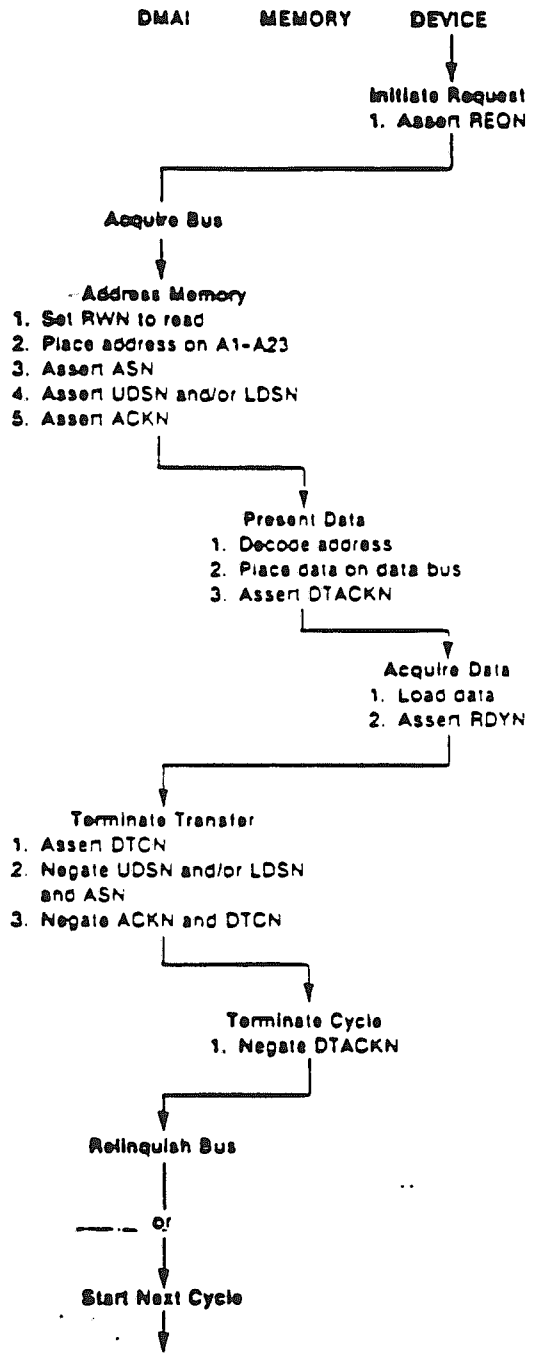


Figure 1. Transfer from Memory to Device Flowchart

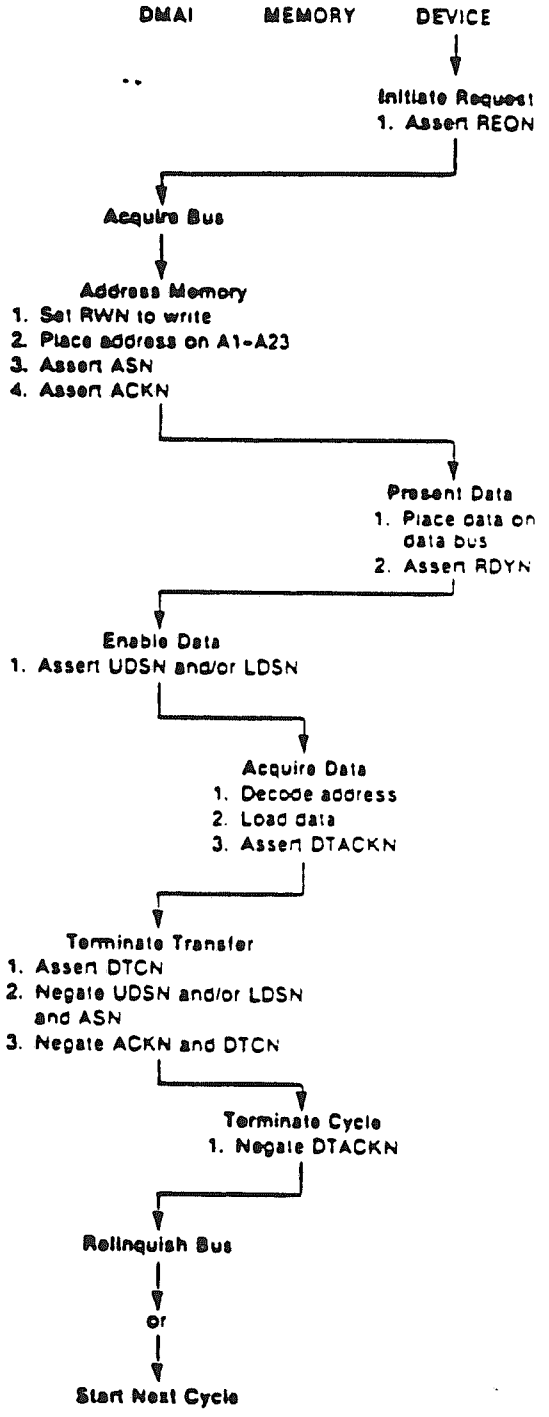


Figure 2. Transfer from Device to Memory Flowchart

normal IVR address should have a zero as its LSB, and the value written at the error IVR address should be the same but with the LSB equal to one.

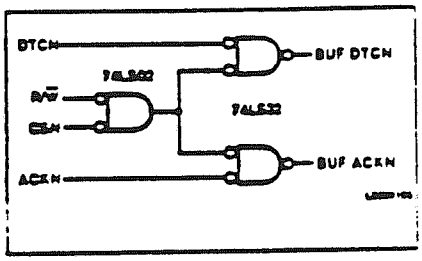
APPLICATIONS

Figure 3 illustrates a typical interconnection of the DMAI in a 68000 based system.

DESIGN NOTE

When clearing the error bit in CSR (bit 12) after a DMAI abort due to a double RERUNN, ACKN and DTCN will both go low concurrent with CSN and DTACKN for one CLK cycle.

To prevent the possibility that the device may misinterpret these signals, it is suggested that these signals be ANDed with CSN (see figure below).



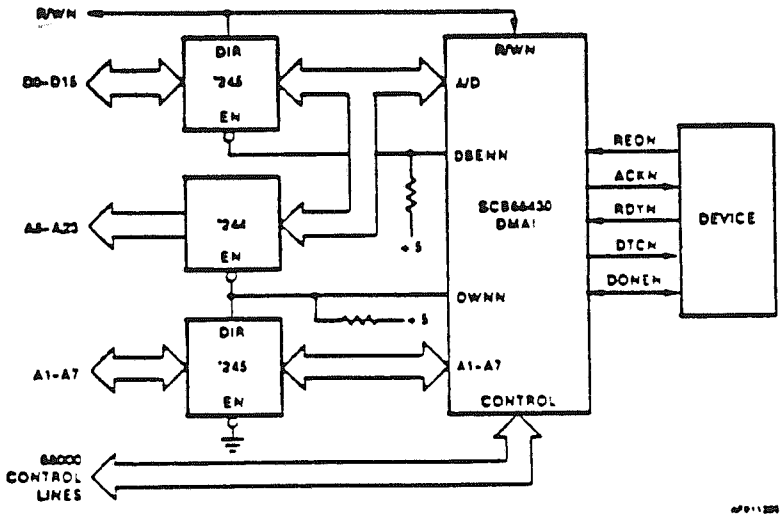


Figure 3. DMAI Application

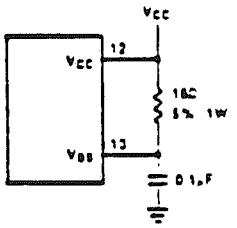


Figure 4. Recommended V_{BB} Test Circuit

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltages V_{CC} and V_{BB}	−0.5 to +7.0	V
Input voltage	−0.5 to +5.5	V
Operating temperature range[2]	0 to +70	°C
Storage temperature	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%, V_{BB} = Figure 4, T_A = 0°C to +70°C[3,4,7]

PARAMETER		TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.0		V
V_{OL}	Output low voltage	I_{OUT} = 5.3mA		0.5	V
V_{OH}	Output high voltage, all outputs except open collector outputs[5]	I_{OUT} = −400µA	2.5		V
I_{IL}	Input low current	V_{IN} = 0.4V		−400	µA
I_{IH}	Input high current	V_{IN} = 2.7V		20	µA
I_{OC}	Open collector off state current[5]	V_{OUT} = 2.4V		20	µA
I_{SC}	Output short circuit current[6]	V_{CC} = max	−40	−100	mA
I_{CC}	V_{CC} supply current	V_{CC} = max		130	mA
I_{BB}	V_{BB} supply current			275	mA

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or at any other conditions other than those indicated in the Electrical Characteristics section of this data sheet is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. Parameters are valid over specified temperature range.
4. All voltage measurements are referenced to ground (V_{SS}). For testing, all signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2.0V as appropriate.
5. IRQN, BRN, DONEN, and OWNN are open collector outputs.
6. No more than one output should be connected to ground at one time.
7. Capacitive test load is 100pF for all pins except DTCN which has a 35pF capacitive test load.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 5%, V_{BB} = Figure 4, T_A = 0°C to +70°C[3,4,7]

NO.	FIGURE	CHARACTERISTICS	TENTATIVE LIMITS				UNIT
			10MHz		12.5MHz		
			Min	Max	Min	Max	
1	5	A1 – A7, ASN, RWN, set-up to UDSN, LDSN low	0		0		ns
2	5	D0 – D15 3-state to invalid data from ASN, CSN, and UDSN or LDSN low	10		10		ns
3	5	DTACKN 3-state to high from ASN, CSN, and UDSN or LDSN low	10		10		ns
4	5	CSN low after UDSN or LDSN low		25		25	ns
5	5, 6	DBENN low after ASN and CSN low		60		60	ns
6	5	D0 – D15 valid data from ASN, CSN, and UDSN or LDSN low		100		100	ns
7	5	DTACKN low after D0 – D15 valid data	−15	30	−15	30	ns
8	5	A1 – A7, ASN, RWN or CSN hold after UDSN and LDSN high	0		0		ns
9	5, 6	DBENN high from either ASN or CSN high		45		45	ns
10	5	D0 – D15 to 3-state from UDSN and LDSN high		80		80	ns
11	5	D0 – D15 to invalid data from UDSN and LDSN high	10		10		ns
12	5, 6	DTACKN high from UDSN and LDSN high		55		55	ns
13	5, 6	DTACK 3-state from either CSN or ASN high		85		85	ns
14	6	A1 – A7, ASN, RWN set-up to UDSN, LDSN low	50		50		ns/s
15	6	CSN set-up before UDSN or LDSN low	20		20		ns
16	6	DTACKN 3-state to high after CSN and ASN low	10		10		ns
17	6	D0 – D15 valid after UDSN or LDSN low		0		0	ns
18	6	DTACKN low from UDSN or LDSN low		100		100	ns
19	6	UDSN and LDSN low time	115		100		ns
20	6	A1 – A7 hold after UDSN and LDSN high	0		0		ns
21	6	ASN, RWN and CSN hold after UDSN and LDSN high	0		0		ns

AC ELECTRICAL CHARACTERISTICS (Continued)

NO.	FIGURE	CHARACTERISTICS	TENTATIVE LIMITS				UNIT
			10MHz		12.5MHz		
			Min	Max	Min	Max	
22	6	D0 - D15 hold after UDSN and LDSN high	0		0		ns
23	7	DBENN low from last low of ASN, IACKN, LDSN		65		65	ns
24	7	D0 - D7 valid after last low of ASN, IACKN, LDSN		105		105	ns
25	7	DTACKN 3-state to high after last low of ASN, IACKN, LDSN		100		100	ns
26	7	DTACKN low after last low of ASN, IACKN, LDSN		110		110	ns
27	7	DBENN high after first high of ASN, IACKN, LDSN		55		55	ns
28	7	D0 - D7 hold after first high of ASN, IACKN, LDSN		60		60	ns
29	7	D0 - D7 3-state after first high of ASN, IACKN, LDSN		80		80	ns
30	7	DTACKN high after first high of ASN, IACKN, LDSN		60		60	ns
31	7	DTACKN 3-state after first high of ASN, IACKN, LDSN		95		95	ns
32	8	BRN high from CLK high		65		65	ns
33	8, 11, 12	BGACKN low from CLK low		75		75	ns
34	8, 11, 12	OWNN low from CLK high		75		75	ns
35	8	BGACKN high from CLK low		75		75	ns
36	8,11,12	OWNN high from CLK high (load dependent)		50		50	ns
37	10	REQN set-up before CLK low	30		30		ns
38	10	REQN hold after CLK high	20		20		ns
39	10	BRN low from CLK high		80		80	ns
41	11, 12	ASN, UDSN, LDSN, RWN 3-state to high from CLK low		75		75	ns
43	11, 12	A1 - A23 to valid ASN	0		0		ns
44	11, 12	ASN low from CLK high		65		65	ns
45	11, 12	LDSN, UDSN low from CLK high		90		90	ns
46	11, 12	ACKN low from CLK high		65		65	ns
47	11, 12	DTACKN set-up to CLK high	30		30		ns
48	11, 12	RDYN set-up to CLK low	30		30		ns
49	11, 12	DTCN low from CLK high		70		70	ns
50	11, 12	ASN high from CLK high		75		75	ns
51	11, 12	LDSN, UDSN, high from CLK high		90		90	ns
52	11, 12	DTACKN, RDYN hold after CLK high	0		0		ns
-	11, 12	ASN, LDSN, UDSN, high from DTCN low	-20		-20		ns
53	11, 12	ACKN high from CLK high		50		50	ns
54	11, 12	DTCN high from CLK high		50		50	ns
55	11, 12	Address valid after CLK low	10		10		ns
-	11, 12	Address valid after ASN high	0		10		ns
56	11, 12	DONEN (output) low from CLK low		120		120	ns
57	11, 12	DONEN (output) high from CLK high		50		50	ns
58	11, 12	DONEN (input) set-up low before CLK low	30		30		ns
59	11, 12	DONEN (input) hold low after CLK high	0		0		ns
60	11, 12	BGACKN, ASN, UDSN, LDSN, RWN to 3-state from CLK low		75		75	ns
62	11, 12	A1 - A23 valid to 3-state from CLK high		100		100	ns
63	12	R/WN low from CLK high		65		65	ns
64	12	R/WN high from CLK high		75		75	ns
65	13	RERUNN set-up low before CLK high	30		30		ns
66	13	RERUNN hold low from CLK high	20		20		ns
67	13	A1 - A23 to idle state from CLK low		100		100	ns
68	13	A1 - A23 to valid after CLK low		85		85	ns

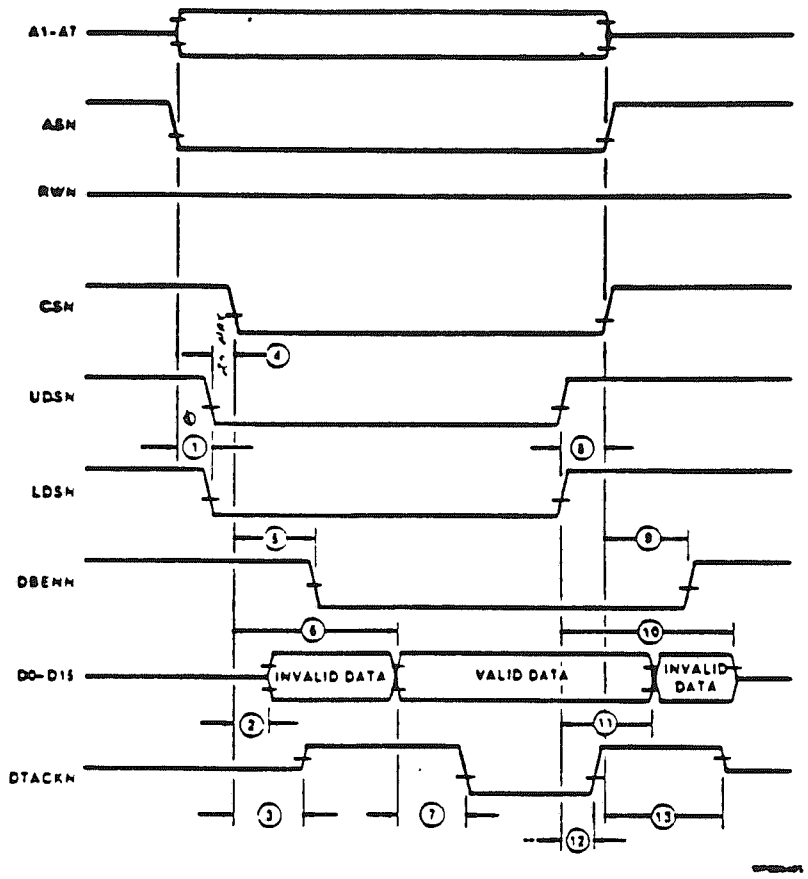


Figure 5. DMAI Read Timing

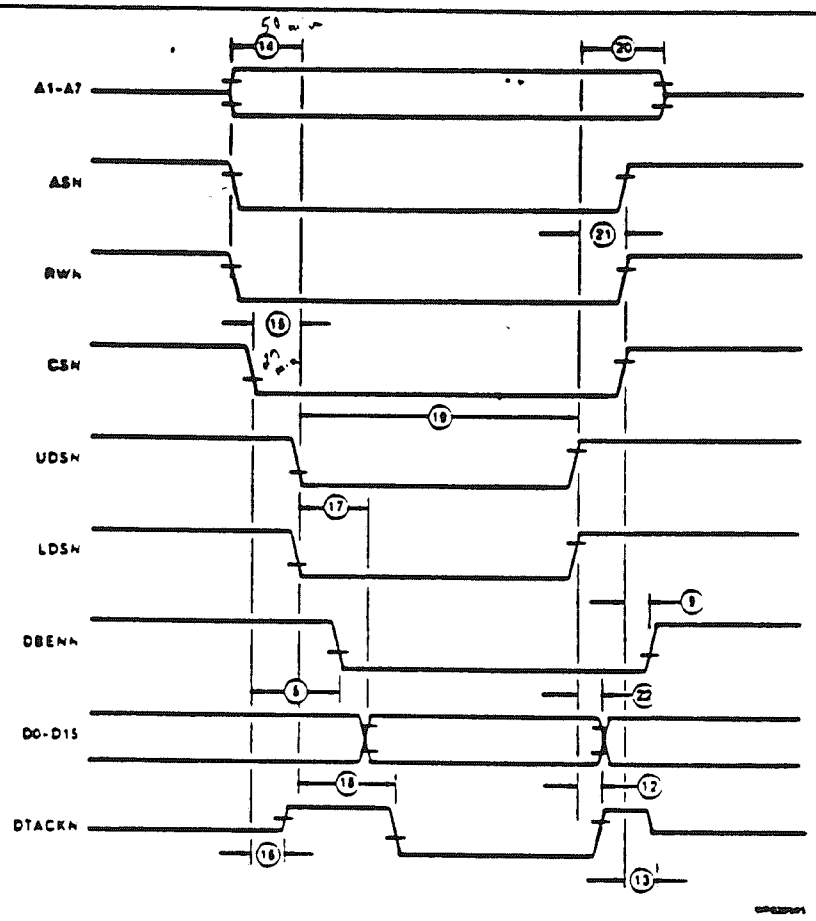


Figure 6. DMAI Write Timing

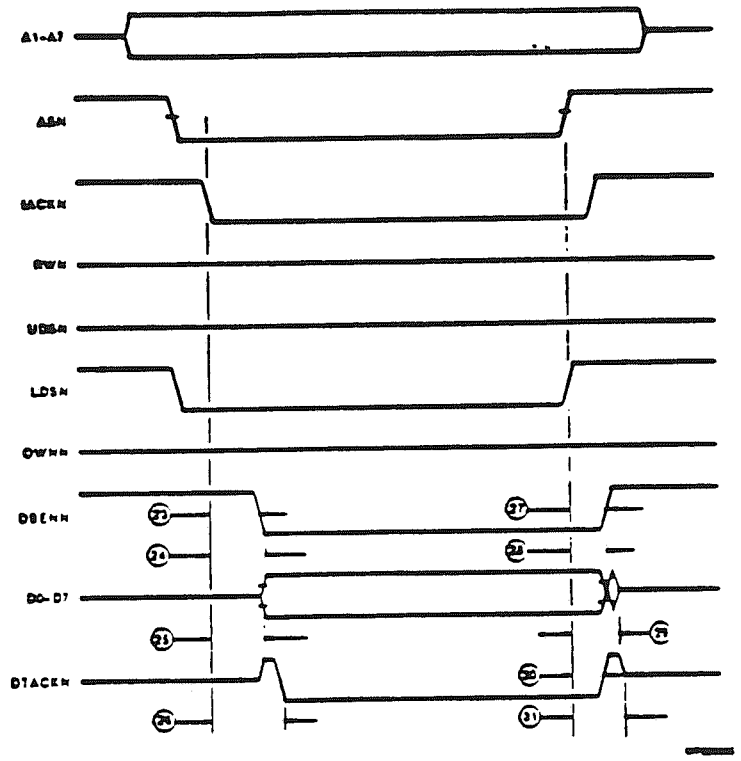
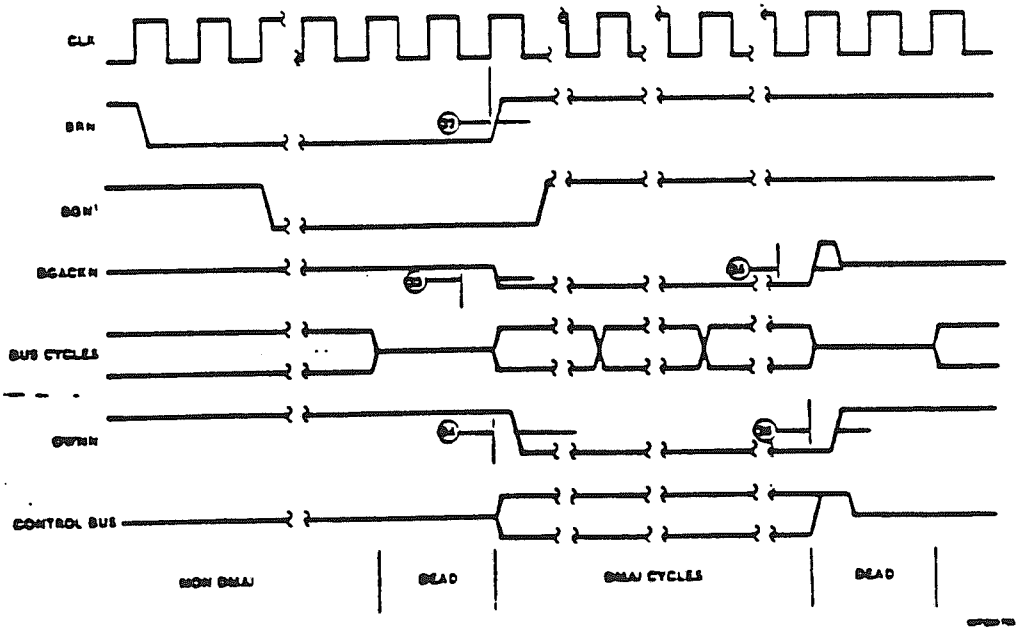


Figure 7. CPU IACK Cycle to DMAI



NOTES:
1. Device will become master if BGN is asserted concurrent with or later than RECN (same clock edge or later).
2. ASN, DTACKN and BGACKN must be negated in order for DMAI to become master. Timing assumes all these negation concurrent with BGN — if not, it is from the latest signal which is negated.

Figure 8. DMAI Bus Arbitration Timing

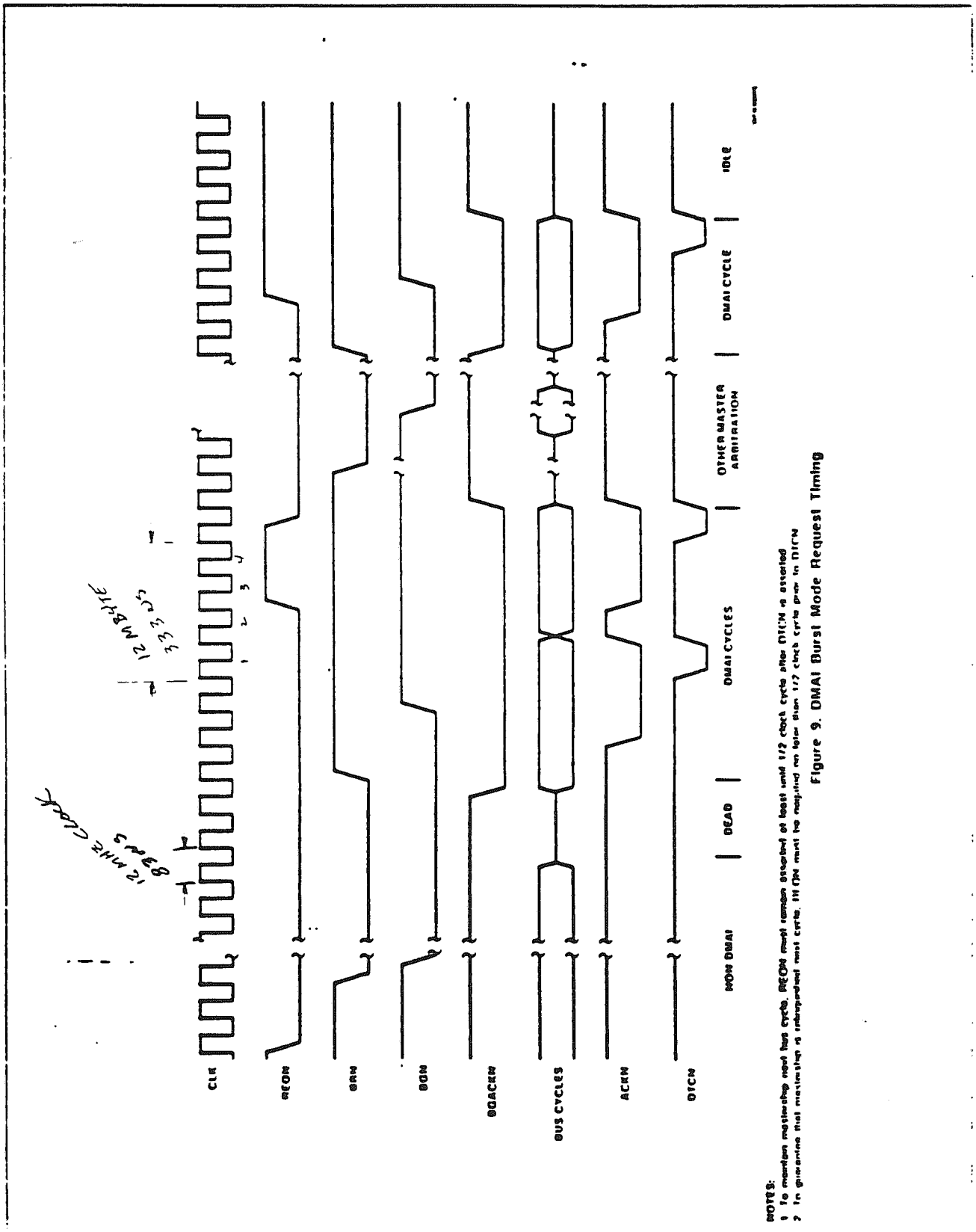
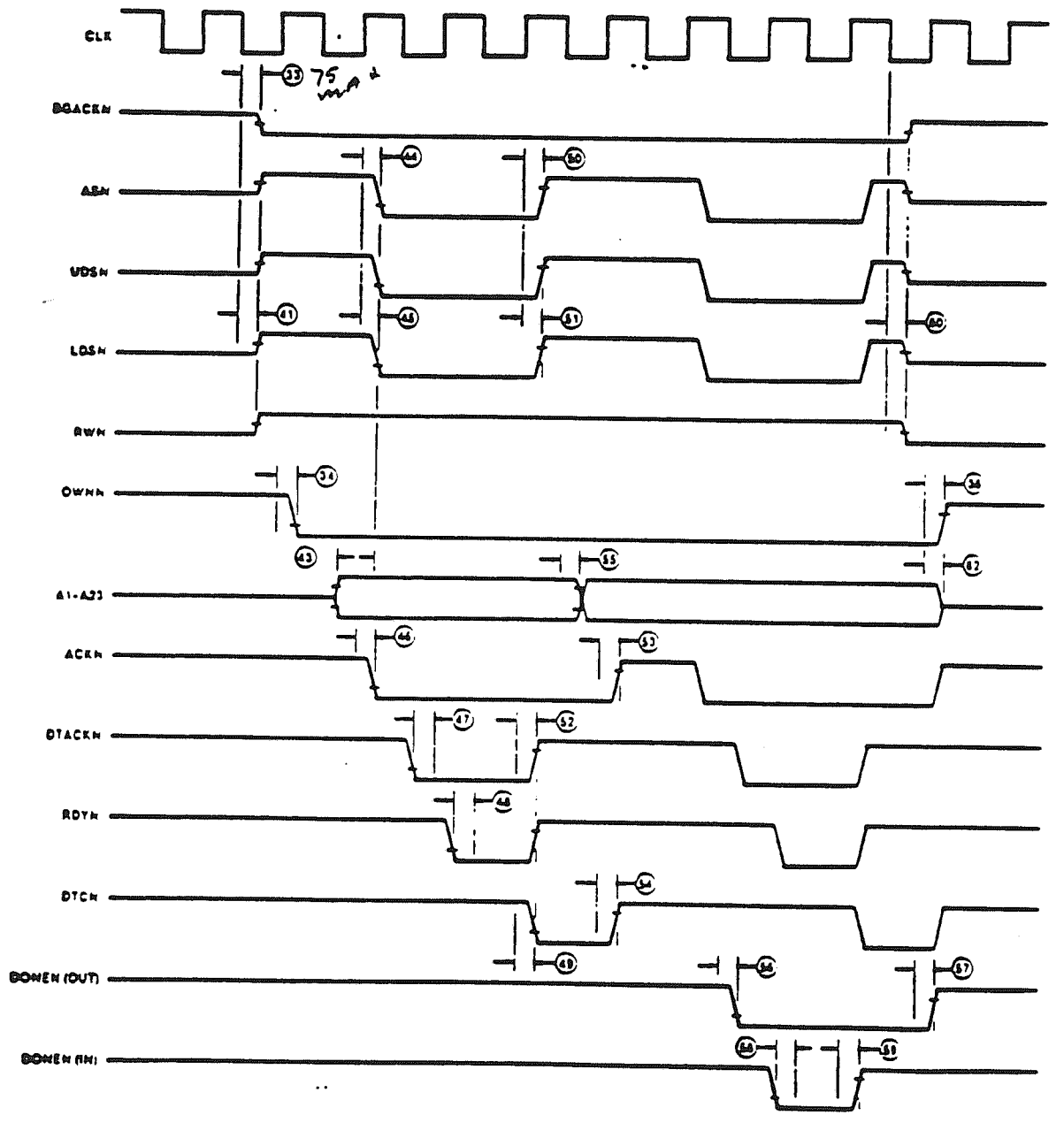
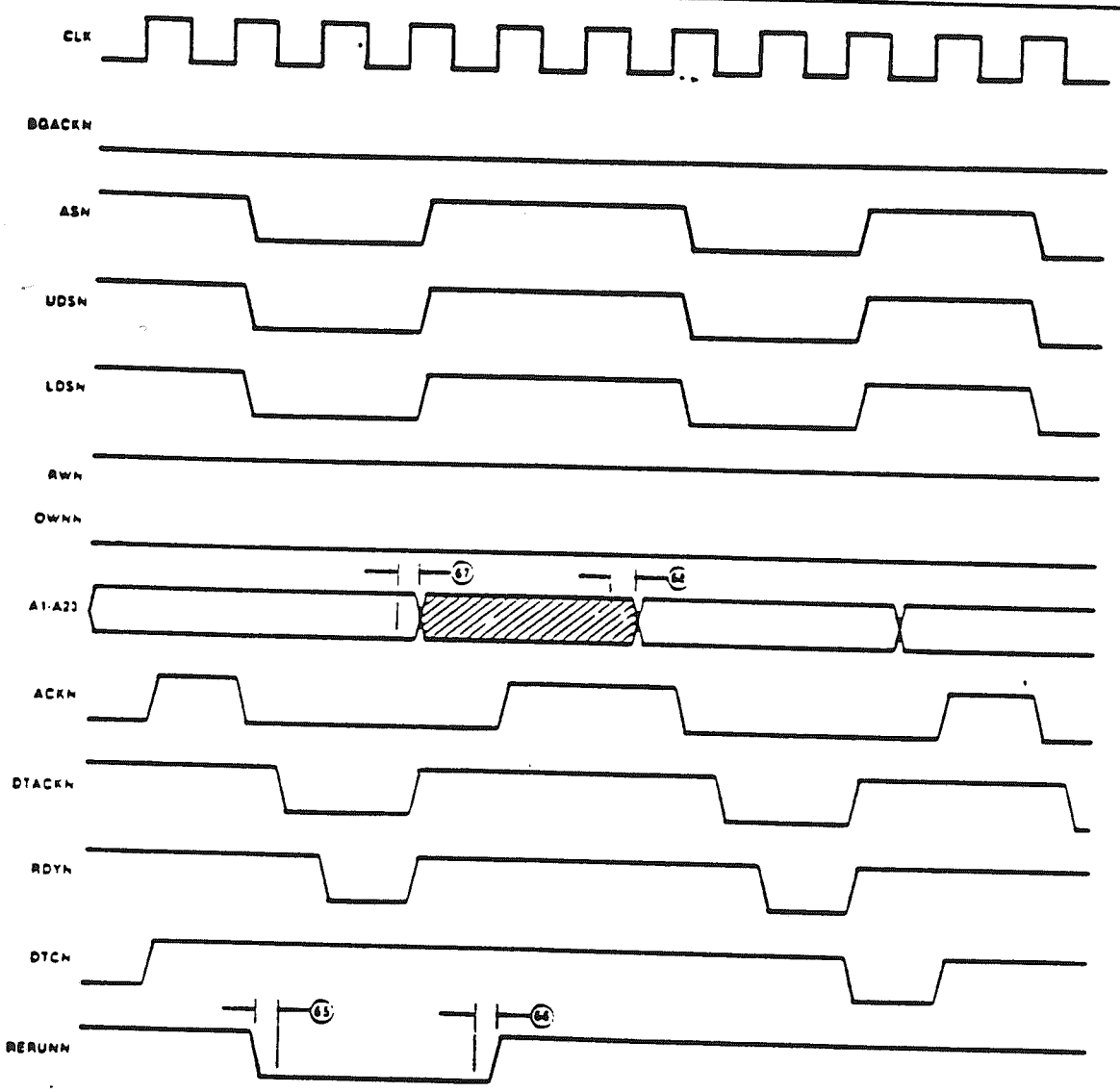


Figure 9. DMAI Burst Mode Request Timing



NOTE:
1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle, depending on byte address.

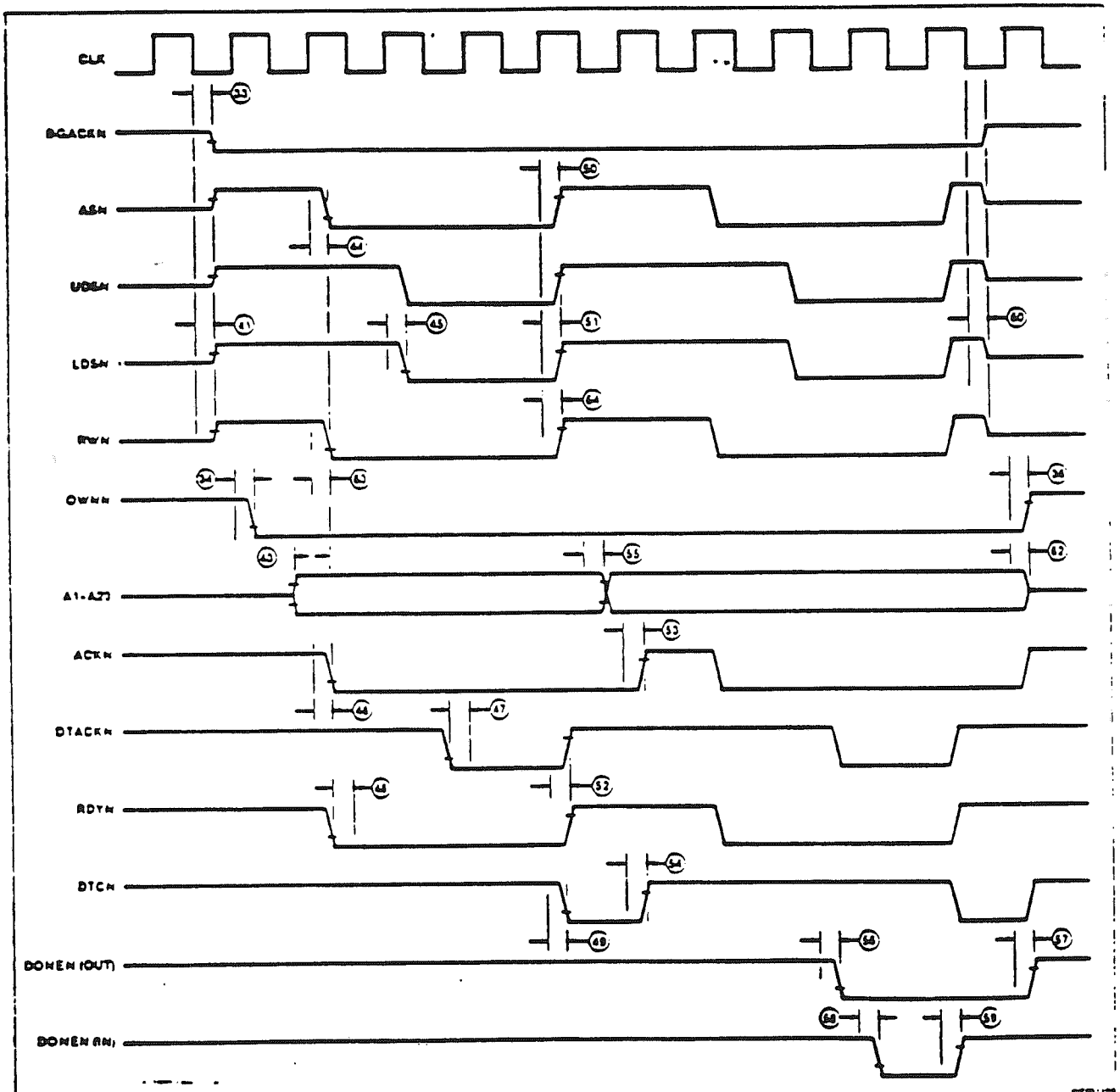
Figure 11. Read from Memory, Write to Device



NOTES

1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle, depending on byte address.
2. DMAI will release the bus after a RERUNN if there is no valid request. The next request will then retry the cycle which was terminated by the RERUNN signal.
3. RERUNN must be asserted no later than DTACKN and RDYN.
4. If a cycle is terminated by RERUNN the transfer count will be one less than the actual data transferred correctly. Two double RERUNN signals on the same cycle will terminate the DMAI operation with a status bit set and an interrupt generated (if enabled).

Figure 13. Rerun Asserted During Read from Memory, Write to Device



NOTE:
1. 16-bit transfer illustrated. For 8-bit transfer either LDSN or UDSN, but not both, will be asserted each cycle depending on byte address.

Figure 12. Write to Memory, Read from Device

APPENDIX C

1749-Z1A FIBER OPTIC U-PORT

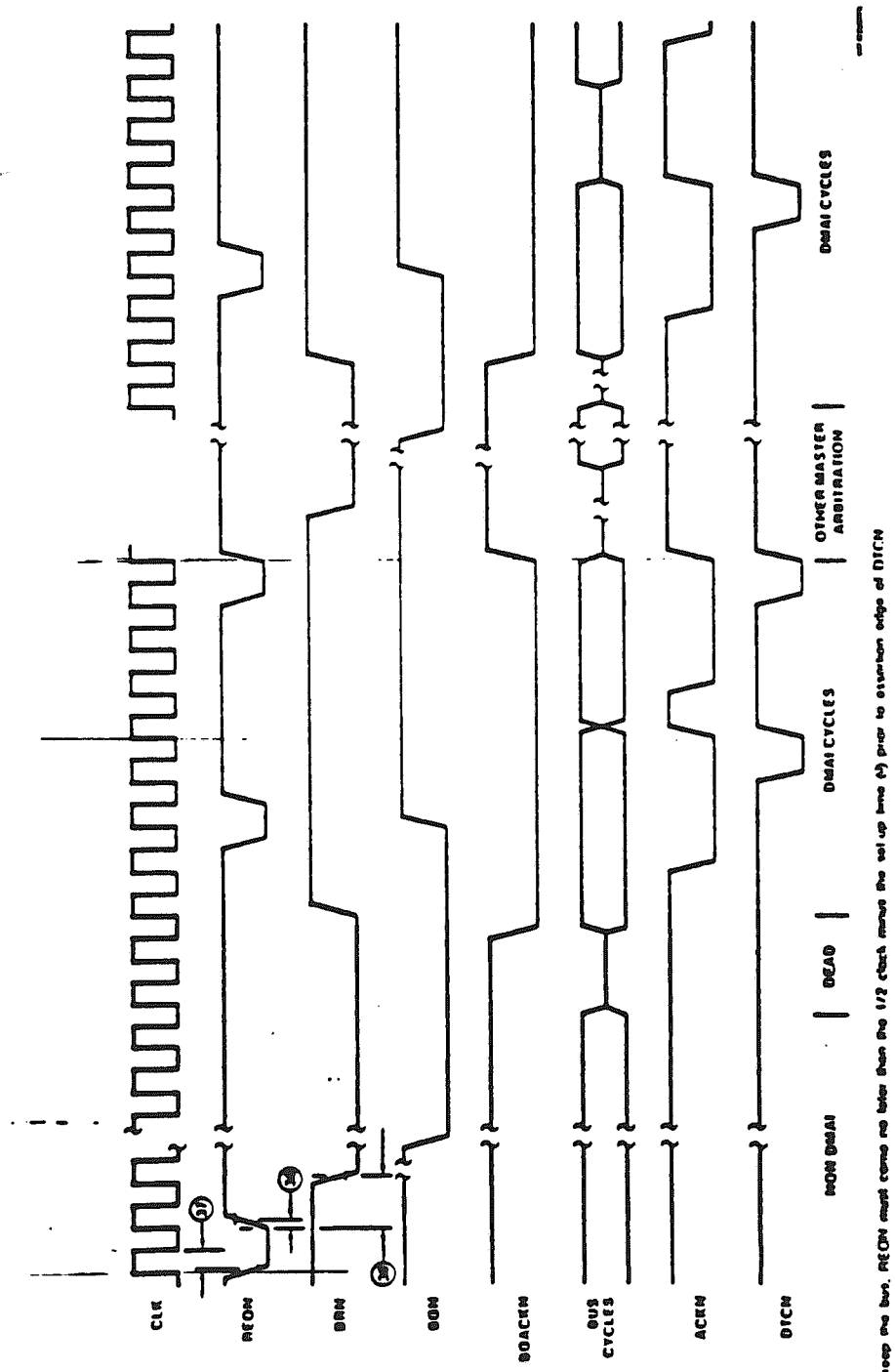


Figure 10. DMAI Cycle Steal Mode Request Timing

1749-Z1A

INSTALLATION

The Model 1749 U-Port Adapter consists of Printed Circuit card PC 302529 and Front Panel FP222140.
If the 1749 U-Port is to be installed in place of an existing 1740 D-Port do the following:

1. Remove the four screws which hold the D-Port to Transmitter card PC502103.
2. Remove the handles and module hold-in screws from the front panel (These parts will be used for the U-Port).
3. Separate the D-Port and Transmitter cards.
4. Remove the half-inch round spacer from the lower front of the Transmitter card.
5. Carefully line-up the two 20-pin connectors between the U-Port PC302529 and Transmitter PC502103 cards and mate together.
6. Use three of the four screws removed in step 1 to attach the boards.
7. Attach PC302529 to FP222140 with HEX-NUTS on Fiber Optic Transmitter and Receiver.
8. Assemble handles and hold-in screws onto FP222140.

PERFORMANCE SPECIFICATIONS

Parameter	Condition	Min	Typ	Max	Units
Optical Output	50um/.21NA Fiber	-21		-14	dbm
Optical Output	62.5um/.29NA Fiber	-16		-09	dbm
Optical Output	100um/.3NA Fiber	-11		-04	dbm
Optical Wavelength			820		nm
Optical Input	50-100um Core Dia.	-29		-08	dbm
Dynamic Range		21			dbm
Input Wavelength			820		nm

STRAP OPTIONS

STRAP	DESCRIPTION
5MHZ/2.5MHZ	These two (2) straps select the serial highway speed. When selecting either 5 MHZ or 2.5 MHZ operation, both the transmitter and receiver strap must be moved. No other adjustments are required.
STP2-STP3	These two (2) transmitter symmetry straps compensate for transmitter circuit delay variations. These straps are set at the factory and should not need to be moved.
MSB	Normally the 2140 SHD puts out 9 Space bytes for read commands and 13 Space bytes for write commands. If for some reason the Serial Crate Controller being driven by the 2140 requires More Space Bytes installing this strap will increase the Space bytes for both reads and writes to 16.

TEST POINTS

Test Points, in the form of holes in the printed circuit card, have been provided to allow scope probing of strategic points in the circuitry. A list of these points and a brief description of the circuit function at each point follows:

TP1	Positive ECL level Manchester data into the data/clock separator latch.
TP2	Ground, a convenient point to ground the scope probe. The scope probe must be grounded at the tip when looking at these high frequency signals.
TP3	Positive ECL level data separator clock.
TP5	Manchester encoded transmitter data output. The hole nearest the TP5 label is ground and the hole next to it is the signal.
TP6	Transmitter byte clock. This point can be used to sync the scope when looking at other test points.
TP7	TTL level 50 MHZ VCO clock.
TP8	Delimiter, a high-to-low transition at this point signals the start of a CAMAC command sent to the transmitter.

GENERAL DESCRIPTION

The Model 1749 U-Port Adapter uses fiber optic cables to provide transmission that is immune to electromagnetic interference and does not cause signal radiation. Being a nearly perfect insulator, the fiber optic cable allows operation with a high voltage potential difference between the Serial Highway Driver and the crates on the highway. The 1749 converts the byte clock and data signals into a self clocking Manchester encoded signal that is transmitted optically through the cable. The 1749 is intended for use with the Model 3939 in-crate U-Port Adapter.

The 1749 normally operates at five megabytes per second. Strap-selection is provided for 2.5 megabytes per second in mixed systems where the "twisted-pair" portion of the highway limits the maximum speed. Since the limiting factor in a fiber is optical loss and not data rate, a five megabyte per second rate can be achieved up to the one kilometer limit, per cable length, of the system.

OPERATION

The Model 1749 U-Port Adapter (UPA) consists of two sections the Transmitter Section and the Receiver Section.

The Transmitter Section generates a crystal controlled byte clock and then uses a basic phase-locked loop, locked to the byte clock, to produce a bit clock 10X the frequency of the byte clock.

Byte data is loaded into shift-register "U17" when decade counter "U6" overflows. Data with a start-bit and a stop-bit attached is shifted into biphase latch "U30". A differential current amplifier is used to switch approximately 65 ma peak-to-peak through the transmitting LED.

The Receiver Section uses a transimpedance amplifier and three stages of limiter amplification, to convert current from the PIN diode to an ECL level, Manchester biphase encoded, data signal. The biphase data signal is separated into NRZ data and clock signals by latch "U42".

Chips "U20", "U21", "U27" and associate gates, form a state machine which frames incoming bit-serial data into byte-serial data. This state machine also produces a symmetrical byte clock, a sequencer clock, and a read clock for the 2140 Serial Highway Receiver card.