Model 2145-Z1B

Enhanced Serial Highway Driver for SCSI

INSTRUCTION MANUAL

July, 1994

CONTENTS

TABLES

FIGURES

Schematic Drawing #232333-C-6624 See Reply Card Following Warranty

WARRANTY
SCK:rem(WP)

SCSI Enhanced Serial Highway Driver

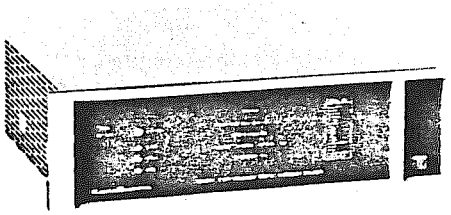
Allows a computer SCSI channel to host a Serial Highway **2145**

Features

- **Provides a dedicated SCSI bus interface to the CAMAC serial highway**
- **Supports the Enhanced highway mode with throughput of 3 Mbytes/s**
- **High-speed hardware list processing**
- **Four megabyte buffer memory**
- **Capability of timer-initiated list processing for synchronous data acquisition**
- **Available with highway port options including fiber optics and transformer isolation**
- **Up to three kilometers between highway nodes at full throughput using fiber-optic transmission**
- **Supports SCSI bus length to six meters (20 feet)**
- **Supports SCSI disconnects and reconnects**
- **Supports Asynchronous Event Notifications (AEN) for Serial Highway Demand messages**
- **Supports up to 62 nodes**

Typical Applications

- **Realtime I/O interface for a personal computer or workstation**
- **Distributed data acquisition and control**
- **Systems requiring high throughput with minimum software overhead**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 2145 Serial Highway Driver (SHD) interfaces to a host computer via the Small Computer Systems Interface (SCSI) bus and complies with ANSI specification X3.131-1986. The SCSI specification defines a standard approach for interfacing disk drives, printers and other devices to one or more host computers. This SHD operates with serial highway data rates to five Mbytes/s. It supports up to 62 remote crates for distributed data acquisition and control. The 2145 includes block-data enhancement to the serial highway, which provides effective data throughput to three Mbytes/s.

The CAMAC serial highway protocol, as defined by IEEE Standard 595, provides for one CAMAC 24-bit Dataway operation per serial highway message. The highway block-mode enhancement contained in the 2145 allows multiple Dataway operations to occur within one highway message. This alone yields a three-fold improvement in throughput. However, the Enhanced Mode uses a pipeline approach, giving a data throughput that is actually over five times as high as previous SHDs.

The 2145 contains a four megabyte memory which is used to buffer CAMAC read data obtained during timer-initiated list processing operations. This buffer memory is used to "hold" a user-programmable number of CAMAC data words. Once the requested number of data words have been acquired by the 2145, it reconnects to the host computer and empties out the contents of the buffer. This mechanism reduces the number of SCSI operations that are required to read out multiple scans of data obtained by the 2145.

Highway Options

The 2145 operates in bit-serial mode to five megabits per second or byte-serial mode to five Mbytes/s. It is available with the standard D-Port highway connectors or a self-contained U-Port adapter. Transformer isolation of the highway is available as well as fiber optics in both bit-serial and byte-serial. Using the fiber optic byte-serial highway option in conjunction with the "long highway" version of the Model 3939 U-Port Adapter at the remote crates, the full three megabyte per second throughput can be obtained with up to three kilometers between crates.

List Processing

Full-speed data throughput is obtained for single-NAF block transfers between the host computer and a single module. This can be extended to multi-NAF scan operations by using the Model 3830 List Sequencer module at remote crates. This module stores up to four NAF lists and operates with the advanced highway protocol. A Command List Processor is included in the 2145 SHD. This List Processor contains a 32 kilobyte RAM memory and supports a large number of lists. Multiple block transfers can be included in a list.

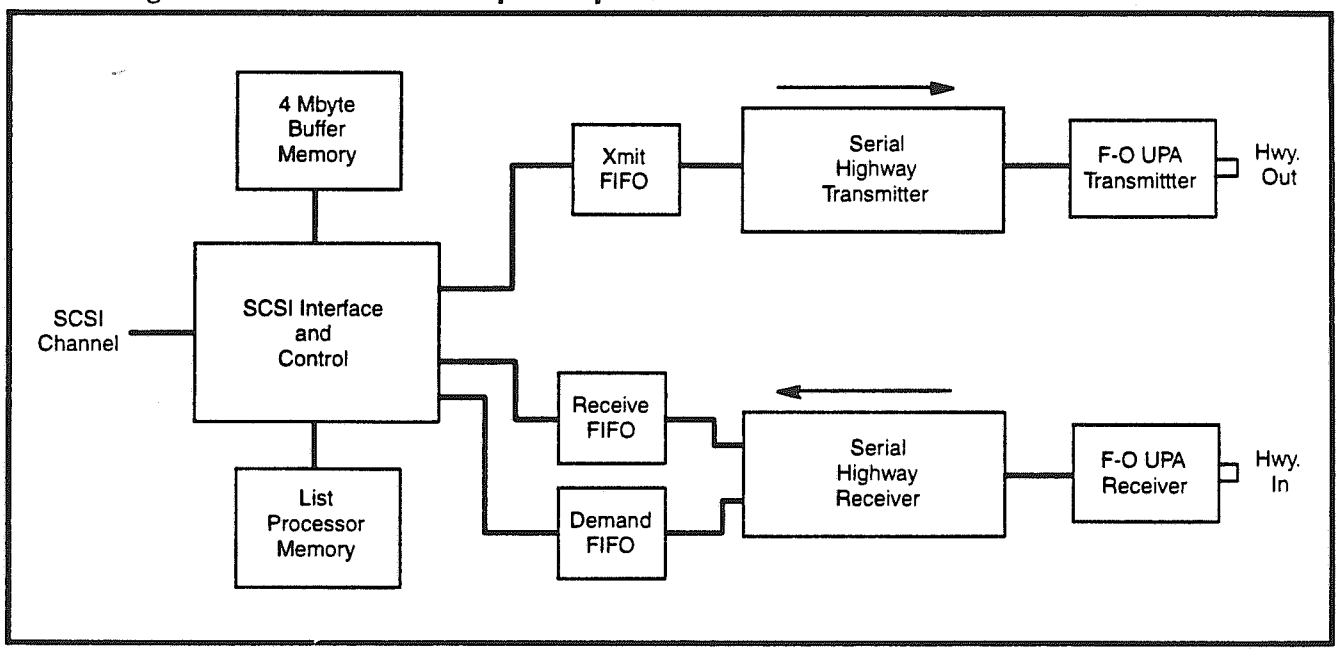
Highway Compatibility

In addition to the Enhanced Mode, the 2145 includes software-selected operating modes for Q-Stop, Q-Ignore, Q-Repeat, and Q-Scan block transfers, making it usable with any type L-2 serial crate controller (SCC) meeting the specifications of IEEE-595. Enhanced-Mode messages require the KSC 3952-Z1E or 3952-Z1F. The compatibility of the enhanced protocol allows "Standard" and "Enhanced" L-2 SCCs to be mixed on the same highway, provided that the software directs enhanced block messages only to the enhanced SCCs.

SCSI bus Interface

The SCSI bus, as used by the 2145, contains an eight-bit data path with parity, nine control signals, terminator power, and associated ground return conductors. All signals are unbalanced, and the maximum total bus length is six meters (20 feet). Third party bus extenders are available to provide balanced-line or fiber optic extensions to the SCSI bus. Two connectors are provided on the rear of the 2145 to "pass through" the SCSI bus. One connector is low-density 50 contact and the other is high-density 50 contact.

Block Diagram (shown with fiber-optic U-port)



Physical Arrangement

The 2145 includes a cabinet that is 3U (5¼ inches) high and is rack-mountable. The connectors for the SCSI bus and the CAMAC serial highway are mounted on the rear-panel. The U-Port options are mounted within the 2145 cabinet assembly.

Ordering Information

Model 2145-Z1A Enhanced Serial Highway Driver, for SCSI host, HP computers

Model 2145-Z1B Enhanced Serial Highway Driver, for SCSI host, DEC computers

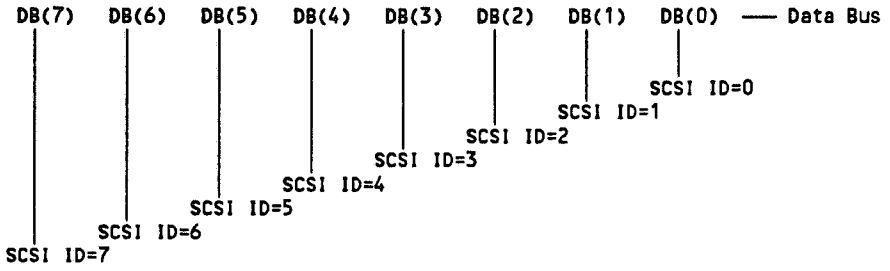
Note: A 1730 D-port or 1736, 1738 or 1739 U-port Adapter must also be ordered to form a complete Serial Highway Driver.

Associated Products

Model 1730-D2B	D-port Adapter, bit-serial & byte-serial, for model 2145
Model 1736-B2B	U-port Adapter, bit-serial, for model 2145
Model 1738-Z2B	U-port Adapter, bit-serial, fiber optic, 820 nm, for model 2145
Model 1739-Z2C	U-port Adapter, byte-serial, fiber optic, 1300 nm, for model 2145
Model 1739-Z2D	U-port Adapter, byte-serial, fiber optic, 820 nm, for model 2145
Model 3830-Z1A	List Sequencer for 3952 Serial Crate Controllers
Model 3939-Z1C	U-port Adapter, byte-serial, fiberoptic, 1300 nm operation
Model 3939-Z2A	U-port Adapter, byte-serial, fiberoptic, 1300 nm operation
Model 3952-Z1G	Enhanced Serial Crate Controller, type L-2, with standard relays
Model 3952-Z1H	Enhanced Serial Crate Controller, type L-2, with high-gauss relays

SCSI BUS

The following is a description of the SCSI specification. Specification details, not applicable to the 2145, have been omitted. Communication on the SCSI bus is allowed between only two SCSI devices at any one given time. A maximum of eight SCSI devices may be present on the SCSI bus. Each SCSI device has an individual SCSI ID bit assigned as shown below.



When two SCSI devices communicate on the SCSI bus, one device acts as the initiator and the other as the target. The initiator invokes an operation and the target performs the operation. A SCSI device usually has a fixed role as an initiator or target. The 2145 is a target device, but can become a temporary initiator. The temporary initiator role is used for sending an Asynchronous Event Notification (AEN) to an initiator. This is used by the 2145 to inform the initiator that a Look-At-Me (LAM) is pending.

Certain SCSI bus functions are assigned to the initiator and also to the target. The initiator arbitrates for the SCSI bus and selects a target. The target may then request the transfer of Command, Status, Data, or other information on the SCSI bus. In some cases, the target may arbitrate for the SCSI bus and reselect an initiator for the purpose of continuing an operation.

Information transfers on the SCSI data bus are asynchronous and follow a Request/Acknowledge handshake protocol. One byte of information is transferred per Req/Ack cycle.

SCSI BUS SIGNALS

There are a total of eighteen signals that the 2145 uses to communicate with an initiator. Nine of these signals are control lines and the other nine are for data. Eight of the data signals are for the eight data bits and the ninth is for data parity. The allocation of these signals on the front panel connectors of the 2145 is found in APPENDIX A. The following is a brief description of the SCSI bus signals:

BSY (BUSY)	Busy is an "OR-tied" signal that is asserted to indicate that the SCSI bus is being used.
SEL (SELECT)	Select is an "OR-tied" signal asserted by the initiator to select a target or for a target to select an initiator.

C/D (CONTROL/DATA)	Control/Data is a signal driven by a target to indicate whether control or data information is on the SCSI data bus. When this signal line is asserted, control information is present on the SCSI data bus.
I/O (INPUT/OUTPUT)	Input/Output is a signal driven by a target to control the direction of data transfer on the SCSI data bus with respect to the initiator. This signal is asserted to indicate data transfer from the target to the initiator. This signal has a second purpose which is to distinguish between SELECTION and RESELECTION phases.
MSG (MESSAGE)	Message is a signal asserted by the target during a message phase.
REQ (REQUEST)	Request is a signal asserted by a target to indicate a request for a Req/Ack data transfer handshake on the SCSI bus.
ACK (ACKNOWLEDGE)	Acknowledge is a signal asserted by an initiator to indicate the acknowledgement for a Req/Ack data transfer handshake.
ATN (ATTENTION)	Attention is a signal asserted by an initiator to indicate the Attention condition. The Attention condition is used to inform a target that the initiator has a Message pending.
RST (RESET)	Reset is an "OR-tied" signal which, when asserted, indicates the Reset condition.
DB(7-0,P) (DATA BUS 7-0,PARITY)	DB(7) through DB(0) are the eight data bits on the SCSI bus and DB(P) is the parity signal. DB(7) is the most significant bit and has the highest priority during an ARBITRATION phase for the SCSI bus. The bit number, significance and priority, decreases downward to DB(0). A data bit is defined as one when the signal line is asserted, and as zero when the signal line is negated. DB(P) is generated to maintain odd parity on the SCSI bus.

SCSI SIGNAL SOURCES

The following table shows which type of SCSI device is allowed to assert each signal. This chart does not show if the source is driving the signal asserted, driving negated, or is passive. All SCSI device drivers that are not active sources are in the passive state. Note that the RESET signal may be sourced by any device at any time.

TABLE 1 - SCSI Signal Source

	SIGNALS				
Bus Phase	BSY	SEL	C/D,I/O MSG,REQ	ACK/ATN	DB(7-0,P)
BUS FREE	NONE	NONE	NONE	NONE	NONE
ARBITRATION	ALL	WINNER	NONE	NONE	SCSI ID
SELECTION	I & T	INITIATOR	NONE	INITIATOR	TARGET
RESELECTION	I & T	TARGET	TARGET	INITIATOR	TARGET
COMMAND	TARGET	NONE	TARGET	INITIATOR	INITIATOR
DATA IN	TARGET	NONE	TARGET	INITIATOR	TARGET
DATA OUT	TARGET	NONE	TARGET	INITIATOR	INITIATOR
STATUS	TARGET	NONE	TARGET	INITIATOR	TARGET
MESSAGE IN	TARGET	NONE	TARGET	INITIATOR	TARGET
MESSAGE OUT	TARGET	NONE	TARGET	INITIATOR	INITIATOR

ALL: The signal is driven by all SCSI devices that are actively arbitrating.

SCSI ID: A unique data bit is driven by each SCSI device that is actively arbitrating. The other seven data bits are not driven by the arbitrating device.

I & T: The signal is driven by the initiator, target, or both as specified in the SELECTION or RESELECTION phase.

INITIATOR: If this signal is to be driven, it is only driven by an active initiator.

TARGET: If the signal is to be driven, it is only driven by an active target.

WINNER: The signal is driven by the one SCSI device that wins the arbitration.

NONE: The signal is NOT driven by any SCSI device.

SCSI BUS TIMING

The following describes some basic timing requirements that are used in the discussion of the SCSI bus phases:

Arbitration Delay (2.2 microseconds).

> This is the minimum time a SCSI device waits from asserting BSY for arbitration until the data bus can be examined to see if arbitration has been won. There is no maximum time specified for this delay.

Assertion Period (90 nanoseconds).

This is the minimum time a target asserts REQ while using synchronous data transfers. This is also the minimum time that an initiator asserts ACK while using synchronous data transfers.

Bus Clear Delay (800 nanoseconds).

This is the maximum time for any SCSI device to stop driving all bus signals after:

1. The BUS FREE phase is detected (indicated by BSY and SEL false for a bus settle delay.

2. SEL is received from another SCSI device during an ARBITRATION phase.

3. The transition of RST to asserted.

Bus Free Delay (800 nanoseconds).

This is the minimum time that a SCSI device waits from detecting the BUS FREE phase until its assertion of BSY when going to the ARBITRATION phase.

Bus Set Delay (1.8 microseconds).

This is the maximum time for a SCSI device to assert BSY and its SCSI ID on the data bus after it detects a BUS FREE phase for the purpose of entering the ARBITRATION phase.

Bus Settle Delay (400 nanoseconds).

This is the time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

Cable Skew Delay (10 nanoseconds).

The maximum difference in propagation time between any two SCSI bus signals when measured between any two SCSI devices.

Data Release Delay (400 nanoseconds).

This is the maximum time for an initiator to release the data bus following the transition of the I/O signal from false to true.

Deskew Delay (45 nanoseconds).

This is the minimum time required for deskew of certain signals.

Hold Time (45 nanoseconds).

This is the minimum time added between the assertion of REQ or ACK and the changing of the data lines to provide hold time in the initiator or target, respectively, using synchronous data transfers.

Negation Period (90 nanoseconds).

This is the minimum time a target negates REQ while using synchronous data transfers. This is also the minimum time an initiator may negate ACK when using synchronous data transfers.

Reset Hold Time (25 microseconds).

This time is the minimum time for which RST is asserted. There is no maximum time specified.

Selection Abort Time (200 microseconds).

This is the maximum time a target (or initiator) may take from its most recent detection of being selected (or reselected) until asserting BSY. This timeout is required to ensure a target (or initiator) does not assert BSY after a SELECTION (or RESELECTION) phase has been aborted.

Selection Timeout Delay (250 milliseconds).

This is the minimum time that an initiator (or target) should wait for a BSY response during a SELECTION (or RESELECTION) phase before starting the timeout procedure.

SCSI BUS PHASES

The SCSI protocol describes eight phases as follows:

BUS FREE phase
ARBITRATION phase
SELECTION phase
RESELECTION phase
COMMAND phase
DATA phase
STATUS phase — These phases are collectively termed information transfer phases.
MESSAGE phase

The SCSI bus can never be in more than one phase at any given time. In the following bus phase descriptions, signals that are not mentioned are not asserted.

BUS FREE Phase

The BUS FREE phase indicates that there is no SCSI device currently using the SCSI bus and that it is available for use. Targets may revert to the BUS FREE phase to indicate an error condition that it does not know how to recover from.

SCSI devices detect the BUS FREE phase when SEL and BSY are both false for at least a bus settle delay.

SCSI devices release all SCSI bus signals within a bus clear delay after SEL and BSY are continuously false for a bus settle delay. If a SCSI device requires more than a bus settle delay to detect a BUS FREE phase, it will release all SCSI bus signals within a bus clear delay minus the excess time needed to detect a BUS FREE phase. The total time to clear the SCSI bus does not exceed a bus settle delay plus a bus clear delay.

ARBITRATION Phase

The ARBITRATION phase allows one SCSI device to obtain control of the SCSI bus so that it may assume the role of a target or initiator. The procedure for a SCSI device to obtain control of the SCSI bus is as follows:

1. The SCSI device must first wait for the BUS FREE phase to occur. The BUS FREE phase is detected when both BSY and SEL are continually and simultaneously false for a minimum of a bus settle delay.

2. The SCSI device must wait a minimum of a bus free delay after the detection of a BUS FREE phase before driving any signal.

3. Following the bus free delay as in step 2, the SCSI device may arbitrate for the SCSI bus by asserting both BSY and its own SCSI ID, however, the SCSI device cannot arbitrate if more than a bus set delay has passed since the last BUS FREE phase was last detected.

4. After waiting at least an arbitration delay, which is measured from its assertion of BSY, the SCSI device examines the data bus. If a higher priority SCSI ID bit is asserted on the data bus (DB(7) has the highest priority), then the SCSI device has lost the arbitration and then removes its asserted signals and returns to step 1. If no other higher priority SCSI ID bit is asserted on the SCSI data bus, then the SCSI device has won the arbitration and asserts the SEL signal. Any other SCSI device that was participating in the arbitration has lost and removes its assertion of BSY and its SCSI ID bit within a bus clear delay after SEL is asserted. A SCSI device that loses the arbitration may return to step 1.

5. The SCSI device that wins arbitration, waits for at least a bus clear delay plus a bus settle delay after asserting SEL before changing any signal states on the SCSI bus.

   Note: The SCSI ID bit is a single bit on the data bus that corresponds to the SCSI device's unique SCSI address.

Parity, DB(P), is not valid during this phase, but cannot be driven to the false state.

SELECTION Phase

The SELECTION phase allows an initiator to select a target for the purpose of initiating a target function. During the SELECTION phase, the I/O signal is negated to differentiate it from the RESELECTION phase.

The SCSI device that won the arbitration has both BSY and SEL asserted and has delayed at least a bus clear delay plus a bus settle delay before terminating the ARBITRATION phase. The SCSI device that won the arbitration becomes the initiator by releasing the I/O signal. The initiator then sets the data bus to a value that is the "OR" of its SCSI ID bit and the targets SCSI ID bit. The initiator waits for at least two deskew delays and releases BSY. The initiator then waits for at least a bus settle delay before looking from a response from the target.

The target determines it has been selected when the SEL signal is asserted and its SCSI ID bit is true and the BSY and I/O signals are false for at least a bus settle delay. The selected target examines the data bus in order to determine the SCSI ID of the selecting initiator. The selected target then asserts the BSY signal within a selection abort time of its most recent detection of being selected. This is required for proper operation of the selection timeout procedure.

At least two deskew delays after the initiator detects BSY is asserted, it releases SEL and then may change the data bus.

SELECTION Timeout Procedure

There are two optional selection timeout procedures specified for clearing the SCSI bus if the initiator waits a minimum of a selection timeout delay and there has been no BSY response from the target.

1. Optionally, the initiator may assert the RST signal.

2. Optionally, the initiator continues to assert SEL and releases the data bus. If the initiator has not detected BSY to be asserted after at least a selection abort time plus two deskew delays, the initiator releases SEL allowing the SCSI bus to go to the BUS FREE phase. SCSI devices must ensure that when responding to selection that a selection was still valid within a selection abort time of their assertion of BSY. Failure to comply with this requirement could result in an improper selection.

RESELECTION Phase

RESELECTION is an optional phase permitting a target to reconnect to an initiator for the purpose of continuing an operation started by the initiator but was suspended by the target. This occurs when the target disconnects by allowing a BUS FREE phase to occur before the

operation was completed. RESELECTION is only used in systems that have the ARBITRATION phase implemented.

After completing the ARBITRATION phase, the winning SCSI device has both the BSY and SEL signals asserted and has delayed at least a bus clear delay plus a bus settle delay. The winning SCSI device becomes the initiator by asserting the I/O signal. The winning SCSI device also sets the data bus to a value that is the "OR" of its SCSI ID and the initiators SCSI ID. The target waits for at least two deskew delays and then releases BSY. The target waits for at least a bus settle delay before looking for a response from the initiator.

The initiator determines if it is reselected when SEL, I/O, and its SCSI ID bit are asserted and BSY is false for at least a bus settle delay. The reselected initiator then examines the data bus to determine the SCSI ID of the reselecting target. The reselected initiator asserts the BSY signal within a selection abort time of its most recent detection of being reselected. This is required for the correct operation of the timeout procedure.

After the target detects BSY, it also asserts BSY and waits at least two deskew delays and then releases SEL. The target may then change the I/O signal and the data bus signals. After the reselected initiator detects SEL is negated, it releases BSY. The target continues to assert BSY until it is ready to relinquish the SCSI bus.

RESELECTION Timeout Procedure

Two optional RESELECTION timeout procedures are specified for clearing the SCSI bus during a RESELECTION phase. If the target waits a minimum of a selection timeout delay and there has been no BSY response from the initiator:

1. Optionally, the target may assert the SCSI RST signal.

2. Optionally, the target may continue asserting SEL and I/O and release the data bus signals. If the target has not detected BSY to be true for at least a selection abort time plus two deskew delays, the target releases SEL and I/O allowing the SCSI bus to go to the BUS FREE phase.

Information Transfer Phases

The COMMAND, DATA, STATUS, and MESSAGE phases are grouped together as information transfer phases. In each of these phases, data is transferred over the SCSI data bus. The actual data transferred depends on the type of operation being performed on the SCSI bus.

The C/D, I/O, and MSG signals are used to distinguish between the different information transfer phases. The target drives these three signals and thereby controls all the changes from one phase to the next. The initiator may request a MESSAGE OUT phase by asserting the ATN signal. The target may cause a BUS FREE phase by releasing the MSG, C/D, I/O and BSY signals.

The following table shows the information transfer phases based upon the MSG, C/D, and I/O signals:

TABLE 2 - SCSI Transfer Phases

SIGNAL					
MSG	C/D	I/O	PHASE	DIRECTION OF TRANSFER	COMMENT
0	0	0	DATA OUT	INITIATOR TO TARGET	DATA PHASE
0	0	1	DATA IN	INITIATOR FROM TARGET	
0	1	0	COMMAND	INITIATOR TO TARGET	
0	1	1	STATUS	INITIATOR FROM TARGET	
1	0	0	RSVD		
1	0	1	RSVD		
1	1	0	MESSAGE OUT	INITIATOR TO TARGET	MESSAGE PHASE
1	1	1	MESSAGE IN	INITIATOR FROM TARGET	

0 = FALSE (NEGATED)
1 = TRUE (ASSERTED)
RSVD = RESERVED FOR FUTURE STANDARDIZATION

The information transfer phases uses one or more REQ/ACK handshakes to control the information transfers. Each REQ/ACK handshake allows the transfer of one information byte. BSY remains asserted and SEL remains negated during the information transfer phases. Also, during the information transfer phases, the target continuously envelops the REQ/ACK handshake(s) with C/D, I/O and MSG. These control signals are valid for a bus settle delay before the assertion of REQ of the first handshake and remain valid until the negation of ACK at the end of the last handshake.

Asynchronous Information Transfers

The target controls the direction of information transfers via the I/O signal. When I/O is asserted, information is transferred from the target to the initiator. When I/O is negated, information is transferred from the initiator to the target.

If I/O is asserted (transfer to the initiator), the target first drives the DB(7-0,P) to their desired values. The target then delays one deskew delay plus a cable skew delay and then asserts REQ. DB(7-0,P) remains valid until ACK is true at the target. The initiator reads DB(7-0,P) after REQ is asserted. The initiator then signals its acceptance of the data by asserting ACK. When ACK becomes true at the target, the target may change or release DB(7-0,P) and negate ACK. After ACK is false, the target may continue the transfer by driving DB(7-0,P) and asserting REQ as above.

If I/O is false (transfer to the target), the target requests information by asserting REQ. The initiator drives DB(7-0,P) to the desired values. It then waits for one deskew delay plus a cable skew delay and asserts ACK. The initiator continues to drive DB(7-0,P) until REQ is false. When ACK becomes true at the target, the target reads DB(7-0,P) and negates REQ. When REQ becomes false at the initiator, the initiator may change or release DB(7-0,P) and negate ACK. The target may continue the transfers by asserting REQ as described above.

Synchronous Information Transfers

Synchronous data transfer is optional and is only used during data phases, DATA IN or DATA OUT. This mode is used in a data phase if a synchronous data transfer agreement has been previously established. Refer to the SYNCHRONOUS DATA TRANSFER REQUEST message for further details.

A REQ/ACK offset is used to specify the maximum number of REQ pulses that can be sent by the target in advance of the number of ACK pulses received from the initiator, which establishes a pacing mechanism. If the number of REQ pulses exceeds the number of ACK pulses by the REQ/ACK offset, the target will not assert REQ signal until after the leading edge of the next ACK pulse is received. For successful completion of the data phase, the number of REQ and ACK pulses must be equal.

The target asserts the REQ signal for a minimum of an assertion period. The target then waits at least the greater of a transfer period from the last transition of the REQ signal to true or a minimum of a negation period from the last transition of the REQ signal to false before re-asserting the REQ signal.

The initiator sends one pulse on the ACK line for each REQ pulse received. The ACK signal may be asserted as soon as the leading edge of the corresponding REQ pulse has been received. The initiator asserts the ACK signal for a minimum of an assertion period. The initiator waits at least the greater of a transfer period from the last transition of the ACK signal to true or for a minimum of a negation period from the last transition of ACK signal to false before re-asserting the ACK signal.

If the I/O signal is true (transfer to the initiator), the target first drives the DB(7-0,P) signals to the desired states. It waits at least one deskew delay plus one cable skew delay and then asserts the REQ signal. The DB(7-0,P) are held valid for a minimum of one deskew delay plus one cable skew delay plus one hold time after the assertion of the REQ signal. The target asserts the REQ signal for a minimum of an assertion period. The target may then negate the REQ signal and change or release the DB(7-0,P) signals. The initiator then reads the data from the DB(7-0,P) lines within one hold time of the transition of the REQ signal to true. The initiator then responds with an ACK pulse.

If the I/O signal is false (transfer to the target), the initiator transfers one byte for every REQ pulse received. After receiving the leading edge of a REQ pulse, the initiator drives the DB(7-0,P) lines to the desired values. It then waits at least one deskew delay plus one cable skew delay and then asserts ACK. The initiator holds the DB(7-0,P) lines valid for a least one deskew delay plus one cable skew delay plus one hold time after the assertion of the ACK signal. The initiator asserts the ACK signal for a minimum of an assertion period. The initiator may then negate the ACK signal and may change or release the DB(7-0,P) signals. The target then reads the data on the DB(7-0,P) lines within one hold time of the transition of the ACK signal to true.

COMMAND Phase

The COMMAND phase allows a target to request command information from an initiator. The target asserts the C/D signal and negates the I/O and MSG signals during the REQ/ACK handshake(s) for this phase.

Data Phase

> The Data phase encompasses both the DATA IN phase and the DATA OUT phase.

DATA IN Phase

> The DATA IN phase allows the target to request that data be sent to the initiator from the target.

DATA OUT Phase

> The DATA OUT phase allows the target to request that data be sent from the initiator to the target.

STATUS Phase

> The STATUS phase allows the target to request that status information be sent from the target to the initiator.

The target asserts the C/D and I/O signals and negates the MSG signal during the REQ/ACK handshake of this phase.

MESSAGE Phase

The message phase is a term that refers to either a MESSAGE IN or a MESSAGE OUT phase. Multiple messages may be sent during either phase. The first byte transferred in either of these phases is either a single-byte message or the first byte of a multi-byte message. Multi-byte messages are wholly contained within a single message phase.

MESSAGE IN Phase

The MESSAGE IN phase allows the target to request that a message(s) be sent to the initiator from the target.

The target asserts the C/D, I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

MESSAGE OUT Phase

The MESSAGE OUT phase allows a target to request that message(s) be sent from the initiator to the target. The target may invoke this phase at any time in response to the ATTENTION condition generated by the initiator.

The target asserts the C/D and MSG signal and negates the I/O signal during the REQ/ACK handshake(s) of this phase.

The target handshake(s) bytes in this phase until ATTENTION is negated by the initiator.

Signal Restriction Between Phases

When the SCSI bus is between two information transfer phases, the following restrictions apply to the SCSI bus signals.

1. The BSY, SEL, REQ, and ACK signals must not change.

2. The C/D, I/O, MSG, and data bus signals may change. When switching the data bus direction from out (initiator driving) to in (target driving), the target must delay driving the data bus by at least a data release time plus a bus settle delay after asserting the I/O signal and the initiator must release the data bus no later than a data release delay after the transition of the I/O signal to true.

   When switching the data bus direction from in (target driving) to out (initiator driving), the target must release the data bus no later than a deskew delay after negating the I/O signal.

3. The ATN and RST signals may change as defined under the descriptions for the ATTENTION and RESET conditions.

SCSI Bus Conditions

The SCSI bus has two asynchronous conditions: the ATTENTION condition and the RESET condition. These cause the SCSI device to perform certain actions and thus alter the phase sequence.

ATTENTION Condition

The ATTENTION condition allows an initiator to inform a target that the initiator has a message ready. The target may retrieve this message at its convenience by executing a MESSAGE OUT phase.

The initiator creates the ATTENTION condition by asserting the ATN signal at any time except during the ARBITRATION or BUS FREE phases.

A target responds with a MESSAGE OUT phase as follows:

1. If the ATN signal becomes true during a COMMAND phase, the target enters the MESSAGE OUT phase after transferring part or all of the command descriptor block bytes.

2. If the ATN signal becomes true during a DATA phase, the target enters the MESSAGE OUT phase at the targets earliest convenience. The initiator continues the REQ/ACK handshake(s) until it detects the phase change.

3. If the ATN signal becomes true during a STATUS phase, the target will enter the MESSAGE OUT phase after the status byte has been acknowledged by the initiator.

4. If the ATN signal becomes true during a MESSAGE IN phase, the target enters the MESSAGE OUT phase before it sends another message. This permits a MESSAGE PARITY ERROR message from the initiator to be associated with the appropriate message.

5. If the ATN signal becomes true during a SELECTION phase and before the initiator releases the BSY signal, the target enters the MESSAGE OUT phase immediately after that SELECTION phase.

6. If the ATN signal becomes true during a RESELECTION phase, the target enters the MESSAGE OUT phase after the target has sent its IDENTIFY message for that RESELECTION phase.

The initiator keeps the ATN signal asserted if more than one message byte is to be transferred. The initiator may negate ATN at any time except while the ACK signal is asserted during a MESSAGE OUT phase. Normally, the initiator negates the ATN signal while the REQ is true and the ACK is false during the last REQ/ACK handshake of the MESSAGE OUT phase.

Reset Condition

The reset condition is used to immediately clear all SCSI devices from the bus. This condition takes precedence over all other phases and conditions. Any SCSI device may generate the reset condition by asserting the RST signal for a minimum of a reset hold time. During the reset condition, the state of all SCSI bus signals is undefined.

All SCSI devices must release all SCSI bus signals (except RST) within a bus clear delay of the transition of the RST to true. The BUS FREE phase always follows a reset condition.

Hard Reset Alternative

The 2145 implements the Hard Reset Alternative. When a reset condition occurs, the 2145:

1. Clears all uncompleted commands.

2. Sets all internal registers to their power-up states.

SCSI BUS PHASE SEQUENCERS

The order in which phases are used on the SCSI bus follows a prescribed sequence. The reset condition can abort any phase and is always followed by a BUS FREE phase. Also, any other phase can be followed by the BUS FREE phase, but many such instances are error conditions. The additional allowable sequences are shown in Figure 1.

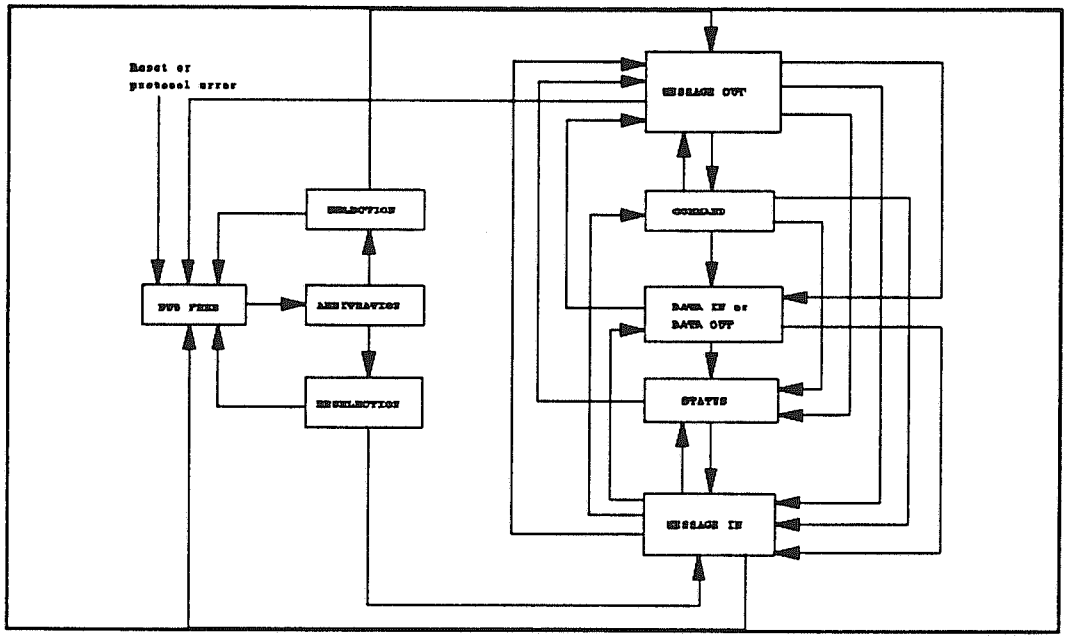


FIGURE 1 - SCSI Bus Phase Sequences

The normal progression is from the BUS FREE phase to ARBITRATION, from ARBITRATION to SELECTION or RESELECTION, and from SELECTION or RESELECTION to one or more of the information transfer phases (COMMAND, DATA, STATUS, or MESSAGE). The final information phase is usually the MESSAGE IN phase where a DISCONNECT or COMMAND COMPLETE message is transferred, followed by the BUS FREE phase.

Message System Specification

The message system allows communication between an initiator and the target for the purpose of physical data path management.

Message Codes

The following table shows the messages that the 2145 implements:

TABLE 3 - 2145 Messages

CODE	SUPPORT INIT	SUPPORT TARG	MESSAGE NAME	DIRECTION		NEGATE ATN BEFORE LAST ACK
06h	O	M	ABORT		OUT	YES
0Ch	O	M	BUS DEVICE RESET		OUT	YES
00h	M	M	COMMAND COMPLETE	IN		---
04h	O	O	DISCONNECT	IN		---
04h	O	O	DISCONNECT		OUT	YES
05h	M	M	INITIATOR DETECTED ERROR		OUT	YES
09h	M	M	MESSAGE PARITY ERROR		OUT	YES
07h	M	M	MESSAGE REJECT	IN	OUT	YES
08h	M	M	NO OPERATION		OUT	YES
***	O	O	SYNCH DATA TRANSFER REQUEST	IN	OUT	YES
80h - FFh	M	M	IDENTIFY		OUT	NO

M -- MANDATORY
IN -- TARGET TO INITIATOR
YES -- INITIATOR MUST NEGATE ATN BEFORE LAST ACK OF MESSAGE
NO -- INITIATOR MAY OR MAY NOT NEGATE ATN BEFORE LAST ACK OF MESSAGE
0 -- OPTIONAL
OUT -- INITIATOR TO TARGET
-- NOT APPLICABLE

SCSI MESSAGES

COMMAND COMPLETE -- 00 Hex

This message is sent from a target to an initiator to indicate that the execution of a command has been completed and that a valid status byte has been sent to the initiator. After successfully sending this message, the target goes to the BUS FREE phase by releasing the BSY signal. The target considers this message transfer to be successful when it detects the negation of ACK for the COMMAND COMPLETE message with the ATN signal false.

DISCONNECT -- 04 Hex

The DISCONNECT message is sent from a target to inform an initiator that the present connection is going to be broken. This disconnection is accomplished by the target releasing the BSY signal. A later reconnection is required in order to complete the current requested command. After successfully sending this message, the target goes to the BUS FREE phase by releasing the BSY signal. The target considers the message transmission successful when it detects the negation of the ACK signal for the DISCONNECT message with the ATN signal false.

This message may also be sent from an initiator to a target to instruct the target to disconnect from the SCSI bus. If this option is supported, and after the DISCONNECT message is

received, the target switches to MESSAGE IN phase, sends the DISCONNECT message to the initiator, and then disconnects from the SCSI bus by releasing the BSY signal. After releasing the BSY signal, the target cannot participate in another ARBITRATION phase until there is a disconnection delay. If this option is not supported, or the target cannot disconnect at the time when it receives the DISCONNECT message from the initiator, the target responds by sending a MESSAGE REJECT message to the initiator.

INITIATOR DETECTED ERROR -- 05 Hex

The INITIATOR DETECTED ERROR message is sent from an initiator to inform a target that an error has occurred. This does not preclude the target from retrying the operation. The source of the error may either be related to previous activity on the SCSI bus or may be internal to the initiator and unrelated to any previous SCSI bus activity.

ABORT -- 06 Hex

The ABORT message is sent from the initiator to the target to clear the present operation. All pending data and status for the initiator that issued the command are cleared, and the target goes to the BUS FREE phase. No status or ending messages are sent for this operation.

MESSAGE REJECT -- 07 Hex

The MESSAGE REJECT is sent from either a target or initiator to indicate that the last message or message byte it received was inappropriate or has not been implemented.

In order to indicate its intentions of sending this message, the initiator asserts the ATN signal prior to its release of the ACK signal for the REQ/ACK handshake of the message byte to be rejected. If the target receives this message under any other circumstances, it rejects this message.

When a target sends this message, it changes to the MESSAGE IN phase and sends this message prior to requesting additional message bytes from the initiator. This provides an interlock so that the initiator can determine which message byte is rejected.

After the target sends a MESSAGE REJECT message and if the ATN signal is still asserted, it returns to the MESSAGE OUT phase. The subsequent MESSAGE OUT phase begins with the first byte of the message.

NO OPERATION -- 08 Hex

The NO OPERATION message is sent from an initiator, in response to a targets request for a message, when the initiator does not currently have any other message to send.

MESSAGE PARITY ERROR -- 09 Hex

The MESSAGE PARITY ERROR message is sent from the initiator to the target to indicate that the last message byte it received had a parity error.

In order to indicate its intention of sending this message, the initiator asserts the ATN signal prior to its release of the ACK signal for the REQ/ACK handshake of the message byte that has the parity error. This provides an interlock so that the target can determine which message byte had the parity error.

If the target returns to the MESSAGE IN phase before switching to some other phase, after receiving the MESSAGE PARITY ERROR message, the target can resend the entire message that had the parity error.

BUS DEVICE RESET -- 0C Hex

The BUS DEVICE RESET message is sent from an initiator to direct a target to clear all current operations. This message forces a hard reset condition to be entered on the SCSI device. The target then goes to the BUS FREE phase after reception of this message.

IDENTIFY 80-FF Hex

The IDENTIFY message may be sent from either an initiator or target for the purpose of establishing a physical path connection between a target and initiator.

Bit Byte	7	6	5	4	3	2	1	0
0	IDENT	DSC	LUNTR	RSVD	RSVD	LUNTRN		

IDENT -- This bit is always set to a one to indicate an IDENTIFY message.

DSC -- This bit is only set to one by the initiator. When set to 1, it indicates that the initiator has the ability to accommodate disconnection and reconnection.

LUNTR -- This bit is set to zero indicates that the IDENTIFY message is directed to a logical unit. This bit is set to one to indicate the IDENTIFY message is directed to a target routine that does not involve a logical unit.

RSVD -- These bits are reserved and must be set to zero.

LUNTRN -- This field is for the logical unit number target routine number. This field specifies a logical unit number if the LUNTR is set to zero. If the LUNTR bit is set to one, this field specifies a target routine number.

Since the 2145 does not implement target routines, the LUNTR bit must be set to zero. Also, since the 2145 does not support multiple logical units, the LUNTRN field must be set to zero.

Synchronous Data Transfer Request

A Synchronous Data Transfer Request (SDTR) message exchange is initiated by a SCSI device whenever a previously arranged data transfer agreement may have become invalid. The agreement becomes invalid after any condition that may leave the data transfer agreement in an undeterminate state such as:

1. after a HARD reset condition
2. after a BUS DEVICE RESET message
3. after a power-up cycle

Any SCSI device that is capable of synchronous data transfers does not respond to this message with a MESSAGE REJECT message.

The SDTR message exchange establishes the allowable transfer periods and the REQ/ACK offsets of the two devices participating in the synchronous data transfer. The transfer period is the minimum time allowed between leading edges of successive REQ pulses and of successive ACK pulses to meet the requirements for successful reception of data.

The REQ/ACK offset is the maximum number of REQ pulses allowed to be outstanding before the leading edge of its corresponding ACK pulse is received at the target. A REQ/ACK offset of zero indicates that the asynchronous data transfer agreement exists. A value of FF hex indicates unlimited REQ\ACK offset.

The device which first sends the SDTR message sets its REQ/ACK offset to a value which it can successfully receive data. If the responding device can also receive data with these values, it returns the same values in its SDTR message. If it requires a larger transfer period, a smaller REQ/ACK offset, or both, it substitutes values in its SDTR message as required, returning unchanged any value not required to be altered. The successful completion of a SDTR message exchange implies an agreement as follows:

Responding Device SDTR Message	Implied Agreement
1. Non-zero REQ/ACK offset	Each device transmits data with a transfer period equal to or greater than, and a REQ/ACK offset equal to or less than the values received in the other devices SDTR message.
2. REQ/ACK offset equal zero	Asynchronous Transfers
3. MESSAGE REJECT	Asynchronous Transfers

If the initiator recognizes that negotiation is required, it asserts the ATN signal and sends a SDTR message to initiate the negotiation process. After successfully completing the MESSAGE OUT phase, the target responds with the proper SDTR message. Following the targets response, the implied agreement for synchronous data transfers is considered to be negated by both the target and initiator if the initiator asserts ATN and the first message out is either a MESSAGE REJECT or MESSAGE PARITY ERROR. In this case, both devices revert to the asynchronous data transfer mode of operation.

SCSI COMMAND SPECIFICATION

This section defines the SCSI commands supported by the 2145. Each command is composed of a group of command bytes and optionally, a group of data bytes. The number of data bytes associated with any given command depends on the command executed and/or the transfer count specified within the command. After ARBITRATION, SELECTION, and any optional message transfer phases, the 2145 enters the COMMAND phase and requests that the initiator send the command data bytes. The opcode of the command determines the number of data bytes for the command. After receiving all the requested data bytes, the 2145 enters either the DATA IN, DATA OUT, or STATUS phase.

Upon the successful, or unsuccessful, completion of an operation, the 2145 returns a status byte to the initiator. The 2145 returns a status byte equal to either zero or two. A status return of zero indicates GOOD. A status byte returned equal to two indicates CHECK CONDITION.

Since most error conditions cannot be adequately described with a status return of just one status byte, a REQUEST SENSE operation is then used to retrieve additional information regarding the CHECK CONDITION.

Command Descriptor Block

A request to a device is made by transferring a command to the target device. This set of command bytes is referred to as the Command Descriptor Block (CDB).

The SCSI specification defines three basic command formats, the six-byte command, the ten-byte command and the twelve-byte command. The 2145 supports the six, ten and twelve byte commands. The SCSI specification refers to the six-byte commands as Group 0 commands ,the ten-byte commands as Group 1 commands and the twelve byte commands as Group 5 commands. The format of the command is recognized by its opcode. Six-byte commands have opcodes in the range of 00_H to $1F_H$; ten-byte commands have opcodes in the range of 20_H to $3F_H$; twelve-byte commands have opcodes in the range of $A0_H$ to BF_H. The format of the first byte of the Command Descriptor Block is shown in the table below.

TABLE 4 - First Byte in Command Description Block

Bit	7	6	5	4	3	2	1	0
	GROUP CODE			COMMAND CODE				

The following table shows a generic six-byte Command Descriptor Block.

TABLE 5 - Six Byte in Command Description Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPERATION CODE							
1	LOGICAL UNIT NUMBER			(MSB)				
2	LOGICAL UNIT ADDRESS (IF REQUIRED)							
3								
4	TRANSFER LENGTH							
5	CONTROL BYTE							

Logical Unit Number

The Logical Unit Number for the 2145 is zero. Logical Unit Numbers 1 through 7 are not accepted unless the command is preceded by a an IDENTIFY message in which the Logical Unit Number (LUN) is zero. In this case, the LUN specified in the command is ignored, and the LUN in the IDENTIFY message is used. If a LUN other than zero is specified in the Command Descriptor Block (CDB), and an IDENTIFY message with a LUN equal to zero is not issued, then the command is terminated with CHECK CONDITION and the sense key set to ILLEGAL REQUEST.

Logical Unit Address

This field is normally used for specifying the start block address for various operations. The 2145 does not use this field for most commands. Refer to the individual command descriptions for details on this field.

Transfer Length

This field is used to specify the number of bytes to be transferred to or from the 2145. For Group zero commands, the acceptable transfer lengths range from 00 to FF Hex. If a value of zero is specified, the number of bytes to be transferred is 256. See the allocation byte length for each command for further details.

For Group one commands, the acceptable transfer lengths range from 0000 to FFFF Hex. If a value of zero is specified, the number of bytes to be transferred is zero.

Reserved

These fields are reserved and must be set to zero.

Control Byte

The Control Byte is the last byte of any Command Descriptor Block. The following table shows the Control Byte.

TABLE 6 - Command Description Block Control Byte

Bit	7	6	5	4	3	2	1	0
	VENDOR UNIQUE		RESERVED				FLAG	LINK

Vendor Unique — This field is for a vendor unique code. For the 2145, no vendor unique codes are specified in this field. This field must be set to zero.

Reserved — This is a reserved field and must be set to zero.

Flag — This bit is not used by the 2145 and must be set to zero.

Link — This bit is set for using linked commands. Since the 2145 does not support linked commands, this bit must be set to zero.

Completion Status Byte

After the target has completed a command, it returns a status byte to reflect the status of the command. This byte is transferred during the Status phase of the operation. The 2145 returns either one of two status responses. A status return of GOOD status indicates that the command terminated successfully. A status return of CHECK CONDITION indicates that an error has occurred or some other unexpected event which requires servicing. After a CHECK CONDITION has been issued, the initiator should execute a REQUEST SENSE operation to obtain details concerning the CHECK CONDITION.

The following table shows the returned Status byte:

TABLE 7 - Status Byte

Bit	7	6	5	4	3	2	1	0
	RESERVED		STATUS BYTE CODE					RSVD

RESERVED — This field is reserved and returned as zero.

STATUS BYTE CODE — This field is used for specifying the status of the command. The following chart shows the status returns. The 2145 only returns the first two types of status.

RESERVED — This bit is reserved and returned as zero

TABLE 8 - Status Byte Bits

Bits of the Status Byte								
7	6	5	4	3	2	1	0	Status
R	R	0	0	0	0	0	R	GOOD
R	R	0	0	0	0	1	R	CHECK CONDITION
R	R	0	0	0	1	0	R	CONDITION MET
R	R	0	0	1	0	0	R	BUSY
R	R	0	1	0	0	0	R	INTERMEDIATE
R	R	0	1	0	1	0	R	INTERMEDIATE -- CONDITION MET
R	R	0	1	1	0	0	R	RESERVATION CONFLICT
R	R	1	0	0	0	1	R	COMMAND TERMINATED
R	R	1	0	1	0	0	R	QUEUE FULL
ALL OTHER CODES								RESERVED

GOOD — This status indicates that the target has successfully executed the command.

CHECK CONDITION — This status indicates that an error has occurred or an unexpected condition has occurred that requires service.

CONDITION MET — This status or INTERMEDIATE CONDITION MET is returned whenever a requested operation is satisfied. (i.e., SEARCH DATA or PRE-FETCH)

BUSY — This status indicates that the target is busy. This status is returned whenever a target is unable to accept a command from an otherwise acceptable initiator. It is recommended that when this status is received that the command be re-issued.

INTERMEDIATE — This status or INTERMEDIATE CONDITION MET is returned for every successfully completed command in a series of linked commands, unless the command is terminated with CHECK CONDITION, RESERVATION CONFLICT, or COMMAND TERMINATED status.

INTERMEDIATE CONDITION MET — This status is the combination of CONDITION MET and INTERMEDIATE.

RESERVATION CONFLICT — This status is returned whenever an initiator attempts to access logical unit or an extent within a logical unit that is reserved with a conflicting reservation type for another SCSI device.

COMMAND TERMINATED — This status is returned whenever the target terminates the current I/O process after receiving a TERMINATE I/O PROCESS message.

QUEUE FULL — This status is returned when a SIMPLE QUEUE TAG, ORDERED QUEUE TAG or TAG HEAD OF QUEUE message is received and the command queue is full.

COMMANDS SUPPORTED BY THE 2145

TABLE 9 - 2145 Commands

OPCODE	COMMAND
00 Hex	TEST UNIT READY
01 Hex	START TIMER
02 Hex	STOP TIMER
03 Hex	REQUEST SENSE
05 Hex	TIMER STATUS
06 Hex	UNBOOK LAM
08 Hex	READ BLOCK
0D Hex	REGISTER ACCESS
0E Hex	RESUME LIST
12 Hex	INQUIRY
1D Hex	SEND DIAGNOSTIC
21 Hex	SINGLE OPERATION
20 Hex	EXECUTE LIST
23 Hex	LOAD LIST
A2 Hex	BLOCK TRANSFER OPERATION

TEST UNIT READY Command

The TEST UNIT READY command is used to determine if the 2145 is capable of receiving and executing a CAMAC command. There is no data phase associated with this command. After the Command Descriptor Block is received, the 2145 enters the Status phase. The 2145 returns status of either CHECK CONDITION or GOOD. After the Status phase, the 2145 sends the Command Complete Message.

The Status byte returned depends on the state of the Serial Highway. If the Serial Highway clock makes a complete path from the serial highway transmitter card to the serial highway receiver card of the 2145, the highway is synchronized. If the highway is in synchronization, the status returned is GOOD. If the highway is not in synchronization, CHECK CONDITION status is returned. The following table shows the Command Descriptor Block for the TEST UNIT READY command.

TABLE 10 - Test Unit Ready Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 00 hex							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 0 to indicate a TEST UNIT READY command.

Byte 1: This byte contains a Logical Unit and Reserved field. These fields MUST be set to zero.

Byte 2: This is a Reserved byte and MUST be set to zero.

Byte 3: This is a Reserved byte and MUST be set to zero.

Byte 4: This is a Reserved byte and MUST be set to zero.

Byte 5: This is the Control byte and MUST be set to zero.

REQUEST SENSE Command

The following table shows the command descriptor block for the Request Sense operation.

TABLE 11 - Request Sense Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 03 hex							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	ALLOCATION LENGTH IN BYTES							
5	VU = 0		RESERVED = 0			F	L	

The Request Sense operation requests that the target return sense data to the initiator. This command is normally executed in response to a CHECK CONDITION status return from another SCSI command.

The sense data contains information regarding the previous command executed. This data is saved for the initiator until it is retrieved. Once the Request Sense is executed, the sense data is cleared (i.e., sense key, sense code,...). Table 11 shows the 6-byte Request Sense command.

Byte 0: This byte is set to 03 hex to indicate a Request Sense operation.

Byte 1: This byte contains the Logical Unit Number to be accessed and a reserved field. For the 2145 these fields MUST be set to zero.

Byte 2: This is a reserved byte and MUST be set to zero.

Byte 3: This is a reserved byte and MUST be set to zero.

Byte 4: This byte is used for specifying the maximum number of bytes that the initiator has allocated for returned sense data. This value can range from 0 to FF hex. If an allocation length of 0 is specified, the 2145 returns no data. The 2145 terminates the data transfer phase when the allocated number of sense bytes have been returned OR when all available sense bytes been returned, whichever is less. For most all cases, an allocation length of 18 bytes is sufficient.

Byte 5: This is the Control byte and MUST be set to zero.

The following table shows the 14 bytes of data returned from a Request Sense operation.

TABLE 12 - 14-Byte Request Sense

Bit Byte	7	6	5	4	3	2	1	0
0	VLD	ERROR CODE = 70 hex						
1	SEGMENT NUMBER							
2	FM	EOM	ILI	RSVD	SENSE KEY			
3	(MSB)	INFORMATION BYTE						
4	INFORMATION BYTE							
5	INFORMATION BYTE							
6	INFORMATION BYTE							(LSB)
7	ADDITIONAL SENSE LENGTH IN BYTES							
8	(MSB)	COMMAND SPECIFIC INFORMATION						
9	COMMAND SPECIFIC INFORMATION							
10	COMMAND SPECIFIC INFORMATION							
11	COMMAND SPECIFIC INFORMATION							
12	ADDITIONAL SENSE CODE							
13	ADDITIONAL SENSE CODE QUALIFIER							

Byte 0: This byte contains a "valid" bit and the error code. If the valid bit is returned as zero, the "information" bytes are not defined. The error code is set to 70 hex to indicate the returned data is for current errors not deferred errors. The 2145 always returns this byte set to 70 hex.

Byte 1: This byte is used for COPY and COMPARE SCSI commands. Since the 2145 does not implement these commands, this byte is returned as zero.

Byte 2: This byte contains the Sense Key and several bits used for sequential access devices. The 2145 uses only the Sense Key field. The remaining bits in this field are set to zero. The Sense Key is a general indicator for the cause of a CHECK CONDITION. Refer to the Sense Key and Codes section of this manual for further details.

Bytes 3 through Bytes 6 are Information bytes. These bytes are not used by the 2145 and are returned as zero.

Model 2145-Z1B

Byte 7: This byte contains the Additional Sense Byte Length. This byte specifies the number of additional bytes, from byte 7, that contain valid sense data. The 2145 sets this byte to 22 hex.

Bytes 8 through Bytes 11 are Command Specific Information Bytes. These bytes are not used by the 2145 and returned as zero.

Byte 12:

This byte contains the Sense Code. The Sense Code provides additional information regarding the cause of the CHECK CONDITION. The code is used in conjunction with the Sense Key to further define the error.

Byte 13:

This byte contains the Sense Code Qualifier. The Sense Code Qualifier provides additional information regarding the cause of the CHECK CONDITION. The qualifier is used in conjunction with the Sense Key and Sense Code to determine the exact cause of the CHECK CONDITION.

Bytes 14 through 85 are used by the KSC Software Driver for the 2145. Those bytes are described below:

BYTE		BYTE	
14	Reserved	50	STAWC BYTE 1
15	Reserved	51	STAWC BYTE 2
16	Reserved	52	STAWC BYTE 3
17	Reserved	53	STAWC BYTE 4
18	STAT BYTE 1	54	STAQXE BYTE 1
19	STAT BYTE 2	55	STAQXE BYTE 2
20	STAT BYTE 3	56	STAQXE BYTE 3
21	STAT BYTE 4	57	STAQXE BYTE 4
22	STACSR BYTE 1	58	WCERS BYTE 1
23	STACSR BYTE 2	59	WCERS BYTE 2
24	STACSR BYTE 3	60	WCERS BYTE 3
25	STACSR BYTE 4	61	WCERS BYTE 4
26	STAERS BYTE 1	62	WCCNT BYTE 1
27	STAERS BYTE 2	63	WCCNT BYTE 2
28	STAERS BYTE 3	64	WCCNT BYTE 3
29	STAERS BYTE 4	65	WCCNT BYTE 4
30	STACCS BYTE 1	66	WCLIS BYTE 1
31	STACCS BYTE 2	67	WCLIS BYTE 2
32	STACCS BYTE 3	68	WCLIS BYTE 3

BYTE		BYTE	
33	STACCS BYTE 4	69	WCLIS BYTE 4
34	STASUM BYTE 1	70	WCDAT BYTE 1
35	STASUM BYTE 2	71	WCDAT BYTE 2
36	STASUM BYTE 3	72	WCDAT BYTE 3
37	STASUM BYTE 4	73	WCDAT BYTE 4
38	STACNT BYTE 1	74	QXEERS BYTE 1
39	STACNT BYTE 2	75	QXEERS BYTE 2
40	STACNT BYTE 3	76	QXEERS BYTE 3
41	STACNT BYTE 4	77	QXEERS BYTE 4
42	STALIS BYTE 1	78	QXELIS BYTE 1
43	STALIS BYTE 2	79	QXELIS BYTE 2
44	STALIS BYTE 3	80	QXELIS BYTE 3
45	STALIS BYTE 4	81	QXELIS BYTE 4
46	STADAT BYTE 1	82	QXEDAT BYTE 1
47	STADAT BYTE 2	83	QXEDAT BYTE 2
48	STADAT BYTE 3	84	QXEDAT BYTE 3
49	STADAT BYTE 4	85	QXEDAT BYTE 4

For further description of these return parameters, please reference your KineticSystems' Software manual.

The following register is returned as part of the STACSR and STAESR return parameters.

Error/Status Register

The Error/Status Register (ESR) is a 32-bit read-only register that reflects the status of the serial highway interface and the list processing hardware. This data is returned during a Request Sense SCSI operation. Refer to the Request Sense section of this manual for additional information. The data from this register is also returned during timer initiated operations that have the Append Status option enabled. Refer to the Append Status section of this manual for details on enabling/disabling the Append Status option. The following shows the bit pattern for the Error/Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CM	TM1	TM0	CMD 1	CMD 0	WS2	WS1	AD	READ	NO HALT	0	0	EC3	EC2	EC1	EC0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	DERR	TMO	NO SYNC	ERR	N>23	LPE	TPE	ADNR	STE	NOX	NOQ

Bit 31 is updated from the command memory when the mode byte is read by the list processor. This value is 0 for CAMAC operations and 1 for non-CAMAC operations.

Bits 30 and 29 are updated from the command memory when a mode byte is read by the list processor. These bits reflect the selected Transfer Mode of the last executed by the list processor.

Bits 28 and 27 are updated from the command memory when a mode byte is read by the list processor. These bits reflect the selected Q-Mode of the last command executed by the list processor.

Bits 26 and 25 are updated from the command memory when a mode byte is read by the list processor. These bits reflect the selected CAMAC Data Word Size of the last command executed by the list processor.

Bit 24 is updated from the command memory when a mode byte is read by the list processor. This bit reflects the state of Abort Disable bit of the last command executed by the list processor.

Bit 23 is updated from by the list processor as the NAF entries from a list are updated by the list processor. If this bit is read as a 1, the last operation executed by the 2145 was a CAMAC read operation. If this bit is read as a 0, the last CAMAC operation was either a CAMAC write or control operation.

Bit 22 is updated by the list processor as the mode byte is read by the list processor. If the last mode byte read by the 2145 was not a HALT instruction, this bit is set.

Bits 21 and 20 are always read as zero.

Bits 19 through 16 are four bits which represent a prioritized error code. This code is updated as a result of a CAMAC operation and is also displayed on the front panel of the 2145. The following chart shows the errors defined for the indicated code. The highest priority error if 0E hex and the lowest in priority is 00.

Hex Code	Error Description
0F	NOT USED - This code will not be generated by the 2145.
0E	DIRECTION ERROR - The execution of a list operation was terminated due to a NAF in the command list that caused a mismatch between the direction of CAMAC operations and the direction specified in the SCSI Execute List command.

0D	NO SYNC - The serial highway is currently not in synchronization. This is most likely due to the loss of the serial highway clock input to the 2145.
0C	ADDRESS NOT RECOGNIZED - The 2145 executed a CAMAC operation that was not accepted by any serial crate controller.
0B	TIMEOUT - The 2145 initiated a serial highway command message and did not receive a reply message within a predefined timeout period.
0A	SERIAL TRANSMISSION ERROR - A serial transmission error occurred on the last CAMAC operation executed by the 2145. The serial transmission error is generated when either of the following bits in the Error/Status Register are set : LPE, TPE,ERR.
09	N GREATER THAN 23 - The 2145 executed a CAMAC Q-Scan operation that caused the CAMAC Station Number to increment to 24.
08	NO X - The 2145 executed an addressed CAMAC operation which resulted in a X-response of zero.
07	NO Q - The 2145 executed an addressed CAMAC operation which resulted in a Q-response of zero.
06	NOT USED - This code will not be generated by the 2145.
05	NOT USED - This code will not be generated by the 2145.
04	REPLY ERROR - The 2145 executed an addressed CAMAC operation which resulted in the ERR bit being set in the serial highway reply message. This indicated that either a NO-X condition occurred or that a parity error was detected by the serial crate controller.
03	NOT USED - This code will not be generated by the 2145.
02	NOT USED - This code will not be generated by the 2145.
01	NO HALT - The mode byte of the last operation executed by the 2145 was not a HALT instruction.
00	NO ERROR - This code is generated when none of the errors 01 through 0F are pending.

Bits 15 through 11 are not used and read as zeros.

Bit 10 is set when the last serial highway reply message received had the DELAYED ERROR (DERR) bit set. This indicates that the previous serial highway operation resulted in the ERR bit being set in its reply message.

Bit 9 is set when the 2145 initiates a serial highway command message and does not receive a reply message within a predefined timeout period.

Bit 8 is set when the 2145 loses highway synchronization. This is usually caused by a loss of the serial highway clock input to the 2145.

Bit 7 is set when the last serial highway command executed by the 2145 returned the ERR bit set in the reply message. This is set when a NO-x response is obtained or the serial crate controller detected a parity error in the command message.

Bit 6 is set when the 2145 executes a Q-Scan operation which results in the 2145 incrementing the CAMAC station number to 24.

Bit 5 is set when the 2145 detects a longitudinal parity error on an incoming reply message.

Bit 4 is set when the 2145 detects a transfers parity error on an incoming reply message.

Bit 3 is set when the 2145 executes a serial highway operation which is not accepted by any serial crate controller.

Bit 2 is a serial transmission error and is set when either of the following bits is set: LPE,TPE,ERR.

Bit 1 is set when the last CAMAC operation resulted with a X-response of zero.

Bit 0 is set when the last CAMAC operation resulted with a Q-response of zero.

Sense Keys and Codes

The following shows the Sense Key, Sense Code, and Sense Code Qualifiers generated by the 2145. All data values are in hex. All sense codes with the value 80 and 81 hex are vendor unique.

Sense Key	Sense Code	Sense Qualifier		Description
00	00	00	NO SENSE	This data is returned to indicate that there is no specific sense key information to be reported. This would be the case for a successful command.
02	04	03	NOT READY	This data is returned if whenever the 2145 cannot be accessed. Operator intervention is required to correct this condition. This key is generated if a TEST UNIT READY

				command is executed and the 2145 does not have highway sync.
04	42	XX	HARDWARE ERROR	This data is returned whenever the 2145 self-test fails. The self-test is entered on power-up or by a self-test request issued by the SEND DIAGNOSTIC command. XX is the code returned to specify the cause of the hardware error. Refer to the SEND DIAGNOSTIC SCSI command description for details regarding the error returns.
05	-	-	ILLEGAL REQUEST	This key is returned to indicate that there was an illegal parameter in the Command Descriptor Block or in the additional parameters supplied for some commands. If the 2145 detects an invalid parameter, it terminates the command without performing any operations.
05	00	00	BAD CONTROL FIELD	This code is returned when the 2145 receives a non-zero control byte in the Command Descriptor Block. This is KSC error code #802.
05	20	00	BAD COMMAND RECEIVED	This code is returned when the 2145 was instructed to execute a SCSI command that has not been implemented. This is KSC error code #831.
05	24	00	BAD RESERVED FIELD	This code is returned when a non-zero reserved field is encountered in the Command Descriptor Block. This is KSC error code #800.
05	24	05	BAD BIC	This code is returned when an invalid Buffer Interval Counter (BIC) value is specified for a START TIMER SCSI command. This is KSC ERROR #828.
05	24	06	BAD TRIGGER	This code is returned when an invalid trigger value was specified for a START

				TIMER SCSI command. This is KSC ERROR #829.
05	25	00	BAD LUN FIELD	This code is returned when a non-zero logical unit number (LUN) is found in the Command Descriptor Block. This is KSC error code #801.
05	80	00	BAD LIST OPCODE	This code is returned when the 2145 encounters a list processing instruction that the 2145 does not implement.
05	80	01	BAD CAMAC FUNCTION	This code is generated when the CAMAC function code does not match the SCSI command requested.
05	80	02	BAD CAMAC MODE	This code is generated when the CAMAC mode byte specifies an operation that the SCSI command does not support. For example, setting the "BLK" mode specifier and requesting a SINGLE SCSI command.
05	80	03	BAD WORD SIZE	This code is generated when the CAMAC mode byte contains an illegal word size.
05	80	04	BAD TIMING	This code is returned when a resume list command was issued, but could not be executed.
05	81	01	BAD LIST ADDRESS	This code is generated when a list processing command is executed with a list address outside the available range. This is KSC ERROR #825.
05	81	01	BAD LIST ADDRESS	This code is returned if the list address specification for a command list operation is out of the allowed range. This is KSC ERROR #825.
05	81	02	BAD REGISTER ACCESS	This code is returned on the read of a write-only register or a write of a read-only register during a REGISTER ACCESS SCSI command. This is KSC ERROR #826.

06	29	00	UNIT ATTENTION	This code is returned when a reset has occurred to the 2145. This reset is generated by a power-up, receiving a SCSI RESET message, or by receiving the assertion of the SCSI bus RESET signal.
09	80	03	N>23, SINGLE NAF	This code is generated when a SINGLE CAMAC operation is requested and the Q-SCAN operation caused the scan increment to station number 24. This code is KSC ERROR #311.
09	80	04	HARDWARE TIMEOUT, SINGLE NAF	This vendor unique code is generated when the 2145 hardware has timed-out trying to obtain a Q = 1 response during a Q-REPEAT operation. If a Q = 1 response is not obtained within the user selectable timeout period, the code is returned. This is KSC ERROR #213.
09	80	05	NO-X, SINGLE NAF	This vendor unique code is generated when a SINGLE CAMAC command resulted in a NO-X condition. This code is KSC ERROR #314.
09	80	06	NO-Q, SINGLE NAF	This vendor unique code is generated when a SINGLE CAMAC command resulted in a NO-Q condition. This code is KSC ERROR #312.
09	80	09	N>23, BLOCK NAF	This code is returned when a Block Transfer operation is requested and the Q-SCAN operation caused the scan to increment to station number 24. This is KSC ERROR #302.
09	80	0A	HARDWARE TIMEOUT, BLOCK NAF	This code is generated when the 2145 hardware has timed-out trying to obtain a Q = 1 response during a Q-REPEAT operation. If a Q = 1 response is not obtained within the user selectable timeout period, the code is returned. This is KSC ERROR #207.

09	80	0B	NO-X, BLOCK NAF	This code is generated when a Block Transfer operation resulted in a NO-X condition. This code is KSC ERROR #305.
09	80	0C	NO-Q, BLOCK NAF	This code is generated when a block transfer operation resulted in a NO-Q condition. This code is KSC ERROR #303.
09	80	10	BLOCK UNDEFINED ERROR	This code is generated when an undefined block transfer error has occurred. This is KSC ERROR code #309.
09	80	11	SINGLE UNDEFINED ERROR	This code is generated when an undefined single error has occurred. This is KSC ERROR #318.
09	81	02	NO HALT	This code is generated when a command list operation is terminated due to an error condition. This code is usually set when an invalid opcode is found in the command list. This is KSC ERROR #112.
09	81	03	REPLY ERROR	This code is generated when a serial highway reply message returned the ERR bit TRUE in the status byte, This indicates that a parity error occurred on the command message or a X-response of zero occurred. This is KSC ERROR #322.
09	81	04	BLOCK STE	This code is generated when a serial transmission error occurs during a block transfer operation. Refer to the Serial Highway Errors section of this manual for additional information. This is KSC ERROR #307.
09	81	05	BLOCK ADNR	This code is generated when a block transfer serial highway operation is executed to a non-existent crate address. This is KSC ERROR #324.
09	81	06	BLOCK NOSYNC	This code is returned when a CAMAC block transfer operation was requested and the serial highway has lost synchronization. This is KSC ERROR #304.

09	81	07	BLOCK DIR	This code is generated when a block transfer operation in a command list changed the direction of the transfers of the list. For example, the Command Descriptor Block specified a write command list and a block transfer read operation was found in the list. This is KSC ERROR #326.
09	81	09	SINGLE STE	This code is generated when a serial transmission error occurs during a single transfer operation. Refer to the Serial Highway Errors section of this manual for additional information. This is KSC ERROR #316.
09	81	0A	SINGLE ADNR	This code is generated when a single transfer serial highway operation is executed to a non-existent crate address. This is KSC ERROR #329.
09	81	0B	SINGLE NOSYNC	This code is returned when a CAMAC single transfer operation was requested and the serial highway has lost synchronization. This is KSC ERROR #313.
09	81	0C	SINGLE DIR	This code is generated when a single transfer operation in a command list changed the direction of the transfers of the list. For example, the Command Descriptor Block specified a write command list and a block transfer read operation was found in the list. This is KSC ERROR #331.
09	81	0E	BAD READ	This code is generated when a READ BLOCK SCSI command is executed and a timer initiated list is not being executed. This is KSC ERROR #820.
09	81	0F	BAD DISCONNECT	This code is generated when the 2145 was not able to disconnect from the SCSI in response to a READ BLOCK SCSI command with disconnect enabled. This is KSC ERROR #823.
09	81	10	BAD RECONNECT	This code is generated when the 2145 could not reconnect to the SCSI bus after a disconnection. This is KSC ERROR #824.

09	81	11	BAD START	This code is generated when a timer initiated list is currently being executed and a subsequent START TIMER SCSI command is received. This is KSC ERROR #821.
09	81	12	BAD TIME	This code is returned when a timer initiated operation ceases due to an error condition and a subsequent READ BLOCK SCSI command is executed to the 2145. This is KSC ERROR #832.
09	81	13	BAD STOP	This code is generated when a STOP TIMER SCSI command is executed and no timer initiated list is being executed. This is KSC ERROR #822.
OB	-	-	ABORTED COMMAND	This key is returned to indicate that the 2145 could not complete the requested operation due to either a CAMAC Abort condition or a SCSI error.
0B	47	00	SCSI PARITY ERROR	This data is returned when a SCSI parity error is detected.
0B	43	00	MESSAGE REJECT ERROR	This data is returned when the 2145 receives a message it does not implement.
0B	80	01	SINGLE ABORT	Single CAMAC Operation Aborted. This data is returned when a CAMAC operation terminates before the requested byte count is exhausted.
0B	80	02	BLOCK ABORT	Block CAMAC Operation Aborted. This vendor unique code is generated when a block transfer operation is terminated before the transfer count is exhausted.

INQUIRY Command

The INQUIRY command is used by an initiator to determine the peripherals attached to the SCSI bus. The following table shows the Command Descriptor Block for the INQUIRY command.

TABLE 13 - INQUIRY Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 12 hex							
1	LUN = 0			RESERVED = 0				EVPD
2	PAGE CODE							
3	RESERVED = 0							
4	ALLOCATION LENGTH IN BYTES							
5	CONTROL BYTE							

Byte 0: This byte is set to 12 hex to indicate an INQUIRY command.

Byte 1: This byte contains a Logical Unit and Reserved field, along with the Enable Vital Product Information (EVPD) bit. Since the 2145 does not support Vital Product Information or Logical Units, this byte MUST be set to zero.

Byte 2: This byte specifies which Page Code of the Vital Product Information is to be returned. Since the 2145 does not support it, this byte MUST be set to zero.

Byte 3: This is a Reserved byte and MUST be set to zero.

Byte 4: This byte specifies the maximum number of data bytes that the initiator has allocated for returned INQUIRY data. An allocation length of zero indicates that the 2145 should return no INQUIRY data. Any other value indicates the maximum number of bytes that shall be returned. The 2145 terminates the DATA IN phase when the allocation length of bytes is exhausted or when all available INQUIRY data has been sent to the initiator, whichever is less. For the 2145 an allocation length of 56 (38 hex) is suggested.

Byte 5: This is the Control byte and MUST be set to zero.

The INQUIRY command returns an 8-byte header followed by product specific information.

The following table shows the 8-byte header.

TABLE 14 - 8-Byte INQUIRY Header Return

Bit Byte	7	6	5	4	3	2	1	0
0	PERIPHERAL QUALIFIER			PERIPHERAL DEVICE TYPE				
1	RMB	RESERVED = 0						
2	ISO VERSION		ECMA VERSION			ANSI VERSION		
3	AENC	TRMIOP	RESERVED = 0			RESPONSE DATA FORMAT		
4	ADDITIONAL INQUIRY BYTE LENGTH							
5	RESERVED = 0							
6	RESERVED = 0							
7	RELADR	WBUS32	WBUS16	SYNC	LINK	RSVD	QUE	SRST

Byte 0: This byte contains the Peripheral Device Type and the Peripheral Qualifier. The 2145 returns this byte with the Peripheral Device Type set to 03 hex, indicating a processor device. The Peripheral Qualifier is returned as zero. If the INQUIRY command is performed to a Logical Unit other than zero, the Peripheral Qualifier returned is set to 03 hex. A return of 03 in this field indicates that the target is not capable of supporting a physical device on this logical unit.

Byte 1: This byte contains the Removable Medium Bit (RMB) and a Reserved field. Since the 2145 does not contain any removable media, this byte is returned as zero.

Byte 2: This byte contains information regarding the guidelines and specifications this product was designed under. The usage of the ISO version and ECMA version fields are defined by the International Organization for Standardization and the European Computer Manufacturers Association, respectively. A value of zero in these fields indicates that the target does not claim compliance with these standards. The ANSI (American National Standard Institute) version field indicates which version of the ANSI SCSI specification this device was implemented under. This field is set to 02 hex by the 2145 to indicate it was implemented under the SCSI-2 specifications. SCSI-2 is an extension to SCSI-1 (X3.131-1986) specification.

Byte 3: This byte contains the Asynchronous Event Notification Capability (AENC) bit, the Terminate I/O Process bit (TRMIOP), and the Response Data Format field. Since the 2145 supports Asynchronous Event Notification for CAMAC Serial Highway Demand Messages (generated by CAMAC Look-At-Me; LAM's) this bit is set to a one. The TRMIOP bit is set to zero indicating that the 2145 does not support the TERMINATE I/O PROCESS message. The Response Data Format field is set to 02 hex by the 2145 indicating that the returned INQUIRY data conforms to SCSI-2 specifications.

Byte 4: This byte specifies the additional length of INQUIRY data words in the parameter list. For the 2145 this value is 52 (34 hex). This value indicates the number of INQUIRY data bytes in the parameter list that are to follow byte four. Therefore,

after byte four is received, an additional 52 data bytes are available in the parameter list.

Byte 5: This byte is a Reserved byte and returned as zero.

Byte 6: This byte ia a Reserved byte and returned as zero.

Byte 7: This byte contains information regarding supported SCSI features on the target. This byte is returned as 0 hex by the 2145. The following describes each bit and the value that is returned by the 2145.

RELADR - The Relative Addressing bit is set to indicate that the target supports the Relative Addressing Mode for this Logical Unit. Since the 2145 does not support Relative Addressing, this bit is returned as zero.

WBUS32 - The Wide Bus 32 bit is set to indicate that the target supports 32-bit wide data transfers. Since the 2145 supports only 8-bit data transfers, this bit is returned as zero.

WBUS16 - The Wide Bus 16 bit is set to indicate that the target supports 16-bit wide data transfers. Since the 2145 supports only 8-bit data transfers, this bit is returned as zero.

SYNC - The Synchronous Transfer bit is set to indicate that the target supports the synchronous data transfers on the SCSI bus. Since the 2145 currently does not support synchronous data transfers, this bit is returned as zero.

LINK - The Linked bit is set to indicate that the target supports linked commands for this Logical Unit. Since the 2145 does not support linked commands, this bit is returned as zero.

RSVD - This is a Reserved bit and returned as zero.

QUE - The Command Queuing is set to indicate that the target supports tagged Command Queuing. Since the 2145 does not support Command Queuing, this bit is returned as zero.

SRST - The Soft Reset bit is set to indicate that the target responds to the RESET condition using the soft reset alternative. Since the 2145 uses the hard reset alternative, this bit is returned as zero.

Bytes 8 through 15 are allocated for the Vendor Identification field. This field contains eight bytes of ASCII data identifying the vendor of this product. Bytes 8 through 15 are shown below with the hex data returned and the corresponding ASCII character.

Byte	Hex data	ACSII character
8	4B	K
9	49	I
10	4E	N
11	53	S
12	59	Y
13	53	S
14	43	C
15	4F	O

Bytes 16 through 31 are allocated for the Product Identification field. This field contains 16 bytes of ASCII data identifying this product. Bytes 16 through 31 are shown below with the hex data returned and the corresponding ASCII character.

Byte	Hex data	ASCII character
16	32	2
17	31	1
18	34	4
19	35	5
20	2D	-
21	5A	Z
22	31	1
23	78	x
24	5F	
25	53	S
26	43	C
27	53	S
28	49	I
29	53	S
30	48	H
31	44	D

Bytes 32 through 35 are allocated for the Product Revision Level field. This field contains four bytes of ASCII data identifying the current revision level of the 2145 hardware. Bytes 32 through 35 are shown below with the hex data returned and the corresponding ASCII characters.

Byte	Hex data	ASCII character
32	31	1
33	2E	.
34	30	0
35	30	0

Bytes 36 through 49 reflect the 2145's current firmware revision level. Bytes 36 through 44 are shown below with the HEX data returned and the corresponding ASCII characters.

Byte	Hex data	ASCII character
36	46	F
37	49	I
38	52	R
39	4D	M
40	57	W
41	41	A
42	52	R
43	45	E
44	20	space

Bytes 45 through 49 reflect the current firmware revision number.
Bytes 50 through 55 are returned as 20 Hex, representing spaces.

SEND DIAGNOSTIC Command

The SEND DIAGNOSTIC command requests the target to perform diagnostic operations on itself, on the logical unit, or both. The 2145 only responds to this command if a request for a self-test is issued. There is no DATA phase associated with this command. After the 2145 receives the request for the self-test, the microprocessor exercises write/read tests to the internal registers. Once the self-test is complete, the 2145 enters the STATUS phase and returns the status byte. If the self-test completed successfully, a status of GOOD is returned. A status response of CHECK CONDITION is returned for a failure during the self-test. For self-test failures, the sense key is set to HARDWARE ERROR.

The following occurs during the self-test:

1. The 2145 issues an interface reset to itself to clear all internal registers.

2. The following registers are checked to verify a clear operation has occurred:

    a. Control/Status Register
    b. Error/Status Register
    c. Demand Register
    d. Timer Control Register

3. A data write/read test is performed to the following registers:

   a. Control/Status Register
   b. Timer Control Register
   c. Command Memory Address Register
   d. Command Memory Data
   e. SBIC Word Count Low
   f. SBIC Word Count Mid
   g. SBIC Word Count High

The following table shows the Command Descriptor Block for the SEND DIAGNOSTIC Command.

TABLE 15 - SEND DIAGNOSTIC Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 1D HEX							
1	LUN = 0			PF	RSVD	SLFTEST	DEVOFL	UNITOFL
2	RESERVED = 0							
3	PARAMETER LIST							
4	LENGTH							
5	CONTROL BYTE							

Byte 0: This byte is set to 1D Hex to indicate a SEND DIAGNOSTIC command.

Byte 1: This byte contains a Logical Unit field, a Reserved bit, and several other bits for SETUP Command.

SINGLE CAMAC OPERATION Command

The SINGLE CAMAC operation command is used for executing single CAMAC operations. The opcode for this command is 21 Hex. If a CAMAC control operation is specified in the CAMAC NAF, there is no data phase. If a CAMAC write or read operation is specified, data transfer will follow the Command phase. The number of bytes transferred during the data phase depends on the CAMAC data word size specification in the Mode Control byte of the CDB. 16-bit transfers require two bytes and 24-bit requires four bytes. Note: For 24-bit CAMAC data word sizes, a dummy byte is transferred over the SCSI bus to ensure longword alignment of data in the host computer.

After the CAMAC operation is executed by the 2145, a Status byte is sent. Either a GOOD status or CHECK CONDITION is returned. CHECK CONDITION is sent if the CAMAC operation was terminated due to an error. This error is dependent on such parameters as the CAMAC Q-response, CAMAC X-response, etc. Refer to the CAMAC Operating Modes section of this manual for further details.

Model 2145-Z1B

The following table shows the Command Descriptor Block for the Single CAMAC Operation command:

TABLE 16 - Single CAMAC Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 21 HEX							
1	LUN = 0			RESERVED = 0				
2	CRATE ADDRESS							
3	MODE CONTROL							
4	NAF HI							
5	NAF LO							
6	RESERVED = 0							
7	RESERVED = 0							
8	RESERVED = 0							
9	CONTROL BYTE							

Byte 0: This byte is set to 21 Hex to indicate a SINGLE operation.

Byte 1: This contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Byte 2: This byte is used for the serial crate address specification.

Byte 3: This byte is used to specify the Mode Control for the CAMAC operation.

Bytes 4 and Bytes 5:
These bytes are used to specify the CAMAC Station Number (N), Subaddress (A), and Function Code (F).

Bytes 6 through Byte 8:
These bytes are reserved and must be set to zero.

Byte 9: This is the Control Byte and must be set to zero.

BLOCK TRANSFER CAMAC OPERATION Command

The BLOCK Transfer CAMAC operation command is used for executing block transfer operations to the CAMAC Dataway. The opcode for this command is A2 Hex. After the 2145 receives the command descriptor block, the Data phase is entered. Data transfer direction depends on the CAMAC Function Code selected. Once data transfers begin, they continue until an error condition occurs or the Transfer Count has been exhausted.

After the Block Transfer operation has been completed by the 2145, a Status byte is sent. Either a GOOD or CHECK CONDITION status is returned. CHECK CONDITION is returned if the CAMAC Block Transfer operation was terminated due to an error. This error is dependent on such parameters as the CAMAC Q-response, X-response, etc. Refer to the CAMAC Operating Modes section of this manual for additional information.

The following table shows the command descriptor block for the BLOCK Transfer CAMAC Operation SCSI command:

TABLE 17 - BLOCK Transfer CAMAC Operation Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = A2 HEX							
1	LUN = 0			RESERVED = 0				
2	CRATE ADDRESS							
3	MODE CONTROL							
4	NAF HI							
5	NAF LO							
6	TRANSFER BYTE COUNT HI							
7	TRANSFER BYTE COUNT MID							
8	TRANSFER BYTE COUNT LO							
9	RESERVED = 0							
10	RESERVED = 0							
11	CONTROL BYTE							

Byte 0: This byte is set to A2 hex to indicate a BLOCK operation.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Byte 2: This byte is used for the serial crate address specification.

Byte 3: This byte is used to specify the Mode Control for the operation.

Bytes 4 and
Bytes 5:

These bytes are used to specify the CAMAC Station Number (N), Subaddress (A), and Function Code (F) to be used for the Block Transfer operation.

Bytes 6-8:

These bytes are used to specify the number of data bytes to be sent or received during a Block Transfer operation. Byte 5 is the most significant byte and byte 7 is the least significant byte. This data is loaded into the SCSI Bus Interface Controller (SBIC) for specifying the total number of data bytes to be transferred. The two's complement of this number is loaded into the 2145 internal byte count register which controls the number of CAMAC Dataway cycles executed.

For example, if a CAMAC Block Transfer of 260 16-Bit words was desired, byte 6 is set to zero, byte 7 is set 1, and byte 8 is set to 8. This would generate 520 byte transfers on the SCSI bus for the requested operation (260 X 2).

Byte 9 and
Byte 10:

This are Reserved bytes and MUST be set to zero.

Byte 11:This is the Control Byte and MUST be set to zero.

BOOK LAM Command

The BOOK LAM command is used to enable the generation of an Asynchronous Event Notification (AEN) when a serial highway Demand Message is generated by a serial crate controller requiring attention. This command enables the LAM MASK register in the specified crate controller for the specified LAM and specifies two CAMAC control NAFs that are executed on the occurrence of the LAM.

The BOOK LAM command has no data phase associated with it. All necessary information is contained in the Command Descriptor Block. After the 2145 receives this command, it enters the status phase. The 2145 returns status of either CHECK CONDITION or GOOD. After the status phase, the 2145 sends the Command Complete Message. The following table shows the Command Descriptor Block for the BOOK LAM command.

TABLE 18 - BOOK LAM Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = A0 HEX							
1	LUN = 0			RESERVED = 0				
2	CRATE ADDRESS							
3	LAM IDENTIFICATION							
4	LAM TYPE							
5	USER DEFINED FIELD 1							
6	USER DEFINED FIELD 2							
7	CLEAR COMMAND NAF HIGH							
8	CLEAR COMMAND NAF LOW							
9	DISABLE COMMAND NAF HIGH							
10	DISABLE COMMAND NAF LOW							
11	CONTROL BYTE							

Byte 0: This byte is set for A0 Hex to indicate a BOOK LAM command.

Byte 1: This byte contains a logical unit field and a reserved field.

Byte 2: This byte specifies the identification of the LAM to be booked. The identification refers to the station number from within the crate of the LAM to be booked. The identification number ranges from LAM 1 through LAM 24.

Byte 3: This byte specifies the type of LAM being booked. This can be either type 0 or 1. When a type 0 LAM occurs, both the CLEAR and DISABLE NAF specifications are executed. When a type 1 LAM occurs, only the CLEAR NAF specification is executed.

Byte 4 through 6:
These bytes are user-defined bytes. These information bytes are returned to the SCSI initiator during the Asynchronous Event Notification.

Bytes 7 and 8:
These bytes are used for specifying the CAMAC CLEAR NAF to be executed when the selected LAM occurs.

Bytes 9 and 10:
These bytes are used for specifying the CAMAC DISABLE NAF to be executed when the selected LAM occurs.

Byte 11:
This is the Control Byte and **MUST** be set to zero.

Please refer to the Asynchronous Event Notification section of this manual for further information.

UNBOOK LAM COMMAND

The UNBOOK LAM command is used to prevent a specific LAM from generating an Asynchronous Event Notification (AEN). After a LAM is booked using the BOOK LAM command, it may be disabled (unbooked) by using the UNBOOK LAM command. This command disables the LAM MASK register for the specified LAM in the corresponding crate.

The UNBOOK LAM command has no data phase associated with it. All necessary information is contained in the Command Descriptor Block. After the 2145 receives the command, it enters the status phase. The 2145 returns status of either CHECK CONDITION or GOOD. After the status phase completes, the Command Complete Message is sent. The following table shows the Command Descriptor Block for the UNBOOK LAM command.

TABLE 19 - Command Descriptor Block for UNBOOK LAM Command

BIT / BYTE	7	6	5	4	3	2	1	0
0	OPCODE = 06 Hex							
1	LUN = 0				RESERVED = 0			
2	CRATE ADDRESS							
3	LAM IDENTIFICATION							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 06 Hex to indicate an UNBOOK LAM command.

Byte 1: This byte contains a logical unit field and a reserved field. This byte **MUST** be set to zero.

Byte 2: This byte specifies the serial crate address for which the LAM is to be unbooked.

Byte 3: This byte specifies the identification of the LAM to be unbooked. The identification refers to the station number within the crate of the LAM to be unbooked. The identification numbers range from LAM1 through LAM24.

Byte 4: These are reserved bytes and **MUST** be set to zero.

Byte 5: This is the Control Byte and **MUST** be set to zero.

REGISTER ACCESS COMMAND

The Register Access Command is used for factory diagnostic purposes. This section is included only for completeness. The user should not use this command.

The REGISTER ACCESS command allows access to various registers on the 2145. The registers are accessed via the microprocessor. The microprocessors PROM and internal RAM cannot be accessed with this command. This command can be used to either write or read data to/from one of the internal registers. Each command transfers either one, two, or four bytes of data. The byte count depends on the register accessed and the access method. This command is used by the manufacturer for diagnostic purposes only. This command is normally not executed by the user. The command is shown here for completeness only.

After the 2145 receives the Command Descriptor Block, it obtains the address of the data to be accessed by reading Bytes 2 and 3 of the CDB. The 2145 then reads Byte 4 to determine the direction of the transfer. If Byte 4 is set to zero, the addressed register is written with the data obtained from the subsequent DATA OUT phase. If Byte 4 is set to one, the addressed register is read and the data is sent to the initiator with a subsequent DATA IN phase. After the DATA phase has been executed, the 2145 returns the Completion Status Byte followed by a COMMAND COMPLETE message. The following table shows the Command Descriptor Block for the REGISTER ACCESS Command:

TABLE 20 - REGISTER ACCESS Command

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 0D HEX							
1	LUN = 0			RESERVED = 0				
2	ADDRESS HIGH							
3	ADDRESS LOW							
4	RESERVED = 0							R/W
5	CONTROL BYTE							

Byte 0: This byte is set to 0D Hex to indicate a REGISTER ACCESS Command.
Byte 1: This byte contains a Logical Unit and Reserved field. This byte MUST be set to zero.
Byte 2: This byte is used for specifying the most significant eight address bits for the data access. This is used in conjunction with Byte 3 for determining the 16-bit address to be accessed.
Byte 3: This byte is used for specifying the least significant eight address bits for the data access. This is used in conjunction with Byte 2 for determining the 16-bit address to be accessed.
Byte 4: This byte contains a Reserved field and a READ/WRITE bit. The Reserved field MUST be set to zero. For reading a 2145 register, the R/W bit must be set to one. A zero indicates the register is to be written.
Byte 5: This is the Control Byte and MUST be set to zero.

Model 2145-Z1B

The following lists the 2145 internal registers, their addresses, the size of the register, and the supported access methods.

Address	Register	Size	Access
0000	Transfer Count Low	8-Bits	Write/Read
0002	Transfer Count Middle	8-Bits	Write/Read
0004	FIFO	8-Bits	Write/Read
0006	Command	8-Bits	Write/Read
0008	Status/Select	8-Bits	Write/Read
000A	Interrupt	8-Bits	Write/Read
000C	Sequence Step / Synchronous Transfer Period	8-Bits	Write/Read
000E	FIFO Flags / Synchronous Transfer Offset	8-Bits	Write/Read
0010	Configuration #1	8-Bits	Write/Read
0012	Clock Conversion	8-Bits	Write/Read
0014	Test	8-Bits	Write/Read
0016	Configuration #2	8-Bits	Write/Read
0018	Configuration #3	8-Bits	Write/Read
001A	Transfer Count High	8-Bits	Write/Read
001C	FIFO Bottom	8-Bits	Read
0080	Timer Control / SCSI ID / Strap Selections	16-Bits	Write/Read
0082	Control/Status	16-Bits	Write/Read
0084	Reserved		
0086	Buffer Interval Counter #1	32-Bits	Write/Read
008A	Buffer End Address / Counter #2	16-Bits	Write/Read
008C	LED Status	8-Bits	Write
0100	DMA Memory Address Low	32-Bits	Write
0104	Reset Interface	--	Write
0106	Buffer End Address #1 Low	32-Bits	Write
010A	Reset CAMAC W/R Data FIFO's	--	Write
010C	Reset Demand FIFO's	--	Write
010E	Execute List	--	Write
0180	Error/Status Register Low	32-Bits	Read
0184	Command Memory Data	32-Bits	Write/Read
0188	CAMAC Word Count	32-Bits	Read
018C	Reset Buffer Address #1	--	Write
018E	Reset Buffer Address #2	--	Write
0200	Command Memory Address	16-Bits	Write/Read
0202	Demand Message	16-Bits	Write/Read

When a 8-bit wide register is accessed, one byte is transferred over the SCSI bus. Similarly, 16-bit registers require two bytes and 32-bit register require 4 bytes. Care should be taken when accessing these registers as SCSI operation may be affected and cause the 2145 to enter an unrecoverable state. The unit may then require the power to be switched off and then on.

The registers located at addresses 0000 through 001C are located on the SCSI bus interface chip (SBIC). For a detailed description of these register, please refer an Emulex FAS236 data sheet/book.

Timer Control/SCSI ID/Strap Selection Register

The Timer Control/SCSI ID/Strap Selection Register (TSCS) contains 8 bits for controlling the timer initiated list executions, one bit reflecting the status of the CAMAC W/R data FIFO, and 7 bits reflecting user selectable parameters for SCSI operation. The following diagram shows the bit pattern for the TSCS register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SCSI ID 2	SCSI ID 1	SCSI ID 0	BYTE ORDR	CBL DLY	FAST SCSI	XTRA	RPY EF	TMR 7	TMR 6	TMR 5	TMR 4	TMR 3	TMR 2	TMR 1	TMR 0

Bit 7 through 0:
These write/read bits are used for selecting the various frequencies at which the timer initiated lists are executed.

Bit 8 is a read-only bit which is 0 when the CAMAC Reply FIFO is empty.

Bit 9 is a read-only bit which reflects the state of the XTRA strap.

Bit 10 is a read-only bit which reflects the state of the FAST SCSI switch.

Bit 11 is a read-only bit which reflects the state of the CABLE DELAY switch.

Bit 12 is a read-only bit which reflects the state of the BYTE ORDER strap.
(This strap is configured at the factory and should not be altered).

Bits 15 through 13 reflect the state of the SCSI ID2 through SCSI ID0 switches.

Timer Data

This byte of data is used to establish the rate at which the timer initiated list is executed. This rate is referred to as the tic rate. There are 153 rates available. The following timer rates are provided by the 2145.

Rates > 99.9999 K

Rate	Hex Data
500.000K	42
333.333K	46
250.000K	41
200.000K	45
166.666K	43
125.000K	02
120.000K	C0
100.000K	60

Model 2145-Z1B

100.00K > Rate > 9.999K

Rate	Hex Data
83.333K	06
62.500K	01
60.000K	C2
50.000K	05
41.666K	03
40.000K	C6
33.333K	66
30.000K	80
25.000K	04
24.000K	C5
20.833K	07
20.000K	65
16.666K	63
15.000K	82
12.500K	22
12.000K	C4
10.000K	50

10.000k > Rate > 999.999

Rate	Hex Data
8333.33	26
7500.00	81
6250.00	21
6000.00	85
5000.00	25
4166.66	23
4000.00	E6
3333.33	56
3000.00	84
2500.00	10
2400.00	E5
2083.33	27
2000.00	55
1666.66	53
1500.00	A2
1250.00	12
1200.00	D0
1000.00	54

1000 > Rate > 99.999

Rate	Hex Data
833.333	16
750.000	A1
625.000	11
600.000	A5
500.000	15
416.666	13
400.000	D6
333.333	76
300.000	90
250.000	14
240.000	D5
208.333	17
200.000	75
166.666	73
150.000	92
125.000	32
120.000	D4
100.000	48

100 > Rate > 9.999

Rate	Hex Data
83.333	36
75.000	91
62.500	31
60.000	95
50.000	35
41.666	33
40.000	F6
33.333	4E
30.000	94
25.000	08
24.000	F5
20.833	37
20.000	4D
16.666	4B
15.000	B2
12.500	0A
12.000	C8
10.000	4C

9.999 > Rate > .999

Rate	Hex Data
8.333	0E
7.500	B1
6.250	09
6.000	B5
5.000	0D
4.166	0B
4.000	CE
3.333	6E
3.000	88
2.500	0C
2.400	CD
2.083	0F
2.000	6D
1.666	6B
1.500	8A
1.250	2A
1.200	CC
1.000	58

Rate < 1.000

Rate	Hex Data
.833333	6F
.750000	89
.625000	29
.600000	8D
.500000	2E
.416666	2B
.400000	EE
.333333	5E
.300000	8C
.250000	18
.240000	ED
.208333	2F
.200000	5D
.166666	5B
.150000	AA

.125000	1A
.120000	D8
.100000	5C
.083333	1E
.075000	A9
.060000	AD
.062500	19
.050000	1D
.041666	1B
.040000	DE
.033333	7E
.030000	98
.025000	1C
.024000	DD
.020833	1F
.020000	7D
.016666	7B
.015000	9A
.012500	3A
.012000	DC
.010000	7C
.008333	3E
.007500	99
.006250	39
.006000	9D
.005000	3D
.004166	3B
.004000	FE
.003000	9C
.002500	3C
.002400	FD
.002083	3F
.002000	FB
.001500	BA
.001200	FC
.001000	BE
.000750	B9
.000600	BD
.000500	BB
.000300	BC
.000250	BF

Control/Status Register

The Control/Status Register (CSR) is a write/read register used to monitor and control the internal circuitry of the 2145. Four bits are used to setup and enable the timer initiated lists, 5 bits reflect the status of the 2145 serial interface hardware, and 6 bits are used to control the SCSI DMA hardware. The following diagram shows the bit pattern for the Control/Status Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	SBIC DMA DIR	SBIC DMA ENA	BUF ENA	BUF SEL	DMA DIR	DMA ENA	DMD	DMD OVF	DONE	ERROR	ABT	APND ST	AUTO SCAN	TRG 1	TRG 0

Bits 0 and 1 are used to configure the timer initiated trigger sequence.

Bit 2 is used to enable/disable the timer initiated list execution.

Bit 3 is used to enable/disable the append status option during list operation.

Bit 4 is a read-only bit which is set when a CAMAC operation terminates with an abort condition.

Bit 5 is a read-only bit which is set when a CAMAC error occurs.

Bit 6 is a read-only bit which is set when the CAMAC hardware is idle.

Bit 7 is a read-only bit which is set whenever the Demand FIFO is full and a subsequent demand message is received.

Bit 8 is a read-only bit which is set as long as the Demand FIFO is not empty.

Bits 9 and 10 are used to control the SCSI DMA circuitry used in conjunction with the normal single and block transfer commands which do not use the automatic trigger features of the 2145.

Bits 11 and 12 are used to control the SCSI DMA circuitry used in conjunction with the automatic trigger features of the 2145.

Bits 13 and 14 are used to control the SCSI DMA circuitry used for sending and receiving non-CAMAC related data over the SCSI bus.

Bit 15 is not used and read as a zero.

Buffer Interval Counter

The Buffer Interval Counter is a 32-bit write/read register which is used when the 2145 is in the timer initiated mode of operation. This counter, which is loaded by the 2145 microprocessor prior to a timed list execution, is loaded with the number of 32 bit words that are to be collected by the 2145's buffer before the host is notified that a buffer full condition occurred.

Buffer End Address/Counter #2

The Buffer End Address/Counter #2 (BEAC2) is a 16-bit write/read register which is used by the 2145 during timer initiated modes of operation. This counter is used as a secondary buffer address pointer/counter. If a timed list is being executed by the 2145, a SCSI request may be made to execute a CAMAC operation in between tics of the internal timer. When this occurs, BEAC2 is used to hold the buffer address.

LED Register

The LED Register is an 8-bit write-only register used for diagnostic purposes. Data written to this register is displayed on the 8 LED's located on the D170 board of the 2145.

DMA Memory Address Register

The DMA Memory Address Register (DMAR) is a 32-bit write-only register. This register/counter is used for specifying the start address for DMA operations from the 2145's buffer memory to the SCSI bus.

Reset Interface

This byte wide register is used to reset the internal circuitry of the 2145. Writing to this register with any data pattern causes the 2145 to reset.

Buffer End Address

The Buffer End Address Register (BEAR) is a 32-bit write-only register which specifies the ending address of the circular buffer used for storing CAMAC read data during timer initiated list execution.

Reset CAMAC Write/Read FIFO

This byte wide register is used to reset the CAMAC Write/Read Data FIFOs in the 2145. Writing to this register with any data pattern causes the FIFOs to be cleared.

Reset Demand FIFO

This byte wide register is used to reset the Demand FIFO in the 2145. Writing to this register with any data pattern causes the Demand FIFO to be cleared.

Execute List

This byte wide register is used to start list execution once a list has been downloaded to the 2145.

Command Memory Data

The Command Memory Data register (CMDR) is a 32-bit write/read register used to hold the command list. This register is actually a port to the 8K X 32 Command Memory. The data that is accessed through this port is pointed to by the Command Memory Address Register. After a write or read to this register, the Command Memory Address Register is automatically incremented.

CAMAC Word Count Register

The CAMAC Word Count Register (WCR) is a 32-bit read-only register which is used for CAMAC block transfer operations. This register is loaded by the 2145 list processor with the word count specification in a list. This value is the two's complement of the maximum number of 16-bit transfers that are to occur during the block transfer operation. After a block transfer operation has executed to completion, the CAMAC WCR contains the value zero. If the block

transfer terminates prematurely, the CAMAC WCR contains the number of 16-bit words not transferred.

Reset Buffer Address Register #1

This byte wide write-only register is used to clear the first Buffer Address Register. Writing to this register with any data pattern causes the register to be reset. This register is used for determining the start address for the buffer into which CAMAC read data words are stored.

Reset Buffer Address Register #2

This byte wide write-only register is used to clear the secondary Buffer Address Register. Writing to this register with any data pattern causes the register to be reset. This register is used as a secondary buffer address.

Command Memory Address Register

The Command Memory Address Register (CMAR) is used for specifying the start address at which Command Memory write and read operations are to occur. After a write or read operation to the Command Memory, the CMAR is automatically incremented. This register is also used for specifying the starting address at which list processing operations are to occur.

Demand Message Register

The Demand Message Register (DMR) is a 512 X 16 FIFO for holding demand messages obtained from the serial highway. The DMR is a 16-bit read-only register. The following shows the bit pattern for the DMR.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	SGL 16	SGL 8	SGL 4	SGL 2	SGL 1	0	0	C32	C16	C8	C4	C2	C1

Bits 14 through 13 are not used and read as zeros.

Bits 12 through 8 are the serial graded LAM encoded bits which provide additional information regarding the demand source within a CAMAC crate.

Bits 7 and 6 are not used and read as zeros.
Bits 5 through 0 indicate which serial highway crate generated the demand message.

LOAD LIST Command

The LOAD LIST command is used for loading the Command Memory within the 2145. The Command Memory is a 8K X 32 static RAM. The address range for this memory is from 0 to 1FFF hex. The memory is used for storing the list(s) to be executed. Refer to the List Processing section of this manual for further details.

The following table shows the Command Descriptor Block for the LOAD LIST command.

TABLE 21 - LOAD LIST Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 23 HEX							
1	LUN = 0			RESERVED = 0				
2	LIST ADDRESS HI							
3	LIST ADDRESS LO							
4	TRANSFER BYTE COUNT HI							
5	TRANSFER BYTE COUNT MID							
6	TRANSFER BYTE COUNT LO							
7	RESERVED							
8	RESERVED							
9	CONTROL BYTE							

Byte 0: This byte is set to 23 hex to indicate a LOAD LIST command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes 2 and Bytes 3:
These bytes specify the starting address for the list load operation. The allowable range for this address is from 0 to 1FFF hex. Byte 2 is the most significant address byte and byte 3 is the least significant.

Bytes 4-6:
These bytes are used to specify the total number of bytes to be sent to the 2145 during the LOAD LIST operation. Byte 4 is the most significant byte and byte 6 is the least significant. The maximum number of transfers is FFFF hex. For example, if it was desired to transfer 576 bytes to the 2145, byte 4 is set to zero, byte 5 is set to 1 and byte 6 is set to 40 hex.

Bytes 7 and Bytes 8:
These are reserved bytes and MUST be set to zero.

Byte 9: This is the Control Byte and MUST be set to zero.

EXECUTE LIST Command

The EXECUTE LIST command is used for initiating the execution of a previously loaded list. The opcode for this command is 20 hex. This command instructs the 2145 to execute the list at the specified starting address. The command also includes the transfer count specification which determines the total number of bytes to be transferred for the entire list. Individual

Block Transfers within the list have their own transfer count specification embedded in the list. Refer to the List Processing section of this manual for further details.

The following table shows the Command Descriptor Block for the EXECUTE LIST command:

TABLE 22 - EXECUTE LIST Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 20 HEX							
1	LUN = 0			RESERVED = 0				
2	LIST ADDRESS HI							
3	LIST ADDRESS LO							
4	TRANSFER BYTE COUNT HI							
5	TRANSFER BYTE COUNT MID							
6	TRANSFER BYTE COUNT LO							
7	RESERVED = 0							R/W
8	RESERVED = 0							
9	CONTROL BYTE							

Byte 0: This byte is set to 20 hex to indicate an EXECUTE LIST command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes 2 and Bytes 3:

These bytes specify the starting address for the execute list operation. The allowable range for this address is from 0 to 1FFF hex. Any specification outside this range results in a CHECK CONDITION with the Sense Key set to Illegal Request, the Sense Code set to 81 hex, and the Sense Code Qualifier set to 01. Byte 2 is the most significant address byte and byte 3 is the least significant.

Bytes 4-6:

These bytes specify the total number of bytes to be transferred to or from the 2145 during list execution. This number is the total transfer length and includes any single transfer and block transfer specifications in the list. Byte 4 is the most significant byte and byte 6 is the least significant. For example, if the list entries require 1056 bytes to be transferred, byte 4 is set to zero, byte 5 is set to 2, and byte 6 is set to 20 hex.

Byte 7: This byte contains a reserved field and a READ/WRITE bit. The reserved field must be set to zero. The READ/WRITE bit must be set to reflect the direction of the SCSI data transfers during the list operation. If the list requires data from the SCSI bus to be used in CAMAC write operations, the R/W bit is set to zero. If the list executes CAMAC read operations, the R/W bit must be set to one.

Byte 8: This byte is reserved and must be set to zero.

Byte 9: This is the Control Byte and MUST be set to zero.

RESUME LIST Command

The RESUME LIST command is used to resume list execution after an error termination. The 2145 uses the last internal list address for the continuation. The word count specification is already stored in the 2145. Refer to the List Processing section of this manual for further details.

The opcode for this command is 0E hex. The following table shows the Command Descriptor Block for the RESUME LIST command.

TABLE 23 - RESUME LIST Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 0E HEX							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 0E hex to indicate a RESUME LIST command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes
2-4: These bytes are reserved and MUST be set to zero.

Byte 5: This is the Control Byte and MUST be set to zero.

START TIMER Command

The START TIMER SCSI command is used to start a previously downloaded command list using the automatic timer initiated execution. After the 2145 accepts the Command Descriptor Block (CDB), it switches to the data phase and retrieves 12 bytes from the initiator. These 12

bytes contain parameters used during the list initiated transfers. Please refer to the Timer Initiated List Execution section of this manual for further information.
After the 2145 receives the timer data, it sw itches to the status phase. If the 2145 is in the process of executing a timer initiated list operation, the status byte is set to CHECK CONDITION, and the Request Sense Key is set to 9, Sense Code is set to 81 hex and the Sense Qualifier is set to 11 hex. If the 2145 is not executing a list operation, a status of GOOD is returned.

The opcode for this command is 01. The following table shows the Command Descriptor Block for the START TIMER command

TABLE 24 - START TIMER Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 01 HEX							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 01 to indicate a START TIMER command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes
2-4: These bytes are reserved and MUST be set to zero.

Byte 5: This is the Control Byte and MUST be set to zero.

The following chart shows the 12 data bytes sent from the initiator to the 2145 during the data phase:

Byte 0: Timer Data
Byte 1: Buffer Interval Count Low
Byte 2: Buffer Interval Count Middle
Byte 3: Buffer Interval Count High
Byte 4: Buffer Ending Address Low
Byte 5: Buffer Ending Address Middle
Byte 6: Buffer Ending Address High
Byte 7: Trigger Mode / Append Status
Byte 8: Reserved
Byte 9: Automatic Scan
Byte 10: Command Memory Address Low
Byte 11: Command Memory Address High

Timer Data

Refer to page 52 for the various timer frequencies.

Buffer Interval Counter

The Buffer Interval Counter (BIC) , which is a 22-bit value, is specified in bytes 1 through 3. This value is used to indicate when the 2145 is to send CAMAC data back to the initiator. The value specified is the number of 32-bit words that are written into the CAMAC read data FIFO before the 2145 sets the internal Buffer Full flag. This flag, when set, allows the host computer to read data acquired during timer initiated transfers from the 2145. Refer to the Timer Initiated List Execution section of this manual for additional information.

7	6	5	4	3	2	1	0	
BIC7	BIC6	BIC5	BIC4	BIC3	BIC2	BIC1	BIC0	Byte 1
BIC15	BIC14	BIC13	BIC12	BIC11	BIC10	BIC9	BIC8	Byte 2
0	0	BIC21	BIC20	BIC19	BIC18	BIC17	BIC16	Byte 3

Buffer Ending Address

The Buffer Ending Address (BEA) is a 22-bit value which specifies the size of the buffer to be used during timer initiated list executions. This value represents the last physical address of the buffer to be written by the CAMAC read circuitry before the buffer address is reset. The address parameter specifies the number of 32-bit entries into the buffer before rollover occurs.

7	6	5	4	3	2	1	0	
BEA7	BEA6	BEA5	BEA4	BEA3	BEA2	BEA1	BEA0	Byte 4
BEA15	BEA14	BEA13	BEA12	BEA11	BEA10	BEA9	BEA8	Byte 5
0	0	BEA21	BEA20	BEA19	BEA18	BEA17	BEA16	Byte 6

Trigger Mode/Append Status

The Trigger Mode/Append Status byte is used for specifying the triggering mechanism for the timer initiated list. Within this byte is also a bit which enables or disables the Append Status option.

7	6	5	4	3	2	1	0	
0	0	0	APD	0	0	TRIG1	TRIG0	Byte 7

The APD bit is used to enable/disable the Append Status option. Setting this bit to a 1 enables append status and a 0 disables. When Append Status is enabled, the 2145's Error/Status Register contents are appended to the end of each list execution. The following diagram shows the bytes returned for the appended status. For a description of each bit, please refer to the Error/Status Register description in this manual.

7	6	5	4	3	2	1	0
CM	TM1	TM0	QM1	QM0	WS2	WS1	AD
READ	NOHLT	0	0	EC3	EC2	EC1	EC0
0	0	0	0	0	DERR	TMO	NOSYN
ERR	N>23	LPE	TPE	ADNR	STE	NOX	NOQ

The TRIG1 and TRIG0 bits are used to specify the triggering mechanism for initiating the list execution using the timer. The binary combination of these bits determine the source of the trigger for list execution. The following chart shows the various options.

TRIG1	TRIG0	Trigger Source
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	Execution of the list commences on the next internal tic of the timer. The rate at which each list iteration occurs is based on the timer data byte.

The Reserved byte is reserved for future enhancements. This byte must be set to a zero.

The Automatic Scan byte must be set to 1 to enable the 2145 to execute timer initiated lists.

The Command Memory Address Low and High byte are set to the initial address of the Command Memory at which list processing operations are to begin. As soon as the initial tic of the timer occurs, the list processing mechanism starts execution at this specified address. As subsequent tics of the timer occur, the 2145 internal command address register is reloaded with this address, and list processing continues.

TIMER STATUS Command

The TIMER STATUS command is used to check the 2145 to see if the block of data acquired during timer initiated list operation is ready to be transferred to the initiator. This command can also be used to verify if the 2145 is currently executing timer initiated operations.

After the 2145 receives the Command Descriptor Block, it changes to the SCSI data phase and returns one byte of data to the initiator. After the byte is returned, the status phase is entered and a GOOD status returned. Once the status is returned, the 2145 issues the COMMAND COMPLETE message.

The opcode for this command is 05. The following table shows the Command Descriptor Block for the TIMER STATUS command

TABLE 25 - TIMER STATUS Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 05 HEX							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 05 to indicate a TIMER STATUS command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes
2-4: These bytes are reserved and MUST be set to zero.

Byte 5: This is the Control Byte and MUST be set to zero.

The 2145 returns one byte of data for this command. The following shows the bit pattern for this byte.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	BSY	RDY

Bits 7 through 2 are not used and read as zeros.

Bit 0 is the READY bit and is used to indicate whether the 2145 is ready to transfer a block of read data acquired during timer initiated list operations. If the 2145 has a buffer full of data to return, this bit is set to a 1; or else it is set to 0 indicating it does not have a buffer full.

Bit 1 is the BUSY bit and indicates whether the 2145 i executing timer initiated list operations. When the bit is returned as a 1, the 2145 is BUSY executing list operations; or else it is returned as a 0.

STOP TIMER Command

The STOP TIMER command is used to stop execution of a currently executing timer initiated list operations which were started using the START TIMER command. After the 2145 receives this command, it checks to see if a timer initiated list operation is executing. If no timer operations are executing, the 2145 switches to the status phase and returns a CHECK CONDITION. If a timer initiated list operation is running, the 2145 stops the operations, switches to the status phase, and then returns a status of GOOD. After the status phase is complete, a COMMAND COMPLETE message is then sent.

The opcode for this command is 02. The following table shows the Command Descriptor Block for the STOP TIMER command

TABLE 26 - STOP TIMER Command Descriptor Block

Bit Byte	7	6	5	4	3	2	1	0
0	OPCODE = 02 HEX							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							
5	CONTROL BYTE							

Byte 0: This byte is set to 02 to indicate a STOP TIMER command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes
2-4: These bytes are reserved and MUST be set to zero.

Byte 5: This is the Control Byte and MUST be set to zero.

READ BLOCK Command

The READ BLOCK command is used to retrieve CAMAC read data obtained by the 2145 during timer initiated list operations. A bit located in byte 4 of the Command Descriptor Block (CDB) provides a mechanism for the 2145 to disconnect from the SCSI bus until CAMAC read data is available. Once read data is available, the 2145 reconnects to the initiator and transfers the required data. This SCSI command does not supply the transfer count of the number of bytes to be returned during the Read Block operation. The amount of data returned depends upon the parameters supplied during the START TIMER command. The number of data bytes returned is the Buffer Interval Counter value passed in the START TIMER command times 4. For example, if the Buffer Interval Counter was set to 1000, the READ BLOCK command will return 4000 bytes when the data is ready. Please refer to the Timer Initiated List Execution section of this manual for additional details.

After the 2145 receives the CDB, it checks to see if an ABORT condition has occurred during execution of the list. If an error has occurred, the 2145 enters the status phase and returns a CHECK CONDITION. If no error occurred, the requested data is transferred to the initiator. After all data is transferred, the status phase is entered and a status byte of GOOD is returned. After the status byte is sent, the 2145 returns the COMMAND COMPLETE message. Please refer to the Timer Initiated List Operations section of this manual for additional details.

The opcode for this command is 08. The following table shows the Command Descriptor Block for the READ BLOCK command.

TABLE 27 - READ BLOCK Command Descriptor Block

Bit / Byte	7	6	5	4	3	2	1	0
0	OPCODE = 08 HEX							
1	LUN = 0			RESERVED = 0				
2	RESERVED = 0							
3	RESERVED = 0							
4	RESERVED = 0							DCN
5	CONTROL BYTE							

Byte 0: This byte is set to 08 to indicate a READ BLOCK command.

Byte 1: This byte contains a Logical Unit field and a reserved field. This byte MUST be set to zero.

Bytes 2-3: These bytes are reserved and MUST be set to zero.

Byte 4: This byte contains a reserved field and the DISCONNECT bit. If this bit is set to a one, the 2145 will disconnect from the SCSI bus if the 2145 is not ready to transfer a block of data. After the data becomes available, the 2145 reconnects to the initiator and transfers the data. If this bit is set to 0, the 2145 does not disconnect from the bus until all requested data has been transferred.

Byte 5: This is the Control Byte and MUST be set to zero.

CAMAC Operating Modes

The 2145 may execute CAMAC operations in either Single Transfer or Block Transfer fashion. During Single Transfer operations, only one CAMAC data word is transferred for each SCSI command executed. During Block Transfer operations, multiple CAMAC data words are transferred for each SCSI command executed.

Single Transfer operations are executed using the SINGLE SCSI command. Block Transfer operations are to be executed using the BLOCK SCSI command.

CAMAC NAF Specifications

Before any addressed CAMAC operation is executed, the CAMAC Station Number (N), Subaddress (A) and Function Code (F) must be specified. This specification is split into two bytes. The following table shows the bits defined in each of the NAF bytes. The bytes are sent to the 2145 in the order shown.

TABLE 28 - NAF High Byte

7	6	5	4	3	2	1	0
0	0	N 16	N 8	N 4	N 2	N 1	A 8

TABLE 29 - NAF Low Byte

7	6	5	4	3	2	1	0
A 4	A 2	A 1	F 16	F 8	F 4	F 2	F 1

The CAMAC Station Number bits, N16 through N1, are used for specifying the CAMAC Station Number to be used during the addressed CAMAC operations. These 5 bits yield a Station Number range from 0 to 31. Station Numbers 0, 24 through 29, and 31 are not used. Station Number 30 is a pseudo-address and is used to address the internal registers of the serial crate controller.

The CAMAC Subaddress bits, A8 through A1, are used to specify the CAMAC Subaddress to be used during an addressed CAMAC operation. These 4 bits yield a subaddress range from 0 to 15.

The CAMAC Function Code bits, F16 through F1, are used to specify the CAMAC Function Code to be used during an addressed CAMAC operation. These 5 bits yield a Function Code range from 0 to 31. The binary combination of the F16 and F8 bits determine the type of CAMAC operation to be performed as shown below:

F16	F8	Operation
0	0	CAMAC READ
0	1	CAMAC CONTROL
1	0	CAMAC WRITE
1	1	CAMAC CONTROL

The NAF specification for the SCSI commands that execute CAMAC operations is found in bytes 5 and 6 of the Command Descriptor Block (CDB). The NAF High is byte 5 and the NAF Low is byte 6. Refer to the individual SCSI Command Descriptions for additional information.

Executing Single Transfer Operations

Single Transfer CAMAC operations are executed using the SINGLE SCSI command. The Mode Control byte of the Command Descriptor Block (CDB) for the SINGLE SCSI command has the following table.

TABLE 30 - SINGLE SCSI Command Mode Control Byte

7	6	5	4	3	2	1	0
0	0	0	QM1	QM0	WS2	WS1	AD

Bits 7 through 6 must be set to zero. These bits are used to define Block Transfer operations. If these bits are non-zero, the operation terminates with a CHECK CONDITION.

BitS 4 and 3 are used to select the desired Q-Mode. The following chart shows the various modes obtained from the binary combination of the Q-Mode bits.

QM1	QM0	Q-Mode
0	0	Q-Stop
0	1	Q-Ignore
1	0	Q-Repeat
1	1	Q-Scan

The Q-Stop mode is selected by setting both QM1 and QM0 to zero. The Q-Ignore mode is selected by setting the QM1 bit to zero and the QM0 bit to one. The difference between these two modes is the Status byte returned after the operation completes. If the Q-Ignore mode was selected, the Q-response is ignored in the generation of the status response. If the Q-Stop mode was selected, and the CAMAC operation resulted in a Q-response of zero, the 2145 returns a Status byte set to CHECK CONDITION. Conversely, if the operation resulted in a Q-response of one, the Status byte returned is set to GOOD. After the Status byte is sent, the 2145 then sends the COMMAND COMPLETE message.

The Q-Repeat mode is selected by setting the QM1 bit to one and the QM0 bit to zero. During Q-Repeat operations the CAMAC command is repeated until a Q-Response of one is received or until a Q-Repeat timeout occurs. Refer to the Q-Repeat Timeout section of this manual for additional details. Once a Q-response of one is obtained, the operation completes and the 2145 returns a Status byte set to GOOD. If a Q-Repeat timeout causes the operation to terminate,

a CHECK CONDITION is returned. After the Status byte is sent, the 2145 then sends the COMMAND COMPLETE message.

The Q-Scan mode of operation is selected by setting both QM1 and QM0 to one. During Q-Scan operations, the 2145 uses the Q-response from obtained from the first CAMAC command executed to determine the Station Number (N) and Subaddress (A) for the next operation. When a SINGLE SCSI command is initiated in the Q-Scan mode, the NAF specification in the SINGLE Command Descriptor Block is executed. If a Q-response of one is obtained, the operation completes with the 2145 returning a Status byte set to GOOD. If a Q-response of zero is received, the 2145 updates the NAF by resetting the Subaddress (A) and incrementing the Station Number (N). If the Station Number is incremented to N=24, the 2145 terminates the transfer and returns CHECK CONDITION. After the Station Number is incremented, another CAMAC operation is executed with the updated NAF. This sequence repeats until a Q-response of one is obtained or a N greater than 23 error occurs. Once a Q-response of one is obtained, the 2145 sends the Status byte set to GOOD. After the Status byte is sent, the 2145 then sends the COMMAND COMPLETE message.

Bits 2 and 1 are set to the desired CAMAC Data Word Size. If the CAMAC function code specified in the CDB is a CAMAC control function, these bits are ignored. The following chart shows the CAMAC data word sizes obtained for the various binary combinations of these bits:

WS2	WS1	CAMAC Data Word Size
0	0	24-Bit
0	1	16-Bit
1	0	Reserved
1	1	Reserved

Please refer to the Data Transfer Formats section of this manual for additional information regarding the data transfers.

Bit 0 is used to enable/disable the generation of CHECK CONDITION based on the CAMAC X-Response. This option has no effect during Q-Scan modes of operation. An X-response of zero during Q-Scan operations is not necessarily an error condition. If the AD bit is set to a zero, a CAMAC X-response of zero causes a status response of CHECK CONDITION. If this bit is set to a one, a CHECK CONDITION status is not returned due to a CAMAC X-Response of zero.

After the 2145 receives the SINGLE SCSI command, it first examines the Mode Control byte. If bits 7 through 4 are not zero, the 2145 switches to the status phase and returns a CHECK CONDITION with the Sense Key set to 5 (Illegal Request). The Sense Code is set to 80 hex and the Sense Code Qualifier is set to 2. After the status is sent, the 2145 then sends the COMMAND COMPLETE message.

Before continuing, the 2145 reads the on-board Error/Status Register to determine if the serial highway is in sync. If the serial highway has synchronization, processing continues. If the 2145 does not have highway sync, the 2145 then switches to the Status phase and sends the CHECK CONDITION status. The Sense Key is set to 2 to indicate that the device is not

ready. The Sense Code is set to 4 and the Sense Code Qualifier is set to 3. After the status is sent, the 2145 sends the COMMAND COMPLETE message.

Once the above parameters are checked, the 2145 creates a command list and initiates its execution. If the CAMAC function code specified a CAMAC Control operation, no SCSI data phase is entered. After the CAMAC control function is detected, the 2145 executes the requested cycle. Once the cycle is complete, the 2145 enters the Status phase and returns the appropriate status. After the status is sent, the 2145 then sends the COMMAND COMPLETE message.

If the CAMAC function code specified a CAMAC write operation, the 2145 switches to the Data In phase. The 2145 expects to receive either two or four bytes of data before executing the CAMAC cycle. The byte count depends on the CAMAC Data Word Size specified. 24-Bit cycles require four bytes and 16-Bit cycles require two bytes. Data is transferred to the 2145 as high byte first. Therefore, if the 24-bit Data Word Size was selected, the data transfer would be a zero byte, CAMAC Write Data bits 17-24 second, 9-16 third, and 1-8 fourth. Once the 2145 has received the correct number of bytes, it executes the CAMAC cycle. After the cycle is complete, the Status phase is entered and the appropriate status is returned. After the status is sent, the 2145 sends the COMMAND COMPLETE message.

If the CAMAC function code specified a CAMAC read operation, the 2145 executes the cycle as soon as the command list has been loaded. Once the cycle is complete, the 2145 enters the Data Out phase and returns the read data obtained from the CAMAC cycle. The number of bytes returned depends on the CAMAC Data Word Size selected. Four bytes are returned for 24-bit operations and two bytes are returned for 16-bit operations. CAMAC Read Data is returned high-byte first, as in the case of CAMAC Write Data. Once the CAMAC Read Data has been sent, the Status phase is entered and the appropriate status is returned. After the status is sent, the 2145 sends the COMMAND COMPLETE message.

The Status byte returned depends on several parameters. These include the selections of the AD (Abort Disable) bit, the QM1 and QM0 (Q Mode) bits, and the CAMAC Q and X responses obtained for the CAMAC operation. If the CAMAC operation resulted in Q and X responses of one, a status of GOOD is returned. If the CAMAC operation resulted in an error, the CHECK CONDITION status is returned with the Sense Key set to 0B hex, the Sense Code set to 80 hex, and the Sense Code Qualifier set to 1.

The following equation describes the definition of an error for the single CAMAC operations.

$$\begin{aligned} \text{ERROR} = {} & \overline{X} * \overline{AD} * \overline{QM2} \\ & \# \overline{X} * \overline{AD} * QM2 * \overline{QM1} \\ & \# \overline{Q} * \overline{QM2} * \overline{QM1} \\ & \# \text{Q-REPEAT TIMEOUT} \\ & \# \text{N GREATER THAN 23} \end{aligned}$$

Executing Block Transfer Operations

Block Transfer operations are used to transfer multiple CAMAC data words to/from an addressed CAMAC module. The Block Transfer operations are executed by using the BLOCK

SCSI command. Three parameters are loaded into the 2145 before the Block Transfer occurs. These parameters are the CAMAC NAF (Station Number, Subaddress, and Function Code), the Mode Control register data, and the transfer count. By using the SCSI BLOCK command, all of the required parameters are passed in the Command Descriptor Block.

The CAMAC NAF is used to determine the CAMAC Station Number, Subaddress and Function Code to be executed during the Block Transfer operation. CAMAC Control commands are not allowed using the Block Transfer commands. If a CAMAC Control operation is specified, a CHECK CONDITION status is returned.

The Mode Control byte for the Block Transfer commands is used to specify the type of Transfer Mode, the CAMAC Data Word Size, and several other parameters concerning the Block Transfer operation. The following table shows the Mode Control byte for the Block Transfer commands. The Transfer Count is used to specify the total number of bytes to be transferred to or from the 2145 during the Data phase of the Block Transfer operation.

Block Transfer Mode Control

TABLE 31 - Block Transfer Mode Control Byte

7	6	5	4	3	2	1	0
0	TM1	TM0	QM1	QM0	WS2	WS1	AD

Bit 7 is not used and must be set to zero.

Bit 6 is used to enable/disable the Enhanced Block Transfer feature of the 2145. This feature is enabled by writing this bit to a one and disabled by writing it to a zero. Refer to the Enhanced Block Transfer section of this manual for further details.

Bit 5 is used to enable/disable the Conservative Block Transfer feature of the 2145. This feature is enabled by setting this bit to a one and disabled by setting it to a zero.

Note: For block transfer operations, either bit 6 or bit 5 **MUST** be set to a one but **NOT** both bits.

Bits 4 and 3 are used to specify the Q-Mode to be used for the block transfer operation. The binary combination of these bits selects the various Q- Modes as follows:

QM1	QM0	Q-Mode
0	0	Q-Stop
0	1	Q-Ignore
1	0	Q-Repeat
1	1	Q-Scan

Bits 2 and 1 are used to specify the CAMAC Data Words Size to be used for the Block Transfer operation. The binary combination of these bits determine the CAMAC Data Word Size as follows:

WS2	WS1	CAMAC Data Word Size
0	0	24-Bit Data Words
0	1	16-Bit Data Words
1	0	Reserved
1	1	Reserved

Bit 0 is used to enable/disable the termination of a Block Transfer operation on the occurrence of a CAMAC X-response of zero. Setting this bit to a one disables the termination of a Block Transfer operation due to a X=0 condition. The X=0 termination is enabled by setting this bit to a zero.

After the 2145 receives a SCSI command instructing it to execute a block transfer operation, it first examines the CAMAC Function Code. If the function specified is a CAMAC Control operation, the 2145 enters the Status phase and returns a CHECK CONDITION with the Sense Key set to 6, the Sense Code set to 80 hex, and the Sense Code Qualifier set to 1. The SCSI command is then terminated. If the CAMAC operation specifies a CAMAC Write or Read command, the 2145 reads the on-board Error/Status Register to determine if the serial highway is in sync. If the serial highway has synchronization, processing continues. If the 2145 does not have highway sync, the 2145 then switches to the Status phase and sends the CHECK CONDITION status. The Sense Key is set to 2 to indicate that the device is not ready. The Sense Code is set to 4 and the Sense Code Qualifier is set to 3. After the status is sent, the 2145 sends the COMMAND COMPLETE message. If the serial highway is in sync, the 2145 then creates a command list and begins execution.

If the CAMAC Function Code specifies a CAMAC read operation, the 2145 executes a serial highway operation which results in a CAMAC Dataway cycle. When the 2145 receives the serial highway reply message, it examines the returned data for validity. During Conservative Block Transfer operations, the 2145 does not sent out subsequent command messages until it receives a reply message. Data validity depends on such parameters as the selected Q-Mode (QM1,QM0), the ABORT DISABLE bit option, and the received CAMAC X and Q responses. Refer to the individual Q-Mode sections of this manual for additional details on data validity.

If the data is valid, the CAMAC read data is placed into a First-In-First-Out (FIFO) memory. The 2145 continues to execute CAMAC operations until the transfer count is exhausted or an error condition occurs. As long as data is available in the FIFO, the SCSI Bus Interface Chip (SBIC) reads the CAMAC read data from the FIFO and transfers it to the SCSI bus. If an error condition occurs, the 2145 ceases executing CAMAC operations, but the SBIC continues sending valid CAMAC data words over the SCSI bus until the FIFO is empty. If the requested SCSI operation completed without any errors, the 2145 enters the Status phase and returns a GOOD status. If the operation resulted in an error, the Status byte is set to CHECK CONDITION. After the status is returned by the 2145, a COMMAND COMPLETE message is sent to the initiator.

If the CAMAC Function Code specified a CAMAC write operation, the SBIC starts obtaining CAMAC write data from the SCSI bus and placing it into a FIFO. This transfer continues until the transfer count is exhausted or an error occurs. When data is available for executing CAMAC operations, the 2145 initiates a serial highway command message which results in a CAMAC Dataway cycle. After the 2145 receives the reply message from the write operation,

the CAMAC Q and X responses are examined to determine the success of the operation. If the data was successfully transferred, the next CAMAC write operation is then executed. The 2145 continues performing CAMAC operations as long as there is write data available in the FIFO and no errors are encountered. If an error occurs, the CAMAC activity ceases and the SBIC stop executing SCSI data transfers. The 2145 terminates the data phase, switches to the status phase, and returns a CHECK CONDITION. If the operation completes without any errors, a status of GOOD is returned to the initiator. Once the status is returned, a COMMAND COMPLETE message is sent.

Conservative Block Transfer Operations

The 2145 supports four types of Conservative Block Transfers; these are Q-Stop, Q-Ignore, Q-Repeat, and Q-Scan. During conservative operation. transfers to/from the CAMAC crate are done in a command/reply fashion. For CAMAC reads, a command message is sent down the serial highway. When the 2145 receives the reply message, it determines if the data it receives is valid and should be stored in the CAMAC read FIFO. Please refer to the individual Q-Mode descriptions for details on data validity. After the read data is stored in the FIFO, the 2145 examines the transfer count to see additional transfers are required. If the transfer count is not yet exhausted, the 2145 the command/reply sequence obtaining CAMAC read data until the operation completes.

When executing CAMAC write operations, the serial highway circuitry waits for the SCSI interface chip to provide CAMAC write data. Once the data is available, the 2145 sends a command message down the serial highway. After the reply message is received, the 2145 examines the transfer count to see if additional transfers are required. If the transfer count is not exhausted, additional command/reply sequences are executed until the operation completes.

Q-Stop Block Transfer Operations

To select the Q-Stop Mode, set both the QM2 and QM1 bits to zeros. During Q-Stop Block Transfer operations, the CAMAC command specified is repeated until the transfer count is exhausted or a Q response of zero is received. The transfer also terminates when an error condition occurs. The following equation describes the ERROR for Q-Stop Block Transfers:

$$\begin{aligned} \text{ERROR} &= \overline{Q} \\ &\quad + \overline{AD} * (\overline{X} + \text{ERR} + \text{LPE} + \text{TPE}) \end{aligned}$$

Q-Ignore Block Transfer Operations

To select the Q-Ignore Mode, set the Q-Mode bit QM2 to a zero and the QM1 bit to a one when loading the Mode Control byte. During Q-Ignore Block Transfers, the CAMAC command specified is repeated until the transfer count is exhausted. The transfer also terminates if an error is encountered. The following equation describes the ERROR for Q-Ignore Block Transfers:

$$\text{ERROR} = \overline{AD} * (\overline{X} + \text{ERR} + \text{LPE} + \text{TPE})$$

Q-Repeat Block Transfer Operations

To select the Q-Repeat Mode, set the QM2 bit to a one and the QM1 bit to a zero when loading the Mode Control byte. During a Q-Repeat Block Transfer operation, the CAMAC command specified is repeated for each data word until a Q response of one is obtained. A Q response of one causes either new write data to be retrieved or read data to be stored. The command is repeated for each data word until the transfer count is exhausted. If a Q response of one is not received for a data word within the user selectable Q-repeat timeout value, the transfer terminates and CHECK CONDITION is returned. This Q-Repeat timeout feature can be disabled by a strap located in the 2145. Refer to the Strap Options section of this manual for further information. The Block Transfer also terminates if an error is encountered. The following equation describes ERROR for Q-Repeat Block Transfer operations:

$$\text{ERROR} = \text{Q-TIMEOUT} + \overline{AD} * (\overline{X} + \text{ERR} + \text{LPT} + \text{TPE})$$

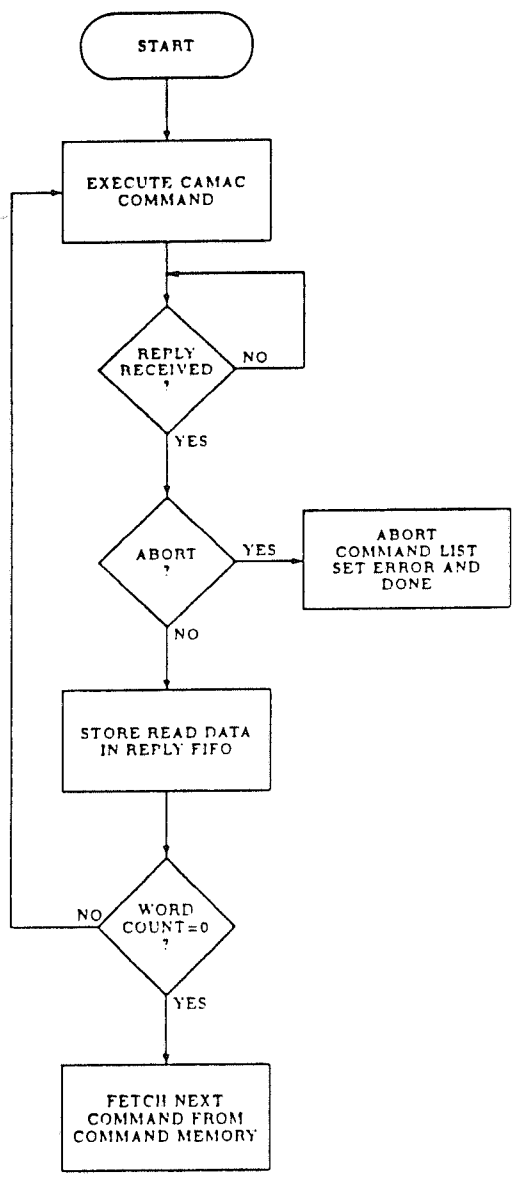
Q-Scan Block Transfer Operations

To select the Q-Scan Mode, set both the Q-Mode bits, QM2 and QM1, to ones when loading the Mode Control byte. During Q-Scan Block Transfer operations, the 2145 uses the Q response from the previously executed CAMAC command to determine the Station Number (N) and Subaddress (A) for the next operation. A Q response of zero indicates that the last valid subaddress of the current Station Number has been accessed. The 2145 responds to a Q response of zero by resetting the Subaddress, incrementing the Station Number, and continuing the scan. A Q response of one indicates that the last CAMAC command was executed to a valid CAMAC address. The 2145 responds to a Q response of one by either storing the read data or retrieving new write data. After a Q response of one is received, the 2145 updates the CAMAC address as follows: the Subaddress is incremented or, if the Subaddress was 15, it is reset to zero, and the Station Number is incremented. Figure 6 illustrates the updating of the CAMAC address based on the CAMAC Q response:

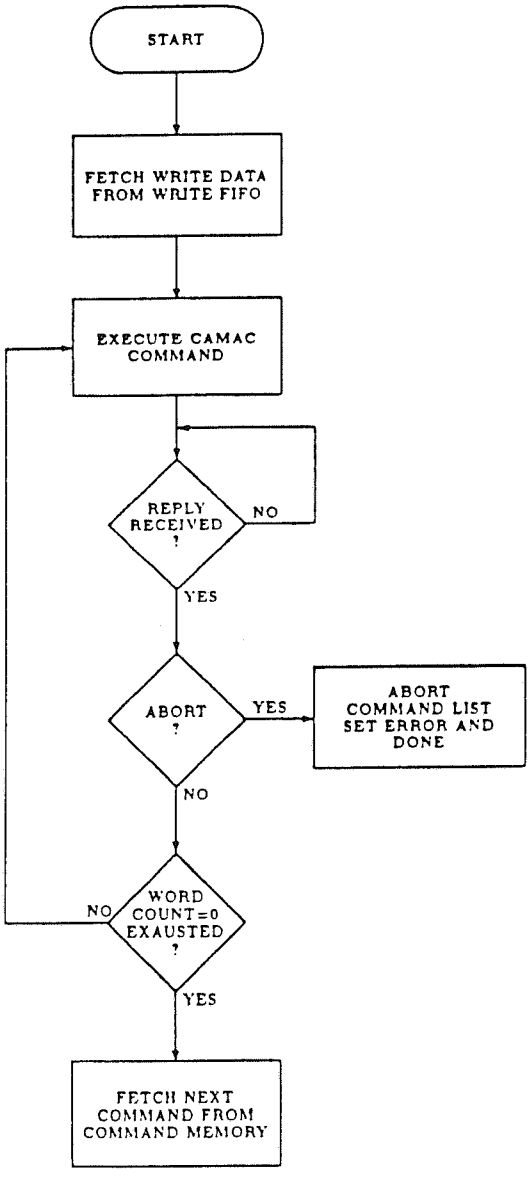
If, due to a programming error, the 2145 increments beyond Station Number 23, the Block Transfer operation is terminated and a CHECK CONDITION is returned.

The following equation describes ERROR for Q-Scan Block Transfer operations.

$$\text{ERROR} = \text{N GREATER THAN 23} + \text{ERR} + \text{LPE} + \text{TPE}$$



IGNORE-Q READ COMMANDS



IGNORE-Q WRITE COMMANDS

FIGURE 2 - Ignore Q-Block Commands

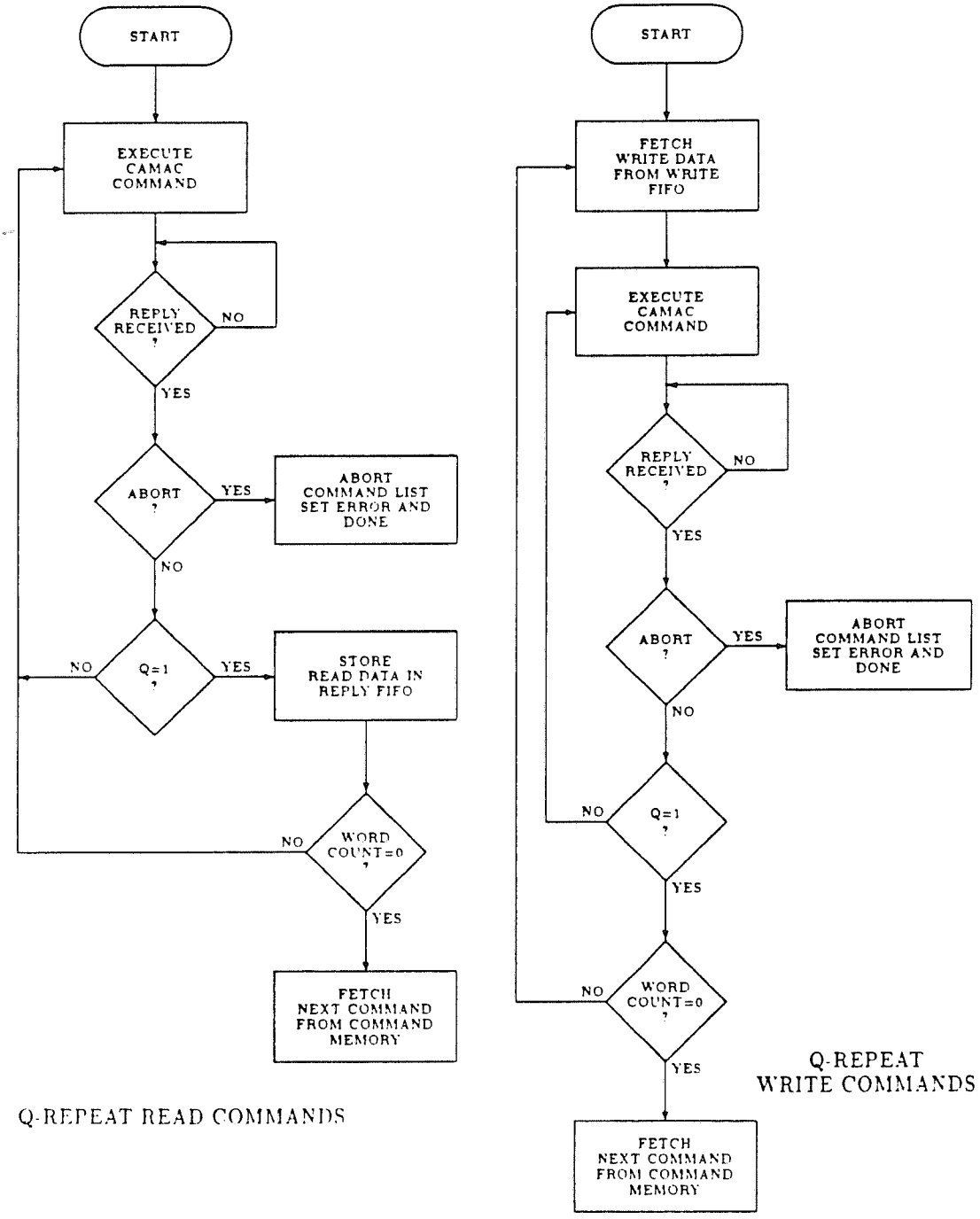


FIGURE 3 - Q-Repeat Block Commands

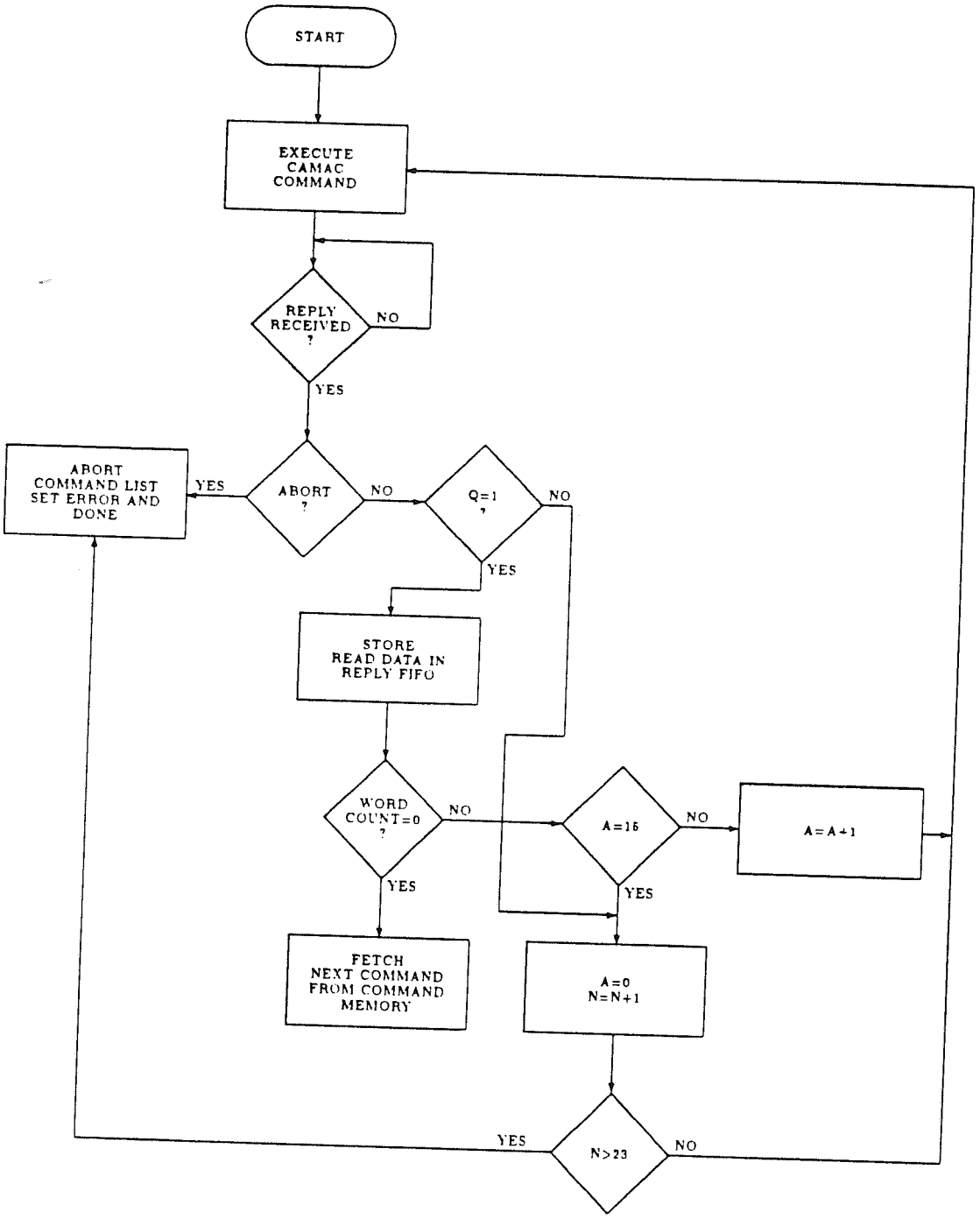


FIGURE 4 - Q-Scan Read Commands

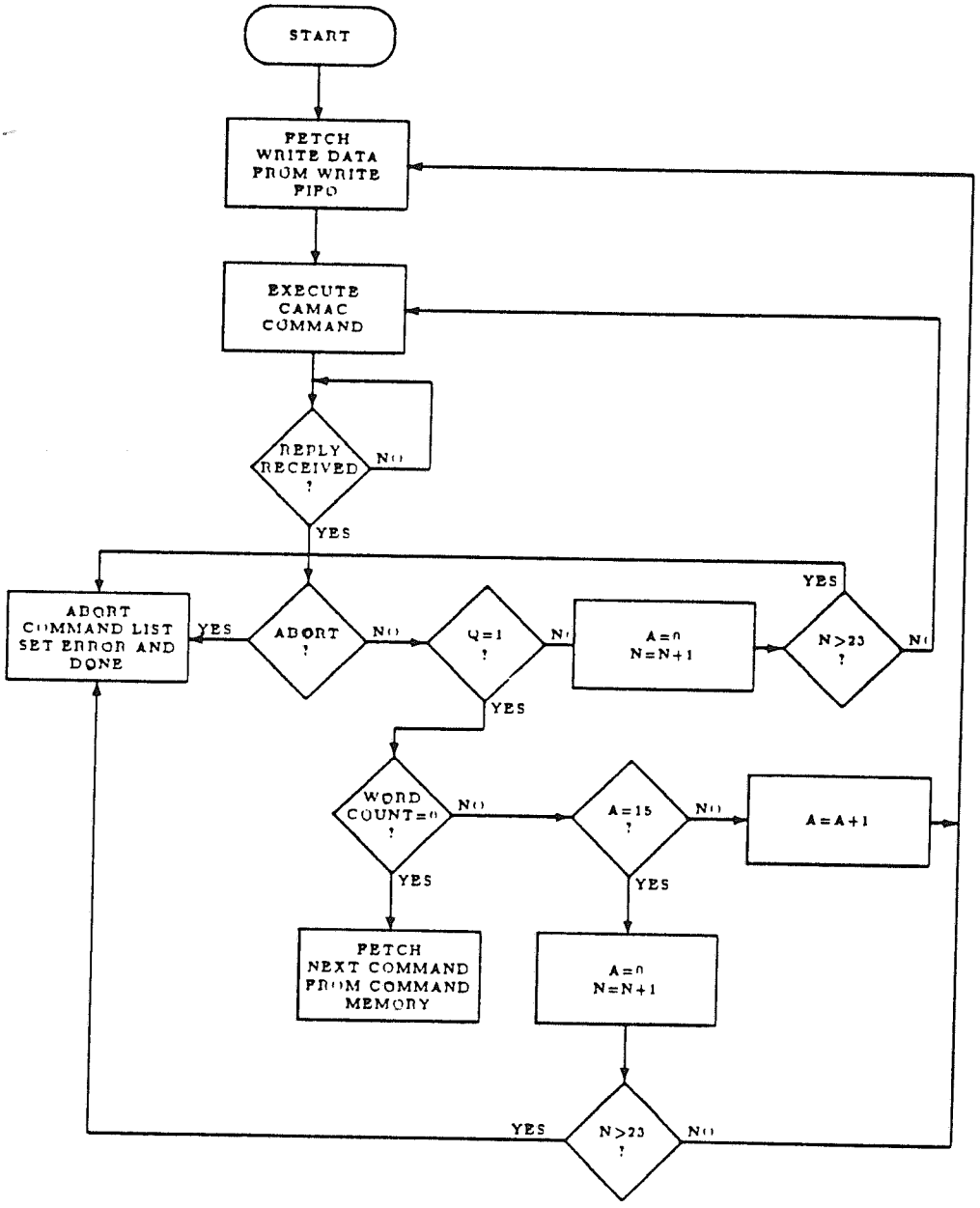


FIGURE 5 - Q-Scan Write Commands

Enhanced Block Transfer Operations

The 2145 provides five types of Enhanced Block Transfer operations. These modes include: Single NAF Q-Stop, Single NAF Q-Ignore, Single NAF Q-Repeat (read only), List Sequence Q-Repeat (read only), and List Sequence Q-Ignore. The two List Sequencing modes require use of the KSC Model 3830-Z1A List Sequencer Module.

In the Enhanced Block Transfer modes, transfers to/from the CAMAC crate are done in a pipelined fashion. Data transmitted onto (or received from) the serial highway are FIFO buffered. The 2145 provides a CAMAC write data FIFO and a separate CAMAC read data FIFO. The FIFO's are a buffering mechanism which is used to absorb timing differences in between the SCSI bus and the serial highway. If the SCSI interface of the host computer can keep up with the 3 Megabyte-per-second maximum data rate for the CAMAC Dataway, the CAMAC write operations will occur once every microsecond. If during the block transfer the host computer cannot keep up with the serial highway, the 2145 inserts "filler" words into the data stream until the computer can either supply more write data or retrieve the read data. The crate controllers are able to detect these "filler" words, discard them, and report this in the status byte of the reply. The 2145 receiver circuitry checks the status byte of each word. If the status byte returned indicates a "filler" status return, both the status byte and the status are discarded.

Enhanced Serial Highway Command/Reply Sequence

The Enhanced Block write operation shown in Figure XX shows the bytes associated with the Enhanced Serial Highway Command/Reply Sequence for a CAMAC write operation. This byte stream is a logical extension of the CAMAC standard for single transactions. A Key element in the sequence is the CONTROL byte. The two LSB's of this byte are decoded by the crate controller and have the following definitions:

D1	D0	Definition
0	0	The received word is not a "filler" word and is not the last word in the block.
0	1	The received word is not a "filler" word and is the last word in the block.
1	0	The received word is a "filler" word and is not the last word in the block.
1	1	The received word is a "filler" word and is the last word in the block.

During CAMAC write transfers, the 2145 inserts "filler" words whenever the CAMAC write FIFO is empty. As soon as additional write data words are loaded into the FIFO by the SCSI interface, the 2145 stops sending "filler" words and resumes sending the actual CAMAC write data.

Model 2145-Z1B

During CAMAC read transfers, the 2145 inserts "filler" words whenever the read reply FIFO exceeds the half-full indicator so that a large enough buffer exists to store remaining reply data words from the highway. As soon as the FIFO is less than half-full, the 2145 stops sending "filler" words and the actual read data is then accepted.

The status byte in the reply for each data word provides the Q and X responses from the module as well as error information. After the first word of a block is received, bit 5 of the status byte, normally set to a 1 to indicate a reply, is set to 0 by the crate controller to indicate a "filler" word. If the receiver encounters a "filler" word, it discards the status byte and the data that follows.

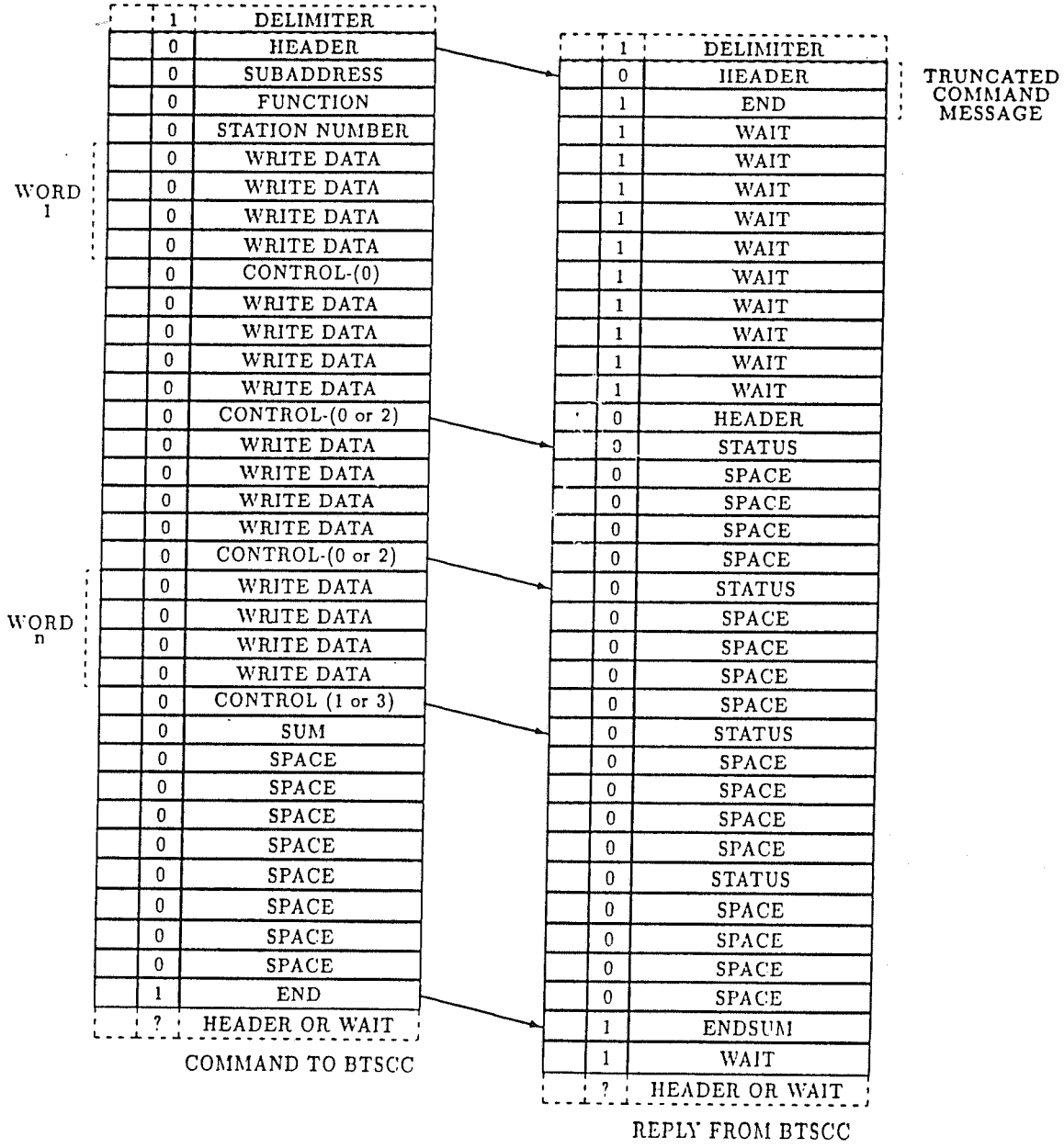


FIGURE 6 - Enhanced Write Commands

The Enhanced Block Read operation shows an Enhanced Serial Highway Command/Reply sequence for a CAMAC read command. This block mode transaction is very similar to the a write operation except that groups of SPACE bytes are provided in the command message to allow space for the read data (6 bits per byte) in the Reply message.

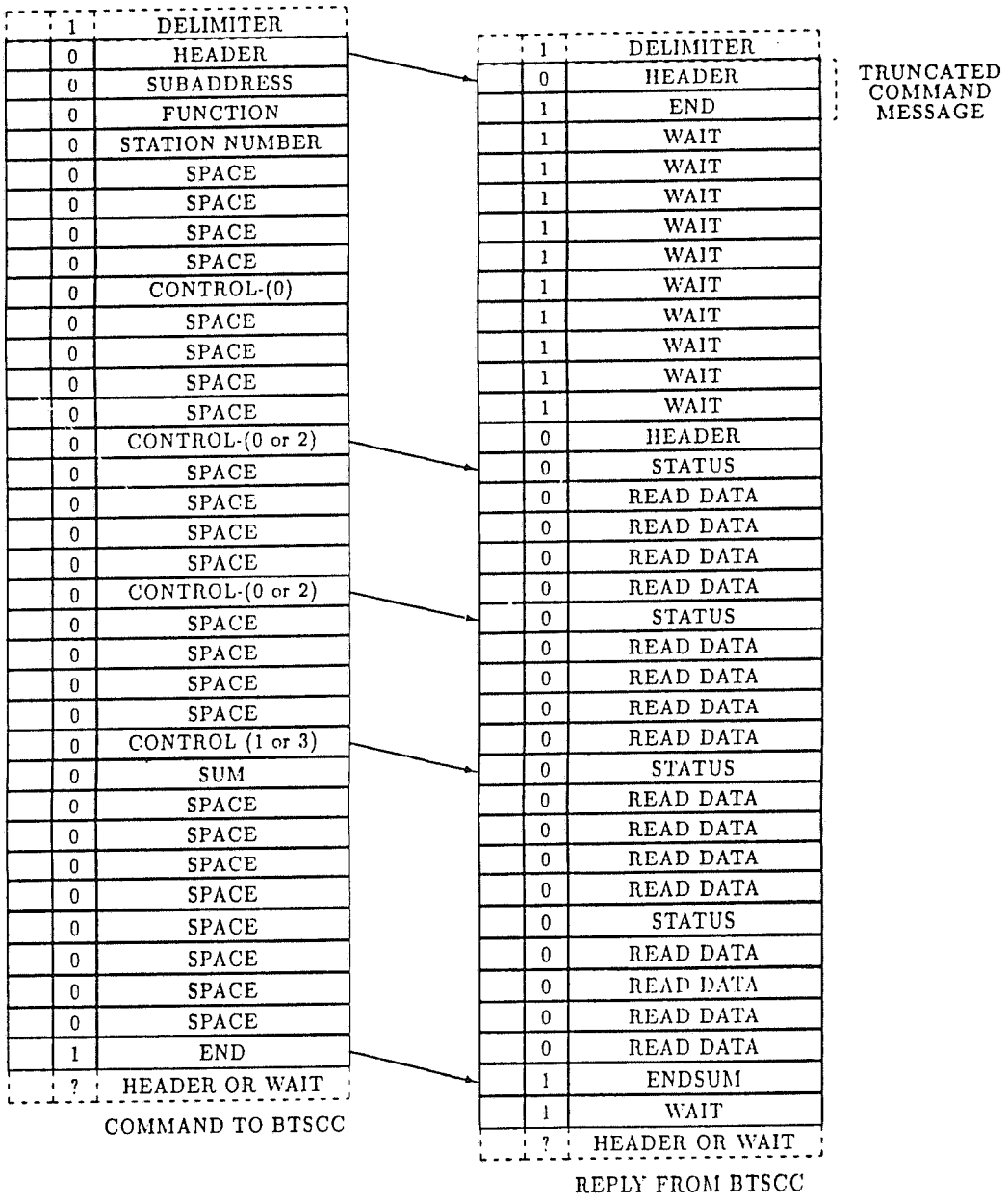


FIGURE 7 - Enhanced Read Command

The following is a description of the Enhanced Serial Highway Block Transfer Modes.

Single NAF Q-Stop Enhanced Block Transfer

To select the Single NAF Q-Stop Enhanced Block Transfer mode of operation, set the TM1 to a 1, TM0 to a 0, QM1 to a 0, and QM0 to a 0. During Q-Stop block transfers, the CAMAC command specified is repeated until a Q-response of zero is obtained or the transfer count is exhausted. The block transfer will also terminate if an error occurs. The following equation describes an ERROR when in the Q-Stop mode.

ERROR = NO-Q
+ AD * (NO-X + ERR + TPE + LPE)

Single NAF Q-Ignore Enhanced Block Transfer

To select the Single NAF Q-Ignore Enhanced Block Transfer mode of operation, set the TM1 bit to 1, TM0 to a 0, QM1 to a 0, and QM0 to 1. During Q-Ignore block transfers, the CAMAC command specified is repeated until the transfer count is exhausted. The operation will also terminate if an error is encountered during the transfer. The following equation describes an ERROR when operating in the Q-Ignore mode.

ERROR = AD * (NO-X + ERR + TPE + LPE)

Single NAF Q-Repeat Enhanced Block Transfer

To select the Single NAF Q-Repeat Enhanced Block Transfer mode of operation, set the TM1 bit to a 1, TM0 to a 0, QM1 to a 1, and QM0 to a 0. Only Q-Repeat read operations may be executed in this mode. Q-Repeat writes are not supported with mode.

When executing Q-Repeat read operations, the 2145 places valid read commands on the serial highway as long as the reply FIFO is not half full. When valid read data is received (Q=1 responses) it is stored in the read reply FIFO and the transfer count is incremented. The block transfer is complete when the transfer count is exhausted. By the time that the 2145 has determined that the transfer count is exhausted, there has been room allocated on the serial highway for additional read data that had not been specified with the transfer count. Thus, care should be taken when using this mode since there is no control on the number of CAMAC read cycles actually performed. The 2145 continues to place read commands on the highway indefinitely if a Q=1 response is not received. Therefore, a strap selectable hardware timeout has been implemented which will terminate the block transfer. Refer to the Strap Options section of this manual for additional information. The following equation describes an ERROR when operating in the Q-Repeat mode.

ERROR = Q-REPEAT TIMEOUT
+ AD * (NO-X + ERR + TPE + LPE)

Enhanced Serial Highway List Sequencing

List sequencing allows Enhanced Serial Highway transfer operation to take place on a predefined list of CAMAC commands. This is accomplished through the use of the KSC Model 3830-Z1A List Sequencer Module. Each CAMAC data word transferred has a corresponding NAF loaded in the List Sequencer Module (LSM). The CAMAC commands loaded in the LSM must be unidirectional. Control commands may be embedded in either a write or read lists as long as data space is allocated to them during the block transfer operation. The data associated with these control commands may be discarded.

There are four lists available within the LSM, two read and two write. Each of these lists can hold up to 512 CAMAC commands. It is also possible to load the LSM in such a way that only two lists are available, one for reads and one for writes. In this case, the list size doubles to 1024 CAMAC commands.

List 0 and List 1 of the LSM contain sets of CAMAC read commands to execute. List 2 and List 3 contain CAMAC write commands. When preparing the 2145 to execute a block transfer using the LSM, a special CAMAC command must be loaded. This special command informs the 3952 Block Transfer Serial Crate Controller (BTSCC)/LSM combination as to which list to use for the block transfer.

Command	NAF List	Data Type
N(30)F(12)A(0)	List 0	Read
N(30)F(12)A(1)	List 1	Read
N(30)F(12)A(2)	List 2	Write
N(30)F(12)A(3)	List 3	Write

When the 3952 BTSCC receives on of these special commands, it enables the list-sequencing block transfer.

Before the list-sequencing operation begins, the 3820 List Sequencer Module must be loaded. Refer to the 3830-Z1A Operating Manual for detailed instructions on loading and using the LSM. When the last NAF is loaded in the LSM for a particular list, bit 16 is set to indicate that this is the last CAMAC NAF for this list. This bit is referred to as the end-of-list flag. If the end-of-list flag is overrun during list sequencing, the LSM will generate a Q=1 and X=0 response. This "special" Q and X response is used to inform the 2145 that the list was overrun. The 2145 does not write this status byte to the internal status register.

Q-Repeat Enhanced Serial Highway List Sequencer Mode

To select the Q-Repeat Enhanced Serial Highway List Sequence mode of operation, set the TM1 bit to 1, TM0 to 0, QM1 to 1, and QM0 to 0. This mode is only available for CAMAC read operations. During CAMAC reads, read reply data is stored in the FIFO whenever a Q=1 response is received in the status byte. A Q=1 response also causes the LSM to increment to the next NAF in the list. A Q=0 response indicates to the LSM that valid data has not been received, preventing the LSM from incrementing to the next NAF. The block transfer continues until the transfer count is exhausted or an error occurs.

Before the block transfer begins, the LSM must be enabled to operate in the Q-Repeat mode. To enable the LSM, execute an F(26)A(0) command addressed to the LSM. To disable Q-Repeat, execute an F(24)A(0) to the LSM.

The following equation describes ERROR when using the Q-Repeat List Sequencing mode.

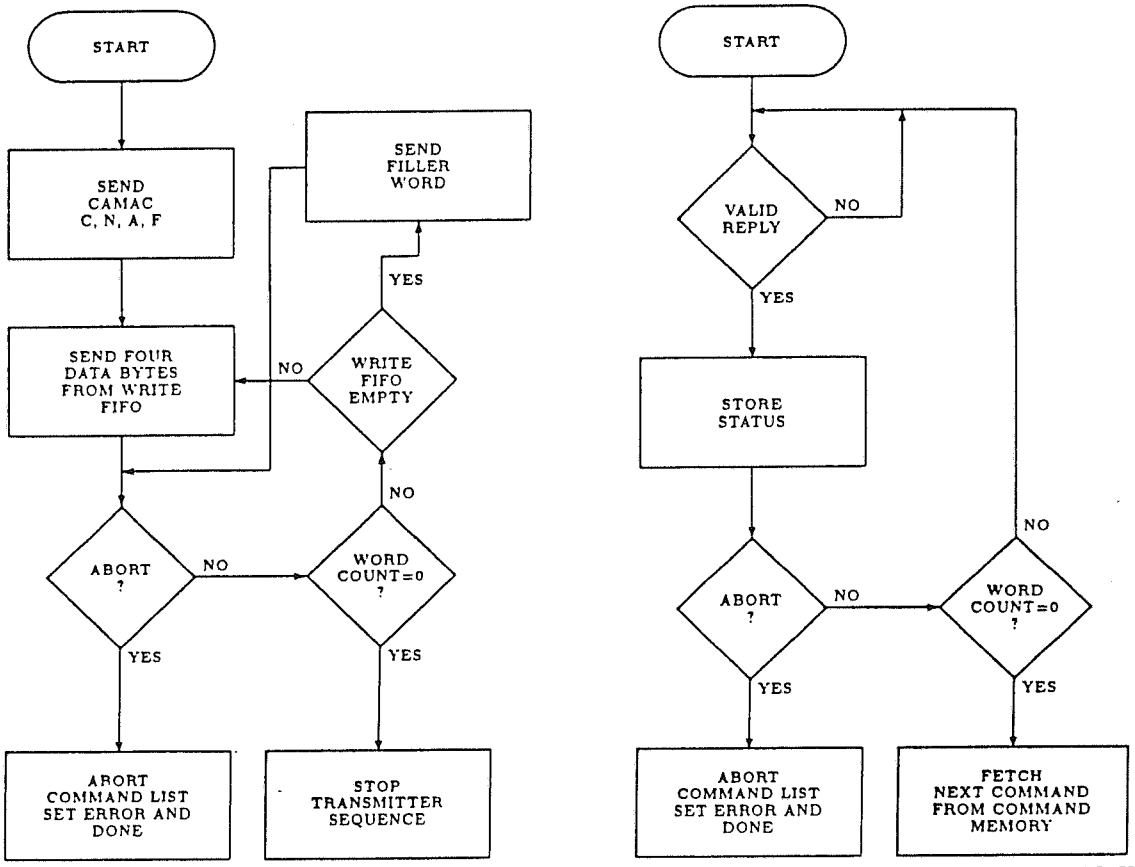
$$ERROR = AD * (ERR + LPE + TPE)$$

Q-Ignore Enhanced Serial Highway List Sequencer Mode

To select the Q-Ignore Enhanced Serial Highway List Sequence mode of operation, set the TM1 bit to 1, TM0 to 0, QM1 to 0, and QM0 to 1. In this mode of operation, the LSM pointer to the individual NAF is incremented after every CAMAC cycle. The block transfer continues until the transfer count is exhausted or an ERROR is encountered. The following equation describes ERROR while in the Q-Ignore mode.

$$ERROR = AD * (ERR + LPE + TPE)$$

Enhanced Serial Highway Flow Diagrams



SERIAL HIGHWAY TRANSMITTER SEQUENCE

SERIAL HIGHWAY RECEIVER SEQUENCE

FIGURE 8 - Enhanced Serial Highway Block Writes

THESE SEQUENCES RUN SIMULTANEOUSLY

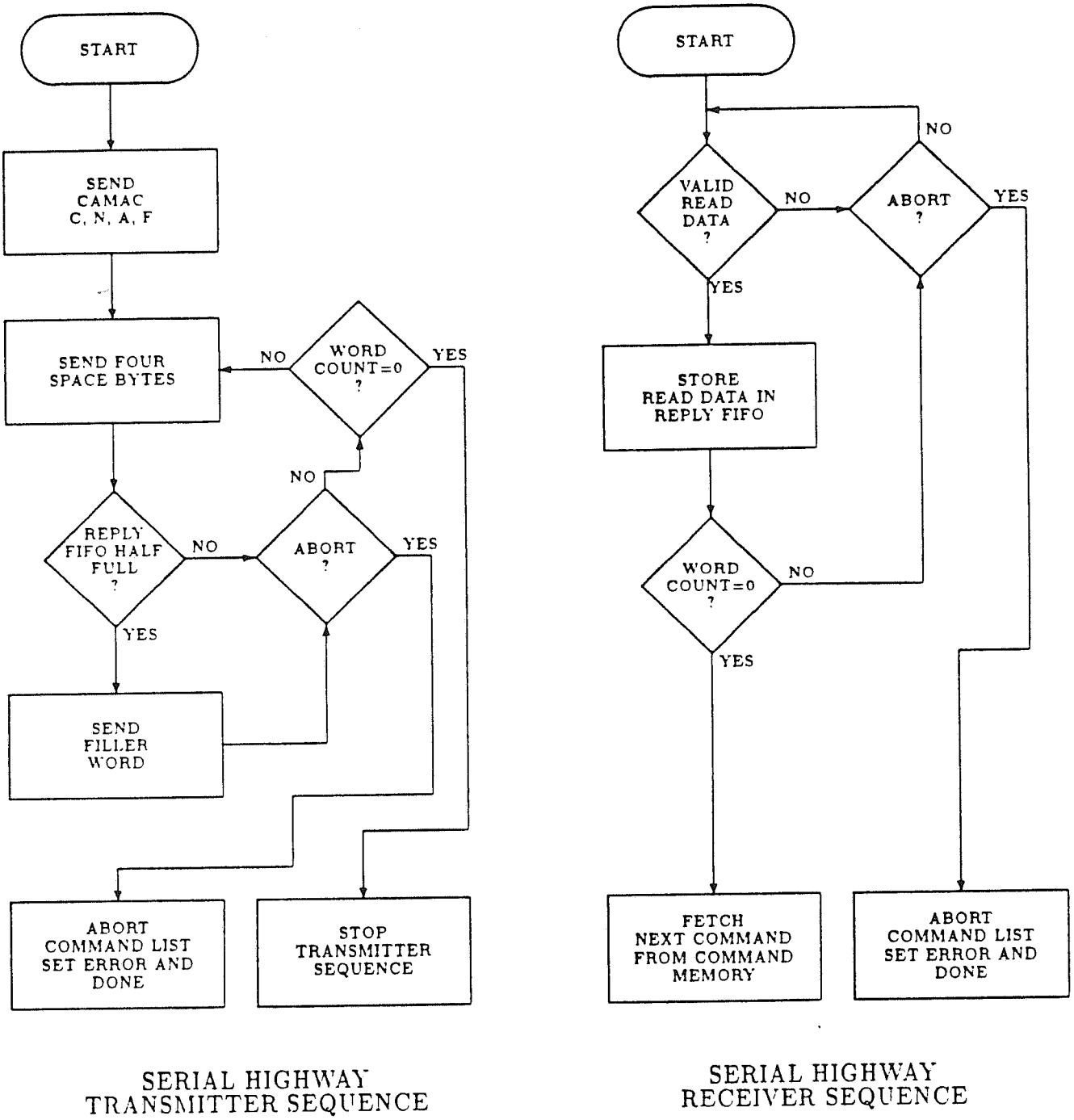
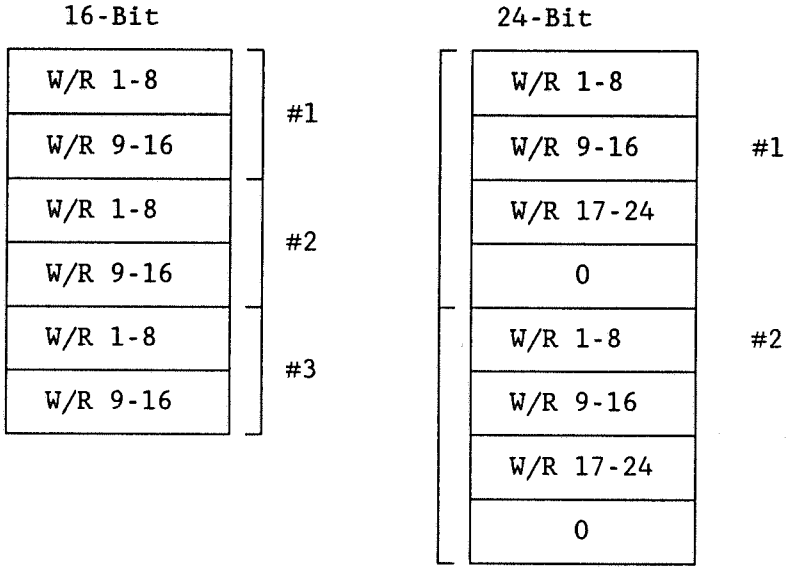


FIGURE 9 - Enhanced Serial Highway Block Reads

Data Storage Format

The Single and Block Transfer operations in the 2145 may use CAMAC data word sizes of either 16 or 24-bits. This selection is made when the Mode Control byte is loaded. The data for CAMAC operations is transferred on the SCSI bus as low-byte first. The following diagrams show the order in which data is sent/received to/from the 2145. The first byte transferred is shown at the top of the diagram and the last byte transferred is at the bottom.



Asynchronous Event Notification

The SCSI Asynchronous Event Notification (AEN) protocol defines a mechanism whereby a target may assume the role of a temporary initiator and request the transfer of data. The 2145 uses the AEN mechanism to report the occurrence of predetermined LAM's (LOOK-AT-MEs) to the SCSI initiator. The 2145 is notified of a LAM by a serial highway demand message. This message contains the serial crate address of the crate generating the LAM and an encoded Serial-Graded-LAM (SGL) pattern. This information is held in the 2145 by a 512 word FIFO.

Before the 2145 can execute an AEN, the desired LAM's must be booked. Booking a LAM refers to enabling the 2145 to sense a specified LAM and take action based upon that LAM. The SCSI BOOK LAM command is used to setup and enable individual LAMs. The BOOK LAM command consists of a LAM Identification, a LAM Type, a CLEAR LAM NAF, a DISABLE LAM NAF, and a few user defined fields. Refer to the BOOK LAM Command section of this manual for further information regarding booking LAMs.

The LAM identification parameter defines the LAM number. This number corresponds to the station number in which the LAM is to be setup and enabled. (LAM Identification 17 corresponds to the LAM generated from station number 17.) The LAM Type parameter specifies the action to be taken once the LAM has been generated. A Type 0 LAM indicates that both the CLEAR and DISABLE NAFs are to be executed. A Type 1 LAM indicates that only the CLEAR NAF is to be executed. The three user defined fields are general purpose and are returned to the "normal" initiator when the AEN occurs.

There are two CAMAC commands specified with the BOOK LAM Command. One command is for the CLEAR operation and the other is for the DISABLE operation. When a selected LAM is generated, the 2145 examines the LAM type and executes the predetermined CAMAC commands. The two commands specified must be CAMAC control operations as there is no mechanism for associating write or read data with a particular LAM.

After the predetermined CAMAC commands are executed, the 2145 becomes a temporary initiator and selects the "normal" initiator as a target. Once the connection is made, a SCSI SEND command is executed. This command instructs the "normal" initiator to receive four bytes of data as specified by the Transfer Count fields in the SEND commands Command Descriptor Block. The "normal" initiator then accepts the four bytes of data from the 2145. This data contains the LAM identification and the three user defined fields. The following shows the order in which the data bytes are transferred.

Byte 1	Crate Address
Byte 2	LAM Identification
Byte 3	User Defined Field 2
Byte 4	User Defined Field 3

These four bytes that are returned are the same data bytes used for the selected LAM when the BOOK LAM was executed. After the "normal" initiator receives the four bytes, it must send the Status Byte and a COMMAND COMPLETE MESSAGE that ends the AEN.

List Processing

The 2145 provides for a means of executing a preloaded list of CAMAC commands, termed List Processing. This list of commands may contain block transfer operations, single CAMAC operations, or CAMAC write operations with the write data embedded in the list. List processing provides a mechanism for executing multiple CAMAC operations with minimum software overhead. Once the list has been loaded in the 2145, the only operation needed to execute the list is the EXECUTE LIST SCSI command. Optionally, timer initiated list operation may occur. To execute this type a list, the START TIMER SCSI command is used. Once the list is started, all elements in the list are executed until a HALT instruction is encountered.

Two other SCSI commands are used for list processing. These commands are the LOAD LIST and RESUME LIST commands. Refer to the individual SCSI command descriptions for the format of each command. The LOAD LIST command is used for sending the list elements to the 2145. The RESUME LIST command is used for resuming list execution once the list has been prematurely terminated due to an error condition.

List Processing Format

The following describes the format of the four types of list instructions. The command instruction types include Single CAMAC operations, Conservative Block Transfer operations, Enhanced Block Transfer operations, and Single Write With In-Line data.

All instructions have a minimum of four bytes. The first and second bytes contain the CAMAC NAF to be executed, the third contains the crate address for the operation, and the fourth byte contains the instruction type. The following describes the first four bytes of any list processing instruction.

Instruction Byte 1

The first byte of the instruction contains the opcode for the instruction. This byte also specifies the CAMAC Transfer Mode, CAMAC Data Word Size, and the Abort Disable selection for CAMAC type instructions. The following table shows the layout of the first instruction byte, the opcode byte.

7	6	5	4	3	2	1	0
CM	OP2	OP1	QM2	QM1	WS2	WS1	AD

Bit 7 is used to specify either CAMAC or non-CAMAC instructions. If this bit is set to a zero, the instruction is a CAMAC type instruction. If this bit is set to one, the instruction is a non-CAMAC operation. The only non-CAMAC operation currently defined is the HALT instruction.

Bits 6 and 5 are used to define the type of CAMAC operation (CM bit is set to zero). If the CM bit is set to one, these bits should be set to zero, which defines the HALT instruction. The following chart shows the type of CAMAC operation defined for the binary combination of these two bits.

OP2	OP1	Instruction
0	0	Single CAMAC Operation
0	1	Conservative Block Transfer Operation
1	0	Enhanced Block Transfer Operation
1	1	Single Write With In-Line Data

Bits 4 and 3 are used to specify the Q-Mode for the CAMAC operation (CM bit is zero). If the CM bit is set to one, these bits should be set to zero to indicate a HALT instruction. The following chart shows the CAMAC Transfer Modes obtained with the binary combination of these bits. Please refer to the Single CAMAC Operations and Block Transfer Operations section of this manual for further information regarding the Transfer Modes.

QM2	QM1	Q-Mode
0	0	Q-Stop Transfers
0	1	Q-Ignore Transfers
1	0	Q-Repeat Transfers
1	1	Q-Scan Transfers

Bits 2 and 1 are used to specify the CAMAC Data Word Size to be used during a CAMAC operation (CM bit is set to zero). If the CM bit is set to one, these bits should be set to zero for the HALT instruction. The following chart shows the CAMAC Data Word Sizes obtained by the binary combination of these bits. Please refer to the Single CAMAC Operations and Block transfer Operation of this manual for additional information.

WS2	WS1	CAMAC Data Word Size
0	0	24-Bit Data Size
0	1	16-Bit Data Size
1	0	Reserved
1	1	Reserved

Bit 0 is used to enable or disable the termination of a CAMAC operation based on the CAMAC X-response. Refer to the Single CAMAC Operations and Block Transfer Operations section of this manual for further information on the use of the ABORT DISABLE bit. For non-CAMAC operations, this bit should be set to zero to indicate a HALT instruction.

Instruction Byte 2

The second byte of the instruction contains the serial crate address to be used for the CAMAC operation. The following table shows the bits defined in the second instruction byte.

7	6	5	4	3	2	1	0
0	0	C32	C16	C8	C4	C2	C1

Bits 7 and 6 are reserved and must be set to zero.

Bits 5 through 0 are used for specifying the serial crate address for the CAMAC operation. The allowable range for the crate address specification is 1 through 62.

Instruction Byte 3

The third byte of the instruction contains a portion of the CAMAC NAF to be used during a CAMAC operation. The fourth byte of the instruction contains the remaining bits for the NAF specification. The following table shows the bits defined in the third instruction byte.

7	6	5	4	3	2	1	0
A4	A2	A1	F16	F8	F4	F2	F1

Bits 7 through 5 are used in conjunction with bit 0 of the first instruction byte for specifying the CAMAC Subaddress to be used during the CAMAC operation.

Bits 4 through 0 are used for specifying the CAMAC Function Code to be executed during the CAMAC operation.

Instruction Byte 4

The fourth byte of the instruction contains a portion of the CAMAC Station Number, Subaddress, and Function Code (NAF) to be used for the command. The third byte of the instruction contains the remaining bits of the NAF. The following table shows the bits defined for the fourth instruction byte:

7	6	5	4	3	2	1	0
0	0	N16	N8	N4	N2	N1	A8

Bits 7 and 6 are not used and must be set to zero.

Bits 5 through 1 are used to specify the CAMAC Station Number to be accessed during the CAMAC operation.

Bit 0 is the most significant bit of the CAMAC Subaddress field. This bit is used in conjunction with bits 7 through 5 of the second instruction byte to form the Subaddress to be used during the CAMAC operation.

Instruction Bytes 5 through 8

These instruction bytes are only required for CAMAC Block Transfer and the Single Write with In-Line Data operations. The Single CAMAC operations and HALT instructions do not use these bytes.

For the Block Transfer operations, these four bytes contain the transfer count for the operation. This transfer count specification is the two's complement form of the actual transfer count. Note that this is different from the transfer count specifications for the SCSI commands. The last and most-significant byte of the four must be set to FF hex. The remaining three bytes are actually used for the transfer count specification.

For the Single Write With In-Line Data instruction, these four bytes are used to contain the CAMAC write data for the operation. The last of the four bytes is not used and should be set to zero. The other three bytes contain the actual CAMAC write data for the command. Byte 7 contains write data bits 17-24, byte 6 contains write data bits 9-16, and byte 5 contains write data bits 1-8.

Single CAMAC Operation Instruction

This instruction is used to execute a single CAMAC operation within the CAMAC crate. This instruction can be used to execute CAMAC read, write, or control operations. For control operations, no data is associated with the instruction. For CAMAC read and write operations, data is transferred to or from the on-board FIFO as required. As with non-list processing, the number of data bytes transferred depends on the CAMAC Data Word Size selection specified with the instruction. The following table shows the instruction format for the Single CAMAC Operation instruction.

TABLE 32 - Single CAMAC Instruction Format

7	6	5	4	3	2	1	0	
0	0	0	QM2	QM1	WS2	WS1	AD	Byte 1
0	0	C32	C16	C8	C4	C2	C1	Byte 2
A4	A2	A1	F16	F8	F4	F2	F1	Byte 3
0	0	N16	N8	N4	N2	N1	A8	Byte 4

Single Write With In-Line Data Instruction

This instruction is used to execute a single CAMAC write operation. The CAMAC write data to be used for the operation is contained in the list. This command is useful for embedding CAMAC write operations in a read list. This instruction may only be used for CAMAC write operations. If a CAMAC read or control operation is specified with this instruction, the processing terminates and a CHECK CONDITION is returned. The Sense Key is set to 5, the Sense Code is set to 80 hex, and the Sense Code Qualifier is set to 1. The following table shows the format of the Single Write with In-Line Data instruction:

TABLE 33 - Single Write w/In-Line Data

7	6	5	4	3	2	1	0	
0	1	1	QM2	QM1	WS2	WS1	A8	Byte 1
0	0	C32	C16	C8	C4	C2	C1	Byte 2
A4	A2	A1	F16	F8	F4	F2	F1	Byte 3
0	0	N16	N8	N4	N2	N1	A8	Byte 4
W8	W7	W6	W5	W4	W3	W2	W1	Byte 5
W16	W15	W14	W13	W12	W11	W10	W9	Byte 6
W24	W23	W22	W21	W20	W19	W18	W17	Byte 7
0	0	0	0	0	0	0	0	Byte 8

Conservative Block Transfer Instruction

This instruction is used for executing a Conservative CAMAC Block Transfer operation. This command is used for executing either CAMAC read or write operations. If a CAMAC control operation is specified, processing terminates and a CHECK CONDITION is returned. The Sense Key is set to 5, the Sense Code is set to 80 hex, and the Sense Code Qualifier is set to one.

Data transfer to/from the CAMAC Dataway during the Block Transfer operation occurs in the same fashion as the non-list processing block transfers. Refer to the Executing Block Transfers section of this manual for additional information.

This instruction requires a transfer word count specification. This differs from the non-list processing transfer count which is specified in bytes. The transfer count for list processing must be in the two's complement form. The following table shows the format for the Conservative Block Transfer Operation instruction.

TABLE 34 - Conservative Block Transfer Operation

7	6	5	4	3	2	1	0	
0	0	1	QM2	QM1	WS2	WS1	AD	Byte 1
0	0	C32	C16	C8	C4	C2	C1	Byte 2
A4	A2	A1	F16	F8	F4	F2	F1	Byte 3
0	0	N16	N8	N4	N2	N1	A8	Byte 4
TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	Byte 5
TC16	TC15	TC14	TC13	TC12	TC11	TC10	TC9	Byte 6
TC24	TC23	TC22	TC21	TC20	TC19	TC18	TC17	Byte 7
1	1	1	1	1	1	1	1	Byte 8

Enhanced Block Transfer Instruction

This instruction is used for executing a Fast CAMAC Block Transfer operation. This command is used for executing either CAMAC read or write operations. If a CAMAC control operation is specified, processing terminates and a CHECK CONDITION is returned. The Sense Key is set to 5, the Sense Code is set to 80 hex, and the Sense Code Qualifier is set to 1. Data transfer to/from the CAMAC Dataway during the Block Transfer operation occurs in the same fashion as the non-list processing block transfers. Refer to the Executing Block Transfers section of this manual for additional information.

This instruction requires a transfer word count specification. This differs from the non-list processing transfer count which is specified in bytes. The transfer count for list processing must be in the two's complement form. The following table shows the format for the Enhanced Block Transfer Operation instruction:

TABLE 35 - Enhanced Block Transfer Operation

7	6	5	4	3	2	1	0	
0	1	0	QM2	QM1	WS2	WS1	AD	Byte 1
0	0	C32	C16	C8	C4	C2	C1	Byte 2
A4	A2	A1	F16	F8	F4	F2	F1	Byte 3
0	0	N16	N8	N4	N2	N1	A8	Byte 4
TC8	TC7	TC6	TC5	TC4	TC3	TC2	TC1	Byte 5
TC16	TC15	TC14	TC13	TC12	TC11	TC10	TC9	Byte 6
TC24	TC23	TC22	TC21	TC20	TC19	TC18	TC17	Byte 7
1	1	1	1	1	1	1	1	Byte 8

HALT Instruction

The HALT instruction is used to signify the end of a list-processing sequence. This is the only non-CAMAC instruction defined. The following table shows the format of the HALT instruction:

TABLE 36 - HALT Instruction Format

7	6	5	4	3	2	1	0	
1	0	0	0	0	0	0	0	Byte 1
0	0	0	0	0	0	0	0	Byte 2
0	0	0	0	0	0	0	0	Byte 3
0	0	0	0	0	0	0	0	Byte 4

List Processing Operation

The list processing operation begins with the list being sent over to the 2145. The list is transferred to the 2145 by using the LOAD LIST instruction. Refer to the LOAD LIST SCSI Command description for the format of the command.

The LOAD LIST command contains two bytes for the specification of the list load address. The valid address range for list processing memory is from 0 to 3FFF hex. This allows for approximately 32 Kilo-bytes of list storage. Care must be taken when loading the list, that the transfer count specification does not cause the 2145 to deposit list data over the 3FFF hex boundary.

The command list sent to the 2145 MUST have data transfers in the same direction. For example, the list MUST contain only CAMAC read operations or only CAMAC write operations. This limitation is only to those operations that require data transfer over the SCSI bus. Since the Single Write With In-Line Data instruction has its write data within the list, this instruction may reside in a CAMAC read list. Also, CAMAC control operations may be embedded anywhere in the list as long as they appear in the correct format.

Once the list is loaded, it is executed by using the EXECUTE LIST SCSI command. In this command, an address specification is used to inform the 2145 as to the initial address of list execution. This allows for multiple sub-lists to reside within the 2145. Again, this address specification must be in the address range of 0 to 3FFF hex. The EXECUTE LIST SCSI command format also requires that a transfer count be specified. This count is the total number of bytes that the 2145 will transfer over the SCSI bus during the execution of the list. This count includes only data transferred during the SCSI Data phase. Therefore, all individual block transfer counts and single transfer counts within the list must be totalled to obtain this number.

When list execution starts, the 2145 reads the first four elements starting at the address specified by the EXECUTE LIST instruction. The first and second are then loaded into the internal CAMAC Command Register of the 2145 and the third byte is placed in the Crate Address register. The fourth byte is then examined to determine the type of instruction. If the

instruction specified a HALT instruction, the 2145 terminates list processing and then sends a Status byte and COMMAND COMPLETE message. If the instruction specified is undefined, the 2145 sends a CHECK CONDITION status with the Sense Key set to 5, the Sense Code set to 80 hex, and the Sense Code Qualifier set to 4. If the instruction was a CAMAC operation, the internal word count and Mode Control registers are loaded and the CAMAC operation begins. After the CAMAC operation is complete, the status is examined. List processing continues if no errors were detected during the operation. If an error occurs, the 2145 switches to the Status phase and returns a CHECK CONDITION. The Sense Key is set to 0B hex, the Sense Code is set to 80 hex, and the Sense Code Qualifier is set to either 1 to 2. The qualifier is set to 1 for Single operations that terminated and set to 2 for Block Transfer operations.

List Processing Example

As an example, assume it is desired to read a two channel analog-to-digital converter (ADC) located in slot number 2. 1024 samples of the analog data are to be taken from each channel. The ADC module is accessed by the following commands:

F(2) A(0) -- Reads the digitized data. Q response of 1 indicates data is valid.

F(17) A(0) -- Selects the channel to be read.
Data = 1 selects channel 1.
Data = 2 selects channel 2.

F(24) A(0) -- Disables ADC conversions.

F(26) A(0) -- Enables ADC conversions.

For this application, an F(17)A(0) with data = 1 is first executed to select the desired channel. An F(26)A(0) is then executed to enable conversions. A Standard CAMAC Block Transfer operation is then executed in the Q-Repeat mode to read the 1024 converted samples. After the samples are read, an F(24)A(0) command is executed to disable the conversions. These steps are then repeated for channel 2.

For this example, the instruction list would appear as follows: (All data shown is in hex).

```
60 ┐
01 │
11 │  Single Write With In-Line Data / 24-Bit / Q-Stop / Abort Enable
04 │  C(1) N(2) F(17) A(0)
01 │  Data High = 0
00 │  Data Middle = 0
00 │  Data Low = 1
00 ┘

00 ┐  Single CAMAC Transfer / 24-Bit / Q-Stop / Abort Enable
01 │  C(1) N(2) F(26) A(0)
1A │
04 ┘
```

```
30 ┐
01 │  Conservative Block Transfer / 24-Bit / Q-Repeat / Abort Enable
02 │  C(1) N(2) F(2) A(0)
04 │  Transfer Byte Count = -(1024 * 4) = -4096
00 │
F0 │
FF │
FF ┘

00 ┐  Single CAMAC Transfer / 24-Bit / Q-stop / Abort Enable
01 │  C(1) N(2) F(24) A(0)
18 │
04 ┘

60 ┐
01 │  Single Write With In-Line Data / 24-Bit / Q-Stop / Abort Enable
11 │  C(1) N(2) F(17) A(0)
04 │  Data High = 0
02 │  Data Middle = 0
00 │  Data Low = 2
00 │
00 ┘

00 ┐  Single CAMAC Transfer / 24_bit / Q-Stop / Abort Enable
01 │  C(1) N(2) F(26) A(0)
1A │
04 ┘

30 ┐
01 │  Conservative Block Transfer / 24-Bit / Q-Repeat / Abort Enable
02 │  C(1) N(2) F(2) A(0)
04 │  Transfer Byte Count = -(1024 * 4) = -4096
00 │
F0 │
FF │
FF ┘

00 ┐  Single CAMAC Transfer / 24-Bit / Q-Stop / Abort Enable
01 │  C(1) N(2) F(24) A(0)
18 │
04 ┘

80 ┐  HALT Instruction
00 │
80 │
00 ┘
```

Timer Initiated List Execution

The 2145 provides an operating mode whereby a list of CAMAC commands can be repetitively executed at a predetermined rate. This rate is referred to as the tic rate. The 2145 supports 153 tic rates ranging from 10 microseconds to 4000 seconds.

The list of CAMAC commands for timer initiated list operations can only contain CAMAC read commands. CAMAC write commands may be embedded in the command list using the Single Inline Write instruction. As with any list, CAMAC control operations may also be placed in the list as long as data space is allocated to them.

All data acquired during the timer initiated list operations is stored in a large buffer. This buffer can contain a maximum of 4 megabytes of acquired CAMAC data. The buffer is used to "hold" a large amount of acquired CAMAC data which reduces the number of times a host

computer must connect to the 2145 to receive data. The buffer can be configured to its maximum size of 4 megabytes or as small as 4 bytes.

The CAMAC data buffer acts as a circular buffer. When a timer initiated operation is started, the received CAMAC data is stored starting at buffer address zero. As additional read data words are received, incremental locations of the buffer are filled. When the buffer address reaches its terminal value, which is specified by the Buffer End Address (BEA) specification in the START TIMER SCSI command, the address is reset to zero and subsequent CAMAC data words are again stored. This circular buffer scheme is used to obtain the CAMAC read data.

A programmable counter is provided which is used as a device for indicating when the 2145 has a buffer full of data to send back to the host computer. This counter is the Buffer Interval Counter (BIC). This counter is initially loaded with the data provided during setup time by the BIC specification in the START TIMER SCSI command. As CAMAC read data words are received by the 2145, this counter is decremented. When the counter reaches zero, the 2145 sets an internal flag called Buffer Full. When the Buffer Full flag is set, the host computer is allowed to read the acquired CAMAC read data. After this counter reaches zero, it is reloaded with the initial data provided at setup. Once the host computer starts reading the bufferred data, the Buffer Full flag is reset.

The CAMAC read data buffer is 32-bits wide. If the 2145 is executing 24-bit CAMAC operations, the 2145 places each 24-bit word into the buffer as each one is received. If 16-bit CAMAC words are used, the 2145 waits for two 16-bit words to be obtained from CAMAC before storing the data into the buffer. If an odd number of 16-bit words are specified for a particular CAMAC operation, a null word is placed into the buffer to ensure that the buffer always ends with an even number of 16-bit words. All specifications concerning the Buffer Interval Counter (BIC) and Buffer Ending Address (BEA) are 32-bit values. The Buffer Ending Address specification is actually a physical address at which the circular buffer rolls over. The value specifies the last location of the buffer which is accessed by CAMAC before the address is reset to zero. Valid entries for the Buffer Ending Address are 00001 through 0FFFFF hex. For example, if the entire buffer is to contain 10000 24-bit CAMAC data words, the BEA would be set to 270F hex. For 10000 16-bit CAMAC words, the BEA would be set to 1387 hex. The BIC specification value is the number of 32-bit values stored in the buffer by the CAMAC read circuitry before a the Buffer Full flag is set. For example, if the host requires readout after the 2145 has acquired 1000 24-bit CAMAC data words the BIC should be set to 1000 decimal (3E8 hex). If the readout required after obtaining 1000 16-bit words, the BIC should be set to 500 decimal (1F4 hex). For an odd number of 16-bit words, the BIC specification must be rounded up to the nearest whole number. For example, if the host requires readout after 501 16-bit CAMAC words, the BIC should be set to 251 decimal (FB hex).

The following diagram illustrates an example configuration in which the entire 4 megabytes (1 megaword) of the buffer is used. The buffer is set up such that the Buffer Full flag is set when the half of the buffer is filled.

For the above example, the Buffer Ending Address is set to FFFFF hex. This specification indicates that after the FFFFF hex address location is accessed that the address register be reset to zero. Therefore, after the 2145 has received 1048576 (100000 hex) 24-bit CAMAC read

data words, the address is reset to zero and buffer filling continues. For this example, the host computer should be allowed to read a block of acquired data when the buffer reaches the half full point. The number of 24-bit CAMAC words to be returned is 524288 (80000 hex). Therefore, the Buffer Interval Counter for this example must be set to 80000 hex. After the BIC is decremented to zero, the internal Buffer Full flag is set, which then allows the host computer to read the CAMAC data. After the flag is set, the BIC is reloaded with the original BIC specified during the START TIMER command. After the host computer starts to read out the CAMAC data, the Buffer Full flag is reset and acquisition continues.

As another example, assume it is desired to read 3800 16-bit words from a CAMAC module. The host computer should be able to readout the CAMAC data when the 2145 has accumulated 38000 16-bit words. For this example, the Buffer Interval Counter would be set to 38000 (9470 hex). Since this amount of data only points to the center of the data buffer, the Buffer Ending Address is the BIC value multiplied by 2, minus 1. Therefore, the BEA value for this example is 75999 (128DF hex).

When executing Timer Initiated Lists, an error may occur if the host computer cannot keep up with the acquisition rate of the 2145. If two Buffer Full conditions occur before the host computer tries to read the data from the initial Buffer Full, the 2145 will cease operation and return a CHECK CONDITION for any subsequent READ BLOCK commands.

SCSI Connectors

The signal allocation of the SCSI connectors is the same for both, so only one allocation is shown. The only difference is in the way the connector pins are numbered.

PIN 1 -- GROUND
PIN 2 -- GROUND
PIN 3 -- GROUND
PIN 4 -- GROUND
PIN 5 -- GROUND
PIN 6 -- GROUND
PIN 7 -- GROUND
PIN 8 -- GROUND
PIN 9 -- GROUND
PIN 10 -- GROUND
PIN 11 -- GROUND
PIN 12 -- RESERVED
PIN 13 -- OPEN
PIN 14 -- RESERVED
PIN 15 -- GROUND
PIN 16 -- GROUND
PIN 17 -- GROUND
PIN 18 -- GROUND
PIN 19 -- GROUND
PIN 20 -- GROUND
PIN 21 -- GROUND
PIN 22 -- GROUND
PIN 26 -- DATA(0)
PIN 27 -- DATA(1)
PIN 28 -- DATA(2)
PIN 29 -- DATA(3)
PIN 30 -- DATA(4)
PIN 31 -- DATA(5)
PIN 32 -- DATA(6)
PIN 33 -- DATA(7)
PIN 34 -- DATA(PARITY)
PIN 35 -- GROUND
PIN 36 -- GROUND
PIN 37 -- RESERVED
PIN 38 -- TERMINATOR POWER
PIN 39 -- RESERVED
PIN 40 -- GROUND
PIN 41 -- ATTENTION
PIN 42 -- GROUND
PIN 43 -- BUSY
PIN 44 -- ACKNOWLEDGE
PIN 45 -- RESET
PIN 46 -- MESSAGE
PIN 47 -- SELECT

Model 2145-Z1B

PIN 23 -- GROUND
PIN 24 -- GROUND
PIN 25 -- GROUND

PIN 48 -- COMMAND/DATA
PIN 49 -- REQUEST
PIN 50 -- INPUT/OUTPUT

Serial Highway Parameter Selection

The 2145 can transmit serial highway bytes of information in either the bit-serial or byte-serial mode. In bit-serial mode, the bytes are transmitted using one data signal and an accompanying bit-clock signal. The 8-bit byte is transmitted with the least significant bit first. It is proceeded by a Start bit (logic 0) and followed by a Stop bit (logic 1).

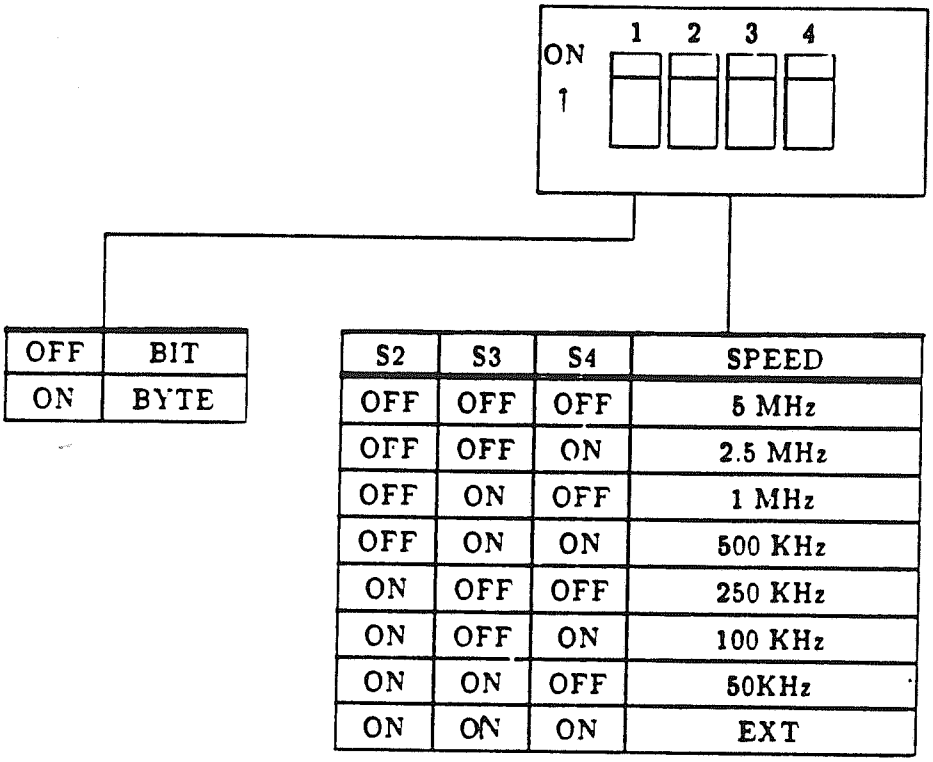
In the byte-serial mode, the bytes are transmitted using eight data signals and an accompanying byte-clock signal. The byte-serial mode increases serial highway data throughput by a factor of ten. A front panel switch selection allows the user to select either bit-serial or byte-serial highway modes. The user also has the ability to select a clock frequency at which the serial highway is to operate. Seven internal frequencies plus an external user supplied clock are front panel switch selectable.

If a 1736 or 1738 bit-serial U-Port adapter is included, S1 is set OFF (bit-serial). If a 1739 byte-serial U-Port adapter is included, S1 is set ON (byte-serial).

If a 1738 or 1739 fiber optic U-Port adapter is included, the normal clock frequency is 5 MHz with S2, S3, and S4 OFF. Frequency selection on the U-Port adapter must match that of the 2185 Serial Highway Driver. Refer to the U-Port Instruction Manual for frequency selection information.

When the 1730 D-Port or 1736 U-Port highway interface is used, the highway speed depends upon the cable type and length used for the highway.

The following chart shows the positions of the switches necessary to obtain the desired serial highway operating mode and speed.



S2	S3	S4	SPEED
OFF	OFF	OFF	5 MHz
OFF	OFF	ON	2.5 MHz
OFF	ON	OFF	1 MHz
OFF	ON	ON	500 KHz
ON	OFF	OFF	250 KHz
ON	OFF	ON	100 KHz
ON	ON	OFF	50KHz
ON	ON	ON	EXT

NOTE: User supplied external clock must be four times the desired highway clock frequency.

FIGURE 10 - Highway Mode and Speed Selection

SCSI Switch Selections

The 2145 may be configured at any one of eight SCSI logical addresses. The switches for this selection are located on the top card in the 2145 chassis. The following diagram shows the location of these switches.

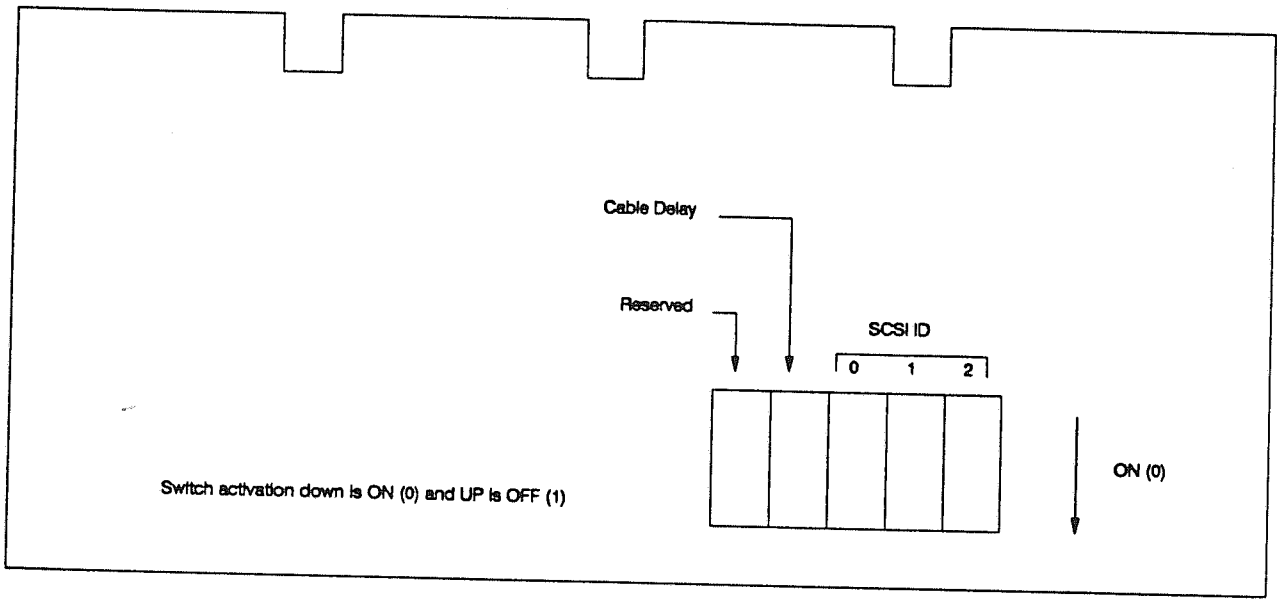


FIGURE 11 - 2145 SCSI Switch Locations

The SCSI ID switches 0, 1 and 2 are used to define the SCSI address. The following SCSI IDs are obtained as follows:

SCSI ID SWITCH 2	1	0	SCSI ID
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0 = ON = CLOSED			

The CABLE DELAY switch is used to increase the minimum data setup time on the SCSI bus. This should only be used when external cabling conditions cause intermittent SCSI timing

violations. Setting this switch OFF (1) enables the additional delay. This switch is normally set in the ON (0) position.

The Reserved switch is fro factory testing and MUST remain in the ON (0) position.

Execution Clock Connectors

This Serial Highway Driver includes an internal execution clock for acquiring blocks of data at precise intervals. This clock can be enabled, disabled, or an external clock selected under computer control. A single-pin (Type 00) LEMO connecter, designated EXEC CLK IN, is provided. This signal is TTL-level and terminated with a voltage divider (220 ohms to +5 volts and 330 ohms to ground) in the 2145. If external clock is selected and a list is armed, the list will be executed on a LOW-to-HIGH transition of the external clock. The external clock must be capable of sinking 30 milliamperes to ground and have a duty cycle in the range of 10 to 90 percent.

Strap Options

Pluggable straps on the Model 2145 logic modules allow the user to choose the following options:

PC304160 Receiver Card (D160)

Timeout Option - During Q-Repeat type operations, this option provides a hardware timeout if a Q-Response of 1 is never returned from the Serial Crate Controller (SCC).

Strap Positions

15S - 15 second timeout (Standard)
7S - 7 second timeout
DIS - Option is disabled

FIFO Word Packing Option - This strap reverses the way 16-bit words are packed into the Data FIFOs.

Strap Positions

2145	Words are packed as shown in the Register Description Chapter of this manual (Standard).
$\overline{2145}$	Non-standard packing (consult factory).

NOTE: This strap is factory configured and should not be moved by the user.

PC304161 Transmitter Card (D161)

Model 2145-Z1B

Increased Space Bytes - If an SCC requiring more space bytes than the KSC 3952 uses, installing this strap will increase the read and write command space bytes to 16.

Strap Positions

ISB - Installed = 16 space bytes

ISB - Not installed = variable number of space bytes depending on highway speed (Standard)

8, 32 Straps Command Memory Address for 8K or 32K memory chips

Strap Positions

8 - 8K Memory (Standard)
32 - 32K Memory (Memory chips must be changed)

Demands

The Model 3952 Serial Crate Controller (SCC) has the ability to alert the 2145 Enhanced Serial Highway Driver (ESHD) that a CAMAC LAM is pending by asynchronously generating and transmitting a Demand message on the serial highway. The contents of this message are stored in the 2145 ESHD's Demand FIFO. The Demand FIFO allows the 2145 ESHD to store up to 512 Demand messages. If the Demand Enable bit is set in the CSR, FP.EIR will pulse and cause an External Interrupt Message (EIM) to be sent to the processor. An interrupt routine, which resets the Demand Enable bit, reads one word from the Demand FIFO and then sets the Demand Enable bit, will interrupt the processor for each word in the Demand FIFO.

Unbypass and Loop Collapse Operations

When executing a Unbypass or Loop Collapse operation to a 3952, special restrictions apply. These two commands to the 3952 cause the serial highway to be momentarily broken. While the highway is "broken", random data is received by the 2145's serial highway receiver circuitry. This causes erratic operation of the receiver sequencer which results in erroneous activity. To prevent this, the 2145 must know in advance that one of these operations is to occur. To execute these operations successfully, follow the procedure below:

UNBYPASS Execute a selective-clear [F(23)] command to the 3952 with data = 4000_8.

LOOP
COLLAPSE Execute a selective-set [F(19)] command to the 3952 with data = 2000_8.

Front Panel Indicators

BUSY — Is a one-shot extended indication of the Command List being executed. BUSY is turned on when the Command List is triggered. BUSY is turned off when a Command List HALT instruction is executed or an Abort List condition occurs. BUSY is also turned off on power-up.

SYNC — This LED is normally on. It is off when the Serial Highway In Clock is not received (open highway) or when the receiver circuitry is not able to establish bit synchronization.

DMD — This LED is turned on when the Demand Message FIFO is not empty. DMD is turned off on power-up, when Demand FIFO is clear and when the FIFO is read empty.

STE — The Serial Transmission Error LED is on when parity errors are occurring on the Serial Highway.

/SQ — NOQ indicates that the last CAMAC operation executed resulted in a Q response of zero.

/SX — NOX indicates that the last CAMAC operation executed resulted in an X response of zero.

Row 2 — These seven LEDs are the seven least significant bits of the Command Mode byte. When an ABORT occurs, these bits will display the Mode byte of the aborted command.

ERROR — These four LEDs indicate the priority encoded result of the last attempt to execute a Command List. See the ERROR Status Register section for an explanation of each code. An ERROR code of one is the normal power-up state.

Front Panel Test Points

T CLK — Transmitter Clock is the Serial Highway Output Clock.

RCLK — Receiver Clock is the Serial Highway Input Clock. A signal at this test point which matches the frequency of T CLK is an indication that the serial highway is operating properly.

External Clock Input

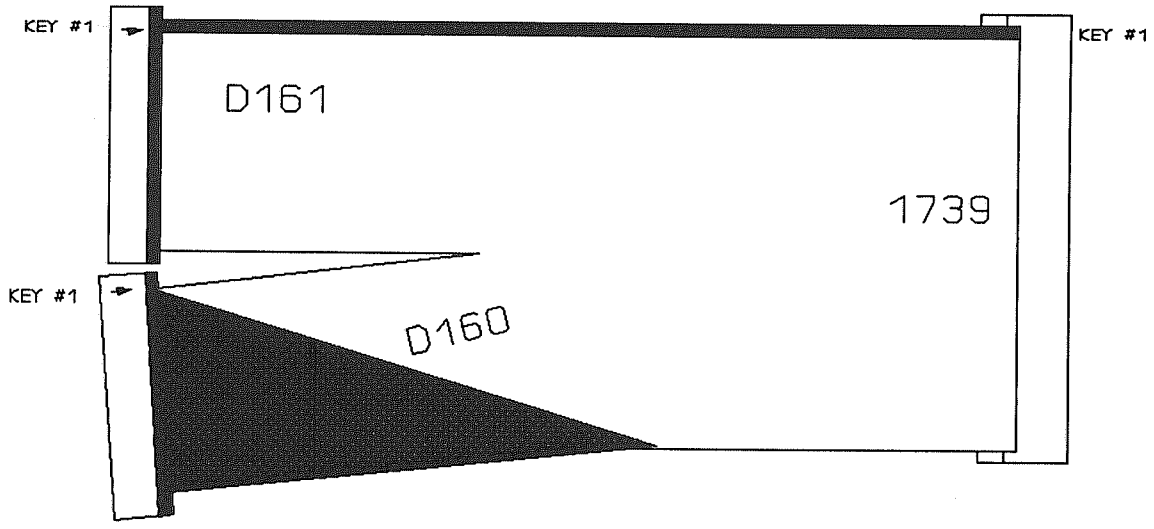
EXT CLK — Is a single pin LEMO connector which allows the user to provide the transmitter clock. The frequency of the external clock must be four times the frequency of the desired serial highway clock. When using the external clock with a U-Port option, make sure the frequency selection of the U-Port matches that of the transmitter clock.

Model 2145-Z1B

Power Supply

Power for the Model 2145 SHD logic circuits is supplied by a Power-one Map 80-4000 switching power supply with automatic 110/220 volt AC input selection. See the data sheet included in this section for complete specifications on this power supply.

2145 cable connections when using the 1739 U-Port



CBL10041

FEATURES

- 80/110 Watts Peak Power
- Four Outputs
- Automatic 110/220 Input Selection
- FCC & VDE EMI, Class "B" (conducted)
- Output Good/Power Fail Signal
- Fully Regulated, All Outputs
- Combination Terminal Block/Quick Disconnect Locking Wafer Connectors
- Two Year Warranty
- VDE, IEC, CSA & UL Safety Specs

DESCRIPTION

The MAP 80 Series is a 80W continuous with peak to 110W, high performance line of single and multiple output power supplies in 7.2" x 4.2" x 1.8" open frame chassis. Engineered with an "International" philosophy the MAP80 series gives the system designer the features that allow maximum flexibility. Features like Automatic AC input Selection, onboard FCC & VDE "B" filtering and power fail are all standard. The chassis accepts M4 or 6-32 screws and has .170" through holes at each corner for worldwide mounting. Universal input and output terminations are provided with Power-One's unique combination terminal block/quick disconnect locking wafer connectors.

INPUT

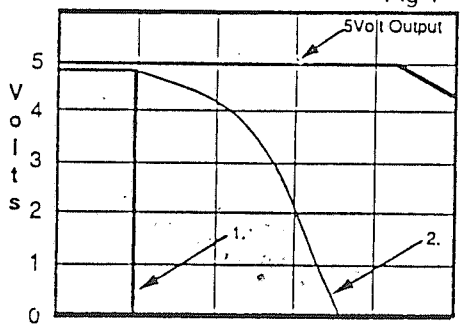
SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
P_{out}	Output Power	50 ° C Ambient convection cooled 50 ° C Ambient convection cooled, peak (2 minute)			80 110	Watts
V_{in}	Input Voltage	AC Input	90 175		135 264	VAC
Iin	Input current	Vin = 90VAC @ 80W		2.5		Arms
$I_{in\ pk}$	Inrush Surge Current	Vin = 264VAC Cold Start			45	Apk
f_i	Input Frequency	With AC input	47		63	Hz
t_{hu}	Hold Up Time	After last AC charge point with 115/230 VAC (80 watts)See Figure 6	20	-		msec
t_{pfw}	Input Power-Fail Warning	Logic signal before regulation circuit due to loss of input power. Internally pulled up to V1. Max sink current = 10mA. See Fig 1				msec
		V_1 @ 10A, V_2 @ 2.5A (80 Watts)	4			
		V_1 @ 1A (5 Watts)	70			
V_{pf}	Power Fail Trip Point	V_1 @ 10A, V_2 @ 2.5A, (80 Watts)		88.5		Volts
t_{ini}	Power up Initialization period	Cold start @ Full Load, 90VAC			5.0	sec
η	Efficiency	V_1 @ 10A, V_2 @ 2.5A (115 VAC)	73			%

All Measurements @ 25° C ambient unless otherwise noted.

DRAWING NO. 58818 REV G

Typical Power Fail Timing

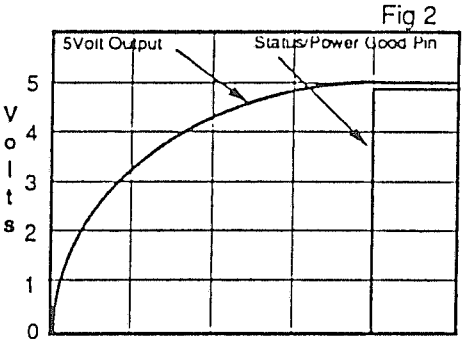
Fig 1



Time: 1ms/DIV

Typical Power Good Timing

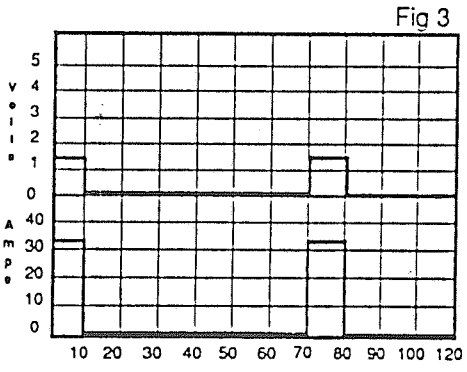
Fig 2



Time: 5ms/DIV

Typical Overload Characteristics

Fig 3



Time (ms)

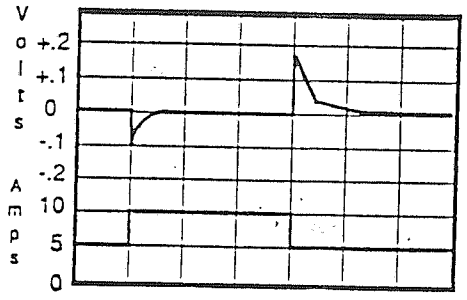
Typical Power Fail Signals
1. Full Load (80Watts)
2. Light Load (5Watts)

MAIN OUTPUT - V1 SPECIFICATION

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
V_o	Output Voltage			5		V
I_o	Output Current	At 50 ° C ambient	0		14	A
P_o	Output Power	At 50 ° C ambient			70	Watts
T_A	Ambient Temp Range		0		50	°C
V_o initial	Initial Voltage Setting	Factory Set	5.0		5.2	V
V_o adj	Output voltage Adj		4.0		5.8	V
$\frac{\Delta V_o}{V_o \Delta T_A}$	Temperature Coefficient	0 to 50 ° C. After initial 1 hour warm-up.			0.02	%/ °C
ΔV_o	Long Term Voltage Drift	1000 hours			0.3	%
Reg_{line}	Line Regulation	Over input operating range			0.2	%
Reg_{load}	Load Regulation	1-14 Amps			1	%
Reg_{cross}	Cross Regulation	Current Step From Min I_o to Max I_o on V_2, V_1 @ 6.4A		0.1		%
I_{omin}	Minimum Load Current		1			A
I_{omax}	Peak	30 Second Duration max duty ratio 10%			16	A
I_{osc}	Short Circuit Current	I_o during restart period See Fig 3		35		A
V_{ovp}	Overvoltage Protection	Trip voltage	5.6		6.8	V
e_n	Noise and Ripple	20 MHz BW (5 min warm-up)			50	mVpp
t_t	Transient Response Time	50% to 100% step, max overshoot ±150 mV. Recovering to within 1% of regulation band. See Fig 4			500	µs
$t_{d\ on}$	Turn-on Delay	Main Output after AC power (cold)			5	sec
t_r	Rise Time	5% to 95% of V_o , V_1 @ 14A See Fig 5			20	ms
t_{os}	Overshoot	Overshoot as a % of V_o - Startup			0	%

Typical Transient Response

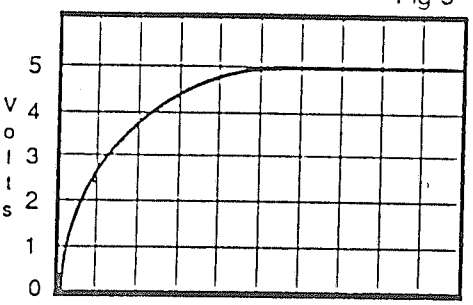
Fig 4



Time: .5 ms/DIV

Typical Rise Time

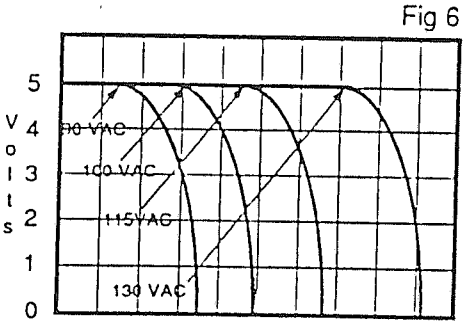
Fig 5



Time: 5ms/DIV

Typical Hold Up as a Function of VAC

Fig 6



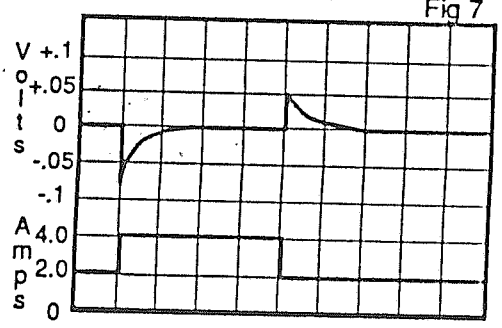
Time: 5ms/DIV

OUTPUT - V2 SPECIFICATION

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
V_o	Output Voltage			12		V
I_o	Output Current	At 50 ° C ambient			4	A
P_o	Output Power	At 50 ° C ambient			48	Watts
T_A	Ambient Temp Range		0		50	°C
V_o initial	Initial Voltage Setting	Factory Set	11.9		12.1	V
V_{oadj}	Output voltage Adj		10.2		13.5	V
$\frac{\Delta V_o}{V_o \Delta T_A}$	Temperature Coefficient	0 to 50 ° C. After initial 1 hour warm-up.			0.02	%/ °C
ΔV_o	Long Term Voltage Drift	1000 hours			0.3	%
Reg_{line}	Line Regulation	Over input operating range, V_1 = 5.2V @ 1.0A			0.2	%
Reg_{load}	Load Regulation	0 - 4 Amp, V_1 = 5.2V @ 1.0A			1	%
Reg_{cross}	Cross Regulation	Current step from Min I_o to Max I_o on V_1, V_2 @ 1A		0.1		%
I_{omin}	Minimum Load Current		0			A
I_{omax}	Peak	1 minute duration, max duty ratio 10%			7	A
I_{osc}	Short Circuit Current	I_o during restart period See Fig 3		18		A
e_n	Noise and Ripple	20 MHz BW (5 min warm-up)			120	mVpp
t_t	Transient Response Time	50% to 100% step, V_1 @ 5A, max overshoot ± 100mv. Recovering to within 1% of regulation band. (See Fig 7)			500	µs
$t_{d\ on}$	Turn-on Delay	After AC power is applied (cold)			5	sec
t_r	Rise Time	5% to 95% of V_o , V_1 @ 5A , V_2 @ 4A (See Fig 8)			20	ms
t_{os}	Overshoot	Overshoot as a % of V_o - Startup			0	%

Typical Transient Response

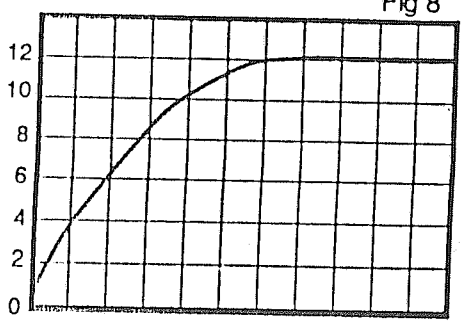
Fig 7



Time: .2ms/DIV

Typical Rise Time

Fig 8



Time: 2ms/DIV

OUTPUT V3 SPECIFICATION

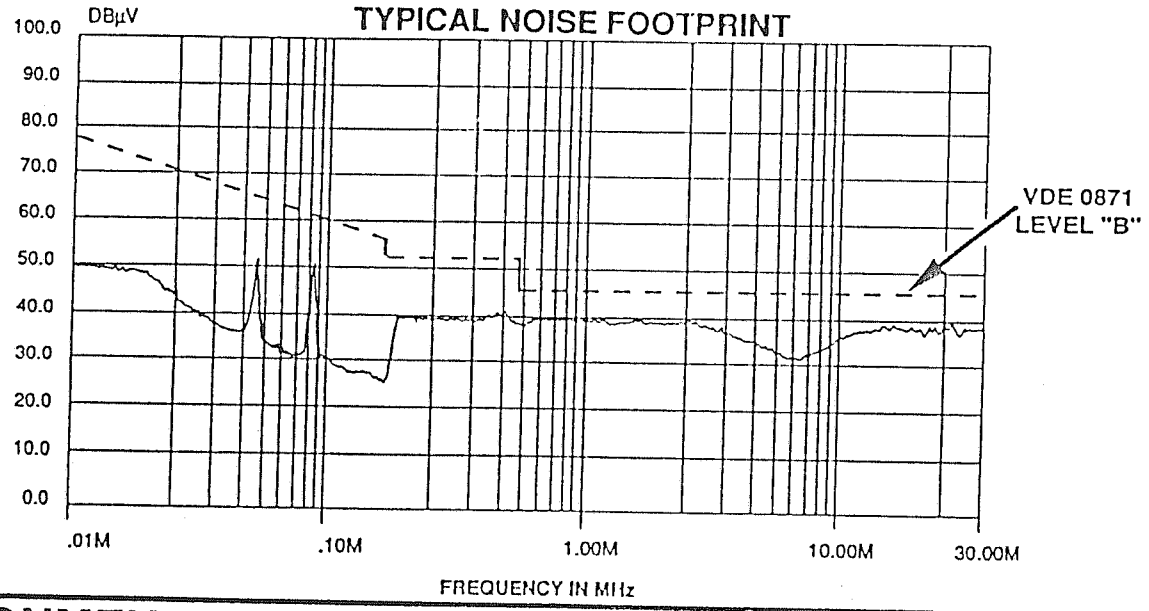
SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
V_o	Output Voltage			-5		V
I_o	Output Current	At 50°C ambient	0		1	A
P_o	Output Power	At 50°C ambient		5		Watts
T_A	Ambient Temp Range		0		50	°C
$V_{o\ initial}$	Initial Voltage Setting		-4.8		-5.2	V
$\frac{\Delta V_o}{\Delta T_A}$	Temperature Coefficient	0 to 50° C. After initial 1 hour warm-up.		1.5		mV/° C
Reg_{line}	Line Regulation	Over input operating range, V_1 = 5.2V @ 1.0A			0.5	%
Reg_{load}	Load Regulation	0 - 1 A , V_1 @ 1.0A			2	%
I_{omin}	Minimum Load Current		0			A
I_{osc}	Short Circuit Current				3	A
e_n	Noise and Ripple	20 MHz BW			50	mVpp
t_t	Transient Response Time	50% to 100% step Recovering to within 1% of regulation band.		50		µs

OUTPUT V4 SPECIFICATION

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
V_o	Output Voltage			-12		V
I_o	Output Current	At 50 ° C ambient	0		1	A
P_o	Output Power	At 50 ° C ambient		12		Watts
T_A	Ambient Temp Range		0		50	°C
$V_{o\ initial}$	Initial Voltage Setting		-11.6		-12.4	V
$\frac{\Delta V_o}{\Delta T_A}$	Temperature Coefficient	0 to 50 ° C After initial 1 hour warm-up		1.5		mV/ °C
Reg_{line}	Line Regulation	Over input operating range, V_1 = 5.2V @ 1.0A			0.5	%
Reg_{load}	Load Regulation	0 - 1A , V_1 = 5.2V @ 1.0A			2	%
I_{omin}	Minimum Load Current		0			A
I_{osc}	Short Circuit Current				3	A
e_n	Noise and Ripple	20 MHz BW			120	mVpp
t_t	Transient Response Time	50% to 100% step Recovering to within 1% of regulation band.		50		µs

SAFETY & EMI

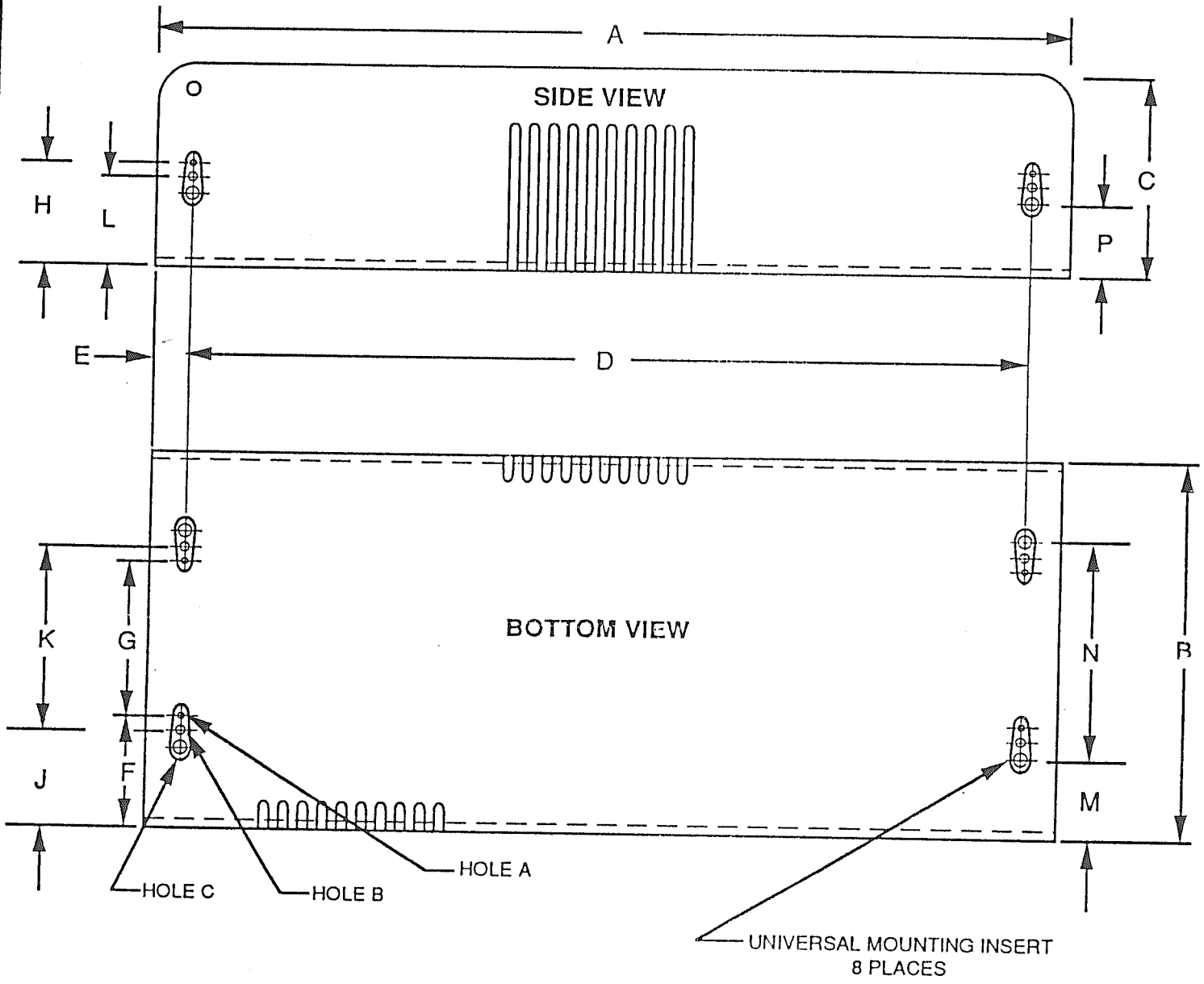
SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
	Agency Approvals	Class I, SELV STANDARDS UL478 (5th Edition) UL1950(D3) IEC 380, 950 (TUV) VDE 0806, 0805 (TUV) CSA 1402 (C) EN60950 (TUV)				
	Dielectric Withstand	Input to Output Input to Chassis Output to Chassis	1500 1500 500			Vrms/1 min Vrms/1 min Vrms/1 min
	Insulation Resistance	Input to Output Input to Chassis Output to Chassis	7 2 2			meg Ohm meg Ohm meg Ohm
	Leakage Current				500	µ Amps
	EMI Conducted	VDE 0871 (at 230VAC level B) FCC 47 CFR Part 15 (115/230VAC, level B)				



ENVIRONMENTAL

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
	Altitude	Operating Non-operating			10000 40000	Feet
	Temperature	Operating Non-operating	0 -40		+50 +85	°C
	Relative Humidity	Non-condensing	5		95	%
	Vibration	Per Mil. Std. 810D Methods 514.3 - 4 and 514.3 - 6				
	Weight				1.7	lbs.

MECHANICAL DIMENSIONS



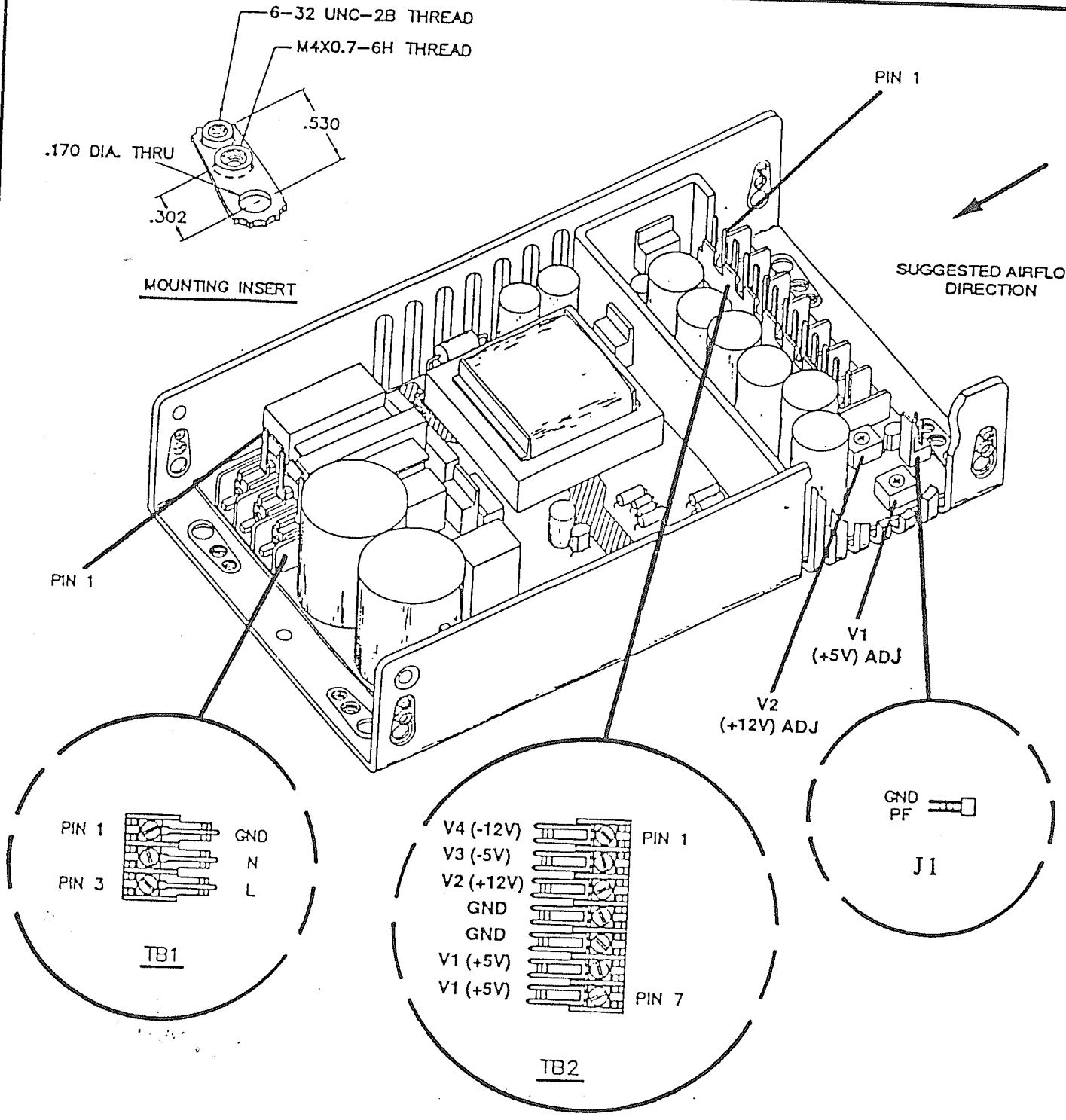
OVERALL SIZE: 7.20" X 4.200" X 1.80"
TOLERANCES: .XXX± . 010 (.254mm)
.XX ±.03 (.76mm)
WEIGHT: 1.7 LB., .771 KG.

DIM	IN	mm
A	7.200	182.880
B	4.200	106.680
C	1.800	45.720
D	6.700	170.180
E	.250	6.350

MOUNTING APPLICATION								
6-32 THREAD HOLE "A"			M4 THREAD HOLE "B"			.170 $^{+.003}_{-.000}$ DIA THRU HOLE "C"		
DIM	IN.	mm	DIM	IN.	mm	DIM	IN.	mm
F	1.015	25.781	J	0.787	19.9898	M	0.485	12.319
G	2.170	55.118	K	2.626	66.7004	N	3.230	82.042
H	1.040	26.416	L	0.812	20.6248	P	0.510	12.954

GENERAL

- TB1/TB2 MATES WITH MOLEX (Series 2139) .156" CENTER CRIMP TERMINAL HOUSING OR EQUIVALENT. ALSO ACCEPTS A SPADE TONGUE TERMINAL WITH A MAX WIDTH OF .255 FOR A NO. 6 STUD.
- J1 MATES WITH MOLEX (Series 2695) .100" CENTER CRIMP TERMINAL HOUSING OR EQUIVALENT.
- TORQUE RANGE FOR CUSTOM MOUNTING INSERT IS 7.5-8.5 INCH LBS.



POWER-ONE, INC.
740 CALLE PLANO CAMARILLO, CALIFORNIA 93010-8583 (805) 987-8741 TWX: 910-336-1297 FAX: (805) 388-0476