Model 2843-Z1A

PCI FIFO Interface

Instruction Manual

May, 1997

Contents

2843 Data Sheet

Features
- Complete Interface between PCI bus and KSC Front-Bus Crate Controllers
- Up to four Crate Controllers on a single bus
- Balanced RS-485 line signaling for high noise immunity
- Transfer rates up to 2.5 megabytes-per-second
- PCI interrupts for FIFO and bus status
- Mounts in any half-height PCI peripheral slot

Applications
- High speed data buffering between CAMAC and PCI bus
- Laboratory Automation
- Industrial Process Control

General Description

The Model 2843 is a computer bus adapter for use with computers incorporating the Peripheral Component Interconnect (PCI) local bus. This device is designed to accept data from devices such as the KineticSystems Model 3982-ZyB Auxiliary Crate Controllers. This configuration of a 2843 and 3982 allows data to be acquired from the 3982's Read Data FIFO register without making use of the CAMAC Dataway. Thus, the 3982 may continue to execute CAMAC I/O operations while at the same time the data is transferred to the host computer through the 2843.

The 2843 supports up to four Front-Bus compatible devices (3982s) via a 50-conductor twisted-pair ribbon cable. Data, strobe and handshake signals utilize RS-485 balanced transmission which yields high noise immunity and overall cable lengths of 90 meters (300 feet). Data transfers between the 3982(s) and the 2843 input FIFO can occur at a maximum rate of 2.5 megabytes-per-second. Interrupt sources within the 2843 include Receive FIFO Full, Receive FIFO Half-Full, Receive FIFO Empty, Transmit (i.e., the 3982's Read Data) FIFO Full, transmit FIFO Empty and several other status sources.

The 2843 uses a 32-bit data path to communicate with the PCI bus. Programmed transfers and Direct Memory Access (DMA) are provided for moving data from the 2843 input FIFO into host memory. The DMA transfers provide a speed efficient mechanism for moving data from the 2843 FIFO to host memory with very little software overhead. The 2843 also contains PCI configuration registers mandated by the PCI specification. These configuration registers permit the 2843 to be installed in a system without preselecting any address switches or straps.

INTERNAL REGISTERS

Address Offset	Register Description	Mnemonic	Write/Read Access
00_{16}	FIFO Data Register	FDR	Read-Only
04_{16}	Control Register	CTR	Write/Read
08_{16}	Status Register	STA	Read-Only
$0C_{16}$	Interrupt Mask Register	IMR	Write/Read
10_{16}	Interrupt Request Register	IRR	Read-Only

Power Requirements

+5 volts - 1800 mA

Ordering Information

Model 2843-Z1A - PCI FIFO Interface
Accessories - Model 3982-ZyB List Sequencing Auxiliary Crate Controller
- Model 5820-Series Front-bus Cable Assembly

Installation

The Model 2843 is designed to fit into any half-size PCI expansion slot. Before the installation is initiated, turn off the power to the computer and remove the power cord. Remove the cover to the computer and locate an empty expansion slot. Remove the blank plate from the mounting rail of the selected slot. Insert the 2843 into the slot and secure the mounting plate with the screw that was removed from the blank plate. Replace the cover on the computer and then plug the power cord back into the unit.

After the 2843 is installed into the host computer, connect one end of a 50-position twisted pair ribbon cable to the 2843. Please observe the keying indicators on the connectors and cable to ensure the connection is correct. Connect the other end of the ribbon cable to the 3982 Front Bus connector.

Apply power to both the CAMAC chassis with the 3982 and the host computer.

PCI Configuration Space

The PCI Specification mandates a 64-byte Configuration Header that describes the requirements of add-in cards. The data contained in this region uniquely identifies the device and allows for generic control of the device. The configuration data indicates the memory requirements of the device along with other device specific information.

This section describes the 64 bytes of configuration space implemented by the 2843. The following diagram is a composite chart showing the configuration header.

	31 16	15 00		
00	Device Identification	Vendor Identification		
04	Status	Command		
08	Class Code			Revision
0C	BIST	Header Type	Latency	Cache Size
10	Base Address Register #1			
14	Base Address Register #2			
18	Base Address Register #3			
1C	Base Address Register #4			

20	Base Address Register #5			
24	Base Address Register #6			
28	Reserved			
2C	Reserved			
30	Expansion ROM Base Address			
34	Reserved			
38	Reserved			
3C	Maximum Latency	Minimum Latency	Interrupt Pin	Interrupt Line

VENDOR IDENTIFICATION Field

The VENDOR IDENTIFICATION field contains read-only bits, which identify the manufacturer of the device. The ID assigned to KineticSystems is 11F4 Hex.

DEVICE IDENTIFICATION Field

The DEVICE IDENTIFICATION field contains read-only bits, which identify a particular device. The DEVICE ID field for this unit is 2843 Hex.

PCI COMMAND Register

The COMMAND field contains write/read bits used to configure basic PCI functions. The following diagram shows the COMMAND field as implemented by the 2843.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FST BTB	SER ENA	0	PER ENA	0	0	0	MAS ENA	MEM ENA	I/O ENA

<15:10> Not Used. These bits are not used and read as zeros.

<9> FAST BACK-TO-BACK is a write/read bit used to enable or disable the 2843 from executing "fast" back-to-back bus master cycles after completing a write cycle. Setting this bit to a one enables fast transfers and a zero disables the mode.

<8> SYSTEM ERROR ENABLE is a write/read bit used to enable and disable the 2843 from driving the PCI SYSTEM ERROR (SERR) signal. This signal is used by the 2843 to inform the host CPU of a parity error during an address

or control portion of a bus operation. Setting this bit to a one enables the 2843 to assert SERR and disabled with a zero.

<7> Not Used. These bits are not used and read as zeros.

<6> PARITY ERROR ENABLE is a write/read bit used to enable and disable the 2843 from driving the PCI PARITY ERROR (PERR) signal. This signal is asserted by the 2843 when a parity error is detected during a data transfer to/from the 2843. The PERR function is enabled by setting this bit to a one and disabled with a zero.

<5:3> Not Used. These bits are not used and read as zeros.

<2> BUS MASTER ENABLE is a write/read bit which enables and disables the 2843 from executing bus master operations. Setting this bit to a one enables the 2843 to function as a bus master and a zero disables the master operation.

<1> MEMORY SPACE ENABLE is a write/read bit that allows the 2843 to function in memory regions that may be defined in one of the base address registers. Since the 2843 is initially configured as an I/O device, this bit should be set to zero.

<0> I/O SPACE ENABLE is a write/read bit that allows the 2843 to function in I/O regions as defined in one of the base address registers. This bit is set to a one, which allows the 2843 to function in I/O regions.

PCI STATUS Register

The PCI STATUS Register is used to record status information regarding PCI bus transfers. This register contains read-only bits and write/read bits. The following diagram shows the Status Register bits implemented by the 2843.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR DET	SIG SER	RCV MAB	RCV TAB	SIG TAB	DEV TM1	DEV TM0	DP RPT	1	0	0	0	0	0	0	0

<15> DETECTED PARITY ERROR is a write/read bit, which is set whenever the 2843 detects a PCI parity error. This bit does not depend on the state of the PAR ENA bit in the PCI COMMAND Register. Once an error has been detected, this may be cleared by writing a one to bit position 15.

<14> SIGNALED SYSTEM ERROR is a write/read bit which is set whenever the 2843 asserts the PCI SYSTEM ERROR (SERR) signal. Once this bit is set, it may be cleared by writing a one to bit position 14.

<13> RECEIVED MASTER ABORT is a write/read bit which is set when the 2843 is accessed as a target and the master aborts the transaction. This bit can be reset by writing a one to this bit position.

<12> RECEIVED TARGET ABORT is a write/read bit which is set when the 2843, acting as a bus master, has initiated a transfer and the addressed target aborts the transfer. This bit can be reset by writing a one to this bit position.

<11> SIGNALED TARGET ABORT is a write/read bit that is set when a bus master accesses the 2843 as a target and the 2843 aborts the cycle. This bit is reset when a one is written to this bit location.

<10:9> DEVICE SELECT TIMING 1 and 0 encode the timing of the PCI DEVSEL (Device Select) signal. This time reflects the slowest time that a device asserts DEVSEL for any bus command except Configuration Read and Configuration Write. Since the 2843 may be accessed in the fast mode, these bits are set to zero.

<8> DATA PARITY REPORTED is a write/read bit, which is set when the 2843 detects a parity error when the 2843 is a bus master. This bit can be reset by writing a one to this bit position.

REVISION Field

The REVISION field contains read-only bits which reflect the current revision level of the 2843. The 2843 starts at revision one and subsequent revisions increment the number.

CLASS CODE Field

The CLASS CODE field actually contains three subfields that represent device characteristics. These three subfields are the BASE CLASS, the SUB-CLASS and the PROG I/F fields. These subfields define such parameters as network controllers, display controllers, video device, etc.

The 2843 does not fit into any of the defined class codes. Therefore, the class code that the 2843 uses is FF0000 Hex which indicates that the 2843 class code is undefined by the PCI specification.

CACHE LINE SIZE Field

The CACHE LINE SIZE field is used by the system to define the cache line size. The 2843 does not use Memory Write and Invalidate PCI bus cycles when operating as a bus master and therefore sets this field to zero.

LATENCY TIMER REGISTER

The LATENCY TIMER REGISTER is only used when the 2843 is operating as a bus master. The value loaded in this register is the minimum number of PCI bus clocks that the 2843 can be guaranteed as a master. After the 2843 becomes bus master and asserts the PCI FRAME signal, the Latency Timer is decremented for each PCI bus clock. Subsequent to the timer decrementing to zero, the 2843 ignores the PCI bus grant signal and continues to transfer data until the timer expires. The value loaded into this register is in multiples of eight clock cycles since the low 3 bits of this field are hardwired to zero. The value loaded into this register at power-up by the 2843 is F8 Hex.

HEADER Field

The HEADER field establishes whether a PCI device contains a single function or multi-function PCI bus agent. Since the 2843 contains only a single function, this field is set to zero.

BUILD IN SELF TEST Field

This field is used to present Built In Self Test diagnostic results to a bus master. The 2843 does not implement BIST and returns a zero for this field.

BASE ADDRESS REGISTERS

The BASE ADDRESS REGISTERS are used to specify the memory or I/O requirements of add-in devices and also to configure the base addresses of these devices.

After power-up, system software can determine how much address space a particular device requires by writing all ones to a base address register and then reading the value back. The device returns zeros in all address bit locations that do not define the base address.

The least significant bit in each of the base address registers is used for specifying the region of address space for which the device is to reside. A value of zero specifies a memory region and a value of one specifies an I/O region. The 2843 is configured to operate in the I/O region.

The 2843 implements two of the Base Address registers. The first Base Address register is used to communicate with the PCI Interface Operational Registers (IOR) and the second is used to communicate with the FIFO Interface Operational Registers (FIOR). The Interface Operational Registers require 16 longwords (64 bytes) of address space. A read of the first base address register after a write of all ones returns the value FFFFFFC1 Hex, indicating a request for 16 longwords of I/O space.

The FIFO Interface Operational Registers require 8 longwords (32 bytes) of address space. A read of the second base address register after a write of all ones returns the value FFFFFFF1 Hex, indicating a request for 8 longwords in I/O space.

After the system software has determined the total address space requirements of the system, it assigns the base addresses to memory and I/O devices by writing their Base Address Registers.

EXPANSION ROM BASE ADDRESS Register

This field is used to assign a physical memory address to expansion ROM in a system. The 2843 does not contain an expansion ROM and therefore does not require use of this field.

INTERRUPT LINE Field

This write/read field is used for communicating interrupt routing information and is configured by the PCI BIOS after power-up. The value in this field informs the system interrupt controller as to which line of the controller the interrupt is connected.

INTERRUPT PIN Field

The INTERRUPT PIN field is read-only and specifies as to which PCI interrupt pin that the 2843 is connected. The 2843 returns a value of one in this field indicating that it uses the INTA interrupt.

MINIMUM GRANT Register

This write/read register is used by bus masters to specify the minimum amount of time the device needs for a period of burst transfers. Since the 2843 does not have this requirement, a value of zero must be used.

2843 Interface Registers

The 2843 Interface Registers are composed of two sets of Interface Registers. The first set, the PCI Interface Operational Registers, is used to configure and monitor the registers inside the PCI Interface chip. This chip is used to configure and monitor DMA operations. This set of registers is defined by Base Address Register #1 from the PCI Configuration Block. The second set of registers, the FIFO Interface Operational Registers, is used to control and monitor various aspects of the FIFO buffer on the 2843. This includes FIFO buffer setup/control and interrupt control. This set of registers is defined by Base Address Register #2 from the PCI Configuration Block.

PCI Interface Operational Registers

The PCI Interface Operational Registers are contained in the PCI interface chip used on the 2843. This chip is the S5933 and is manufactured by Applied Micro Circuits Corporation. The base address of these registers is loaded by power-on BIOS routines and is contained in the Base Address Register #1 location of the PCI Configuration Registers.

Note: All references to Incoming and Outgoing are referred to the host. An Outgoing operation is a write operation from the host and an Incoming operation is a read operation from the 2843.

The following chart shows the various PCI Interface Registers along with their offsets from the base address.

Offset	Register	Access	
0	Outgoing Mailbox #1	W/R	*
4	Outgoing Mailbox #2	W/R	*
8	Outgoing Mailbox #3	W/R	*
C	Outgoing Mailbox #4	W/R	*
10	Incoming Mailbox #1	R	*
14	Incoming Mailbox #2	R	*
18	Incoming Mailbox #3	R	*
1C	Incoming Mailbox #4	R	*
20	Data FIFO	W/R	
24	Master Write Address	W/R	
28	Master Write Transfer Count	W/R	
2C	Master Read Address	W/R	*
30	Master Read Transfer Count	W/R	*
34	Mailbox Empty/Full Status	W/R	*
38	Interrupt Control/Status	W/R	
3C	Bus Master Control/Status	W/R	

* These registers are found in the PCI Interface Controller but not used by the 2843.

Outgoing/Incoming Mailboxes

The Incoming and Outgoing Mailboxes are not used by the 2843.

Data FIFO Register

The Data FIFO Register is a write/read register located at an offset of 20 hex from the selected base address register #1 and is composed of two 8 x 32- bit FIFOs located in the PCI interface chip. When executing FIFO buffer operations under DMA, all data collected from the front-bus device is captured by these FIFOs. Data transfers to or from these FIFOs can be done by either programmed transfers executed by the host or by allowing the 2843 to become a bus master and transfer the data.

Several status indicators are provided which indicate the amount of data contained in the PCI interface chip FIFOs. The Bus Master Control/Status register contains 6 status bits that correspond to the PCI Interface chip internal FIFOs.

Note that when DMA operations are used, the front bus data is stored in the FIFO Data Register at offset 0 from the FIFO Interface Operational Registers.

Master Write Address Register

The Master Write Address Register is a write/read register located at an offset of 24 hex from the selected base address #1 and is used to specify the initial address accessed by the 2843 during DMA transfers from the 2843 to the PCI memory. A read of this register contains the last address that was accessed during a bus master write operation executed by the 2843. This address is actually pointing to one longword beyond the last address accessed since the memory address is incremented after each execution of a data transfer. All DMA transfers must begin on a longword boundary. The following diagram shows the bit pattern for the Master Write Address Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MWAR 31	MWAR 30	MWAR 29	MWAR 28	MWAR 27	MWAR 26	MWAR 25	MWAR 24	MWAR 23	MWAR 22	MWAR 21	MWAR 20	MWAR 19	MWAR 18	MWAR 17	MWAR 16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MWAR 15	MWAR 14	MWAR 13	MWAR 12	MWAR 11	MWAR 10	MWAR 09	MWAR 08	MWAR 07	MWAR 06	MWAR 05	MWAR 04	MWAR 03	MWAR 02	0	0

<31:2> MASTER WRITE ADDRESS 31 through 2 are write/read bits used to specify the initial DMA address during block transfer operations. Reading this register returns the last address accessed during a DMA operation.

<1:0> These bits are not used since the DMA operations execute longword (32-bit) transfers.

Master Write Transfer Count Register

The Master Write Transfer Count Register is a write/read register located at an offset of 28 hex from the selected base address #1 and is loaded with the number of bytes to transfer from the 2843 to PCI memory during a DMA operation. This counter is decremented by four for every PCI bus cycle executed, since the 2843 transfers only 32-bit data words during DMA. When this counter is decremented to zero, the DMA operation terminates and an interrupt may be optionally generated to the PCI bus. The following diagram shows the bit pattern for the Master Write Transfer Count Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	MWTC 25	MWTC 24	MWTC 23	MWTC 22	MWTC 21	MWTC 20	MWTC 19	MWTC 18	MWTC 17	MWTC 16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MWT MWTC 15	MWTC 14	MWTC 13	MWTC 12	MWTC 11	MWTC 10	MWTC 09	MWTC 08	MWTC 07	MWTC 06	MWTC 05	MWTC 04	MWTC 03	MWTC 02	MWTC 01	MWTC 00

<31:26> These bits are not used and read as zeros.

<25:00> MASTER WRITE TRANSFER COUNT 31 through 0 are write/read bits used to specify the maximum number of bytes to transfer from the 2843 to PCI memory during DMA operations.

Master Read Address Register

The 2843 does not use this register since DMA operations always occur from the 2843 to PCI memory.

Master Read Transfer Count Register

The 2843 does not use this register since DMA operations always occur from the 2843 to PCI memory.

Mailbox Empty/Full Status Register

This register is not used by the 2843 but is shown here for completeness.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IMB 4D	IMB 4C	IMB 4B	IMB 4A	IMB 3D	IMB 3C	IMB 3B	IMB 3A	IMB 2D	IMB 2C	IMB 2B	IMB 2A	IMB 1D	IMB 1C	IMB 1B	IMB 1A
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OMB 4D	OMB 4C	OMB 4B	OMB 4A	OMB 3D	OMB 3C	OMB 3B	OMB 3A	OMB 2D	OMB 2C	OMB 2B	OMB 2A	OMB 1D	OMB 1C	OMB 1B	OMB 1A

PCI Interface Interrupt Control/Status Register

The PCI Interface Interrupt Control/Status Register of the PCI Interface Operational Registers is located at an offset of 38 hex from the selected base address #1 and used to monitor and control interrupts generated by the PCI interface chip. Before an interrupt is sourced from the interface chip to the PCI bus, it must be enabled with the PCI INTERRUPT MASK bit in the Interrupt Mask Register of the FIFO Interface Operational Registers.

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The following shows the bit pattern for the Interrupt Control/Status Register of the PCI Interface Operational Registers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	INT REQ	0	TAR ABT	MAS ABT	RTC	WTC	IMB SRC	OMB SRC
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RTC IE	WTC IE	0	IMB IE	IMB EMB	IMB EMA	IMB EBB	IMB EBA	0	0	0	OMB IE	OMB EMB	OMB EMA	OMB EBB	OMB EBA

<31:24> These 8 bits control endian conversion and must be set to zero for the 2843 to operate properly.

<23> INTERRUPT REQUEST is a read-only bit that is set when the PCI interface chip is requesting service. This bit reflects the interrupt output of the PCI chip and does not indicate that the PCI bus interrupt is asserted. If the PCI Interrupt Enable bit of the Interrupt Control/Status Register of the Highway Operational Registers is set to a one, this bit indicates that a PCI bus interrupt is requested.

<22> This bit is not used and read as a zero.

<21> TARGET ABORT is a read/write-to-clear bit that indicates when the 2843 executes a bus master transfer and the addressed target aborts the transfer. An interrupt source is generated when this bit is set. This bit is cleared by writing a one to this bit position.

<20> MASTER ABORT is a read/write-to-clear bit that indicates when the 2843 executes a bus master operation and the addressed target does not respond. An interrupt source is generated when this bit is set. A write operation to this register with this bit set to a one clears the bit.

<19> READ TRANSFER COMPLETE is a read/write-to-clear bit that is set when the Master Read Transfer Count Register is decremented to zero. Since the 2843 only executes memory writes, this bit is not used.

<18> WRITE TRANSFER COMPLETE is a read/write-to-clear bit that is set when the Master Write Transfer Count Register is decremented to zero.

<17> INCOMING MAILBOX INTERRUPT SOURCE is a read/write-to-clear bit that is set to a one when the mailbox selected by bits 12 through 8 of this register are written. Since the 2843 does not use the mailbox registers, this bit should not be set.

<16> OUTGOING MAILBOX INTERRUPT SOURCE is a read/write-to-clear bit that is set to a one when the mailbox selected by bits 4 through 0 of this register is read. Since the 2843 does not use the mailbox registers, this bit should not be set.

<15> READ TRANSFER COMPLETE INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of an interrupt when the read transfer count is exhausted. Since the 2843 only executes memory write operations, this bit is not used.

<14> WRITE TRANSFER COMPLETE INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of an interrupt when the write transfer count is exhausted.

<13> This bit is not used and read as a zero.

<12> INCOMING MAILBOX INTERRUPT ENABLE is a write/read bit that is used to enable/disable the generation of an interrupt source when a preselected incoming mailbox register is written. Bits 11 through 8 of this register select which mailbox register write operation will generate the interrupt source.

<11:10> INCOMING INTERRUPT SELECT bits are used to select which incoming mailbox write operations are to generate an interrupt source. Since the 2843 does not used the mailbox registers, these bits should be set to zero.

<9:8> INCOMING MAILBOX BYTE INTERRUPT SELECT bits are used to select which byte of the mailbox, selected by bits 11 and 10 of this register, is actually to cause the interrupt source. Since the 2843 does not used the mailbox registers, these bits should be set to zero.

<7:5> These bits are not used and read as zeros.

<4> OUTGOING MAILBOX INTERRUPT ENABLE is a write/read bit that is used to enable/disable the generation of an interrupt when a preselected outgoing mailbox register is written. Since the 2843 does not used the mailbox registers, these bits should be set to zero.

<3:2> OUTGOING INTERRUPT SELECT bits are used to select which outgoing mailbox write operations are to generate an interrupt source. Since the 2843 does not used the mailbox registers, these bits should be set to zero.

<1:0> OUTGOING MAILBOX BYTE INTERRUPT SELECT bits are used to select which byte of the mailbox, selected by bits 3 and 2 of this register, is actually to cause the interrupt source. Since the 2843 does not used the mailbox

used the mailbox registers, these bits should be set to zero.

Bus Master Control/Status Register

The Bus Master Control/Status Register is used to monitor/control bus master operations and to check status of the two PCI interface chip FIFOs. The following diagram shows the bit pattern for the Bus Master Control/Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	MBX RST	INF RST	OTF RST	AON RST	0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
0	RDT ENA	0	0	0	WTT ENA	0	0	ITC ZERO	OTC ZERO	IFE MT	IFI 4+	IFI FUL	OTF MT	OTF 4+	OTF FUL

The bits shown as zeros in the preceding bit layout must be set to zeros when writing to the Bus Master Control/Status Register. The bits that have non-zero indications are the only useful bits in this register. The remaining bits are reserved for diagnostic purposes. Even though some of these bits are shown as zeros, they may eventually be read as ones. Note that the Inbound FIFO refers to the internal PCI controller interface chips' FIFO for executing read operations from the FIFO on the 2843 directed towards the PCI memory.

<31:28> These bits are not used but must be written to zero.

<27> MAILBOX FLAG RESET is a write-only bit which resets all of the mailbox status flags.

<26> INBOUND FIFO RESET is a write-only bit which clears the inbound FIFO, Inbound FIFO +4 bit, Inbound FIFO Full and sets the Inbound FIFO Empty flag.

<25> OUTBOUND FIFO RESET is a write-only bit which clears the outbound FIFO, Outbound FIFO +4 bit, Outbound FIFO Full and sets the Outbound FIFO Empty bit.

<24> ADD-ON RESET is a write-only bit which, when set to a one, resets all of the FIFO Interface Operational Registers.

<23:14> These bits are not used but must be written to zero.

<13:11> These bits are not used but must be written to zero.

<10> WRITE TRANSFER ENABLE (WTT ENA) is a write/read bit used to enable DMA operations from the 2843 to PCI memory for FIFO read operations. Setting this bit to a zero before the transfer count expires suspends the active

transfer.

<09:08> These bits are not used but must be written to zero.

<07> INBOUND TERMINAL COUNT ZERO (ITC ZERO) is a read-only bit that is set to a one indicating that the Master Write Transfer Count is zero.

<07> OUTBOUND TERMINAL COUNT ZERO (OTC ZERO) is a read-only bit that is set to a one indicating that the Master Read Transfer Count is zero. This bit is not used by the 2843 since only PCI memory writes are executed.

<5> INBOUND FIFO EMPTY is a read-only bit which is set when the inbound FIFO contains no data.

<4> INBOUND FIFO +4 is a read-only bit and is set to a one as long as there are at least 4 longwords of data in the inbound FIFO.

<3> INBOUND FIFO FULL is a read-only bit that is set when the incoming FIFO is full.

<2> OUTBOUND FIFO EMPTY is a read-only bit which is set when the outbound FIFO contains no data.

<1> OUTBOUND FIFO +4 is a read-only bit and is set to a one as long as there are at least 4 longwords of data in the outbound FIFO.

<0> OUTBOUND FIFO FULL is a read-only bit that is set when the outbound FIFO is full.

FIFO Interface Operational Registers

The following section describes the registers used to control and monitor operations directed toward the front bus readout of the 3982 List Sequencing Auxiliary Crate Controller. The base address of these registers is set dynamically when the computer is powered-up and the BIOS routines are executed. The PCI BIOS determines the resources required by each PCI device and allocates memory and I/O resources accordingly. After the setup has been completed, the Base Address Register #2 from the PCI Interface Registers may be read to determine the base address allocated to the 2843 FIFO Interface Operational Registers by the PCI BIOS.

The following chart shows the various registers used to monitor and control the FIFO Interface operations.

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Address Offset	Register Description	Mnemonic	Write/Read Access
00_{16}	FIFO Data Register	FDR	Read-Only
04_{16}	Control Register	CTR	Write/Read
08_{16}	Status Register	STA	Read-Only
$0C_{16}$	Interrupt Mask Register	IMR	Write/Read
10_{16}	Interrupt Request Register	IRR	Read-Only

FIFO Data Register

The FIFO Data Register is a read-only register located at an offset of 00_{16} from the allocated base address of the 2843. This register is used to retrieve data read from the 3982 List Sequencing Auxiliary Crate Controller (LSACC). This register is a port to a 2048 x 16 First-In-First-Out Memory. The FIFO can hold up to 2048 16-bit CAMAC data words or 1024 24-bit CAMAC data words. A specification within the Control Register of the 2843 controls the CAMAC data word size. The following diagrams show the storage in the FIFO register for both 16 and 24-bit CAMAC data words.

This diagram shows the 16-bit storage format where a 16-bit CAMAC data word occupies one FIFO storage location. This storage mode is selected when the WS bit in the Control Register is set to one.

	15 00
First	CAMAC Data Word #1
Second	CAMAC Data Word #2
Third	CAMAC Data Word #3
Fourth	CAMAC Data Word #4
Fifth	CAMAC Data Word #5
Sixth	CAMAC Data Word #6

This diagram shows the 24-bit storage format where a 24-bit CAMAC data word occupies two FIFO storage locations. This storage mode is selected when the WS bit in the Control Register is set to zero.

	15 00
First	CAMAC Data Word #1 LO
Second	CAMAC Data Word #2 HI
Third	CAMAC Data Word #3 LO
Fourth	CAMAC Data Word #4 HI
Fifth	CAMAC Data Word #5 LO
Sixth	CAMAC Data Word #6 HI

The FIFO contents may be cleared by setting the RST FIFO bit in the Control Register of the 2843. This bit causes the internal pointers of the FIFO to be reset indicating a FIFO EMPTY condition.

The FIFO Data Register can be read by I/O accesses to the 2843. Before the FIFO Data Register is read, the RFIFO EMPTY bit in the Status Register must be examined. If the RFIFO EMPTY bit is set to a one, the FIFO Data Register does not contain any data and therefore should not be read. Reading the FIFO Data Register while it is empty results in indeterminate data. If the RFIFO EMPTY bit in the Status Register is set to a zero, the FIFO Data Register is not empty and may be read. Please refer to the previous two diagrams that illustrate the data storage as the FIFO is read.

A more efficient mechanism to retrieve the data from the FIFO is to allow the 2843 to execute Direct Memory Access (DMA) to store the data into the host memory automatically. This eliminates the need for the host computer to continually poll the RFIFO EMPTY bit in the Status Register for each access to the FIFO Data Register. Please refer to the Direct Memory Access section of this manual for additional information.

The following diagram shows the bit pattern for the FIFO Data Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FDR 15	FDR 14	FDR 13	FDR 12	FDR 11	FDR 10	FDR 9	FDR 8	FDR 7	FDR 6	FDR 5	FDR 4	FDR 3	FDR 2	FDR 1	FDR 0

Bit(s)	Mnemonic	Description
<31:16>	Not Used	These bits are not used and read as zeros.
<15:0>	FDR15-0	FIFO Data Register 15 through 0 are read-only bits used to read CAMAC data words retrieved from the 3982.

Control Register

The Control Register is a write/read register located at an offset of 04_{16} from the allocated base address of the 2843. This register is used to setup and enable various features of the 2843. Several enable/disable bits are found in this register to enable overall interrupt requests, enable CAMAC data to move from the 3982 to the 2843 FIFO, and to enable DMA transfers. The following diagram shows the bit layout for the Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	WS	0	0	DMA ENA	AD 1	AD 0	INT ENA	FIFO CLR	FIFO ENA

Bit(s)	Mnemonic	Description
<31:9>	Not Used	These bits are not used and read as zeros.

<8>	WS	WORD SIZE is a write/read bit used to determine the format for data storage in the FIFO. Setting this bit to a zero selects 24-bit CAMAC data words and a one selects 16-bit CAMAC data words. 16-bit CAMAC data words require one storage location in the FIFO and 24-bit CAMAC data words require two locations.
<7:6>	Not Used	These bits are not used and read as zeros.
<5>	DMA ENA	DMA ENABLE is a write/read bit used to enable/disable movement of data from the FIFOs located on the 2843 to host memory. Setting this bit to a one enable the DMA activity and a zero disables DMA. Please refer to the DMA section of this manual for additional information.
<4:3>	AD1-0	FRONT BUS ADDRESS 1 and 0 are write/read bits used to select which 3982 is addressed during a front bus readout operation. These two bits allow up to four 3982's to reside on a single bus. These bits should only be altered while front bus readout activity is disabled. Changing these bits while readout is enabled can result in erroneous behavior.
<2>	INT ENA	INTERRUPT ENABLE is a write/read bit used to enable/disable the 2843 from generating a PCI interrupt request. In order for the 2843 to generate a PCI interrupt request, this bit must be set to a one. Setting this bit to a zero prevents the 2843 from asserting a PCI interrupt request.
<1>	FIFO CLR	FIFO CLEAR is a write-only bit used to clear the FIFOs on the 2843. Writing this bit location to a one causes the FIFOs to be reset. After the FIFOs are reset, the RFIFO EMPTY bit is set to a one. This bit is not latched and is read as a zero.
<0>	FIFO ENA	FIFO ENABLE is a write/read bit that is used to enable/disable the movement of data from the 3982 to the 2843. Setting this bit to a one enables the transfer of data from the 3982 to the 2843 FIFO. Data transfers continue as long as there is room in the 2843 FIFO for data and the 3982 contains data to be moved. The transfer of data ceases once the FIFO ENABLE bit is set to a zero.

Status Register

The Status Register is a read-only register located at an offset of 08_{16} from the allocated base address of the 2843. This register is used to monitor various status bits reflecting conditions on the 2843 and the 3982. These bits indicate FIFO status on the 2843, FIFO status on the 3982, and execution status of the 3982. The following diagram shows the bit pattern for the Status Register.

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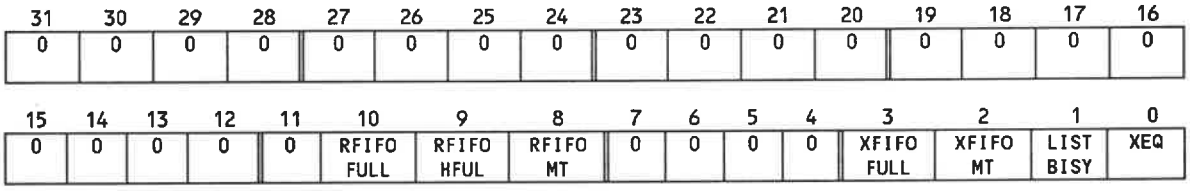
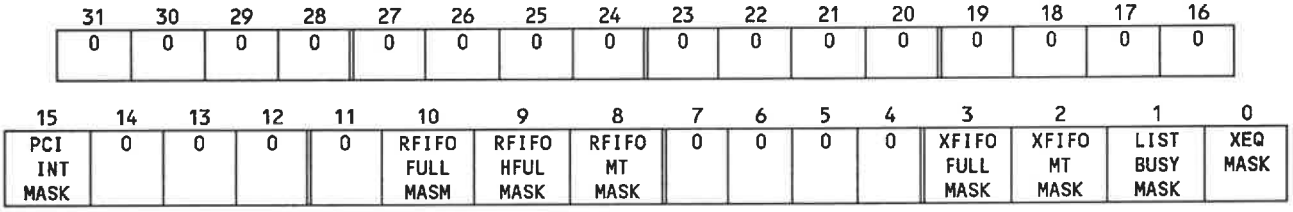


Bit(s)	Mnemonic	Description
<31:11>	Not Used	These bits are not used and read as zeros.
<10>	RFIFO FULL	RFIFO FULL is a read-only bit which is set to a one when the FIFO on the 2843 contains 2048 elements. When this FIFO is full, no additional data is transferred from the 3982 to the 2843 until a data word is removed from the FIFO. This bit is reset to zero as long as there is less than 2048 elements in the FIFO.
<9>	RFIFO HFUL	RFIFO HALF FULL is a read-bit which is set to a one when the FIFO on the 2843 contains at least 1024 elements. This bit is reset to zero if the FIFO contains less than 1024 elements.
<8>	RFIFO MT	RFIFO EMPTY is a read-only bit which is set to a one when the FIFO on the 2843 contains no data. When the FIFO is empty, the RFIFO EMPTY bit will be reset to zero as soon as a data word is transferred from the 3982 to the 2843.
<7:4>	Not Used	These bits are not used and read as zeros.
<3>	XFIFO FULL	XFIFO FULL is a read-only bit that is set to a one when the read data FIFO on the addressed 3982 is full. This full indication will be set at various times depending on the size of the FIFOs on the 3982 being addressed. Please refer to the 3982 manual for the details on the amount of read data FIFO memory on the addressed module. The XFIFO FULL bit is reset to zero as long as the read data FIFO on the addressed 3982 is not full.
<2>	XFIFO MT	XFIFO EMPTY is a read-only bit that is set to a one when the read data FIFO on the addressed 3982 does not contain any data. When this FIFO is empty, no front bus readout operations may occur to the addressed 3982. The XFIFO EMPTY bit is reset to zero as soon as the addressed 3982 executes a valid CAMAC read

		operation that causes a CAMAC data word to be stored in the 3982's read data FIFO.
<1>	LIST BUSY	LIST BUSY is a read-only bit that is set to a one as long as the addressed 3982 is busy executing a list of CAMAC commands. Once the list of commands has been executed and the 3982 ceases dataway activity, this bit is then reset to zero.
<0>	XEQ	XEQ is a read-only bit that is set to a one as long as the addressed 3982 is enabled for list execution. Reading this bit set to a one does not necessarily indicate that the addressed 3982 is executing a list, it merely indicates that it is enabled to execute a list. This bit is read as a zero when the addressed 3982 is not enabled to execute a list .

Interrupt Mask Register

The Interrupt Mask Register is a write/read register located at an offset of $0C_{16}$ from the allocated base address of the 2843. This register is used to individually enable or disable interrupt sources from generating an interrupt request. Any bit set to a one in this register enables the corresponding signal to generate an interrupt request and a zero disables the signal from generating an interrupt request. In order for an interrupt to be generated to the PCI bus, a masked on interrupt source must occur AND the INTERRUPT ENABLE bit in the Control Register of the 2843 must be set to a one. If all of these conditions are true, the 2843 asserts a PCI interrupt request on the INTA line. After an interrupt request has been made, the host computer may then read the Interrupt Request Register to determine the source of the interrupt. The following diagram shows the bit layout for the Interrupt Mask Register.



Bit(s)	Mnemonic	Description
<31:16>	Not Used	These bits are not used and read as zeros.
<15>	PCI INT MASK	PCI INTERRUPT Mask is a write/read bit used to enable the generation of a PCI interrupt request when the PCI interface chip requests service. Setting this bit

	to a one enables the interrupt request and a zero disables the interrupt request. Please refer to the PCI Interface Interrupt Control/Status Register for additional information regarding the various PCI interface chip interrupt sources.
<14:11>Not Used	These bits are not used and read as zeros.
<10> RFIFO FULL MASK	RFIFO FULL INTERRUPT MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the FIFO on the 2843 makes the transition from not full to full. This transition indicates that the 2843 FIFO contains 2048 data elements and cannot retrieve additional words from the 3982 until some of the FIFO contents are read. Setting this bit to a zero disables this interrupt source.
<9> RFIFO HFULL MASK	RFIFO HALF FULL INTERRUPT MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the FIFO on the 2843 makes the transition from less than half full to half full. This transition occurs when there are 1024 words in the FIFO and an additional word is received from the 3982. Setting this bit to a zero disables this interrupt source.
<8> RFIFO MT MASK	RFIFO EMPTY INTERRUPT MASK is a write/read bit used to enable/disable generation of a PCI interrupt request when the FIFO on the 2843 makes the transition from not empty to empty. This interrupt is enabled when the bit is set to one and disabled by setting this bit to a zero.
<7:4> Not Used	These bits are not used and read as zeros.
<3> XFIFO FULL MASK	XFIFO FULL INTERRUPT MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the FIFO on the addressed 3982 makes the transition from not full to full. The number of data words that actually causes this transition depends on the option of the 3982 and the read data FIFO size. Setting this bit enables the interrupt source and a zero disables the source.

<2>	XFIFO MT MASK	XFIFO EMPTY INTERRUPT MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the FIFO on the addressed 3982 masks the transition from not empty to empty. This source is enabled by setting this bit to a one and disabled by setting the bit to a zero.
<1>	LIST BUSY MASK	LIST BUSY INTERRUPT MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the addressed 3982 completes one iteration of a list processing operation. This interrupt source is enabled by setting this bit to a one and disabled by setting the bit to a zero.
<0>	XEQ MASK	EXECUTE ENABLE MASK is a write/read bit used to enable/disable the generation of a PCI interrupt request when the addressed 3982 masks the transition from execution enabled to execution disabled. This interrupt source is enabled by setting this bit to a one and disabled by setting this bit to a zero.

Interrupt Request Register

The Interrupt Request Register is a read-only register located at an offset of 10_{16} from the allocated base address of the 2843. This register is used to determine the cause of an interrupt request generated by the 2843. Each bit that is read back as a one in this register is contributing to the interrupt request and needs to be serviced. Any bit that is read back as a one is automatically cleared to a zero following a read of this register.

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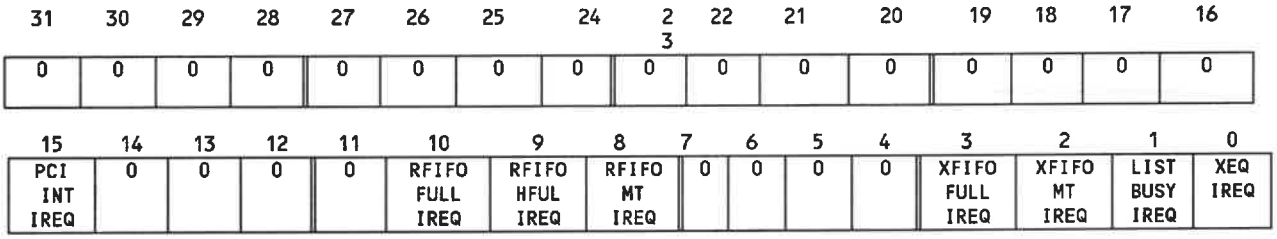
The following diagram shows the bit pattern for the Interrupt Request Register.



Bit(s)	Mnemonic	Description
<31:16>	Not Used	These bits are not used and read as zero.
<15>	PCI INT IREQ	PCI INTERFACE CHIP INTERRUPT REQUEST is a read-only bit that is set to a one when the PCI INTERRUPT MASK bit is enabled and the PCI interface chip requests service. The actual source of the interrupt within the interface chip can be resolved by reading the PCI Interface Interrupt Control/Status Register. This bit is reset to zero after it has been read as a one by programmed I/O.
<14:11>	Not Used	These bits are not used and read as zeros.
<10>	RFIFO FULL IREQ	RFIFO FULL INTERRUPT REQUEST is a read-only bit which is set to a one when the RFIFO FULL MASK bit is enabled and the FIFO on the 2843 makes the transition from not full to full. This transition occurs when there are 2047 elements in the FIFO and an additional element is entered. This bit is reset to zero after it has been read as a one by programmed I/O.
<9>	RFIFO HFUL IREQ	RFIFO HALF FULL INTERRUPT REQUEST is a read-only bit which is set to a one when the RFIFO HFUL MASK bit is enabled and the FIFO on the 2843 makes the transition from not half full to half full. This transition occurs when the FIFO contains 1024 words and an additional word is received from the 3982. This bit is reset to zero after it has been read as a one by programmed I/O.

<8>	RFIFO MT IREQ	RFIFO EMPTY INTERRUPT REQUEST is a read-only bit which is set to a one when the RFIFO MT MASK bit is set to a one and the FIFO on the 2843 makes the transition from not empty to empty. This bit is reset to zero after this bit is read as a one by programmed I/O.
<7:4>	Not Used	These bits are not used and read as zeros.
<3>	XFIFO FULL IREQ	XFIFO FULL INTERRUPT REQUEST is a read-only bit which is set to a one when the XFIFO FULL MASK bit is set to a one and the addressed 3982 read data FIFO masks the transition from not full to full. This bit is reset to zero after this bit is read as a one by programmed I/O.
<2>	XFIFO MT IREQ	XFIFO EMPTY INTERRUPT REQUEST is a read-only bit which is set to a one when the XFIFO EMPTY INTERRUPT MASK bit is set to a one and the addressed 3982 read data FIFO makes the transition from not empty to empty. This bit is reset to zero after this bit is read as a one by programmed I/O.
<1>	LIST BUSY IREQ	LIST BUSY INTERRUPT REQUEST is a read-only bit that is set to a one when the LIST BUSY MASK bit is set to a one and the addressed 3982 completes one iteration of a list processing operation. This bit is rest to zero after this bit is read as a one by programmed I/O.
<0>	XEQ IREQ	EXECUTE ENABLE INTERRUPT REQUEST is a read-only bit that is set to a one when the EXECUTE ENABLE MASK bit is set to a one and the addressed 3982 makes the transition from execution enabled to execution disabled. This bit is reset to zero when this bit is read as a one by programmed I/O.

Direct Memory Access Operation

The FIFO on the 2843 can be read by programmed I/O. Before the FIFO Data Register may be read, the RFIFO EMPTY bit in the Status Register must first be read. If the RFIFO EMPTY bit is read as a one, the 2843 FIFO contains no valid data and cannot be read. If the RFIFO EMPTY bit is read as a zero, it indicates that the 2843 FIFO contains data that may be read out through the FIFO Data Register.

This can be an inefficient mechanism to read out FIFO data since a polling operation must be executed to the Status Register for each access to the FIFO Data Register. By using Direct Memory Access (DMA), the data moved from the 3982 into the 2843 FIFO may be placed directly into host memory by the 2843.

Since PCI is based primarily on 32-bit data words, the 2843 uses this data word size when executing DMA transfers. One 32-bit word of PCI host memory is used to contain a 24-bit CAMAC data word. The 2843 buffers two 16-bit CAMAC data words before moving that data to host memory. The following diagrams show the two data storage formats when executing DMA.

For 24-bit CAMAC data words, the storage in host memory appears as follows:

Offset	31-------24	23 ----------00
00_{16}	00000000	CAMAC Data Word #1
04_{16}	00000000	CAMAC Data Word #2
08_{16}	00000000	CAMAC Data Word #3
$0C_{16}$	00000000	CAMAC Data Word #4
10_{16}	00000000	CAMAC Data Word #5
14_{16}	00000000	CAMAC Data Word #6

For 16-bit CAMAC data words, the storage in host memory appears as follows:

Offset	31----------16	15----------00
00_{16}	CAMAC Data Word #2	CAMAC Data Word #1
04_{16}	CAMAC Data Word #4	CAMAC Data Word #3
08_{16}	CAMAC Data Word #6	CAMAC Data Word #5
$0C_{16}$	CAMAC Data Word #8	CAMAC Data Word #7
10_{16}	CAMAC Data Word #10	CAMAC Data Word #9
14_{16}	CAMAC Data Word #12	CAMAC Data Word #11

To use DMA, several registers on the 2843 must be programmed to setup the operation. These registers are used to specify the initial PCI memory address where read data is to placed and a transfer count specifying the total number of words to move to host memory. Once these parameters have been specified, the DMA mechanism may then be enabled to start transferring data.

The following procedure can be used to transfer data from the read data FIFO on the 3982, through the FIFO on the 2843 and then stored in PCI memory. This procedure assumes that the 3982 has been setup and ready to acquire data.

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1.) Load the Master Write Transfer Count Register of the PCI Interface Registers with the number of bytes of data to transfer from the 2843 to PCI memory. This value must be divisible by four since the 2843 transfers only 32-bit data words to memory.

2.) Load the Master Write Address Register of the PCI Interface Registers with the initial address where CAMAC read data is to be stored in host memory. This address must be longword aligned.

3.) In the Bus Master Control/Status Register of the PCI Interface Registers, set the INBOUND FIFO RESET (bit 26) to clear the 8 word FIFO inside the PCI Interface controller chip.

4.) In the Bus Master Control/Status Register of the PCI Interface Registers, set the WRITE TRANSFER ENABLE (bit 10) to a one to enable the DMA transfers to memory.

5.) In the Control Register of the FIFO Interface Operational Registers, select the word size for the transfer using bit 8, the Front Bus Address of the 3982 to be accessed with bits 4 and 3, the DMA ENABLE (bit 5) to a one, and the FIFO ENABLE (bit 0) to a one.

6.) Wait for the WRITE TRANSFER COUNT ZERO bit in the Bus Master Control/Status Register of the PCI Interface Registers to be set to a one indicating that the requested number of data words has been transferred to memory. If polling for transfer completion is not desired, use interrupts to inform the user application when the transfer is complete. To interrupt the application when the transfer is complete, set the WRITE TRANSFER COMPLETE INTERRUPT ENABLE bit to a one in the Interrupt Control/Status Register of the PCI Interface Registers. Also, enable the 2843 to generate and interrupt from the PCI interface chip by setting the PCI INTERRUPT MASK bit to a one in the Interrupt Mask Register of the FIFO Operational Registers and set the INTERRUPT ENABLE bit in the Control Register of the FIFO Operational Registers to a one.

7.) After a requested block transfer is complete, reset the WRITE TRANSFER ENABLE bit in the Bus Master Control/Status Register of the PCI Interface Registers to a zero and clear the DMA ENABLE bit in the Control Register of the FIFO Operational Registers to a zero.

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The following section of this manual shows a sample of a C function used to enable the DMA mechanism of the 2843.

```
/*************************************************************************/
/*    Inputs to this routine are as follows:                             */
/*      base1_2843 -> This input is the base address of the PCI Interface */
/*                    Chips operational registers                        */
/*      base2_2843 -> This input is the base address of the FIFO Interface*/
/*                          Operational Registers.                       */
/*      *data        -> Data array for data storage                                 */
/*      count        -> this input is the number of longwords to transfer  */
/*                    for the operation.                                 */
/*************************************************************************/
#define ushort unsigned short
#define ulong unsigned long


unsigned long inpl(unsigned short address);

void dma_block_read_24(ushort base1_2843,
                       ushort base2_2843,
                       ulong huge *data,
                       ulong count)
  {

  ushort fifo = base1_2843 + 0x20;
  ushort bmcsr = base1_2843 + 0x3c;
  ushort mwar = base1_2843 + 0x24;
  ushort mwtcr = base1_2843 + 0x28;

  ushort ctr = base2_2843 + 0x04;

  ulong  mardata,byte_count,llp,ldata,stmo,done;
  ushort exit,sdata,sdatalo,sdatahi;
  short err;


  ldata = (ulong )data;          /* get address of data array */
  mardata = ((ldata & 0xffff0000) >> 12) + (ldata & 0xffff);
  outl(mwar,mardata);            /* load memory address register */

  byte_count = count*4;          /* get longword count to byte count */
  outl(mwtcr,byte_count);        /* load transfer count */

  ldata = 0x600000;              /* data to reset both PCI fifos */
  outl(bmcsr,ldata);          /* reset fifos */
  ldata = 0x400;                 /* data to enable PCI memory writes */
  outl(bmcsr,ldata);          /* enable pci memory writes  */
  ldata = 0x21L;                 /* data to enable DMA and FIFO buffer */
  outl(ctr,ldata);               /* write csr to enable fifo & DMA */
  exit=0;                                /* setup for timeout & wait for done */
  stmo=0;
  while((stmo != 0x7ffff) && ((inpl(bmcsr) & 0x80) != 0x80)) {
    stmo++;
    }
  if (stmo == 0x7ffff) {
    printf("\n\nTimed out waiting for TRANSFER COMPLETE  ..\n");
    }
  ldata = 0x600000;              /* data to reset fifos & stop DMA */
  outl(bmcsr,ldata);          /* reset fifos & stop dma */
  }
```

Front Bus

The Front Bus is a 50-conductor twisted pair flat ribbon cable which contains 16 data bits, 2 strobe signals, and 8 status signals. The bus uses RS-485 balanced signaling to provide high noise immunity and long cable lengths. The maximum signaling distance for the 2843 to a 3982 is 100 feet. The following chart shows the signal allocation on the front bus.

Note: The AD1 and AD0 signals are single-ended and terminated with a 2200 ohm resistor to +5 volts.

Pin	Signal	Pin	Signal
1	DATA0+	26	DATA12-
2	DATA0-	27	DATA13+
3	DATA1+	28	DATA13-
4	DATA1-	29	DATA14+
5	DATA2+	30	DATA14-
6	DATA2-	31	DATA15+
7	DATA3+	32	DATA15-
8	DATA3-	33	STB HIGH+
9	DATA4+	34	STB HIGH-
10	DATA4-	35	STB LOW+
11	DATA5+	36	STB LOW-
12	DATA5-	37	DIRECTION+
13	DATA6+	38	DIRECTION-
14	DATA6-	39	AD0
15	DATA7+	40	AD1
16	DATA7-	41	FIFO FULL+
17	DATA8+	42	FIFO FULL-
18	DATA8-	43	FIFO EMPTY+
19	DATA9+	44	FIFO EMPTY-
20	DATA9-	45	XEQ+
21	DATA10+	46	XEQ-
22	DATA10-	47	LIST-IN-PROGRESS+
23	DATA11+	48	LIST-IN-PROGRESS-
24	DATA11-	49	ACKNOWLEDGE+
25	DATA12+	50	ACKNOWLEDGE-

Front Bus Transfers

Data is transferred from the addressed Front Bus module to the FIFO Interface at the request of the FIFO Interface. Once the FIFO Interface is enabled with the FIFO ENABLE bit in the Control Register is the FIFO Interface Registers, data transfer may proceed.

A state machine on the 2843 examines the FIFO EMPTY signal transmitted from the addressed module. If the addressed modules' FIFO EMPTY signal is asserted, the state machine waits until the FIFO EMPTY signal is negated, indicating that the addressed device has data available for transmission. Once the FIFO EMPTY signal is negated, the state machine on the 2843 asserts the signal STROBE LOW to the addressed module. The addressed module responds to the assertion of this signal by placing the lower 16-bits of a CAMAC data word onto the Front Bus data lines and then asserts the ACKNOWLEDGE signal. When the 2843 receives the ACKNOWLEDGE signal, it latches the lower 16-bits of CAMAC data and then stores it into the on-board FIFO. The state machine then examines the WORD SIZE bit to verify the size of the CAMAC data words to transfer. If the WORD SIZE bit is set to a one, indicating 16-bit CAMAC data words, the state machine returns to the beginning of its sequence and checks the FIFO flags. If the WORD SIZE bit is zero, the state machine asserts the signal STROBE HIGH. Upon receiving the STROBE HIGH signal, the addressed module responds by placing the upper 8-bits of CAMAC data onto the Front Bus and then asserts the ACKNOWLEDGE signal. When the 2843 receives the ACKNOWLEDGE signal, it latches the data and stores it into the on-board FIFO.

This sequence is repeated for each data word as long as the addressed front-bus device contains data ready to transmit and the 2843 has room available in the on-board FIFO for the received data.

Warranty

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KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired product to the purchaser, if located in the United States and Switzerland, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

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Products will not be accepted for credit or exchange without the prior written approval of KineticSystems. If it is necessary to return a product for repair replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center prior to shipping the product to KineticSystems. The following steps should be taken before returning any product:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

USA, Canada, and Mexico
KineticSystems Corporation
Repair Service Center
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