Model 2927-Z1A

16-bit IBM PC/AT® Interface w/DMA

INSTRUCTION MANUAL

September, 1991

*****Special Option*****

Model 2927-S001

16-bit IBM PC/AT® Interface w/DMA

October, 1995

*****Special Option*****

Model 2927-S001

The Model 2927-S001 is the same as the Model 2927-Z1A except that if scan reaches an open slot (NoQ, NoX condition) Q-Scan mode will stop scanning.

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FIGURES

SCHEMATIC DRAWING #132313-C-6070

See Reply Card Following Warranty

WARRANTY

KJC:rem(WP)

KineticSystems Corporation

Standardized Data Acquisition and Control Systems **2927**

16-bit IBM PC/AT® Interface w/DMA

ADVANCE INFORMATION

(Revised Sept. 91)

FEATURES

- **Provide dedicated PC/AT interface**
- **Used with 3922 Crate Controllers**
- **Up to eight crate controllers addressed on a single bus**
- **Mounts in any 16-bit expansion slot of an IBM PC/AT, Compaq 386 or other compatible CPU**
- **Interrupts for Done and LAM response**
- **RS-485 balanced line signaling between the 2927 and 3922(s) for high noise immunity**
- **Supports crate controller bus lengths to 90 meters (300 feet)**
- **Includes switch-selectable address registers**
- **Supports DMA data transfers up to 900 kilobytes per second**
- **Strap selection for DMA channel and Interrupt Request level**
- **Driver support software available**

APPLICATIONS

- **Interface CAMAC to IBM PC/AT**
- **General-purpose data acquisition and control**
- **Laboratory automation**
- **Industrial process control**

GENERAL DESCRIPTION

The Model 2927 is a computer bus adapter for use with the IBM PC/AT, Compaq 386, or other fully compatible computer. It mounts in any available 16-bit expansion slot within the computer, and communicates with the host using a 16-bit data path.

The 2927 supports up to eight Model 3922 crate controllers via a Model 5843-Txyz 40-conductor, twisted-pair ribbon cable. (Order this cable separately.) Signaling on this bus is accomplished with RS-485 balanced-line drivers and receivers, giving high noise immunity and allowing an overall cable distance between the computer interface and the last 3922 of up to 90 meters (300 feet). The last 3922 on the Parallel Bus is terminated with a termination card (provided with the 3922).

Program transfers as well as DMA data blocks are supported by these 2927. The DMA channel provides speed-efficient block transfers with the following modes of operation: Q-Scan, Q-Stop, Wait Until Q, and Stop on Word Count. Interrupt capability is provided. An interrupt can be generated by DMA Done or by a pending LAM. In response to a LAM interrupt, the host computer performs a parallel poll of the 3922s via the 2927. In response to the parallel poll, each 3922 requesting service asserts one of the eight data lines (i.e., Crate 5 asserts Data Line 5). This method increases the efficiency of the interrupt service routine in multicrate systems.

An on-board switch on the 2927 is used to select the base address in the PC's I/O page. Strap options on the module select the DMA channel number as well as the interrupt request level for both the Done and LAM interrupts.

Please contact KSC for additional information on software driver support and other interfaces for personal computers.

INTERNAL REGISTERS

Offset	Mnemonic	Meaning
0	CSR	Control/Status Register
2	MCR	Mode Control Register
4	CCR	Crate Controller Address Register
6	NAF	CAMAC Command Register
8	DLR	Data Register - Low Order Word
A	DHR	Data Register - High Order Byte
C	SRR	Service Request Register
E	TCR	Transfer Count Register

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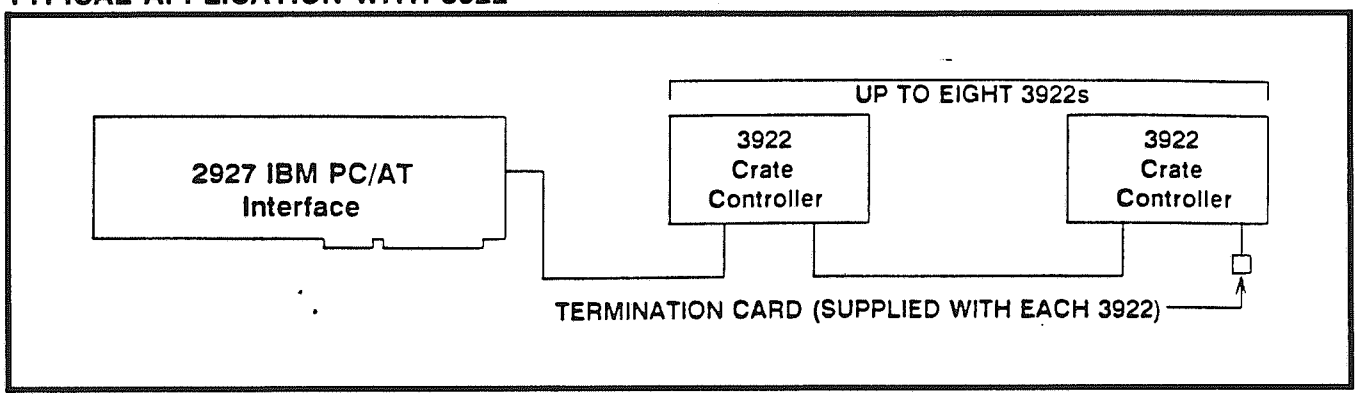
TYPICAL APPLICATION WITH 3922



POWER REQUIREMENTS

+5 volts — 2500 mA

ORDERING INFORMATION

Weight: .3 kg. (10.6 oz.)

Model 2927-Z1A — 16-bit PC/AT Interface

Accessories — Model 5843-Txyz Series Interface Bus Cable (one required for each Model 3922)
Model 6110-1G MS/DOS Driver for IBM PC/AT
Model 3922-Z1B Parallel Bus Crate Controller

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INSTALLATION

The Model 2927 is designed to fit into a full size, 16-bit expansion slot of an IBM PC/AT, COMPAQ 386, or compatible computer. After selecting the base address, DMA channel, and interrupt request levels (Refer to the Switch and Strap sections of this manual), the 2927 is ready to be installed in the computer.

Remove the cover of the computer. Locate an empty 16-bit expansion slot and remove the blank plate from the mounting rail. Insert the 2927 into the slot and secure it with the screw that was used for the blank plate. Replace the cover of the computer.

Insert one end of the 40-conductor twisted pair ribbon cable into the 40-position header located on the rear of the 2927. Connect the other end of the ribbon cable to the first 3922 in the chain. Refer to the 3922 instruction manual for the connections to be made to the 3922.

OPERATION

Communication between the PC and the 2927 is accomplished via I/O commands. A six-position "DIP" switch allows the user to select the base address of the eight internal registers on the 2927. The six switches select the upper six bits of the 10-bit I/O address, thus placing the 2927's base address on 16 byte boundaries. Crate address, Control/Status information, and data are transferred to and from the 3922(s) via the K-Bus cable. At the initiation of a K-Bus cycle, a header byte is transmitted across the bus. This byte contains the crate address, operation mode, and word size of the operation to be performed.

By writing registers on the 2927, the user determines the type of transfer, CAMAC command to be executed, etc. When the "GO" bit is set, the 2927 initiates the proper cycle. The header byte for the cycle is followed by data transfer for CAMAC read or write operations.

ADDRESS SELECTION

The address of the eight I/O registers in the 2927 are selected from the PC's 10-bit I/O address space. The base address of the 2927 is the first byte within a block of 16 bytes. The base address selected has the least significant Hexadecimal digit of zero.

WHEN SELECTING A BASE ADDRESS, CARE MUST BE TAKEN TO AVOID ADDRESSES ASSIGNED TO OTHER DEVICES ON THE PC'S I/O ADDRESS BUS.

The switches A9 through A4 determine the base address of the 2927. Bits 9 through 4 are selectable via the switches. Bits 0 through 3 are always a logic 0. The bit pattern of the base address is shown in the following diagram:

09	08	07	06	05	04	03	02	01	00
A9	A8	A7	A6	A5	A4	0	0	0	0

When the switch is in the on (closed) position, the corresponding address bit is set to a logic 0. With the switch in the off (open) position, the corresponding address bit is set to a logic 1.

For example, the bit pattern for base address 2F0 hex is shown in the following diagram.

09	08	07	06	05	04	03	02	01	00
1	0	1	1	1	1	0	0	0	0

Therefore, to obtain this base address the switches A9 through A4 must be set to the following pattern; OFF, ON, OFF, OFF, OFF, OFF.

INTERRUPT AND DMA CHANNEL STRAPS

The 2927 contains straps for the selection of the PC DMA Channel and Interrupt Request Level.

The DMA channel can be strapped for either Channel 5, Channel 6, or Channel 7. When selecting a DMA channel, be sure no other device in the PC is using that channel. Refer to Figure 1 for the location of these straps.

The 2927 can be strapped for various Interrupt Request Levels. Straps are provided for selection of a DONE or RFS Interrupt. The Interrupt Request Levels available on the 2927 are 3, 4, 5, 7, 10, 11, 12 and 15. The RFS Request Level can also be strapped to match the DONE Interrupt Request Level. This is done by placing the SRQ strap in the R = D position and selecting the appropriate Interrupt Request Level with the DONE strap.

The DONE Interrupt can be disabled for NAF transfers. This is done by placing the NAF ENA/DIS strap in the Disable strap. When the strap is in the Disable position, the completion of a NAF transfer will not cause a PC interrupt. To allow NAF transfers to cause a DONE Interrupt, place the strap in the ENA position. Refer to Figure 1 for the location of these straps.

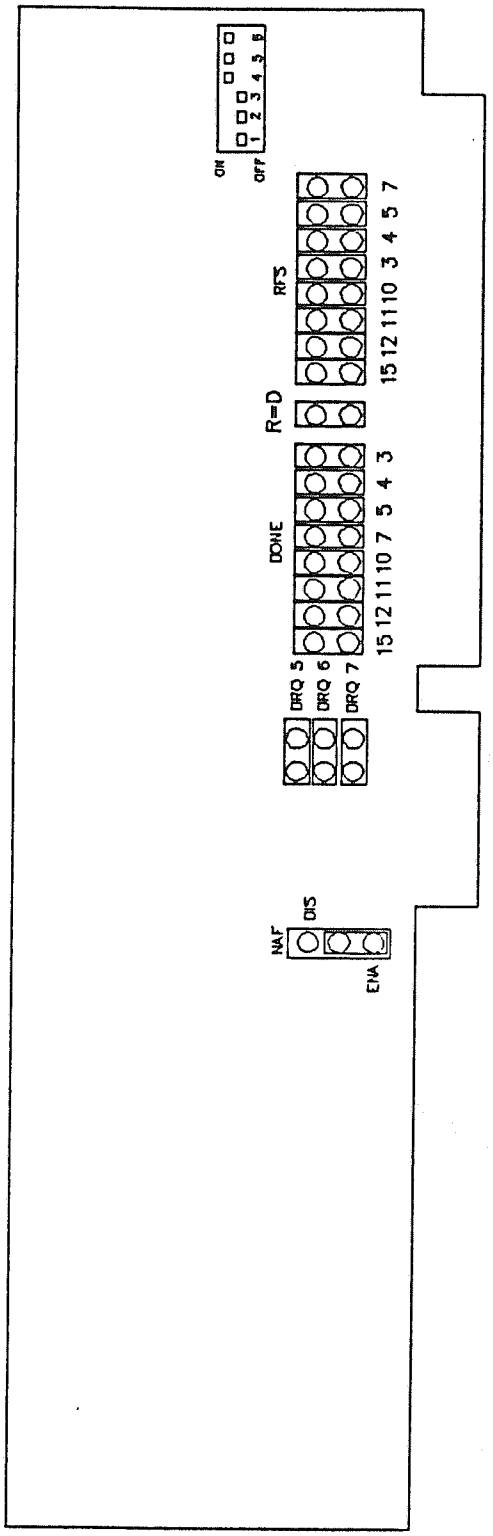


FIGURE 1 - 2927 STRAP & SWITCH LOCATIONS

INTERNAL REGISTERS

The Control/Status Register

The Control/Status Register (CSR) is used to monitor and control the 2927 operations. Bit 0 is set to initiate CAMAC operations. Bits 3 and 4 reflect the interface identification revision of the 2927. Bit 6 is set to allow a PC interrupt upon completion of a K-Bus operation. Bits 7, 13, 14, and 15 reflect operation status. Bit 8 is set to allow a PC interrupt upon receipt of a Request-For-Service from a 3922 Crate Controller. Bit 9 is set when a CAMAC LAM is pending. Bit 10 is set to initiate a Parallel Poll operation on the K-bus. Bit 12 is used to reset the 2927 to a power-up state.

CONTROL/STATUS REGISTER (CSR) Offset:0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	ABT	INFO TMO	RST IFC	0	PP	RFS	RFS I.E.	DNE	DNE I.E.	0	ID2	ID1	NO X	NO Q	GO

Bit	Signal Name	Description
15	ERROR	**ERROR** is a read-only bit which is set when an operation terminated with an error. The following is a definition of error: ERROR = INFO TMO + ABORT
14	ABORT	**ABORT** is a read-only bit which is set when an operation is terminated due to one of the following conditions: ABORT = (BM*/$\overline{TM2}$*/$\overline{TM1}$*NOQ) + (BM*TM2*TM1*N>23) + (BM*/$\overline{TM2}$*NOX*$\overline{AD}$) +(BM*TM2*/$\overline{TM1}$*QRPT TMO) BM - Block Mode (Bit 5 of the MCR) TM2 - Transfer Mode 2 (Bit 4 of the MCR) TM1 - Transfer Mode 1 (Bit 3 of the MCR) NOQ - CAMAC Q-response = 0 (Bit 1 of the CSR) N>23 - Station Number (N) greater than 23 NOX - CAMAC X-response = 0 (Bit 2 of the CSR) AD - Abort Disable (Bit 0 of the MCR) QRPT TMO - Q-repeat Timeout (Block Mode 2 does not receive a CAMAC Q-response = 1 within 60 milliseconds)
13	INFO TMO	**INFORMATION BUS TIMEOUT** is a read-only bit which is set when a timeout has occurred during a 3922/2927 transfer.
12	RST IFC	**RESET INTERFACE** is a write-only bit which, when written to a one, resets the 2927 to a power up state. This bit is not latched.

11	NOT USED	Read as zero.
10	PP	**PARALLEL POLL** is a write-only bit which when set initiates a K-Bus Parallel Poll operation. This bit is not latched.
		NOTE: The SRR must be read immediately following a Parallel Poll operation.
9	RFS	**REQUEST-FOR-SERVICE** is a read-only bit which is set when a CAMAC LAM is pending from a 3922.
8	RFS I.E.	**REQUEST FOR SERVICE INTERRUPT ENABLE** is a read/write bit, which is set to allow a PC interrupt to be set when the RFS bit is asserted.
7	DNE	**DONE** is a read-only bit which is set when the 2927 has completed an operation. This bit is cleared while the 2927 is busy.
6	DNE I.E.	**DONE INTERRUPT ENABLE** is a read write bit which is set to enable a PC interrupt when the 2927 completes an operation.
5	NOT USED	Read as zero.
4,3	ID2,ID1	**INTERFACE ID2, ID1** are read-only bits. These bits are used to determine the interface revision.
2	NOX	**NO-X**, when set, indicates that the last CAMAC transfer ended with an X-response of zero.
1	NOQ	**NO-Q**, when set, indicates that the last CAMAC transfer ended with a Q-response of zero.
0	GO	**GO** is a write-only bit which is used to initiate programmed transfer of DMA operations. This bit is read as a zero.

Bits 15-13, 8, and 6 are reset on power-up, "RESET INTERFACE", or PC RST-DRV. Bit 7 is set on power-up. Bits 2 and 1 are set on power-up as a result of the CAMAC Initialize (Z) cycle.

The Mode Control Register

The Mode Control Register (MCR) is used to specify the mode of operation. Bit 5 is set to specify DMA modes of operation, and is cleared to indicate programmed control operation. Bits 4 and 3 are used to specify the DMA transfer mode (these bits are ignored when bit 5 is a zero). Bits 2 and 1 are used to specify the CAMAC word size, and affect both DMA and programmed transfer modes of operation. Bit 0 is used to enable or disable block transfer termination on the receipt of a CAMAC NO-X condition. All bits in the MCR are cleared on power-up, "RESET INTERFACE", or PC RST-DRV.

MODE CONTROL REGISTER (MCR) Offset:2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	BLK	TM2	TM1	WS2	WS1	AD

Bit	Signal Name	Description
15-6	NOT USED	Read as zeros.
5	BLK	**BLOCK MODE** is set to a 1 to specify DMA modes of operation. The transfer mode type is selected by TM2 and TM1. When BLK is set to a 0, program control operations are executed. Bits TM2 and TM1 are ignored for program transfer operations.
4,3	TM2,TM1	**TRANSFER MODE 2 and 1** are used to select the DMA transfer mode type:

TM2	TM1	TRANSFER MODE
0	0	Q-STOP
0	1	Q-IGNORE
1	0	Q-REPEAT
1	1	Q-SCAN

These bits are ignored for programmed transfers.

2,1	WS2,WS1	**WORD SIZE 2 and 1** are used to select the size of the CAMAC data word to be transferred. These bits affect both DMA and Programmed transfer modes of operation.

WS2	WS1	CAMAC WORD SIZE
0	0	24 Bit
0	1	16 Bit
1	0	8 Bit
1	1	RESERVED

0	AD	**ABORT DISABLE** is set to a 1 to allow block transfer termination due to a NO-X response. This bit is ignored during Q-SCAN operations.

The CAMAC Crate Address Register

The CAMAC Crate Address Register (CCR) selects the "current crate" for all addressed operations. All operations executed by the 2927 are directed to the crate specified in the CAMAC Crate Address Register. Note that the contents of this register are used during the

writing and reading of the CAMAC Command Register. This register is reset on power-up, "RESET INTERFACE", or PC RST-DRV.

CAMAC CRATE ADDRESS REGISTER (CCR) Offset:4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	C4	C2	C1

Bit	Signal Name	Description
15-3	NOT USED	Read as zeros.
2-0	C4,C2,C1	**CRATE ADDRESS 4, 2, and 1** are used to determine which 3922 is to be accessed during the next K-Bus operations. The crate address range is from zero to seven.

The CAMAC Command Register

The CAMAC Command Register (NAF) is used to specify the CAMAC function code (F), subaddress (A), and station number (N) that are to be used during a CAMAC operation.

The NAF registers are actually located on the 3922s. Thus, when I/O operations are executed to the NAF register, a K-Bus transfer is executed between the 2927 and the currently addressed 3922. If an attempt to do a NAF read or write to a non-existent 3922 crate address, an info bus time-out (bit 13 of the CSR) will occur.

Since the NAF register is located on the 3922, reading of the NAF register is a two step process. First, bit 15 (RD NAF) of the NAF register must be written to a one. This initiates the K-Bus NAF register read operation. Upon receipt of the DNE bit in the CSR, the NAF register data can be read by doing a read operation to the NAF register I/O address. The data returned is the contents of the NAF register for the current crate address.

CAMAC COMMAND REGISTER (NAF) Offset:6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RD NAF	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

Bit	Signal Name	Description
15	RD NAF	**READ NAF** is a write only bit which is set to initiate a K-Bus NAF read operation to the current crate address. Upon completion of the NAF read operation, the CAMAC command data can be read by doing a read operation to the NAF register's I/O address. This bit is read as zero.
14	NOT USED	Read as zero.

13-9	N16 - N1	**STATION NUMBER 16 to 1** specifies the CAMAC station number N(1) to N(31), which is to be addressed during a CAMAC operation.
8-5	A8 - A1	**SUBADDRESS 8 to 1** specifies which CAMAC subaddress A(0) to A(15), is to be used by the addressed CAMAC operation.
4-0	F16 - F1	**FUNCTION CODE 16 to 1** selects the CAMAC function code F(0) through F(31). The binary combination of the F16 and F8 bits determine the type of CAMAC operation as follows:

F16	F8	OPERATION
0	0	CAMAC READ
0	1	CAMAC CONTROL
1	0	CAMAC WRITE
1	1	CAMAC CONTROL

The Data Low Register

The Data Low Register (DLR) is used to access the lower 16-bits of the 24-bit CAMAC data word. During CAMAC write operations, F(16) - F(23), the contents of the DLR are used to generate the data signals on the CAMAC write data lines W1 through W16. During CAMAC read operations, F(0) - F(7), the DLR is loaded with the data signals from the CAMAC read data lines R1 through R16.

DATA LOW REGISTER (DLR) Offset:8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W 16	R/W 15	R/W 14	R/W 13	R/W 12	R/W 11	R/W 10	R/W 9	R/W 8	R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1

Bit	Signal Name	Description
15-0	R/W16 - R/W1	**R/W16-R/W1** provide access to the lower 16-bits of the CAMAC data word.

The Data High Register

The Data High Register (DHR) is used to access the upper 8-bits of the 24-bit CAMAC data word. During CAMAC write operations, F(16) - F(23), the contents of the DHR are used to generate the data signals on the CAMAC write data lines W17 through W24. During CAMAC read operations, F(0) - F(7), the DHR is loaded with the data signals from the CAMAC read data lines R17 through R24.

DATA HIGH REGISTER (DHR) Offset:A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	R/W 24	R/W 23	R/W 22	R/W 21	R/W 20	R/W 19	R/W 18	R/W 17

Bit	Signal Name	Description
15-8	NOT USED	Read as zero.
7-0	R/W24 - R/W17	**R/W24-R/W17** provide access to the upper 8-bits of the CAMAC data word.

The Service Request Register

The Service Request Register (SRR) provides information regarding pending LAMs (Request-for-Service) in a multi-crate system. After executing a Parallel Poll by setting bit 10 in the CSR, the SRR can be read to determine which 3922s have a LAM pending.

The lower eight bits represent the eight possible crate addresses. A true bit (1) in the SRR indicates that its associated crate has a LAM pending and is asserting the LAM Request-for-Service line.

To get valid data in the SRR, a Parallel Poll must be generated. Upon receiving DONE from the Parallel Poll operation, the SRR must be read. This must occur before any subsequent NAF or CAMAC data operations are attempted.

SERVICE REQUEST REGISTER (SRR) Offset:C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0

Bit	Signal Name	Description
15-8	NOT USED	Read as zeros.
7-0	C7 - C0	**CRATE 7-0** are set when their associated crate addresses are requesting service.

The Transfer Count Register

The Transfer Count Register (TCR) is used during DMA read operations to determine the total number of data bytes to be transferred across the K-Bus. The TCR is loaded with the two's complement of the number of 16-bit words to be transferred to the computer. This number is the 2's complement of the number written to the PC's DMA controller transfer count register.

This register is used only during DMA read operations (transferring data from the 2927 to the PC's memory). The DMA write word count is controlled by the PC's DMA controller.

Refer to the PC's Hardware Reference Guide for information on programming the PC's DMA controller.

TRANSFER COUNT REGISTER (TCR) Offset:E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 9	TC 8	TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0

Bit	Signal Name	Description
15-0	TC15 - TC0	**TRANSFER COUNT 15 to 0** are written with the number of 16-bit words to be transferred to the PC's memory during DMA read operations. This number must be the number written to the DMA controller's Transfer Count Register. This register is not used for DMA write operations (transfers from the PC's memory to the 2927). Word count for DMA write operations is controlled by the DMA controller on the PC.

PROGRAMMED TRANSFERS

The 2927 provides a programmed transfer mode of operation. Under programmed transfer, all data transfers to or from the 2927 are done via programmed I/O. Programmed transfers may be executed using either 16- or 24-bit CAMAC data word sizes. The size of the CAMAC data words transferred is determined by the Word Size bits (WS2 and WS1) in the Mode Control Register (MCR). The Transfer Mode bits (TM2 and TM1) in the Mode Control Register are ignored during programmed transfer operations.

The following describes the software sequences necessary to execute CAMAC Read, Write and Control operations.

Programmed Transfer Read Operation (F16=0 : F8=0)

1.) Load the CAMAC Read command to be executed in the NAF.

2.) Wait for the DONE bit in the CSR to become true.

3.) Load the MCR with:
   a. BLK bit set to a "0".
   b. The appropriate CAMAC data word size (WS2,WS1).
   c. Set/Clear AD as required.

4.) Load the CSR with:
   a. GO bit set to a "1".

b. Set/clear DONE Interrupt Enable as required. (See note).

5.) Wait for DONE in the CSR to become true.

6.) If a 24-bit CAMAC data word size was selected, fetch the upper 8-bits of the CAMAC Read data word from the DHR.

7.) Fetch the lower 16-bits of the CAMAC Read data word from the DLR.

8.) Check the NO-Q and NO-X bits in the CSR to verify data validity.

Programmed Transfer Write Operation (F16=1 : F8=0)

1.) Load the CAMAC Write command to be executed in the NAF.

2.) Wait for the DONE bit in the CSR to become true.

3.) Load the MCR with:
a. BLK bit set to a "0".
b. The appropriate CAMAC data word size (WS2,WS1).
c. Set/Clear AD as required.

4.) If 24-bit CAMAC data word size was selected, load the upper 8-bits of the CAMAC Write data word in the DHR.

5.) Load the lower 16-bits of the CAMAC Write data word in the DHR.

6.) Load the CSR with:
a. GO bit set to a "1".
b. Set/clear DONE Interrupt Enable as required. (See note).

7.) Wait for the DONE bit in the CSR to become true.

8.) Check the NO-Q and NO-X bits in the CSR to verify that the addressed module accepted the CAMAC Write operation.

Programmed Transfer Control Operation (F16=0 : F8=1 or F16=1 : F8=1)

1.) Load the CAMAC Control command to be executed in the NAF.

2.) Wait for the DONE bit in the CSR to become true.

3.) Load the MCR with:
a. BLK bit set to a "0".
b. Set/Clear AD as required.

4.) Load the CSR with:
a. GO bit set to a "1".
b. Set/clear DONE Interrupt Enable as required. (See note).

5.) Wait for the DONE bit in the CSR to become true.

6.) Check the NO-Q and NO-X bits in the CSR to verify if the operation was successfully executed.

> NOTE: WHEN USING THE 2927 WITH THE DONE INTERRUPT ENABLED, IGNORE THE STEP WHICH INCLUDES WAITING FOR DONE SINCE THE ASSERTION OF THE DONE BIT GENERATES AN INTERRUPT.

STANDARD DMA BLOCK TRANSFERS

The 2927 supports four types of DMA block transfers. These transfer modes include Q-Stop, Q-Ignore, Q-Repeat, and Q-Scan. In each of the DMA transfer modes, initial conditions are loaded via programmed I/O. Data transfers to or from the computer memory are done using the Direct-Memory-Access (DMA) feature of the PC. The actual DMA data transfers are not performed by the 2927 CAMAC interface circuitry but by DMA controllers which are a part of the PC. Therefore, the DMA controllers must be properly loaded before a DMA block transfer operation may begin. Refer to the section "Programming The DMA Controllers" for further information.

During CAMAC Read block transfers, a CAMAC Read operation is first executed. After the CAMAC Read command is executed, the data is checked for validity. Data validity depends on such parameters as the Transfer Mode selected (TM2, TM1) and the CAMAC Q- and X-responses. Refer to the individual transfer mode sections for further information regarding data validity. If valid data is received, the 2927 generates a request to the DMA controller to store the read data obtained. During the DMA transfer, the 2927 checks the PC bus signal "T/C" (terminal count) which, when true, indicates that this is the last word for the DMA block transfer operation. After checking the "T/C" signal, the 2927 either sets DONE or check for TCO. (Transfer Count Overflow) in the TCR. If TCO is detected, the 2927 waits for T/C from the PC bus. If TCO is not detected, the 2927 collects the next byte of DATA from the K-Bus. When executing CAMAC Write commands, the 2927 first obtains the CAMAC Write data via DMA. During the DMA transfer the 2927 checks the "T/C" signal to see if this data word is the last CAMAC Write data word. After obtaining the data, the 2927 executes a K-bus transfer. If "T/C" was true during the last DMA transfer, the 2927 sets the DONE bit after the CAMAC cycle is completed. If "T/C" was not set, the 2927 fetches the next CAMAC Write data word and continues this sequence until either "T/C" is set or until the block transfer operation is terminated due to an ABORT condition.

Data transfers to/from the PC memory are done in a pipelined fashion. During DMA Write Operations, the 2927 does not wait for successful completion of the CAMAC operation before it requests the next CAMAC Write data word from memory. When both of the Write data buffers are full, the DMA process ceases until one of the buffers goes empty. This continues until the terminal count is reached. This allows the 2927 to retrieve data from memory while Dataway cycles are occurring.

The following section describes the operation and software sequences necessary to execute DMA block transfers.

Read or Write DMA Block Transfer Loading Sequence

1.) Load the CAMAC command to be executed in the NAF.

2.) Wait for the DONE bit to become asserted.

3.) Load the MCR with:
   a. BLK bit set to a "1".
   b. The appropriate CAMAC data word size (WS2, WS1).
   c. Set/clear AD as required.

4.) Initialize the DMA controller for the block transfer as follows:

   a. Write the DMA page address for the desired channel.
   b. Write the data buffer address in the two-byte Base-Address Register.
   c. Write the data buffer length in the two-byte Word Count Register.
   d. Write the Mode Register of the DMA controller to indicate the type of transfer to be performed.
   e. Mask "on" the desired DMA channel by writing the Mask Register.

5.) Load the CSR with:
   a. GO bit set to a "1".
   b. Set/clear DONE Interrupt Enable as required. (See note)

6.) Wait for the DONE bit in the CSR to become true.

7.) Read the CSR and check the NO-Q, NO-X, ERROR, ABORT,and N>23/QMO bits to verify that the block transfer operation was successfully executed.

> NOTE: WHEN USING THE 2927 WITH THE DONE INTERRUPT ENABLED, IGNORE THE STEP WHICH INCLUDES WAITING FOR DONE SINCE THE ASSERTION OF THE DONE BIT GENERATES AN INTERRUPT.

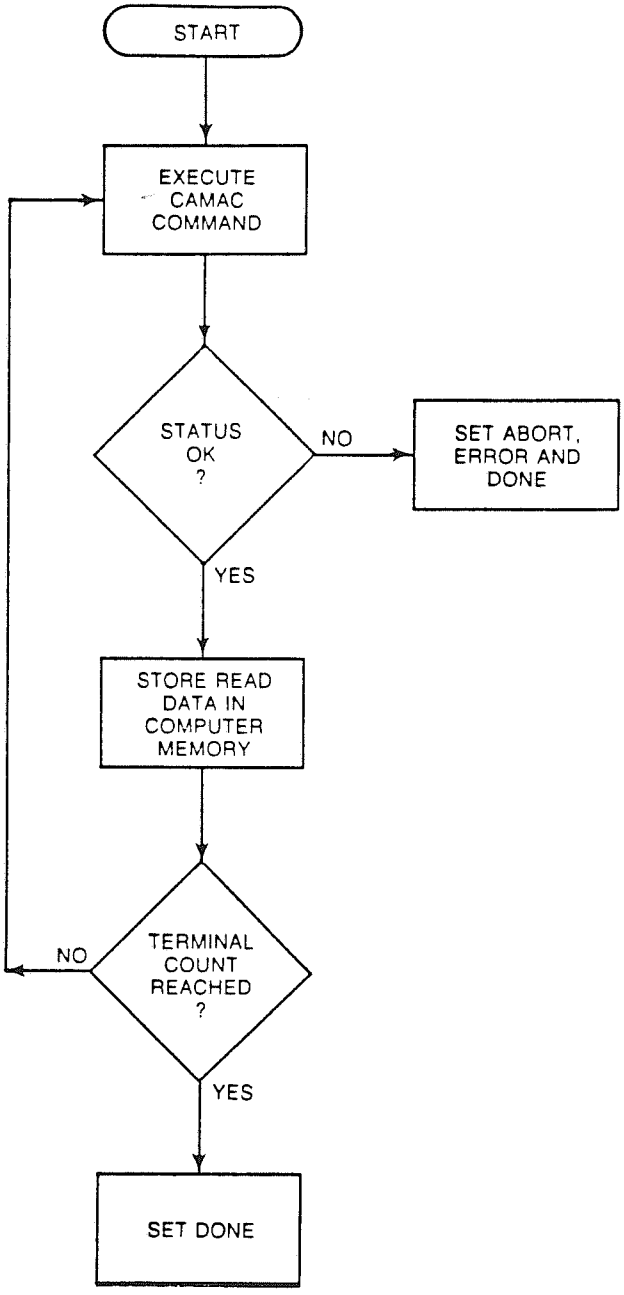
Q-Stop Block Transfer (TM2=0 : TM1=0)

To select the Q-Stop block transfer mode of operation, clear both of the Transfer Mode bits when writing to the MCR. During Q-Stop block transfer operations, the CAMAC command specified in the NAF register is repeated until a Q-Response of zero is received or the terminal count is reached. The block transfer will also terminate if an ABORT condition occurs. The following equation describes ABORT for the Q-Stop block transfer mode:

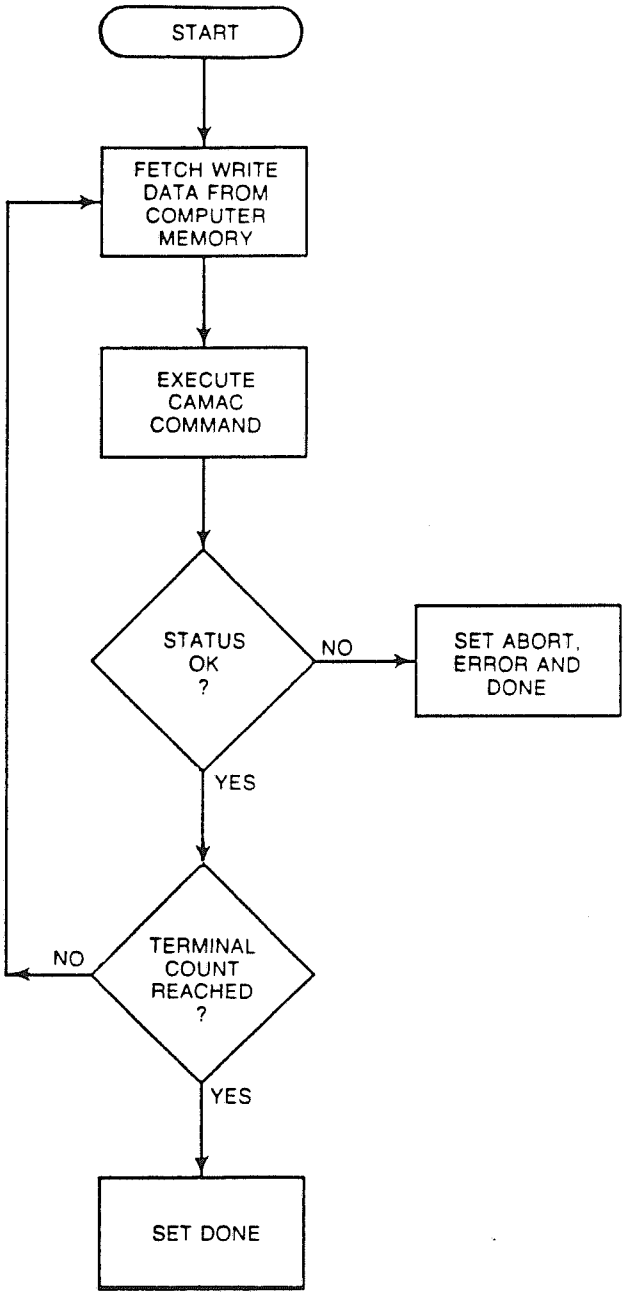
$$\text{ABORT} = \text{NO-Q} + \overline{\text{AD}} * \text{NO-X}$$

The following diagrams are simplified flow diagrams for Q-Stop block transfer Writes and Reads:

FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-STOP & Q-IGNORE READ COMMANDS



FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-STOP Q-IGNORE WRITE COMMANDS



Q-Ignore Block Transfer (TM2=0 : TM1=1)

To select the Q-Ignore block transfer mode of operation, set the Transfer Mode bit TM2 to a "0" and TM1 to a "1" when writing to the MCR. During Q-Ignore block transfer operations, the CAMAC command specified in the NAF register is repeated until the terminal count is reached. The block transfer will also terminate if an ABORT condition occurs. The following equation describes ABORT for the Q-Ignore block transfer mode:

$$\text{ABORT} = \overline{\text{AD}} * \text{NO-X}$$

The diagram on page 15 is a simplified flow diagram for Q-Ignore block transfer Writes and Reads.

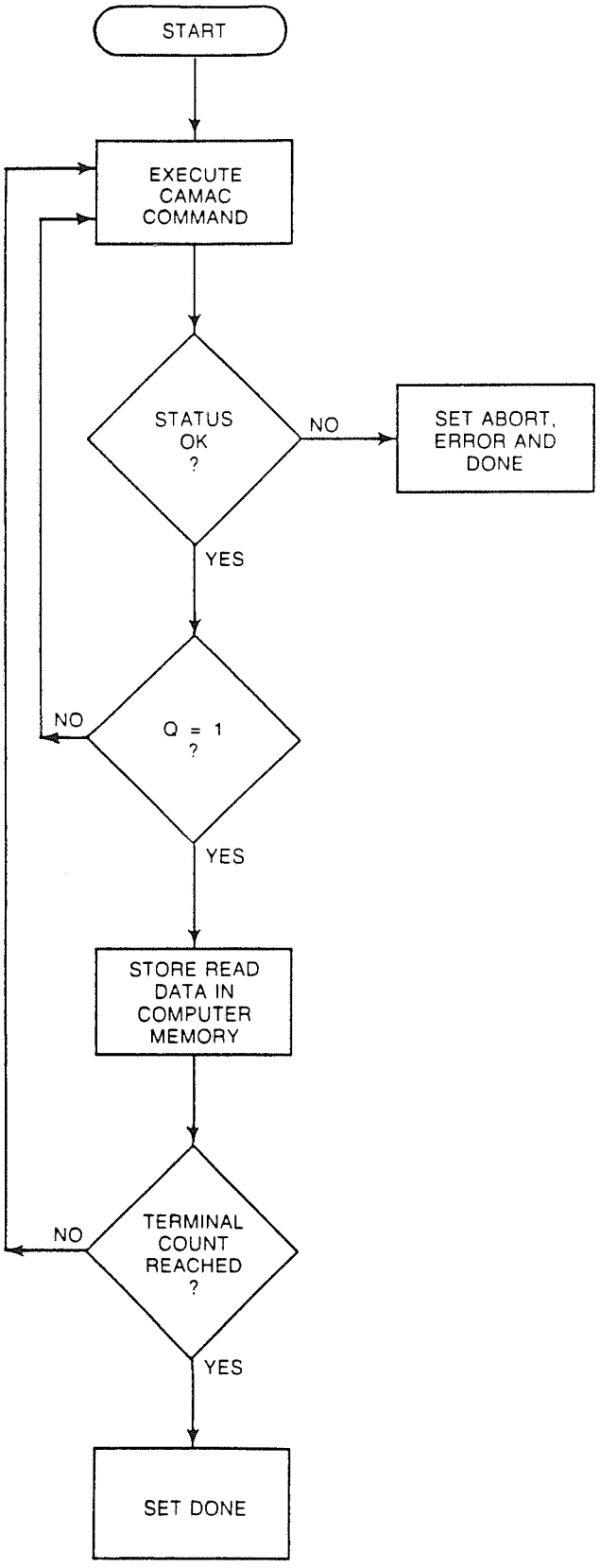
Q-Repeat Block Transfer (TM2=1 : TM1=0)

To select the Q-Repeat block transfer mode of operation, set the Transfer Mode bit TM2 to a "1" and TM1 to a "0" when writing to the MCR. During a Q-Repeat block transfer operation, the CAMAC command specified in the NAF register is repeated for each data word until a Q-Response of "1" is obtained. A Q-Response of "1" causes either new Write data to be fetched or Read data to be stored. The command is repeated for each data word until the terminal count is reached. If a Q-Response of "1" is not obtained for a data word within 200 milliseconds, the QTMO bit in the CSR is set and the operation terminates. The following equation describes ABORT for the Q-Repeat block transfer mode:

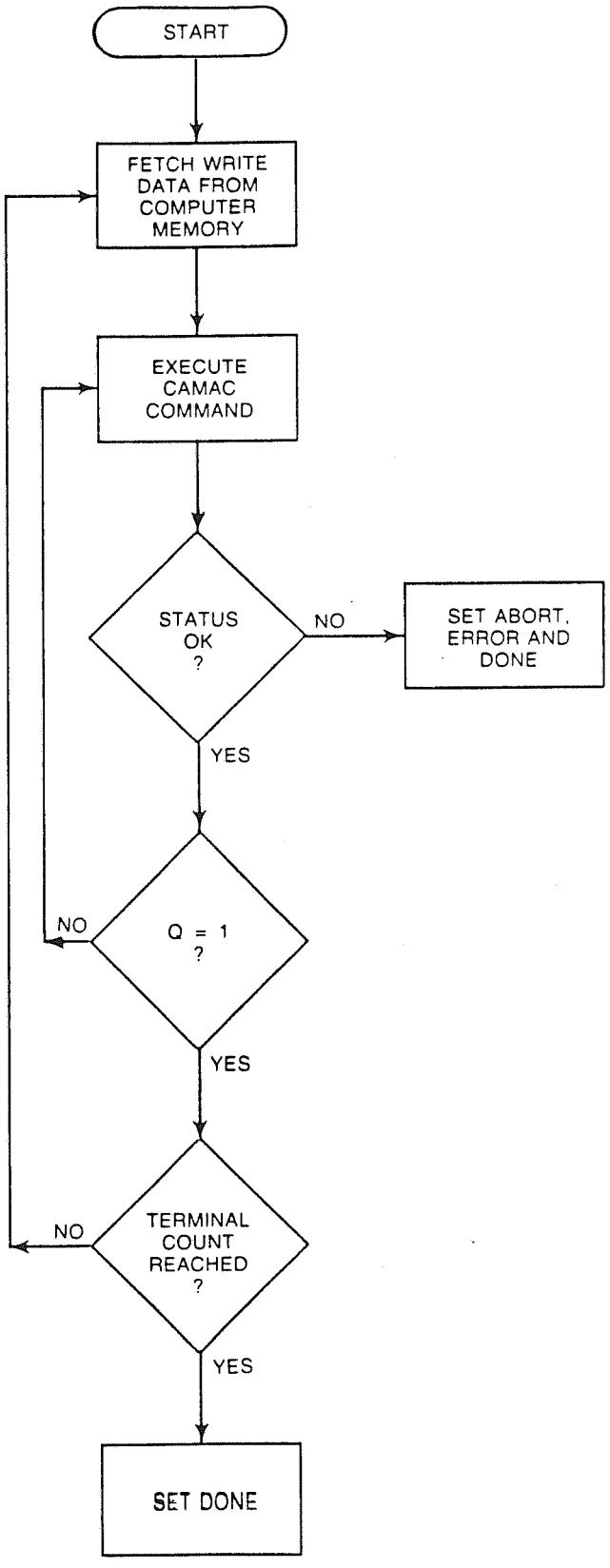
$$\text{ABORT} = \text{QTMO} + \overline{\text{AD}} * \text{NO-X}$$

The following diagram is a simplified flow diagram for Q-Repeat block transfer Writes and Reads.

FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-REPEAT READ COMMANDS



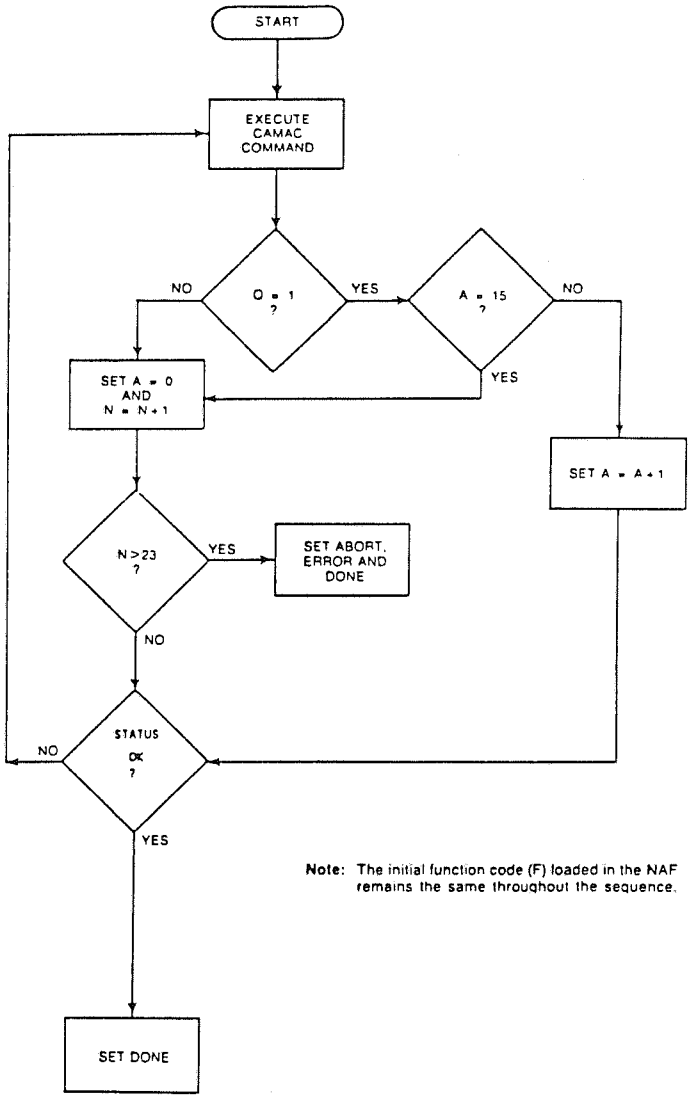
FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-REPEAT WRITE COMMANDS



Q-Scan Block Transfer (TM2=1 : TM1=1)

To select the Q-Scan block transfer mode of operation, set both of the Transfer Mode bits to a "1" when writing to the MCR. During Q-Scan block transfers, the 2927 uses the Q-Response from the previous command to determine the station number (N) and subaddress (A) for the next operation. A Q-Response of zero indicates that the last valid subaddress of the current station number has been accessed. The 2927 responds to a Q-Response of zero by resetting the subaddress, incrementing the station number, and continuing the scan. A Q-Response of one indicates that the last command was executed to a valid CAMAC address. The 2927 responds to a Q-Response of one by either storing the Read data or fetching new Write data. After a Q=1 is received, the 2927 updates the CAMAC address as follows: the subaddress is incremented or, if the subaddress was 15, it is reset to zero, and the station number is incremented. The following flow chart illustrates the updating of the CAMAC station number and subaddress based on the CAMAC Q-response:

FLOW DIAGRAM FOR 2927 Q-SCAN ADDRESS UPDATING



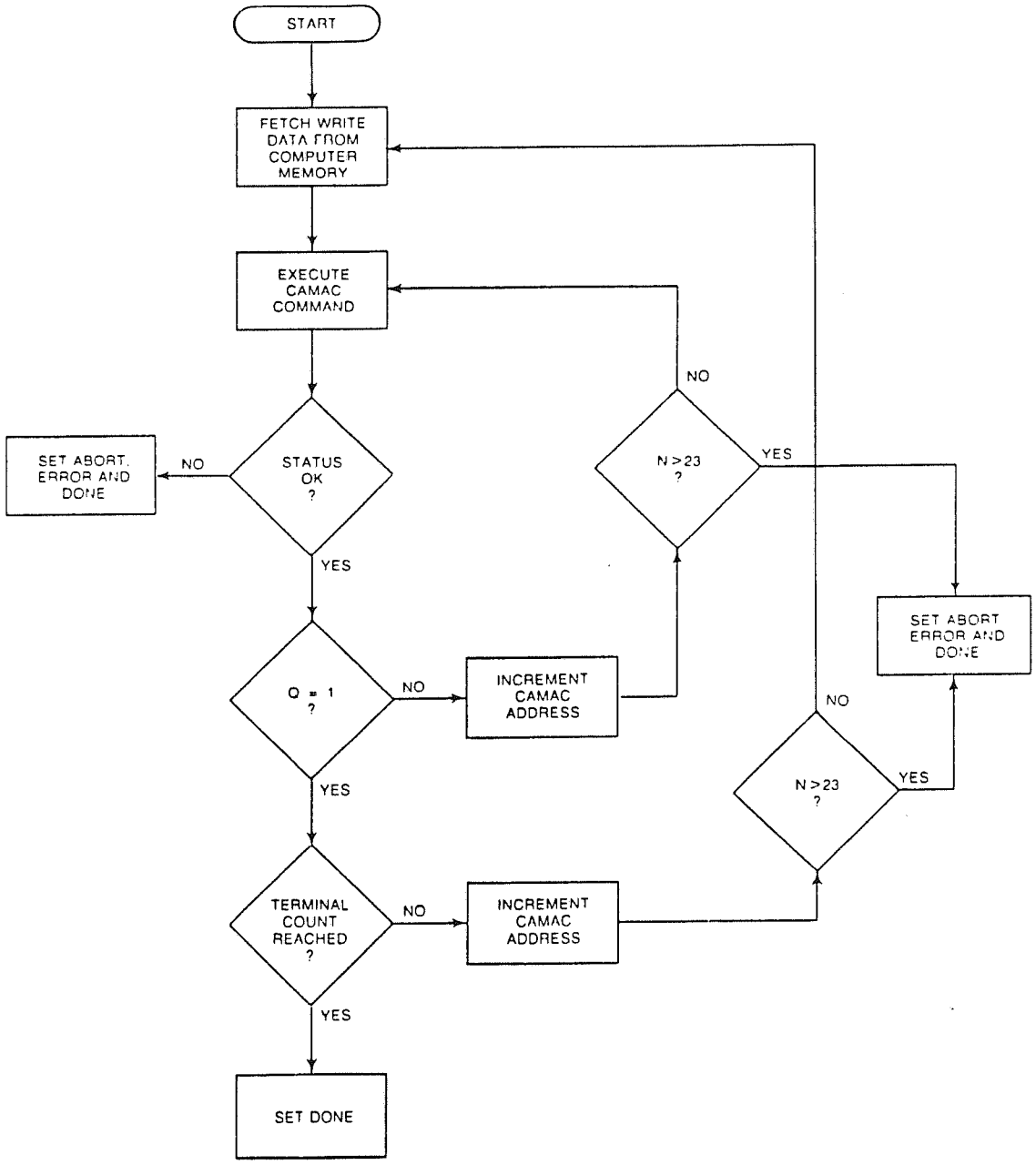
Note: The initial function code (F) loaded in the NAF remains the same throughout the sequence.

If, due to a programming error, the 2927 increments beyond station number 23, the block transfer is terminated with the N>23 bit set in the CSR. The following equation describes ABORT for the Q-Scan block transfer mode:

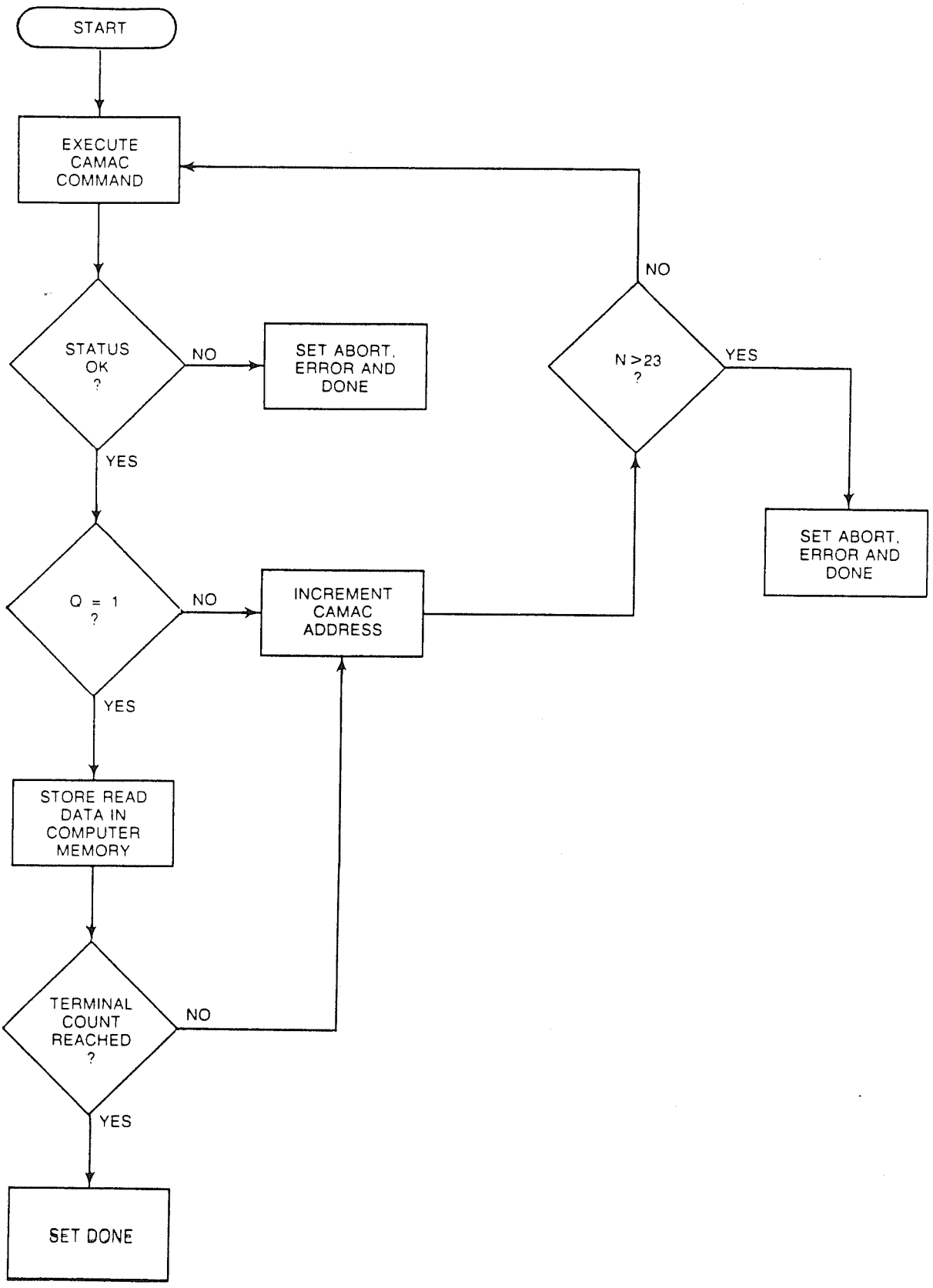
$$ABORT = N>23$$

The following diagram is a simplified flow diagram for Q-Scan block transfer Writes and Reads:

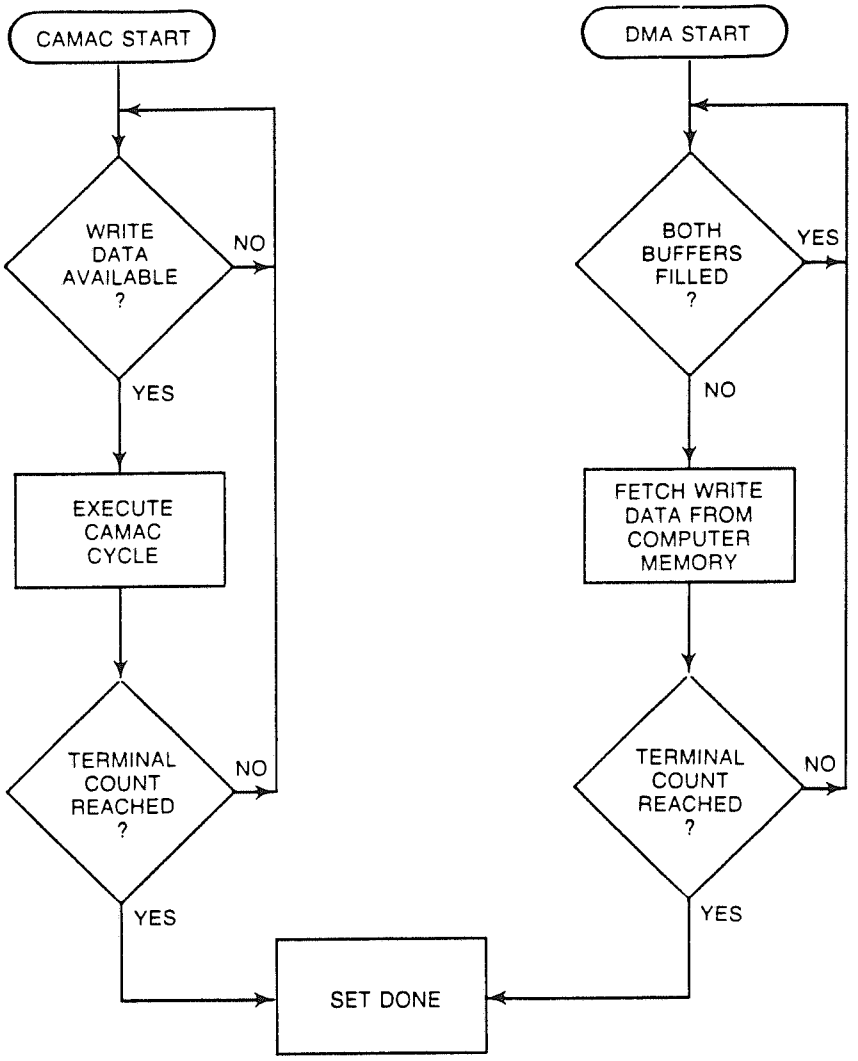
FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-SCAN WRITE COMMANDS



FLOW DIAGRAM FOR 2927 BLOCK TRANSFER Q-SCAN READ COMMANDS



DMA WRITE FLOW DIAGRAMS



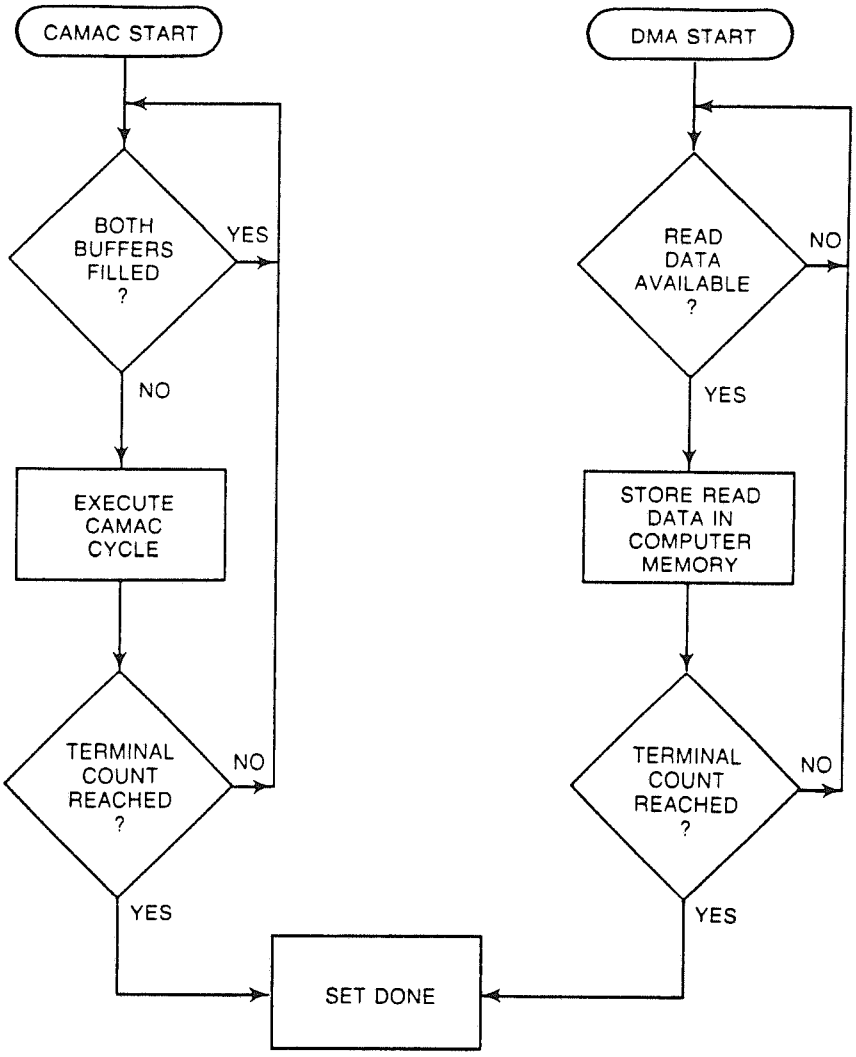
Since CAMAC Write data words are fetched from computer memory regardless of the validity of the previous CAMAC operation, extra programming steps are necessary for continuing these operations which terminate due to an ABORT condition. A bit in the Control/Status register, Buffer Full (bit 10), indicates whether a CAMAC data word is remaining in one of the Write data buffers. If Buffer Full was set at the end of an operation terminated by ABORT, the first buffer contains the CAMAC data word that generated the ABORT and the second buffer contains a CAMAC data word that has not been executed. If Buffer Full is cleared at the end of an operation terminated by ABORT, the first buffer contains the CAMAC data word that generated the ABORT and the second buffer is empty.

The following chart shows the decrement values necessary to restart a Double-Buffered DMA write operation that terminated due to ABORT:

	Buffer Full = 0		Buffer Full = 1	
	16-Bit	24-Bit	16-Bit	24-Bit
Decrement Memory Address by:	2	4	4	8
Decrement Word Count by:	1	2	2	4

In DMA Read operations, the 2927 does not wait for the previous Read data to be stored in computer memory before requesting subsequent Dataway cycles. K-bus cycles are executed as long as there is room in the read data buffers. When both buffers become full, Dataway activity ceases until one of the Read data buffers becomes empty. The DMA process continues as long as there is Read data in one of the buffers and the terminal count has not been reached.

READ FLOW DIAGRAMS



PROGRAMMING THE DMA CONTROLLERS

Due to the design of the PC, minimal programming is needed to setup the DMA controllers for a DMA operation. The Basic Input/Output System (BIOS) in the PC initializes the DMA controllers, leaving a few user supplied parameters to be loaded. The DMA subsection of the PC is made up of two Intel 8237 DMA controller chips which are incorporated into one of the chips of the 5 chip computer set. For a detailed explanation of the DMA controllers, refer to the following books:

1.) "Interfacing to the IBM Personal Computer," by Lewis C. Eggebrecht.

2.) "1985 Microsystem Components Handbook, Volume 1," Intel Corporation, Santa Clara, California.

3.) "Technical Reference - Personal Computer AT," International Business Machines Corporation, Boca Raton, Florida.

The PC contains two DMA controllers. DMA channels 0 through 3 are located in DMA controller 1. These four channels support 8-bit DMA data transfers between 8-bit I/O devices and 8- or 16-bit system memory. Each of the four channels can transfer data throughout the 16-megabyte system memory address space. Each of these channels can transfer 64 kilobytes of data per block transfer. DMA channels 4 through 7 are located in DMA controller 2. Channel 4 is used to cascade DMA controller 1. The remaining three channels support 16-bit DMA data transfers between 16-bit I/O devices and 16-bit memory. Each of these three channels can transfer data throughout the 16-megabyte system memory address space. Each channel can transfer 128 kilobytes of data per block transfer. DMA transfers initiated by these DMA channels cannot start on odd-byte boundaries. The following chart shows the allocation of the DMA controller channels.

DMA Controller 1 (8-Bit)		**DMA Controller 2 (16-Bit)**	
Channel 0	Memory Refresh	Channel 4	Cascade for Controller 1
Channel 1	SDLC	Channel 5	Spare
Channel 2	Floppy Disk	Channel 6	Spare
Channel 3	Spare	Channel 7	Spare

Since both the CAMAC DMA interface and RAM access circuitry only support 16-bit DMA transfers, DMA channels 5, 6, and 7 are the only ones available for use. The following describes only the DMA controller for channels 5 through 7. For completeness, DMA channel 4 is shown but cannot be used, since it is used for cascading the DMA controller for channels 0 through 3.

The 8237 DMA Controller for DMA channels 4 through 7 is located at hex I/O addresses C0 through DF. The I/O Addresses of C0 through CF contain the Write/Read registers for the DMA starting memory address, current memory address, starting word count, and current word count for each channel. The second group of I/O addresses, from hex D0 through DF, contain the Control and Status registers that define each channel's operation. The following table shows the address assignments for the Control and Status Registers:

I/O READ ADDRESS	FUNCTION
0D0	READ STATUS REGISTER
0D2	NOT USED
0D4	NOT USED
0D6	NOT USED
0D8	NOT USED
0DA	READ TEMPORARY REGISTER
0DC	NOT USED
0DE	NOT USED

I/O WRITE ADDRESS	FUNCTION
0D0	WRITE COMMAND REGISTER
0D2	WRITE REQUEST REGISTER
0D4	WRITE SINGLE-MASK BIT REGISTER
0D6	WRITE MODE REGISTER
0D8	CLEAR BYTE POINTER FLIP-FLOP
0DA	MASTER CLEAR
0DC	CLEAR MASK REGISTER
0DE	WRITE ALL MASK REGISTER

WRITE COMMAND REGISTER

The command register is initialized by the BIOS during the power-up sequence. The user need not alter this register's contents.

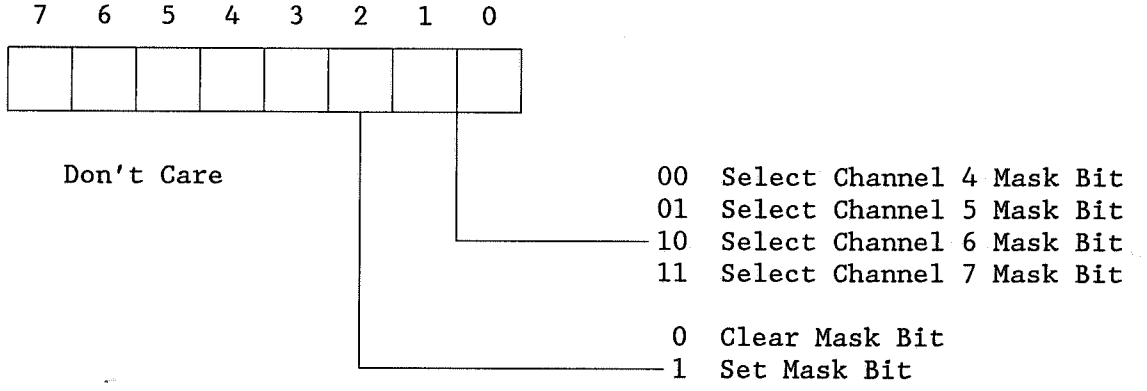
WRITE REQUEST REGISTER

This register is used to generate DMA requests under software control. This register should only be used when the DMA controller is set into the block mode. For normal block transfers operations, this register is not used.

WRITE SINGLE-MASK BIT REGISTER

Writing this register allows the individual DMA channels to be either masked on or off. Clearing the mask bit (writing it to zero) enables the selected channel to operate. Setting the mask bit (writing it to one) disables the selected channel from operating. The following diagram shows the bit pattern of the single-mask bit register:

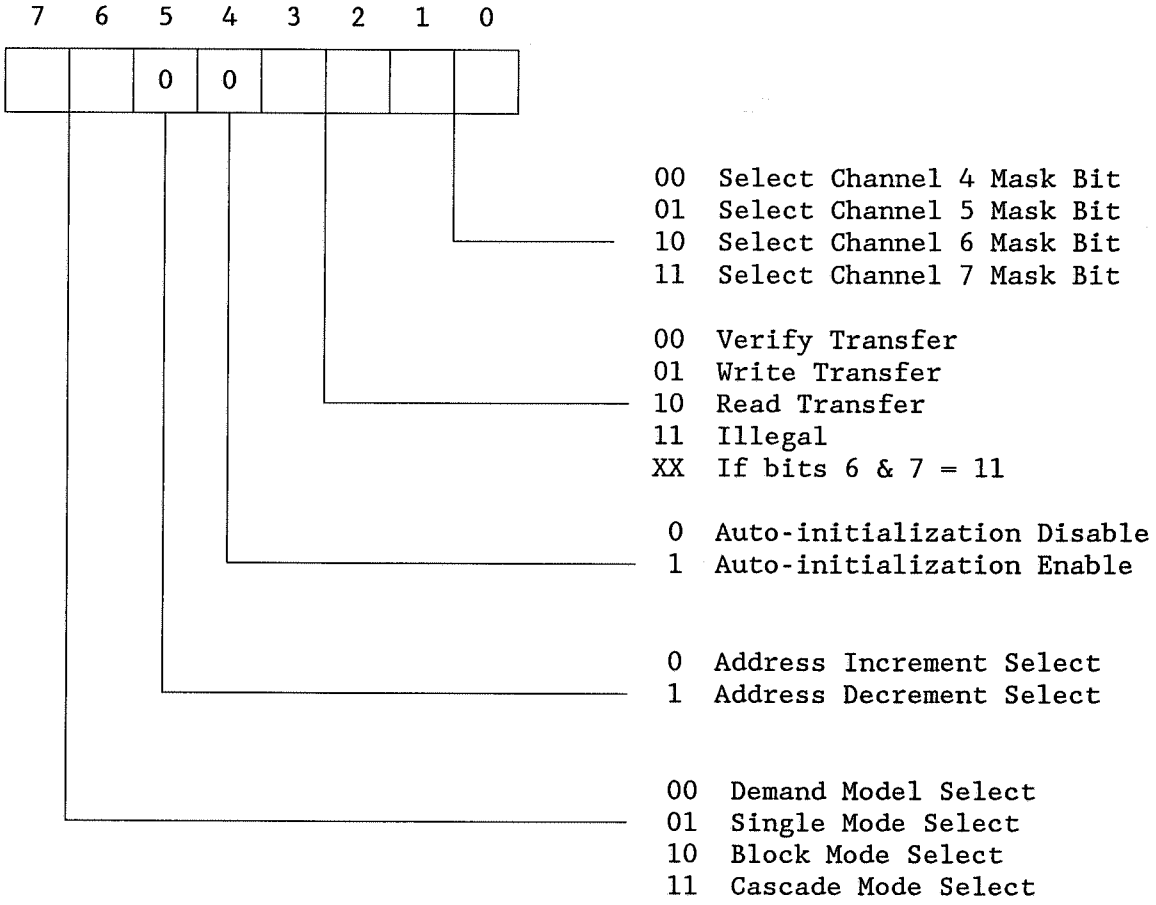
WRITE SINGLE - MASK BIT REGISTER



Write Mode Register

The following diagram shows the bits defined in the Mode Register.

MODE REGISTER



When writing to the Mode Register to setup a CAMAC DMA transfer, bits 4, 5 and 7 should be set to zero and bit 6 set to a one. This, along with the desired channel select enables the appropriate DMA channel for the single block mode of operation. When setting up for using the RAM access feature of the 2927,

RAM access feature of the 2927, bits 4 and 5 are set to zero and bits 6 and 7 are set to one. This, along with the desired channel select enables the appropriate DMA channel for the cascade mode of operation.

Bits 0 and 1 select the channel to be acted upon. Bits 2 and 3 select the DMA transfer mode direction (write or read). Note that the direction that is loaded in this register is in reference to the PC. Therefore, for a CAMAC Write operation, the DMA controller would be setup for read transfers. The 2927 is executing CAMAC Write operations which require the DMA controller to execute reads from memory. Conversely, for CAMAC Read operations, the DMA controller is setup for write transfers. The 2927 is executing CAMAC Read commands which require the DMA controller to execute writes to memory.

CLEAR BYTE POINTER FLIP-FLOP

A write operation to I/O port address 0D8 hex clears the internal flip-flop that is used to select either the high-byte or low-byte for the 16-bit words stored at I/O addresses C0 through CF. Writing to this port address guarantees that the next write or read operation to hex I/O address C0 through CF selects the lower byte first. After writing or reading any address from C0 through CF, the byte pointer flip-flop is toggled which then points to the other byte of the 16-bit word. Note that there is no data associated with this command.

MASTER CLEAR

When an I/O write operation is performed to port address DA hex, the DMA controller is cleared. After the clear is executed, it is then necessary to reinitialize the DMA controller.

CLEAR MASK REGISTER

Writing to this register, at I/O address DC hex, causes all of the DMA channel mask bits to be reset, thus enabling all four channels. It is recommended that this command **NOT** be used.

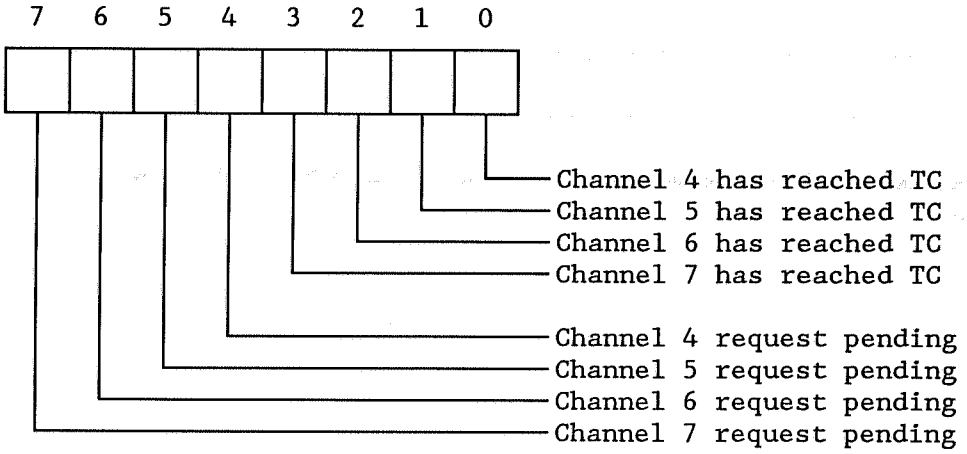
WRITE ALL MASK REGISTER BITS

This register is written at I/O port address of DE hex. It is used to individually and simultaneously control the DMA channels Mask Register bits. It is recommended that this command **NOT** be used.

READ STATUS REGISTER

To obtain the DMA controllers status, execute an I/O read operation to I/O port address D0 hex. This register contains status bits which indicate that a particular DMA channel has reached its terminal count and, thus, has completed a DMA block mode of operation. The register also contains status bits which indicate that a particular channel has a DMA request pending. The following diagram shows the bits defined in the Status Register:

STATUS REGISTER



READ TEMPORARY REGISTER

After a memory-to-memory transfer, the value of the last byte transferred is obtained by reading this register. Since the memory-to-memory transfers are unavailable in the PC environment, this register is not used.

ADDRESS AND WORD COUNT REGISTERS

Each DMA channel has a write/read register for specifying/reading the memory address and a second for the word count. The starting memory address is loaded into the Base Register in the controller by writing to the appropriate I/O address for the desired channel. These registers are updated after each DMA cycle and can be read to obtain the current memory address and word count.

Each of these registers contain 16-bits of data. However, the DMA controllers contain only 8-bit write/read ports. To write the 16-bit word, the lower byte is written to the I/O port address, followed by writing the upper byte to the same port address. To read the 16-bits of data, two I/O read operations are performed to the same I/O port address. Prior to a two-byte read or write operation to the DMA controller, a write operation to I/O port address D8 hex is executed to assure that the Byte Pointer Flip-Flop has been reset to select the lower byte of the 16-bit word.

For DMA channel 5, the I/O address for the Base and Current Address registers is C4 hex. Similarly, the I/O address for the Base and Current Word Count register of channel 5 is C6 hex. For DMA channel 6, the two I/O port addresses are C8 and CA hex, respectively. Note that the first I/O write or read operation to these DMA channel addresses involves register bits 0 through 7. The second operation involves register bits 8 through 15. The following diagram shows the address field which is loaded into the DMA controller's address register:

ADDRESS FIELD DIAGRAM
(LOW BYTE)
FIRST WORD

7	6	5	4	3	2	1	0
A8	A7	A6	A5	A4	A3	A2	A1

FLIP/FLOP = 0

(HIGH BYTE)
SECOND WORD

7	6	5	4	3	2	1	0
A16	A15	A14	A13	A12	A11	A10	A09

FLIP/FLOP = 1

The following chart shows the hex I/O port addresses used in writing and reading the Memory Address and Word Count registers.

CHANNEL	REGISTER	OPERATION	ADDRESS	FLIP FLOP	DATA BUS
4	BASE AND CURRENT ADDRESS	WRITE	C0	0	A1-A8
			C0	1	A9-A16
	CURRENT ADDRESS	READ	C0	0	A1-A8
			C0	1	A9-A16
	BASE AND CURRENT WORD COUNT	WRITE	C2	0	W0-W7
			C2	1	W8-W15
	CURRENT WORD COUNT	READ	C2	0	W0-W7
			C2	1	W8-W15
5	BASE AND CURRENT ADDRESS	WRITE	C4	0	A1-A8
			C4	1	A9-A16
	CURRENT ADDRESS	READ	C4	0	A1-A8
			C4	1	A9-A16
	BASE AND CURRENT WORD COUNT	WRITE	C6	0	W0-W7
			C6	1	W8-W15
	CURRENT WORD COUNT	READ	C6	0	W0-W7
			C6	1	W8-W15
6	BASE AND CURRENT ADDRESS	WRITE	C8	0	A1-A8
			C8	1	A9-A16
	CURRENT ADDRESS	READ	C8	0	A1-A8
			C8	1	A9-A16
	BASE AND CURRENT WORD COUNT	WRITE	CA	0	W0-W7
			CA	1	W8-W15
	CURRENT WORD COUNT	READ	CA	0	W0-W7
			CA	1	W8-W15
7	BASE AND CURRENT ADDRESS	WRITE	CC	0	A1-A8
			CC	1	A9-A16
	CURRENT ADDRESS	READ	CC	0	A1-A8
			CC	1	A9-A16
	BASE AND CURRENT WORD COUNT	WRITE	CE	0	W0-W7
			CE	1	W8-W15
	CURRENT WORD COUNT	READ	CE	0	W0-W7
			CE	1	W8-W15

DMA PAGE REGISTERS

When the DMA controllers are accessing memory, they supply the system address bits A1 through A16. A0 is always forced false (0) since this DMA controller can only perform word accesses to memory. This accounts for 17 of the address bits in the 24 bit address field. The other 7 address bits used during DMA accesses to memory are supplied by the DMA Page Registers. The following diagram shows the address generation for a DMA cycle:

Source	DMA PAGE REGISTER								DMA CONTROLLER																
Address	A23	A22	A21	A20	A19	A18	A17	0	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01

ADDRESS GENERATION DIAGRAM

Each DMA channel has its own DMA Page Register. The following diagram shows the I/O address location for each of the DMA Page registers:

PAGE REGISTER	HEX I/O ADDRESS
CHANNEL 0	87
CHANNEL 1	83
CHANNEL 2	81
CHANNEL 3	82
CHANNEL 5	88
CHANNEL 6	89
CHANNEL 7	8A
REFRESH	8F

DMA PROGRAMMING NOTES

1.) Due to the PC hardware design, the word count is one less than the calculated result; i.e., a word count of 31 for a 24-bit CAMAC data word size results in 16 CAMAC Dataway operations.

2927 REGISTER TABLE

CSR Offset:0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	ABT	INFO TMO	RST	0	PP	RFS	RFS I.E.	DNE	DNE I.E.	0	ID2	ID1	NO X	NO Q	GO

MCR Offset:2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	BLK	TM2	TM1	WS2	WS1	AD

CCR Offset:4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	C4	C2	C1

NAF Offset:6

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RD NAF	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

DLR Offset:8

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W 16	R/W 15	R/W 14	R/W 13	R/W 12	R/W 11	R/W 10	R/W 9	R/W 8	R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1

DHR Offset:A

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	R/W 24	R/W 23	R/W 22	R/W 21	R/W 20	R/W 19	R/W 18	R/W 17

SRR Offset:C

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	C7	C6	C5	C4	C3	C2	C1	C0

TCR Offset:E

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 9	TC 8	TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0

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2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
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5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com