Model 2932-Z1A/Z1B

Macintosh II/QUADRA™ Interface w/DMA

INSTRUCTION MANUAL

September, 1993

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MJS:rem(WP)

KineticSystems Corporation

Standardized Data Acquisition and Control Systems **2932**

Macintosh II/QUADRA™ Interface w/DMA

ADVANCE INFORMATION

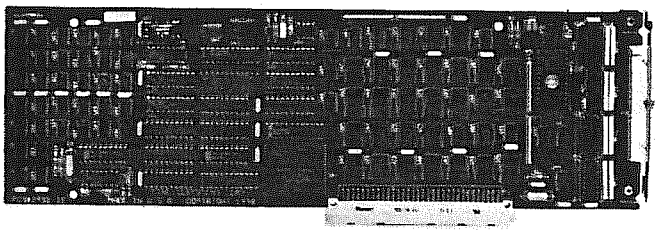
(Rev. Sept. 1993)

FEATURES

- Provides a dedicated Macintosh II through QUADRA 950 Interface
- Used with associated 3922 crate controllers
- Up to eight crate controllers on a single bus
- RS-485 balanced-line signaling between the 2932 and 3922s for high noise Immunity
- Supports crate controller bus lengths to 91 meters (300 feet)
- Supports DMA data transfers
- Provides Interrupt capability for DMA Done and LAM response
- Provides declaration ROM to be called by slot manager

APPLICATIONS

- Interface CAMAC to Macintosh II through QUADRA 950 personal computers
- General-purpose data acquisition and control
- Laboratory automation
- Industrial process control



GENERAL DESCRIPTION

The Model 2932 is a computer bus adapter arranged for use with the NuBus™ implemented on Apple's Macintosh II through QUADRA 950 personal computers. The adapter supports up to eight Model 3922 crate controllers on a Model 5843-Txyz 40-conductor, twisted-pair ribbon cable. (Order this cable separately.) Signaling on this bus is accomplished with RS-485 balanced-line drivers and receivers, giving high noise immunity and allowing an overall cable distance between the 2932 and the last 3922 of up to 91 meters (300 feet). The last 3922 on the Parallel Bus is terminated with a termination card (one provided per 2932).

The 2932 supports DMA transfers between the 2932 and Macintosh memory. Although the Macintosh II does not support block transfers on the NuBus, single or block transfers between the 2932 and 3922 are supported. This allows for speed-efficient transfers (up to 1MByte per second) with the following modes of operation: Q-Scan, Q-Stop, Q-Repeat, and Q-Ignore.

Interrupt capability is provided. An interrupt can be generated by DMA Done or by a pending LAM. In response to a LAM interrupt, the host computer performs a parallel poll of the 3922s via the 2932. In response to the parallel poll, each 3922 requesting service asserts one of the eight data lines (i.e., Crate 3 asserts Data Line 3). This method increases the efficiency of the interrupt service routine in multicrate systems.

INTERNAL REGISTERS

Offset	Mnemonic	Meaning
00	CSR	Control Status Register
04	MCR	Mode Control Register
08	CCR	CAMAC Crate Register
0C	NAF	CAMAC Command Register
10	DR	CAMAC Data Register
14	SRR	Service Request Register
18	WCR	Word Count Register
1C	MAR	Memory Address Register

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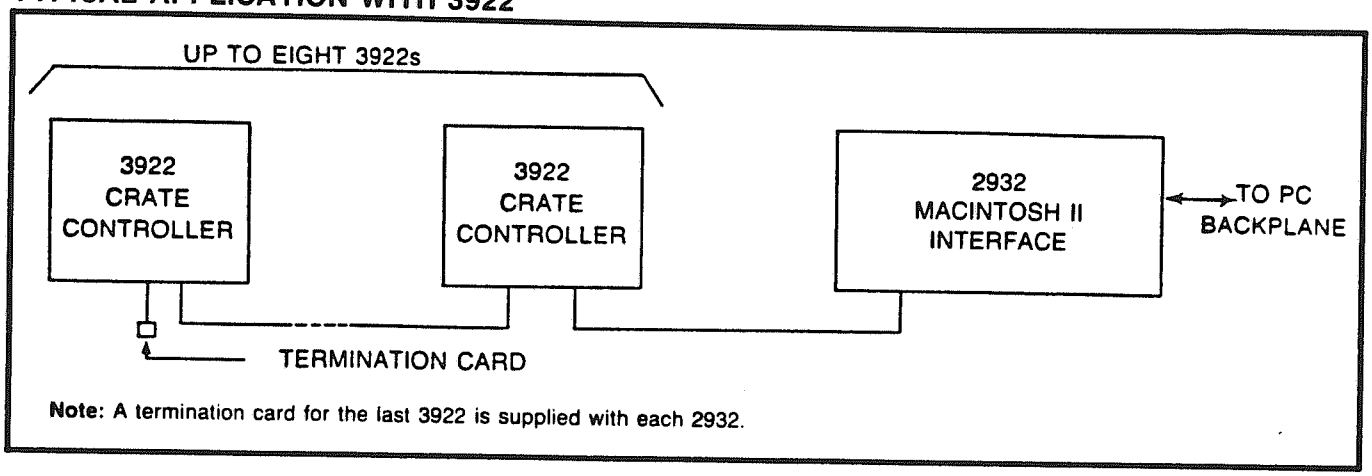
TYPICAL APPLICATION WITH 3922



Note: A termination card for the last 3922 is supplied with each 2932.

ORDERING INFORMATION

Model 2932-Z1A	–	Macintosh II Interface
Model 2932-Z1B	–	Macintosh II through QUADRA 950 Interface
Accessories	–	Model 5843-Txyz Series Interface Bus Cable (required)
	–	Model 3922-Z1A Parallel Bus Crate Controller
	–	Model 6010-1B Macintosh Driver for the Model 2932

INSTALLING THE CRATE CONTROLLER

Operating Option Selections

Determine if the 3922 is to be used as a main crate controller (in a stand-alone system) or as an auxiliary crate controller (with another computer being the main host for the crate). The 3922 is shipped from the factory as a main crate controller. If it is to be used as such, proceed to **Installing the 3922-2932.**

If the 3922 is to be used as an auxiliary crate controller, remove the resistor packs and the resistors from both the left and right (A and B) boards of the 3922. Otherwise, proceed to **Installing the 3922-2932.** To convert the 3922 from a main to an auxiliary crate controller, perform the following operations:

1. Remove the rear panel from the 3922. Retain the screws and PC finger insulation.

2. Remove the two screws that hold the A board to the front panel (the left-hand board when viewed from the front panel).

3. Gently separate the A board from the B board. It might be helpful to **slightly** loosen the two screws that hold the B board to the front panel.

4. On the B (right-hand) board, remove the nine resistor packs located by the Dataway fingers. Also, remove the 100 ohm resistor located between IC locations J and K.

5. On the A board, remove the six resistor packs that are loaded in sockets located on the left-hand side of the PC board. These are marked RN1-RN6.

6. Store the resistor packs for future use.

7. Reassemble 3922 crate controller.

Installing the 3922-2932

Locate the 3922 Crate Controller. Locate the free end of the bus cable (KSC #5843-Txyz) from the 2932. All main crate controllers must be inserted into the right-hand stations of the crate (slots 24 and 25 of a full-size crate). Auxiliary crate controllers can be placed in any available stations **except the main station**. Starting from the rear of the crate, thread the bus cable through the rear I/O opening in the area where the 3922 will be placed. **BE SURE THAT POWER TO THE CRATE IS "OFF".**

Referring to Figures 1 and 2, note the location of the data-bus connectors, DB1 and DB2, on the A board and the Auxiliary Controller Bus (ACB) connector on the B board. With the 3922 facing left side up, connect the bus cable from the 2932 to Connector DB1. Match the key indicator (arrow) on the 3922. Connect the terminator to Connector DB2. Note that the

terminator should also have its key indicator toward the bottom of the module. If two or more 3922s are used, find the bus cable for interconnecting the 3922 with the next one on the bus. Thread this cable through the rear I/O opening in the crate and connect it to Connector DB 2 (with the key toward the bottom of the module). Repeat this operation for all crates on the bus. The last 3922 on the bus will use the terminator in Connector DB2.

Slide the 3922 into the appropriate slots in the crate. Be sure that the bus cable does not "snag". When the 3922 is almost fully inserted, tighten the jackscrew until it is fully seated.

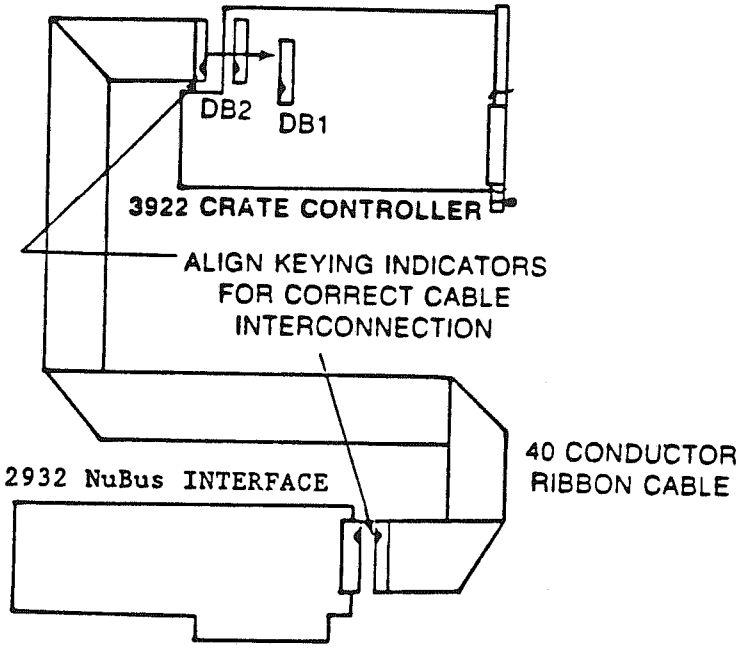


Figure 1: 2932 Cable Interconnection

Notes:

1. N = 30 for all commands.

2. X = 1 is returned for all valid commands.

3. Q = 0 is returned if the front-panel on-line switch is in an "off-line" position. The only command that will be executed when the 3922 is off-line is N(30).F(1).A(0), Read Status Register.

FRONT PANEL SET-UP

Set the front-panel thumb-wheel address switch to the desired address. This is generally "one" for a single-crate system. In multicrate systems, verify that no other 3922 has the same address. The order of addresses need not bear any relationship to the physical order of the crates on the bus. Connect the Request. Connect Grant In, and Grant Out LEMO connectors as appropriate for the system.

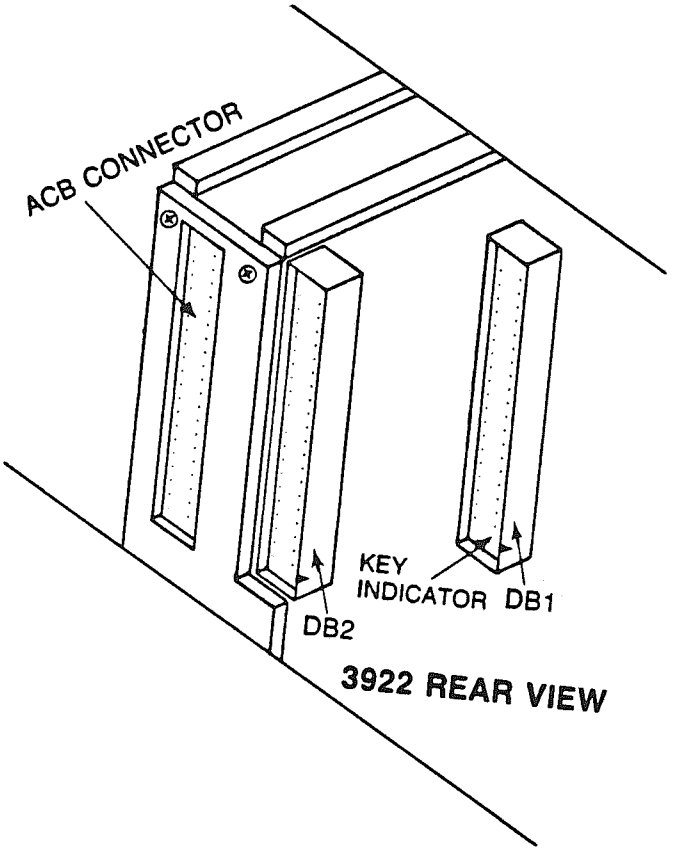


Figure 2: Connector Locations on the 3922

Note that, in a single-controller system, Request MUST be connected to Grant In before the 3922 can function.

Power can now be applied to the CAMAC crate(s).

ADDRESSING

The Base Address for the 2932 is in the form $FSS08000_H$ where S represents the NuBus slot designator.

As an example, if the 2932 was located in NuBus slot D, its Base Address would be $FDD08000_H$.

Model 2932-Z1A/Z1B

The registers on the 2932 are as follows:

Base Address	+ $00\text{-}03_H$	(Control/Status Register)
	+ $04\text{-}07_H$	(Mode Control Register)
	+ $08\text{-}0B_H$	(CAMAC Crate Register)
	+ $0C\text{-}0F_H$	(CAMAC Command Register) (NAF)
	+ $10\text{-}13_H$	(Date Register)*
	+ $14\text{-}17_H$	(Service Request Register)
	+ $18\text{-}1B_H$	(Word Count Register)
	+ $1C\text{-}1F_H$	(Memory Address Register)

Except for the Data Register, these registers require 32 Bit wide (word) NuBus data transactions to and from the registers.

* The Date Register can be written or read using 8-bit (Byte), 16-bit (HALFword), or 32-bit (word) NuBus data transactions.

REGISTER DESCRIPTIONS

The Control/Status Register

The Control/Status Register (CSR) is used to monitor and control 2932 operations. Bit 0 is set to initiate 2932/3922 operations. Bits 1 and 2 contain information regarding the CAMAC, Q, and X-responses. Bits 3-4 reflect the interface identification of the 2932. Bit 5 is set before a Read of the command (NAF) Register. Bit 6 is set to allow an interrupt to be generated upon completion of a CAMAC operation. Bits 7, 14 and 15 reflect operation status. Bit 8 is set to allow an interrupt to be generated when a CAMAC LAM is asserted. Bit 9 is set when a CAMAC LAM is pending. Bit 10 reflects status concerning Q-SCAN and Q-REPEAT operations. Bit 11 is set when a DMA operation initiated by the 2932 resulted in a bus timeout. Bit 12 is set to reset the 2932 to a power-up state. Bit 13 is set when a timeout occurs on the 2932/3922 interconnection bus.

Since the CSR contains Read-Only, Write-Only, and Read/Write bits, two bit patterns are shown. The first pattern shows the bits defined during a read operation and the second one during a write cycle.

CONTROL STATUS REGISTER (CSR) OFFSET: 0_H

31 READ FSS08000-FSS08003$_H$ 16

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ERR	ABRT	INFO TMO	0	NXM	N>23 QRPT TMO	RFS PND	RFS IE	DONE	DONE IE	0	1D2	1D1	NO X	NO Q	0

15 0

31 WRITE FSS08004-FSS08007 16

X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
X	X	X	RST IFC	X	X	X	RFS IE	X	DONE IE	RD NAF	X	X	X	X	GO

15 0

X = Don't Care

BIT	MNEMONIC	DESCRIPTION
31-16	NOT USED	Read as zeros.
15	ERROR	**ERROR** is a read-only bit which is set when an operation is terminated with an error. The following is a logical definition of error:

ERROR = ABORT + INFO TMO + NXM

14 ABORT **ABORT** is a read-only bit which is set when an operation is terminated due to one of the following conditions in the ABORT definition.

$$ABORT = (BM \cdot \overline{TM2} \cdot \overline{TM1} \cdot NOQ) + (BM \cdot TM2 \cdot TM1 \cdot N>23)$$
$$+ (BM \cdot \overline{TM2} \cdot \overline{TM1} \cdot NOX \cdot AD)$$
$$+ (TM2 \cdot \overline{TM1} \cdot QRPT\ TMO)$$

BM	- Block Mode (bit 5 or MCR)
TM2	- Transfer Mode 2 (bit 4 of MCR)
TM1	- Transfer Mode 1 (bit 3 of MCR)
NO-Q	- CAMAC Q-Response = 0 (bit 1 of CSR)
N>23	- Station Number (N) > 23 (bit 10 of CSR)
NO-X	- CAMAC X-response = 0 (bit 2 of CSR)
AD	- Abort Disable (bit 0 of MCR)
QRPT TMO	- Q-repeat Timeout (bit 10 of CSR)

13 INFO TMO **INFORMATION BUS TIMEOUT** is a read-only bit which is set when a timeout has occurred during a 2932/3922 bus transaction.

12 RST IFC **RESET INTERFACE** is a write-only bit which resets the 2932 to a power-up state. This bit is not latched.

11	NXM	**NON-EXISTENT MEMORY** is a read-only bit which is set when the 2932 executes a DMA operation to memory and does not receive a response within 30 microseconds.
10	N>23/QRPT TMO	**STATION NUMBER** (N)>23/Q-Repeat Timeout. This bit is set by one of two conditions: executing Q-SCAN operations and NO-Qs were received, causing the 3922 to scan past station number 23 (the last I/O module slot in the crate); or executing a Q-REPEAT operation and a Q=1 response was not received within 60 milliseconds.
9	RFS PND	**REQUEST-FOR-SERVICE PENDING** is a read-only bit which is set when a CAMAC LAM is pending from a 3922.
8	RFS I.E.	**REQUEST-FOR-SERVICE INTERRUPT ENABLE** is a read/write bit which is set to enable an interrupt when the RFS PND bit is asserted.
7	DONE	**DONE** is a read-only bit which is set when the 2932 has completed an operation. This bit is reset to 0 while the interface is busy.
6	DONE I.E.	**DONE INTERRUPT ENABLE** is a read/write bit which is set to enable an interrupt when the 2932 completes an operation.
5	RD NAF	is set before a read of the CAMAC Command Register. Setting this bit downloads the NAF parameters from the selected 3922 into the 2932.
4-3	ID2, ID1	**INTERFACE ID2 and ID1** are read-only bits. These bits are read as zeros.
2	NO-X	**NO-X.** When set, indicates that the last CAMAC operation executed resulted in an X-response of zero.
1	NO-Q	**NO-Q.** When set, indicates that the last CAMAC operation executed resulted in a Q-response of zero.
0	GO	**GO** is a write-only bit which initiates programmed transfers or DMA operations.

Bits 15-13, 11, 10, 8, and 6 are reset on power-up, NuBus Reset and "RESET INTERFACE". Bit 7, 2 and 1 are set on power-up.

The Mode Control Register

The Mode Control Register (MCR) is used to specify a mode of operation. Bit 5 is set to specify DMA modes of operation and is cleared for programmed (single) transfer modes. Bits 4 and 3 are used to specify the DMA transfer mode (i.e., DMA=1). (These bits are ignored if DMA=0.)

Q-STOP Block Transfer (TM2 = 0: TM1 =0)

To select the Q-STOP block transfer mode, clear both of the transfer mode bits when writing to the MCR. During Q-STOP operations, the CAMAC command specified in the NAF is repeated until a Q-RESPONSE of zero is received or the word count is exhausted. The block transfer will also terminate if an "ERROR" (Bit 15 of the CSR) or "ABORT" (Bit 14 of the CSR) is generated.

The following equations describe "ERROR" and "ABORT" for the Q-STOP block transfer mode.

$$\text{ERROR} = \text{ABORT} + \text{NXM} + \text{INFO TMO}$$

$$\text{ABORT} = \text{NO-Q} + (\overline{\text{AD}} \cdot \text{NO-X})$$

IGNORE-Q Block Transfer (TM2 = 0: TM1 = 1)

To select the IGNORE-Q block transfer mode, set TM2 to 0 and TM1 to 1. During an IGNORE-Q block transfer operation, the CAMAC command specified in the Command Register is repeated until the word count is exhausted. The block transfer will also terminate if an "ERROR" or "ABORT" is generated. The following equations describe "ERROR" and "ABORT" for the IGNORE-Q block transfer mode.

$$\text{ERROR} = \text{ABORT} + \text{NXM} + \text{INFO TMO}$$

$$\text{ABORT} + \overline{\text{AD}} \cdot \text{NO-X}$$

Q-REPEAT Block Transfer (TM2 = 1: TM1 = 0)

To select the Q-REPEAT block transfer mode, set TM2 to 1 and TM1 to 0. During a Q-REPEAT block transfer operation, the CAMAC command loaded in the NAF is repeated for each data word until a Q-RESPONSE of 1 is obtained. A Q-RESPONSE of 1 causes either new write data to be fetched or read data to be stored. The command is repeated for each data word until the word count is exhausted. If a Q=1 response is not obtained within 60 milliseconds, the "QRPT TMO" bit (Bit 10 of the CSR) is set and the operation terminates. The following equations describe "ERROR" and "ABORT" when in the Q-REPEAT block transfer mode.

$$\text{ERROR} = \text{ABORT} + \text{NXM} + \text{INFO TMO}$$

$$ABORT = QRPT\ TMO + (\overline{AD} \cdot NO\text{-}X)$$

Q-SCAN Block Transfer (TM2 = 1: TM1 = 1)

To select the Q-SCAN block transfer mode of operation, set both TM2 and TM1 to one. During Q-SCAN block transfers, the 3922 uses the Q-RESPONSE from the previous command to determine the station number (N) and subaddress (A) for the next operation. A Q-RESPONSE of zero indicates that the last valid subaddress of the current station number has been accessed. The 3922 responds to a Q=0 by resetting the subaddress, incrementing the station number, and continuing the scan. A Q-RESPONSE of one indicates that the last command was executed to a valid CAMAC address. The 2932/3922 responds to a Q=1 by either storing the read data or fetching new write data. When a Q=1 response is obtained, the 3922 updates the CAMAC address as follows: the subaddress is incremented or, if the subaddress was 15, it is reset to zero, and the station number is incremented. If, due to a programming error, the 3922 increments beyond station number 23, the block transfer will terminate with the "N>23" bit (Bit 10 of the CSR) set. The following equation is the definition of "ERROR" and "ABORT" when using the Q-SCAN mode of operation.

$$ERROR = ABORT + NXM + INFO\ TMO$$
$$ABORT = N>23$$

Bits 2 and 1 are used to specify the CAMAC word size and affect both DMA and programmed control transfers. Bit 0 is used to enable/disable block transfer termination on the receipt of a NO-X response (X=0). All bits in the MCR are cleared on power-up, NuBus Reset, and "RESET INTERFACE". All bits specified in the MCR are read/write bits.

MODE CONTROL REGISTER (MCR) OFFSET: 4_H

FSS08004 - FSS08007$_H$

31															16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	DMA	TM2	TM1	WS2	WS1	AD
15															0

BIT	MNEMONIC	DESCRIPTION
31-6	Not Used	Read as zeros.
5	DMA	**DIRECT MEMORY ACCESS** is set to a 1 to specify DMA modes of operation. The transfer mode type is selected by TM2 and TM1.
4-3	TM2,TM1	**TRANSFER MODE 2 AND 1** are used for selecting the transfer mode type:

TM2	TM1	TRANSFER MODE
0	0	Q-STOP
0	1	IGNORE-Q

1	0	Q-REPEAT
1	1	Q-SCAN

These bits are ignored during programmed transfers (i.e., DMA=0).

2-1 WS2,WS1 **WORD SIZE 2 and 1** are used to select the size of the CAMAC word to be transferred. These bits affect both DMA and programmed transfer operations:

WS2	WS1	CAMAC WORD SIZE
0	0	24 Bit
0	1	16 Bit
1	0	8 Bit
1	1	RESERVED

0 AD **ABORT DISABLE** is set to a 1 to disable block transfer termination due to a NO-X (X=0) response. This bit is ignored on Q-SCAN operations.

The CAMAC Crate Register

The CAMAC Crate Register (CCR) selects the "current crate" for all addressed operations. All operations executed by the 3922 are directed to the crate specified in the CAMAC Crate Register. Legal crate addresses range from 0 to 7. This register is reset on power-up, NuBus Reset, and "RESET INTERFACE". These are write/read bits.

CAMAC CRATE RESISTER (CCR) OFFSET: 8_H

FSS08008 - FSS0800BH

31														16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	C4	C2	C1
15															0

BIT	MNEMONIC	DESCRIPTION
31-3	Not Used	Read as zeros.
2-0	C4,C2,C1	**CRATE ADDRESS 4, 2 and 1** are used to specify which 3922 is accessed during addressed operations. The crate address may range from zero to seven.

The CAMAC Command Register

The CAMAC Command Register (NAF) is used to specify the CAMAC station number (N), subaddress (A), and function code (F) to be used during a CAMAC operation.

When the NAF register is read, the data contained in the NAF register for the "current crate" is returned. If the register is written, the NAF data for the "current crate" is updated. These registers are actually located on the 3922 crate controllers and not on the 2932. Thus, when I/O commands are executed to the NAF register, a bus transfer is executed between the 2932 and 3922. When writing the NAF Register, once the 2932 has received the data, it will automatically start a transfer to the "current crate". The "DONE" bit in the CSR will be cleared until the transfer is complete. When reading the NAF, bit 5 of the CSR must first be set. This will cause the 2932 to download the NAF of the "current crate". Again the "DONE" bit will be cleared until the transfer is complete. Once DONE is set, the NAF of the "current crate" can be read.

THE CAMAC COMMAND REGISTER (NAF) OFFSET: OC_H

FSS0800C - FSS0800FH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

BIT	MNEMONIC	DESCRIPTION
31-14	Not Used	Read as zeros.
13-9	N16-N1	**STATION NUMBER 16 to 1** specifies which CAMAC station number, N (1) through N (31), is to be addressed by the CAMAC operation. For Q-Scan operations, this is the initial slot to be accessed.
8-5	A8-A1	**SUBADDRESS 8 to 1** specifies which CAMAC subaddress, A (0) through A (15), is to be used by the addressed CAMAC operation. For Q-Scan operations, this is the first subaddress in the initial station number to be accessed.
4-0	F16-F1	**FUNCTION CODE 16 to 1** selects the CAMAC function code, F (0) through F (31). The choice of function code and subaddress to be used for a particular transfer is dependent on the I/O module being addressed by N. Refer to the Instruction Manual for the module in question.

F16	F8	RANGE	COMMAND TYPE
0	0	F(0) — F(7)	READ
0	1	F(8) — F(15)	CONTROL
1	0	F(16) — F(23)	WRITE
1	1	F(24) — F(31)	CONTROL

The Data Register

The Data Register (DR) is used to access the CAMAC data word. During a CAMAC write operation, [F(16)-F(23)] the contents of the Data Register are used to generate the data signals on the CAMAC write data lines (W24 through W1). During a CAMAC read operation, [F(0)-F(7)], the Data Register is loaded with the data signals present on the CAMAC read data lines R24 through R1.

This is a unique register. The Data Register can be accessed through Nubus word, HALFword and Byte transactions. The advantage of this feature is, it allows the user to access only the Bytes that will be transferred on the CAMAC cycle. Example: if a CAMAC Read operation was executed with the CAMAC word size set to 16-bits, the 3922 would only transfer the lower 16-bits to the Data Register. Thus, if a Nubus word transaction was then executed to obtain the results, bits 23-16 would contain the data from the last 24-bit CAMAC Read. If a Nubus HALFword transaction was executed, only the 16-bits of concern would be obtained.

DATA REGISTER (DR) OFFSET: 10_H

FSS08010 - FSS08013$_H$

31															16
0	0	0	0	0	0	0	0	24	23	22	21	20	19	18	17
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
15															0

BIT	MNEMONIC	DESCRIPTION
31-24	Not Used	Read as zeros.
23-0	R/W24-RW1	**R/W24-R/W1** provide access to the CAMAC data word.

The Service Request Register

The Service Request Register (SRR) provides information regarding CAMAC Look-at-Me signals (Request-for-Service) in a multicrate system. When this register is read, the 2932 issues a Parallel Poll to all 3922s connected to the bus.

The 8-bits represent the eight possible crate addresses. A true bit (1) in the SRR indicates that its associated crate is asserting the LAM Request-for-Service line. If any 3922 is requesting service, the "RFS PND" (Bit 9 of the CSR) is set.

SERVICE REQUEST REGISTER (SRR) OFFSET: 14_H

FSS08014 - FSS08017$_H$

31															16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	L_{C7}	L_{C6}	L_{C5}	L_{C4}	L_{C3}	L_{C2}	L_{C1}	L_{C0}
15															0

BIT	MNEMONIC	DESCRIPTION
31-8	Not Used	Read as zeros.
7-0	L_{C7}-L_{C0}	L_C **7-0** are set when their associated crate addresses are requesting service.

The Word Count Register

The Word Count Register (WCR) is used to specify the number of transfers to or from computer memory during a DMA mode of operation. The two's complement of the number of words to be transferred is loaded in the WCR. All bits in the WCR are read/write bits.

WORD COUNT REGISTER (WCR) OFFSET: 18_H

FSS08018 - FSS0801B$_H$

31															16
32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
15															0

The Memory Address Register

The Memory Address Register (MAR) is used to specify the address field used by the 2932 for DMA transfers to or from computer memory. All bits in the MAR are read/write bits.

MEMORY ADDRESS REGISTER (MAR) OFFSET: $1C_H$

FSS0801C - FSS0801F$_H$

31															16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A0
15															0

2932 OPERATING MODES

Programmed Transfers

The 2932 provides a programmed transfer mode of operation. Under programmed transfer, all transfers to or from the 2932 are done via programmed I/O. Programmed transfers may be executed with either 8-, 16-, or 24-bit CAMAC data words. The size of the data word

transferred is determined by setting the Word Size bits (bits 2 and 1) in the Mode Control Register. The Transfer Mode bits (bits 4 and 3 of the MCR) are ignored in programmed transfer modes.

NOTE: When executing 8- or 16-bit word size read commands, the CAMAC data register on the 2932 is updated with the corresponding number of bits. As an example, assume a 24-bit read operation has occurred to a module with all data bits true. After this operation, the Data Register contains FFFFFFFF. If an 8-bit CAMAC read is then executed to a module with all bits false, the Data Register contains FFFFFF00. Only the low-order bits are transferred to the Data Register on the 8-bit read operation.

The following describes the sequences necessary to execute CAMAC read, write and control functions using programmed transfers.

Programmed Transfer Read Operation (F16=0: F8=0)

1. Load the crate address for the CAMAC operation in the CCR.
2. Load the CAMAC NAF command in the Command Register.
3. Wait for DONE (Bit 7) in the CSR to become true.
4. Load the MCR with:
   a. DMA (bit 5) set to 0.
   b. The appropriate CAMAC data word size WS2, WS1 (bits 2 and 1).
   c. Set or clear AbortDisable (bit 0) as required.
5. Load the CSR with:
   a. Set or clear DONE interrupt enable (bit 6) as required (See Note Below).
   b. GO (bit 0) set to 1.
6. Wait for DONE (bit 7) in the CSR to become true.
7. Fetch the CAMAC read data from the Date Register.
8. Read the CSR to check for any errors.

Programmed Transfer Control Operation (F16=0: F8=1 or F16=1: F8=1)

1. Load the crate address for the CAMAC operation in the CCR.
2. Load the CAMAC NAF command in the Command Register.

3. Wait for DONE (Bit 7) in CSR to become true.

4. Load the MCR with:

   a. DMA (Bit 5) set to 0.
   b. Set or clear AbortDisable (Bit 0) as required.

5. Load the CSR with:

   a. Set or clear DONE interrupt enable (Bit 6) as required (See Note Below).
   b. GO (Bit 0) set to 1.

Programmed Transfer Write Operation (F16=1: F8=0)

1. Load the crate address for the CAMAC operation in the CCR.

2. Load the CAMAC NAF command in the Command Register.

3. Wait for DONE (Bit 7) in CSR to become true.

4. Load the MCR with:

   a. DMA (Bit 5) set to 0.
   b. The appropriate CAMAC data word size WS2, WS1 (bits 2-1).
   c. Set or clear AbortDisable (Bit 0) as required.

5. Load the CAMAC write data word in the DR.

6. Load the CSR with:

   a. Set or clear DONE interrupt enable (Bit 6) as required (See Note).
   b. GO (Bit 0) set to 1.

7. Wait for DONE (Bit 7) in the CSR to become true.

8. Read the CSR to check for any errors.

NOTE: When using the 2932 with interrupts enabled, ignore the step which includes waiting for "DONE" since the assertion of the "DONE" bit generates an interrupt.

The following are definitions for ERROR and ABORT when executing operations in the programmed transfer mode.

$$ABORT = NO\text{-}X \cdot \overline{AD}$$

$$ERROR = ABORT$$

where

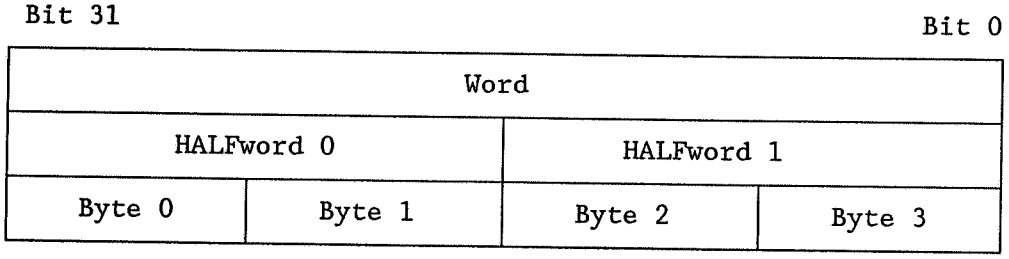
NO-X is the NO-X response bit (Bit 2) of the CSR

AD is AbortDisable (Bit 0) of the MCR

Block Transfer

The 2932 supports four types of DMA transfers: Q-Stop, Q-Ignore, Q-Repeat and Q-Scan. In each of these modes, the initial conditions are loaded under programmed I/O. Data transfers to or from computer memory are done using Direct Memory Access (DMA) through the Nubus slot.

Nubus supports reads and writes of three data sizes: Byte (8), HALFword (16), and Word (32). The base unit of addressability is a Nubus word. A Nubus word can then be broken down into 2-HALF words or 4 Bytes.



When addressing MAC Memory, the Nubus Address AD32-AD2 specifies the word, while AD1-AD0 specifies which Byte or group of Bytes (within the word) will be transferred between Nubus and computer memory.

This arrangement of decoding makes it necessary to modify Bits A1 and A0 when loading the Memory Address Register (MAR), since these bits, along with WS2 (Bit 2 of MCR), determine what part of the Nubus word will be transferred. The CAMAC word size must be taken into consideration when selecting the initial state of A1 and A0. The table below shows the correlation between WS2 and Address Bits A1-A0. WS2 along with Address Bits A1 and A0 specify the transfer mode (Byte, Halfword, Word). That mode also determines which part of the Addressed Word is to be transferred.

Model 2932-Z1A/Z1B

(MCR) WS2	(MAR) A1	(MAR) A0	
H	H	H	Byte 3
H	H	L	Byte 2
H	L	H	Byte 1
H	L	L	Byte 0
L	H	H	HALFword 1
L	H	L	- - - - -
L	L	H	HALFword 0
L	L	L	Word

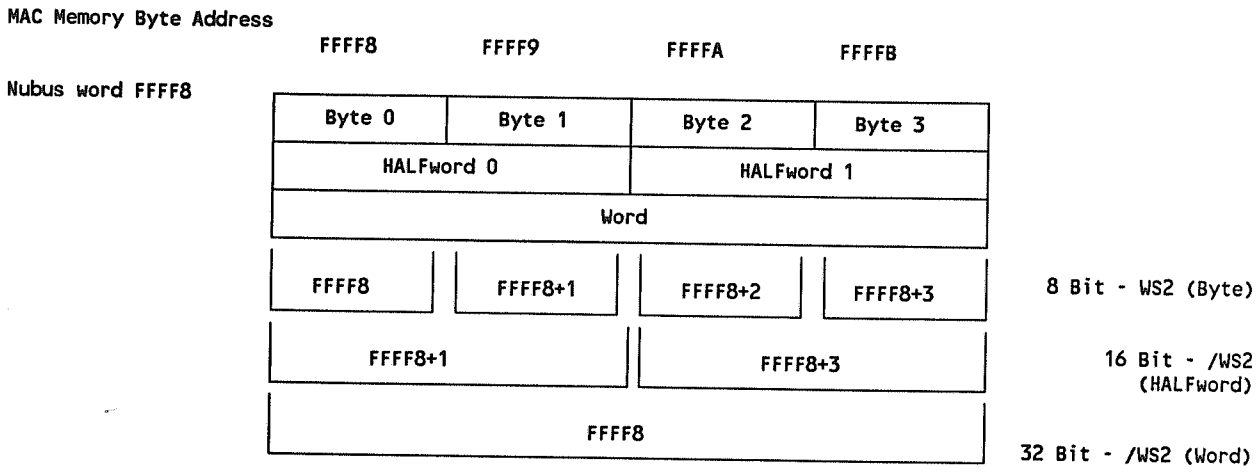
If the CAMAC wordsize is set to 8 Bits (WS2=1, WS1=0 in MCR), the Nubus transfer will be a Byte transfer. Bits A1 and A0 in MAR determine which Byte of the word specified by Bits AD32-AD2 will be transferred first. Once the transfer is complete, the MAR is incremented by 1 to the next Byte and transferred. This is repeated until the DMA operation is complete.

If CAMAC wordsize is set to 16 Bits (WS2=0, WS1=1 in MCR), the Nubus transfer will be a HALFword transfer. Bits A1 and A0 in the MAR will determine which HALFword will be transferred from the specified word. Once the transfer is complete, the MAR is incremented by 2 to the next HALFword and transferred. This is repeated until the DMA operation is terminated.

If CAMAC wordsize is set to 24 Bits (WS2=0, WS1=0), then A1 and A0 would both be set low which would result in a word transfer. Once the transfer is complete, the MAR is incremented by 4 to the next word and so on. In a word transfer, the upper Data Byte (Bits 31-24) is a Dummy Byte with all Bits false.

Example 16 Bit Write:

If 16-Bit Data is stored starting at Memory Address $FFFF8_H$ and a retrieve is desired (CAMAC Write), Nubus HALFword transfers would be used. The MAR should be loaded with $FFFF8_H$ +1 since data is starting at HALFword 0 of Nubus word FFFF8.



Example 8 Bit Read:

If 8 Bit data is being Read from CAMAC and Data storage is desired starting at memory location FFFFA, Nubus byte transfers should be used and the MAR should be loaded with FFFF8+2 since FFFFA is Byte 2 of word FFFF8.

NOTE: A Nubus word boundary is a memory address with both address bits A1 and A0 False: e.g., FFFF0, FFFF4, FFFF8, FFFFC.

The following describes the sequence necessary to execute CAMAC read or write commands in the block transfer mode.

Read or Write Block Transfer Register Loading Sequence

1. Load the crate address for the block transfer in the CCR.
2. Load the CAMAC NAF command in the Command Register.
3. Wait for DONE (Bit 7) to be true in CSR.
4. Load the MCR with:
   a. DMA (Bit 5) set to 1.
   b. TM2 (Bit 4) and TM1 (Bit 3) as required.

TM2	TM1	OPERATION
0	0	Q-STOP
0	1	IGNORE-Q
1	0	Q-REPEAT
1	1	Q-SCAN

c. WS2 (Bit 2) and WS1 (Bit 1) as required.

WS2	WS1	WORD SIZE
0	0	24-Bit
0	1	16-Bit
1	0	8-Bit
1	1	RESERVED

d. Set or clear AbortDisable as required.

5. Load the starting address of the data list in the MAR with Bits A1 and A0 set appropriately.

6. Load the two's complement of the number of DMA transfers between the 2932 and computer memory in the WCR.

7. Load the CSR with:

   a. Set or clear DONE interrupt enable as required (See Note).
   b. GO (Bit 0) set to 1.

8. Wait for "DONE" in the CSR to become true.

9. Read the CSR to check for any errors.

NOTE: When using the 2932 with interrupts enabled, ignore the step which includes waiting for the "DONE" bit since the assertion of "DONE" generates an interrupt.

ERROR RESTART OF BLOCK TRANSFERS

Since the CAMAC data is buffered on both the 2922 and the 3922, the memory address registers and word counts do not reflect the actual number of CAMAC words transferred. Therefore, certain modes of operation terminated by an "ERROR" cannot be restarted due to the indeterminate number of data words transferred.

Operations that cannot be restarted include:

1. Any operation terminated by a NO-X condition.

2. Any read operation executed with the 3922 enabled in the "double buffer" mode. (For information on double buffer mode see Model 3922 Crate Controller "Features and Operations".

3. Q-REPEAT or Q-SCAN writes.

4. Q-STOP block transfer write that terminates with a Q=0 and the word count is exhausted.

The following describes the necessary steps involved for restarting block transfers that terminate due to an "ERROR" or "ABORT".

Q-STOP reads terminated by a Q=0:

	8-Bit	16-Bit	24-Bit
Decrement MAR by	1	2	4
Decrement WCR by	1	1	1

After resetting the MAR and WCR, restart the operation by setting "GO".

Q-STOP writes terminated by a Q=0, while the word count is not exhausted: it will be necessary to read the 3922 status register to determine the state of bit 15, "Write Buffer Full". This bit is set when an operation terminates due to a Q-0 response, during a Q-STOP block transfer operation, and the 3922 is "holding" one more CAMAC write data word in its buffer.

	WRITE BUFFER FULL=0			WRITE BUFFER FULL=1		
	8-Bit	16-Bit	24-Bit	8-Bit	16-Bit	24-Bit
Decrement MAR by	5	6	12	6	8	16
Decrement WCR by	5	3	3	6	4	4

After resetting the MAR and WCR, restart by setting "GO".

Q-REPEAT reads terminated by Q-REPEAT Timeout (QRPT TMO): restart by setting "GO".

2932/3922 INTERCONNECTION BUS

The interconnection bus is a 40-wire twisted pair ribbon cable that runs from the 2932's I/O connector to the first 3922 Crate Controller in the CAMAC system. Parallel connectors on the 3922s permit the expansion of this bus to as many as eight CAMAC crates. Balanced RS-485 signalling is used between the 2932 and 3922s to enhance performance.

The interconnection bus is a multiplexed 8-bit address/data bus. Before data transfers occur on the bus, the 2932 enables a header byte which enables 1 of the 3922s to either receive or transmit data. Each 3922 is preset to a unique crate address via front-panel switch used to compare with the incoming header byte. If a 3922 recognizes its crate address, it prepares for the data transfer portion of the cycle. An information-bus-timeout (INFO TMO) will occur if a header byte is asserted and the addressed 3922 does not respond within 7 microseconds.

The protocol for single-CAMAC-word transfers, which depends upon the word size selection in the header byte (8-, 16- or 24- bit), is as follows:

8-bit CAMAC word size	ADDRESS/DATA LO
16-bit CAMAC word size	ADDRESS/DATA LO/DATA MID
24-bit CAMAC word size	ADDRESS/DATA LO/DATA MID/DATA HI

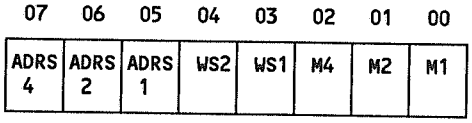
Note that the ADDRESS is transmitted by the 2932, while DATA is transmitted by either the 2932 or 3922, depending upon the data direction (read or write operation).

For multiple-CAMAC-word transfers, a single ADDRESS header is followed by the data, as shown:

ADDRESS/CAMAC WORD 1/CAMAC WORD 2/. . . ./CAMAC WORD N

Note that the CAMAC word contains one, two, or three bytes of data, depending upon the word-size selection in the ADDRESS header. Dataless CAMAC operations (F8=1) involve only the ADDRESS header, with no data following.

The header byte is shown below:



NOTE: The Header Byte is composed by selected bits within the 2932 registers, this Byte as shown is transparent.

BIT MNEMONIC DESCRIPTION

7-5 Address Binary 3922 Crate Address - Selects Crate Address 0-7.

4-3 Word Size

WS2	WS1	Word Size
0	0	24-bit
0	1	16-bit
1	0	8-bit
1	1	RESERVED

2-0 Mode Select

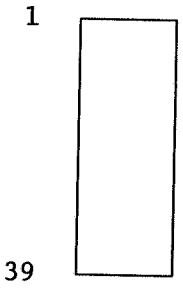
Binary Operations Mode

M4	M2	M1	OPERATION
0	0	0	Q-STOP Operation
0	0	1	IGNORE-Q Operation
0	1	0	Q-REPEAT Operation
0	1	1	Q-SCAN Operation
1	0	0	SINGLE Operation
1	0	1	RESERVED
1	1	0	NAF1 (Lower byte of NAF)
1	1	1	NAF2 (Upper byte of NAF)

The following shows the signals present on the interconnection bus along with a brief description of their function.

Dataway Q	DWQ	When asserted, indicates that the current Dataway operation gave a Q=1 response: Q=0 if negated.
Dataway X	DWX	When asserted, indicates that the current Dataway operation gave a X=1 response: X=0, if negated.
Data Read	DRD	When asserted, indicates that the 3922 should supply read data.
Data Write	DWT	When asserted, indicates that write data is available to the 3922.
Info Bus	$D_{<7:0>}$	Used for address, R/W data, and parallel poll information.
Look-At-Me	LAM	When asserted, indicates that a LAM request for service is pending. Multiple 3922s may assert this line.
Master Busy	MBSY	When asserted, indicates that Address information can be strobed into the 3922. This is negated to indicate "End of Transfer" or to abort the present transfer.
Parallel Poll	Poll	When asserted, indicates that a Parallel Poll operation is in progress.
Slave Busy	SBSY	When asserted, indicates that the addressed 3922 has not yet completed a data transaction. When negated, indicates that the 3922 has completed the transaction. This line can be negated by the 3922 to abort the present transfer.
Slave Flag	SFLG	Asserted by a 3922 to indicate a Reply Response from either a DRD or DWT.
Slave F8	SF8	When asserted, indicates that F8=1 in the "CURRENT" 3922.
Slave F16	SF16	When asserted, indicates that F16=1 is in the "CURRENT" 3922.

PIN OUT



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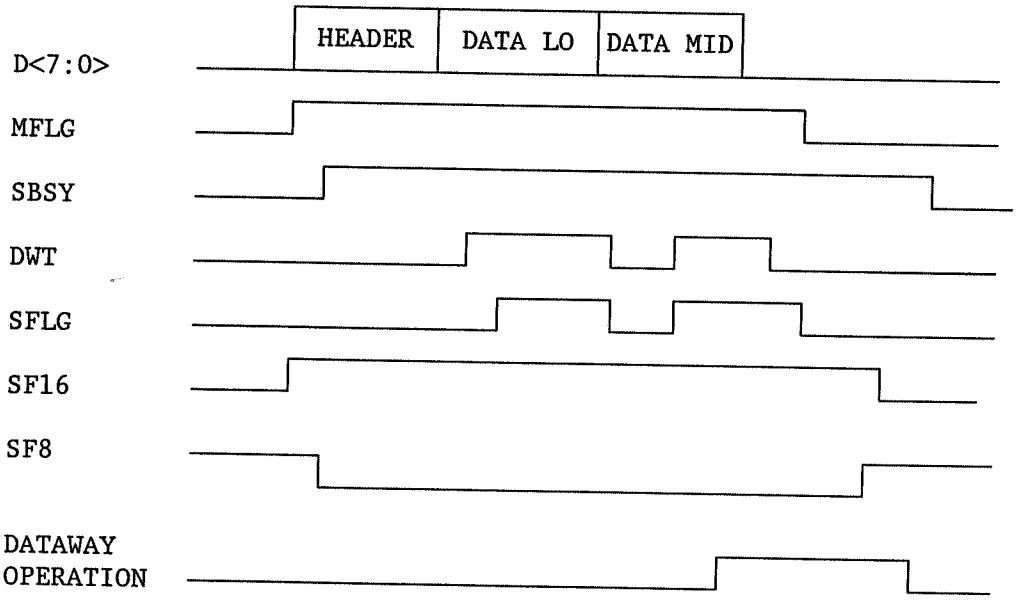
FACE VIEW

Pin		Pin	
1	MBSY	21	DWX
2	/MBSY	22	/DWX
3	GND	23	LAM
4	GND	24	/LAM
5	SFLG	25	D7
6	/SFLG	26	/D7
7	DWT	27	D6
8	/DWT	28	/D6
9	DRD	29	D5
10	/DRD	30	/D5
11	SF8	31	D4
12	/SF8	32	/D4
13	SF16	33	D3
14	/SF16	34	/D3
15	POLL	35	D2
16	/POLL	36	/D2
17	SBSY	37	D1
18	/SBSY	38	/D1
19	DWQ	39	D0
20	/DWQ	40	/D0

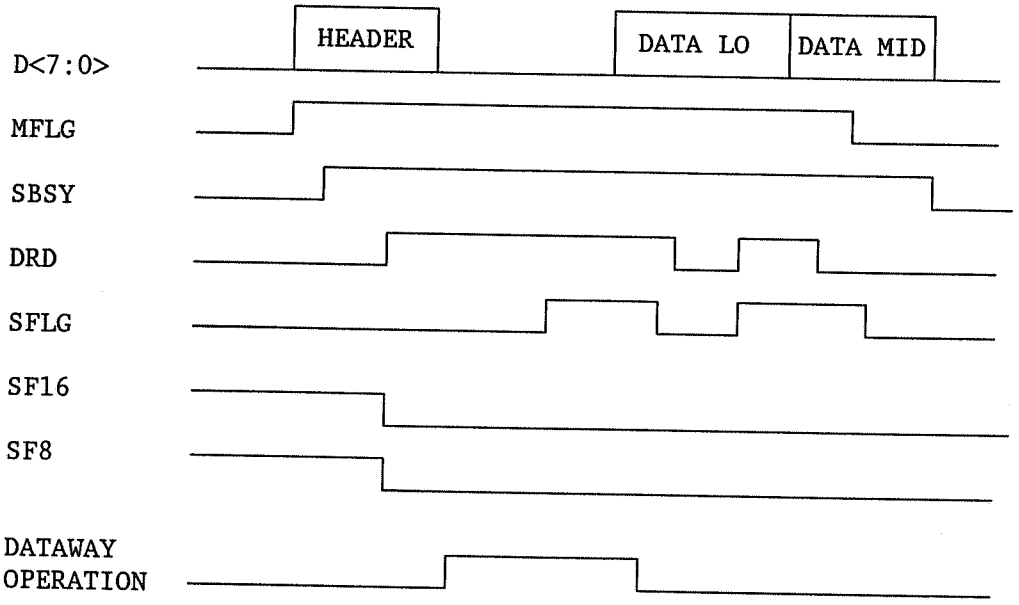
Model 2932-Z1A/Z1B

The following diagram shows a typical write and read sequence over the interconnection bus.

16-BIT CAMAC WRITE OPERATION



16-BIT CAMAC READ OPERATION



MODEL 3922 CRATE CONTROLLER

Features and Operation

The Model 3922 meets all the requirements of IEEE Standard 583 for CAMAC crate Controllers. It forms the communications link between the 2932 Mac Interface and the I/O modules in the CAMAC crate. When used with the 2932, the 3922 performs a wide variety of CAMAC commands to modules in the crate. The 2932/3922 combination supports program transfers as well as high-speed DMA operations. The 3922 also contains several internal registers that can be read or written at pseudo-address N(30). As a main crate controller, the 3922 supports auxiliary crate controllers as specified by IEEE Standard 675. The 3922 can also be easily field-changed to become an auxiliary crate controller.

One to eight 3922s can be connected to a single 2932 Mac Interface. Each 3922 includes a front-panel switch that allows address selection from 0 to 7. Multiple 3922s are interconnected on a loop-though basis and the last 3922 can be up to 300 feet from the 2932 PC Interface. The last 3922 also requires a termination card inserted into one of its bus connectors.

To achieve higher speed DMA data transfers, the 3922s Read's Read and Write Data Registers can be double-buffered. This allows a Dataway cycle to be requested and executed while data is transferred across the 2932/3922 bus. This buffering produces a side effect during Read operation. Then the 2932 terminates a DMA transfer, the 3922 has already performed one or more Dataway operations to fill its buffer. This can cause a problem in some instances. Two operating states are provided for DMA Read operations. By clearing the bit in the 3922 Status Register, the single-buffer mode performs a Read operation only when 2932 requests data. By setting this bit, double-buffer mode is selected. Double buffering results in some increase in throughput. Single-buffer mode should be used for Q-REPEAT and Q-SCAN operations or for other Read transfers where extra Dataway cycles result in lost data.

Address Selection

A front-panel, thumb-wheel switch allows you to select each 3922's address. Any address from 0 to 7 can be selected. However, all 3922s connected to single 2932s should have this switch set to different addresses.

Registers

CAMAC commands are performed to modules within the crate using Station address 1 through 23. Internal registers in the 3922 are accessed in the same manner as module registers but use pseudo-address N(30). There are five 3922 internal commands. These are: Read Status, Read LAM Pattern, Read LAM Mask, Write Status, and Write LAM Mask. The N(30) commands are shown here:

Model 2932-Z1A/Z1B

Command	Q-Response	Action
F(1) · A(0)	ONLINE	Read Status
F(1) · A(12)	ONLINE	Read LAM Pattern
F(1) · A(13)	ONLINE	Read LAM Mask
F(17) · A(0)	ONLINE	Write Status
F(17) · A(13)	ONLINE	Write LAM Mask

Status Register N(30) · F(17) · A(0), N(30) · F(1) · A(0)

The Status Register has the following format:

BIT	WRITE OPERATION	READ OPERATION
1	Generate Z	0
2	Generate C	0
3	Set Inhibit	Inhibit (Crate Controller Register State)
4	0	0
5	0	0
6	0	0
7	0	Dataway Inhibit
8	Double-Buffer Mode	Double-Buffer Mode
9	Enable Service Request	Service Request Enabled
10	Set Internal L24	Internal L24 Set
11	0	0
12	0	0
13	0	0
14	0	Front-Panel Switch Off-Line
15	0	Write Buffer Full
16		Selected LAM Present
17-24	0	0

A detailed description of the bits in the 3922 Stats Register is provided here:

MODEL 3922 CRATE CONTROLLER

BIT	DESCRIPTION
1	By setting this bit with the 3922 on-line, the crate controller executes a CAMAC Initialize (Z) operation. This bit is always read back as zero.
2	By setting this bit with the 3922 on-line, the crate controller executes a CAMAC Clear (C) operation. This bit is always read back as zero.

3	By setting this bit, the 3922 asserts the Dataway Inhibit line. With the 3922 asserting the Inhibit line, both bits 3 and 7 will return a value of **ONE** when the Status Register is read.
4-6	Not used, read as zeroes.
7	This Read-only bit indicates the state of the Inhibit line on the CAMAC Dataway. Note that other modules such as the 3655 can assert the Inhibit line.
8	By setting this bit, all DMA Read operations are executed in double-buffer mode. In this mode, a Dataway Read operation is executed and transferred to the 3922 buffer as soon as a DAMs transfer request is made. This double-buffering allows extra Dataway operations to occur when the block is terminated. If this bit is cleared (single-buffer mode), a DMA Dataway Read operation is executed only after the 2932 Mac Interface requests data. Single-buffered mode should be used for Q-REPEAT and Q-SCAN operation or other transfers where extra Dataway operations will result in lost data. This is a Read/Write bit.
9	By setting this bit, a Service Request is made to the 2932 whenever a module Look-at-Me (LAM) is pending and that LAM is enabled in the LAM Mask Register. This is a Read/Write bit.
10	This bit sets the internal L24 signal. The L24 signal can be used for software and hardware testing associated with the Service Request. This bit is Read/Write.
11-13	Not used, read as zeroes.
14	This Read-only bit indicates the status of the front-panel on-line switch. With the 3922 in the off-line state, only the Status Register can be read. No other commands will be executed by the 3922.
15	This is a Read-only bit which is set when a Q-STOP operation is terminated due to a Q=0 response and the 3922 contains a CAMAC write data word in its buffer.
16	This Read-only bit indicates that a selected LAM is present in the CAMAC crate. The "SLP" condition is TRUE only when one or more LAM requests (L1 to L24) are asserted and the LAM Mask bits)s) associated with the LAM request(s) are TRUE.
17-24	Not used, read as zeroes.

LAM Register N(30) · F(1) · A(12)

This is a 24-bit register which indicates the present state of all LAM requests in the CAMAC crate. Each bit corresponds to the appropriate Station in the crate (L(9) is associated with N(9) etc.).

LAM Mask Register N(30) · F(1) · A(13), N(30) · F(17) · A(13)

The LAM Mask Register is used to select those LAM requests from modules that cause a Request-for-Service (Selected LAMs Present) to be forwarded to the 2932. For example, if Bits 2, 3 and 8 are TRUE in the LAM Mask Register and all other bits are FALSE, only L(2), L(3) or L(8) can cause a Service Request.

3922 FRONT PANEL

Switches

Crate Address	A thumb-wheel switch which selects the crate address for the 3922. The address ranges from 0 to 7.
On-Line	Manually places the 3922 on-line or off-line. No Dataway operations are executed when the 3922 is off-line.
Z/C	Performs a manual Dataway Z or C to the CAMAC crate. Note that the 3922 must be off-line for this switch to have any effect.

LEDs:

BUSY	Flashes whenever the 3922 is performing a Dataway operation.
NO-Q	The last CAMAC operation, including an N(30) command, sets this LED "ON" when a Q=0 condition occurs.
NO-X	The last CAMAC operation, including an N(30) command, sets this LED "ON" when a X=0 condition occurs.
Inhibit	This LED is "ON" whenever the Dataway Inhibit line is asserted.
SLP	This LED is "ON" when a selected LAM is present.

LEMOs:

BUSY	A low-true TTL signal when Dataway BUSY is TRUE.
Request	Part of the auxiliary crate controller (ACC) protocol. Note that Request MUST be patched to Grant In for a main crate controller (even when no ACCs are used).
Grant In	Part of the ACC protocol. Patched to Request or Grant Out from a higher priority crate controller.
Grant Out	Part of the ACC protocol. Patched to Grant In of a lower priority crate controller.

REGISTER LAYOUT

Model 2932-Z1A/Z1B