Model 2935-Z1A

16-Bit EISA Interface Card w/DMA

INSTRUCTION MANUAL

October, 1991

CONTENTS

FIGURES

KJC:rem(WP)

INSTALLATION

The Model 2935 is designed to fit into any full size EISA expansion slot. After selecting the DMA channel and interrupt request level, the 2935 is ready to be installed into the computer.

Remove the cover of the computer. Locate an empty EISA slot and remove the blank plate from the mounting rail. Insert the 2935 into the slot and secure with the screw that was used for the blank plate. Replace the cover on the computer.

Insert the 100 position connector of the interface cable into the 2935 connector and the other end into the 3987 front-panel connector. Refer to the 3987 manual for connections to the crate controller.

OPERATION

Communication between the 2935 and EISA computer is accomplished via I/O commands. The 2935 is used to load the 3987 list memory and enable the 3987 list execution. The 2935 can then send or receive CAMAC data between the 3987 and the EISA computer. The 2935 can also directly read and write the 3987's internal registers allowing the transfer of status and operation information. Refer to the 3987 operating manual for a complete description of these registers and their functions.

INTERRUPT LEVEL AND DMA CHANNEL STRAPS

The 2935 contains straps for the selection of EISA DMA channel and interrupt request level.

The DMA channel can be strapped for either Channel 0, Channel 1, Channel 2, Channel 3, Channel 5, Channel 6, or Channel 7. When selecting a DMA Channel, care must be taken to be sure no other device is using that channel. Also, the DMA channel request (DRQ) and DMA channel acknowledge (DAK) straps must be set for the same channel. Refer to Figure 1 (see page 3) for the location of these straps.

The 2935 can be strapped for various Interrupt Request Levels. The Interrupt Request Levels available for the 2935 to use are 0, 3, 4, 5, 7, 10, 11, 12 and 15. Refer to Figure 1 (see page 3) for the location of these straps.

EISA REGISTER DESCRIPTION

The 2935 contains five 8-bit registers used for EISA identification and control. These registers are located at $0zC80_h$ - $0zC84_h$ (z represents the EISA slot number). Addresses $0zC80_h$ through $0zC83_h$ are a unique 2935 product identification number.

Address $0zC84_h$ is the 2935 Expansion Board Control Port. Bit one of this port is used to enable or disable the 2935. With this bit set, the 2935 is enabled and can perform any of its functions. With bit one set to a zero, the 2935 will not perform any communication with the 3987, but will still allow the on-board registers to be read and written.

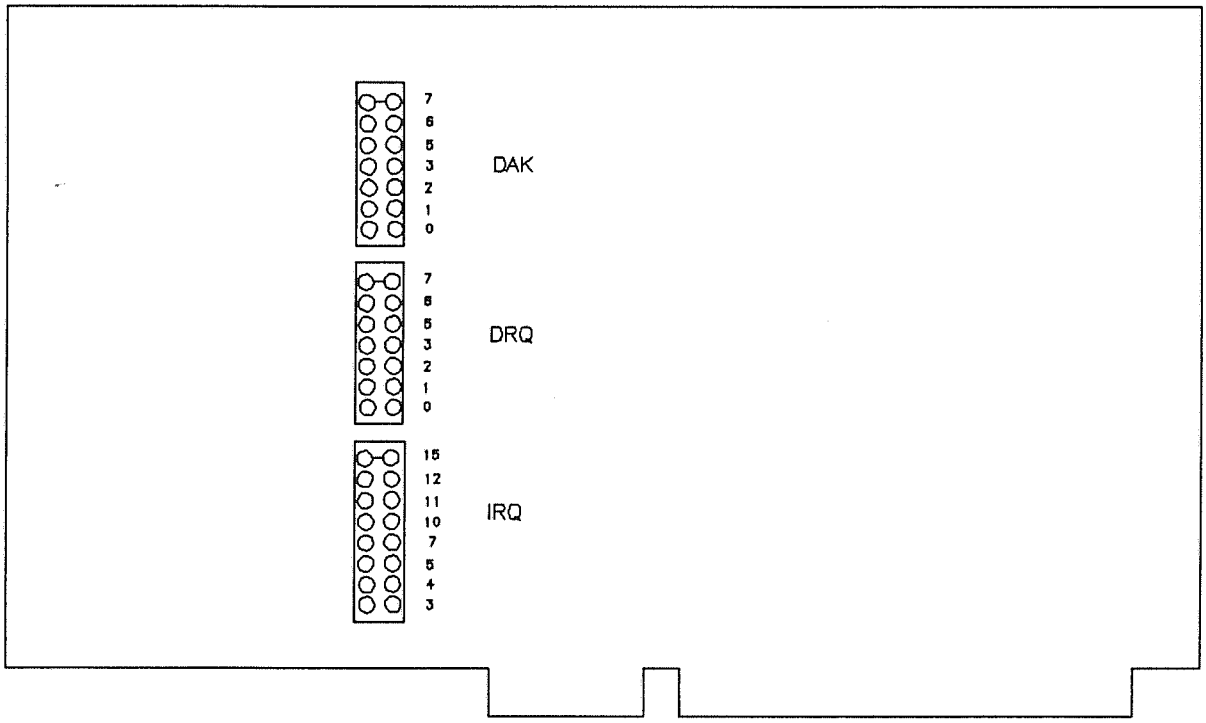


FIGURE 1 - 2935 Strap Locations

COMMUNICATION REGISTERS

In addition to the EISA registers, the 2935 uses I/O addresses for direct communication with the 3987. These registers have a base address of $0zC00_h$ (z represents the EISA slot number). The 2935 has one on-board register at offset 0 from the communication register base. It is denoted as the Card Control/Status Register. All other communication registers are located on the 3987. The following table shows the communication registers and their offsets. Refer to the 3987 manual for a complete description of these registers.

Communication Registers

Base = $0zC00_h$

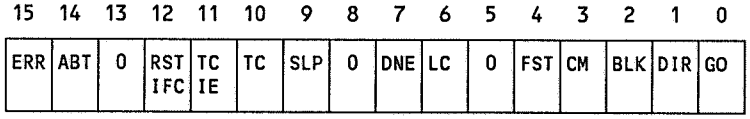
Address	Register Description
Base + 0	Card Control/Status Register
Base + 2	Control/Status Register
Base + 4	Mode Control Register
Base + 6	CNAF Register
Base + 8	Data FIFO Register
Base + A	Word Count Register
Base + C	LAMLO Register
Base + E	LAMHI Register
Base + 10	LAM Mask LO Register
Base + 12	LAM Mask HI Register
Base + 14	Command Memory Address Register
Base + 16	Command Memory Data Register
Base + 18	CAMAC Control/Status Register
Base + 20	Transfer Count Register

Note: All register offsets are in hexadecimal.

Card Control/Status Register

The Card Control/Status Register (CRDCSR) is located on the 2935 and is used to control 2935 operation as well as monitor the 2935 and 3987 status. Bit 15 is used to monitor the 3987 error condition. Bit 14 will be set if the 3987 has aborted its current list operation. Bit 9 is set when a LAM is present in the 3987's CAMAC Crate. Bit 7 is set when the 2935 has completed its current DMA operation. Bit 6 is set when the 3987 has completed its current list. Bits 4 through 0 are used to control the various types of operation modes for DMA transfers to and from the 3987.

CARD CONTROL/STATUS REGISTER (CRDCSR) Offset:0



Bit	Signal Name	Description
15	ERROR	**ERROR** is a read only bit which when set, indicates that the last list operation in the 3987 terminated with an error. The following is a definition of error: ERROR = ABORT
14	ABORT	**ABORT** is a read only bit which when set, indicates that the 3987 list was aborted. Refer to the 3987 manual for a description of the abort equation.
13	Not Used	This bit is not used and is read as zeros.
12	RST IFC	**RESET INTERFACE** is a write only bit, which when set, initializes the 2935 to a power up state.

NOTE: Presetting the 2935 clears the ENABLE bit in the card - Configuration Register

11	TC IE	**TERMINAL COUNT INTERRUPT ENABLE** is a read/write bit, when set, will cause the 2935 to generate and Interrupt Request upon receipt of TERM COUNT from the EISA DMA Controller.
10	TC	**TERMINAL COUNT** is a read only bit, which when set, indicates that the EISA DMA Controller has issued a TERMINAL COUNT for the 2935's DMA Channel. This bit is cleared upon reading the CRDCSR.
9	SLP	**SELECTED LAMS PRESENT** is a read only bit which when set, indicates that the 3987 has a CAMAC LAM pending in its crate. Refer to the 3987 manual for a complete description of the LAM registers.
8	Not Used	This bit is not used and is read as zero.
7	DMA DONE	**DMA DONE** is a read only bit which when set, indicates that the 2935 has completed its DMA operation on the EISA bus. Care must be taken when using this bit to monitor the 2935 operation. During CAMAC block writes, this bit can be set before all the CAMAC operations have completed.
6	LIST COMPLETE	**LIST COMPLETE** is a read only bit which when set, indicates that the 3987 list has completed. This bit monitors the STS0 (DONE) signal which is returned from

		the 3987. Refer to the 3987 operating manual for a complete definition of the STS0 signal.
5	TCR ENA	**TRANSFER COUNT REGISTER ENABLE** is a read/write bit which when set enables the 2935 On-Board Transfer Count Register to control the number of words which are transferred across the AFI bus during DMA Read Operations. When cleared, the 2935 relies on the EISA DMA Controller to terminate AFI Handshake.
4	FAST	**FAST** is a read/write bit which when set, places the 2935 into a fast handshake mode. This mode allows block transfers between the 2935 and 3987 to reach speeds of up to 4 megabytes. Refer to the handshake description section of this manual for a complete description of the different handshake modes.
3	CM	**COMMAND MEMORY** is a read/write bit which when set, indicates that DMA transfers are to be executed to the command memory of the 3987. Refer to the 3987 manual for a complete description on building a command list.
2	BLK	The **BLOCK** bit is a read/write bit which when set, indicates that the DMA function for CAMAC data will not terminate on TC from the EISA bus DMA Controller. Instead, the 2935 will continue to execute the block until the go bit is written to a zero. This feature is useful when using the 3987 in the automatic mode.
1	DIR	The **DIRECTION** bit is a read/write bit which when set, places the 2935 in the DMA read mode. When in this mode, the 2935 will receive data from the memory located on the EISA bus for transfer to the 3987. When cleared, the 2935 is in the DMA write mode and will write data from the 3987 to the memory located on the EISA bus. Data can be either CAMAC read/write data or 3987 Command Memory data. This is determined by the state of the CM (bit 3) bit.
0	GO	When set, the **GO** bit enables the 2935 to begin DMA transfers across the EISA bus. With the **BLOCK** bit set to zero, the **GO** bit will be cleared by TC from the EISA bus DMA controller or by the 3987 issuing a PEND control signal. Refer to the 3987 manual for a description of the PEND operation.

The following table describes the various combinations of the lower four bits of the CRDCSR.

CM	BLK	DIR	GO	
0	0	0	1	Single TC CAMAC Data Read
0	0	1	1	Single TC CAMAC Data Write
0	1	0	1	Multiple TC CAMAC Data Read
0	1	1	1	Multiple TC CAMAC Data Write
1	0	0	1	Single TC Command Memory Read
1	0	1	1	Single TC Command Memory Write

All other combinations of these bits are invalid.

TRANSFER COUNT REGISTER (TCR) Offset:20_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 9	TC 8	TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0

The TCR is used to control handshaking data between the 3987 and 2935. When the TCR_ENABLE bit is set in the CARD CSR, the Transfer Count Register is Enabled.

During EISA DMA READ Operations the TCR determines the number of words which will be transferred to the 2935 from the 3987. The TCR should be written with the same value as the EISA DMA Controller's Word Count Register

This number is one less than the number of words required. Refer to the EISA Specification for a complete description of the DMA Controller.

The purpose of this register is to prevent extra data to be transferred to the 2935. This can happen if the 3987 has more data available than the requested EISA DMA Word Count. By utilizing the TCR, the 2935 will only request the designated number of data words.

When the TCR is disabled. The 2935 will continually request data from the 3987 until the EISA DMA Controller asserts the TCNT SIGNAL on the EISA bus. This could result in up to 1024 words of data getting purged from the 2935's Data FIFO.

NOTE: The TCR is only utilized during DMA READ OPERATIONS.

HANDSHAKE DESCRIPTIONS

The 2935 uses two different types of handshake methods with the 3987. In the slow mode, the 2935 waits for the 3987 to negate the PFLG signal before asserting a PCTL signal.

In the Fast mode of handshake, the 2935 does not wait for the 3987 to negate PFLG before asserting the next PCTL. This mode allows the 2935 to transfer data to or from the 3987 at a four megabyte rate, freeing the EISA bus for other operations during the 3987 execution of the command list.

Although the 2935 and 3987 will function in either handshake mode, the fast handshake method is recommended for normal operation. This method will allow the 2935 and 3987 to operate at their peak efficiency.

Fast Mode Write to 3987

In the Fast mode, the 2935 looks like a FIFO buffer in the transfer data path.

In Write transfers, the PCTL line is the same as a FIFO Output Ready signal, and PFLG acts like a Shift-Out pulse. With a valid word at the FIFO output, PFLG(SO) is asserted, and moves the word onto the bus. PCTL(OR) toggles deasserted, then asserted if there is another word to transmit.

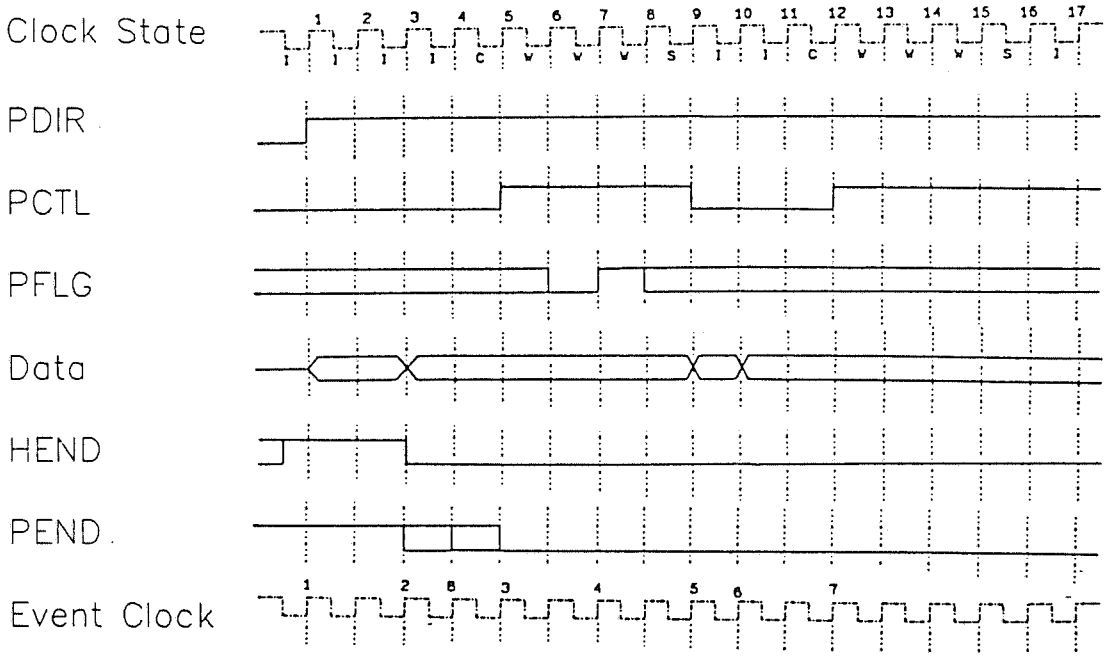


FIGURE 2 - Output FIFO Handshake

1. 2935 asserts PDIR to indicate output transfer. Driver outputs enabled.
2. Data available. 2935 asserts HEND if this is the last word.
3. Wait two clock pulses. 2935 asserts PCTL, irrespective of PFLG.
4. When it can accept data, the 3987 asserts PFLG to acknowledge PCTL.
5. 2935 deasserts PCTL in response to PFLG. PFLG may change levels, data become invalid.
6. New data available from 2935.
7. Wait two clock pulses. 2935 asserts PCTL, irrespective of PFLG.
8. If the 3587 has asserted PEND before this time,the new transfer will not occur. To terminate transmission requires only a falling PEND edge, not a pulse.

Fast Mode Read from 3987

For input transfers, the PCTL line looks like a FIFO Input Ready signal, and PFLG acts like a Shift-In pulse. With room for at least one word in the 2935 FIFO buffer, it asserts PCTL (IR), the PFLG(SI) pulse moves a word into the buffer and PCTL toggles deasserted, then asserted if there is room for another word.

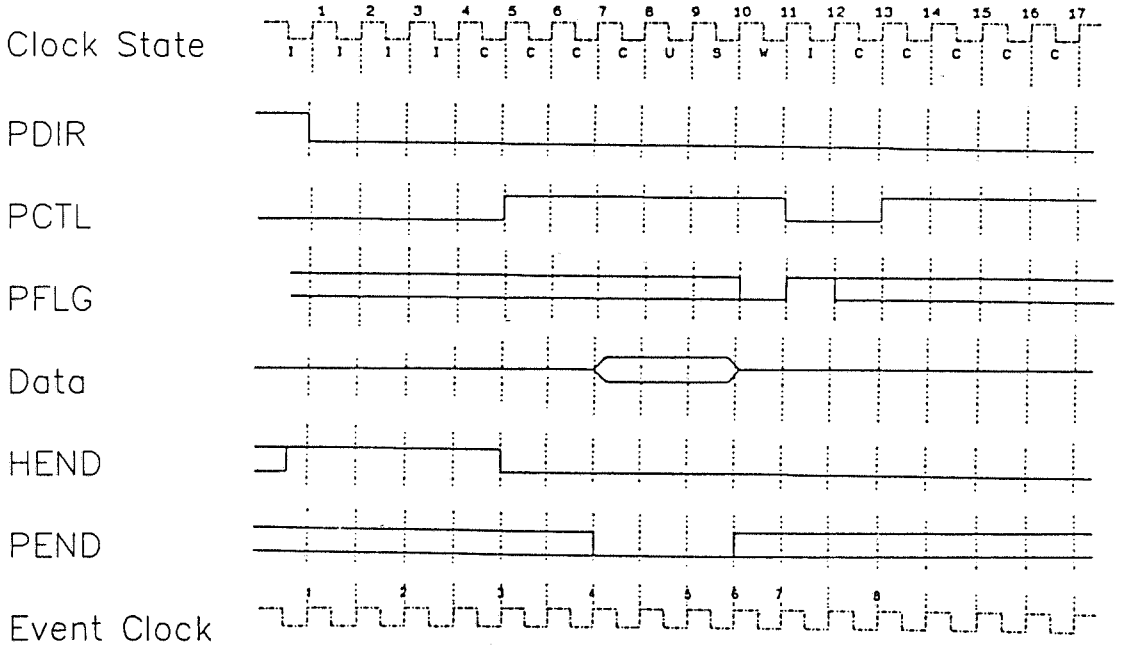


FIGURE 3 - Input FIFO Handshake

1. 2935 deasserts PDIR to indicate an input transfer. 3987 can drive inputs any time.
2. 2935 FIFO buffer must have room for data, i.e., FIFO not full.
3. 2935 asserts PCTL and deasserts HEND. PFLG may be high or low. For a final transfer, HEND is asserted (low).

4. 3987 asserts PFLG to acknowledge PCTL. Data must be valid, PEND deasserted (unless the last word). This illustration shows the final transfer in the transaction.
5. Data latched in buffer.
6. Latching complete. Data and PEND can change (this may happen as last as 7).
7. 2935 deasserts PCTL to acknowledge PFLG assertion. The FIFO buffer is ready again (may happen later). When it is, the cycle may start again.
8. 2935 reasserts PCTL starting next cycle, irrespective of PFLG state.

Normal Mode Handshake Write to 3987

In Normal mode, the handshake lasts only as long as both PCTL and PFLG are in their asserted states.

The 2935 starts the transfer by driving its own PCTL signal asserted. The 3987 responds with its PFLG line.

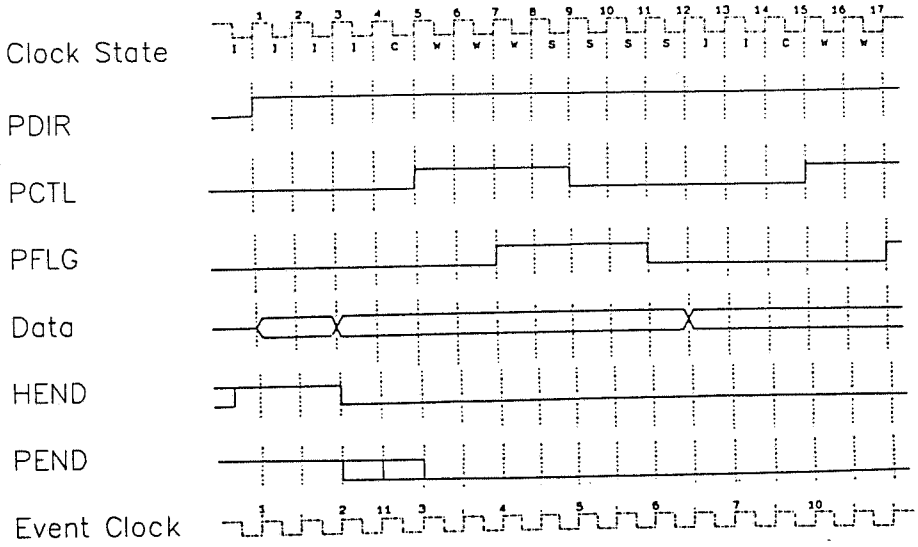


FIGURE 4 - Output Full Master Handshake

1. 2935 asserts PDIR to indicate output transfer. Driver outputs enabled.
2. Output data available (HEND asserted if last word).
3. After waiting two clock pulses, AFI asserts PCTL.
4. 3987 acknowledges PCTL by asserting (high) PFLG (this happens if 3987 can accept data, otherwise, wait).
5. After one clock pulse, 2935 deasserts PCTL to acknowledge PFLG.
6. After waiting (50ns, here), 3987 deasserts (low) PFLG.
7. Output data available (HEND asserted if last word).
8. After waiting two clock pulses, 2935 asserts PCTL.
9. With PEND asserted before this clock edge, no new transfer occurs. To abort another transfer requires only a PEND falling edge, not a full pulse.

Normal Mode Read from 3987 Handshake

In Normal Read mode, the 2935 commands the 3987 to send any data it has available. The first signal to change states is the PDIR line.

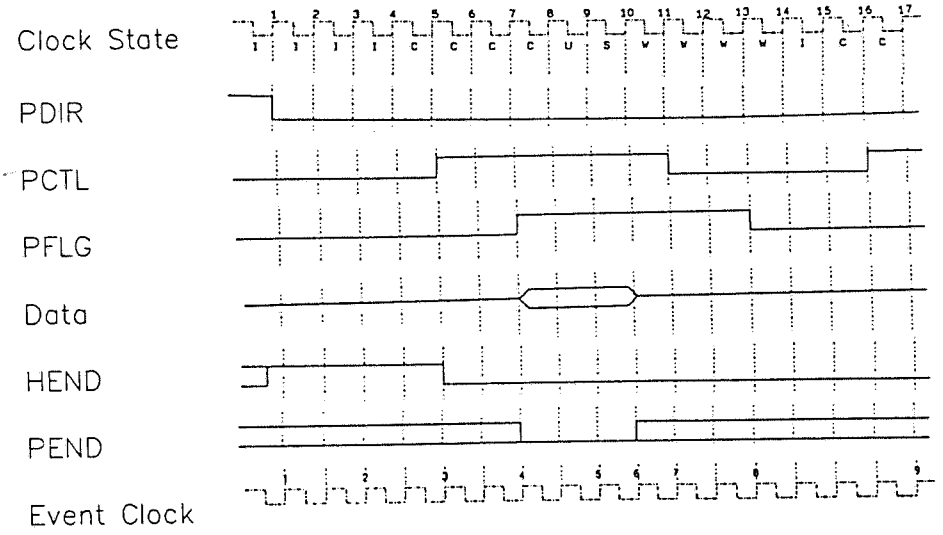


FIGURE 5 - Input Full Master Handshake

1. 2935 deasserts PDIR to indicate input transfer. 3987 may now drive receive data bus.
2. 2935 waits for data FIFO not full.
3. 2935 asserts PCTL (high). For a final transfer, 2935 asserts HEND (low).
4. 3987 asserts PFLG to acknowledge PCTL. Data must be valid at this time. Unless this is the last word in the transaction, PEND must be deasserted. This illustration shows the final word transfer.
5. 2935 latches data.
6. Buffer finishes latching data (data and PEND will change before step 7).
7. 2935 deasserts PCTL, acknowledging PFLG. Buffer may be able to accept more data now.
8. 3987 deasserts PFLG to acknowledge falling PCTL.
9. A new cycle begins.

DMA CONTROLLER

Due to the design of the EISA bus, minimal programming is needed to setup the DMA controllers for a DMA operation. The Basic Input/Output System (BIOS) in the system board will initialize the DMA controllers, leaving a few user supplied parameters to be loaded. The DMA subsection of the EISA bus is made compatible to two Intel 8237 DMA controller chips.

The DMA controller has channels 0-3 and 5-7 available for use. Channel 4 is used as a cascade channel to maintain compatibility with the EISA standard DMA system. Any of the available channels can be programmed to support 16-bit DMA data transfers between 16-bit I/O devices and 16-bit memory. Each channel can transfer data throughout the 16-megabyte system memory address space. One difference in the EISA system is that the DMA channel can transfer data across the 128 kilobyte page boundary. This allows large DMA block transfers and can start at virtually any free memory location.

The following table is a list of DMA controller register addresses:

DMA CONTROLLER REGISTER PORTS

I/O Port Address	Register Description
0000h	DMA Ch-0 Base & Current Address register
0001h	DMA Ch-0 Base & Current Count register
0002h	DMA Ch-1 Base & Current Address register
0003h	DMA Ch-1 Base & Current Count register
0004h	DMA Ch-2 Base & Current Address register
0005h	DMA Ch-2 Base & Current Count register
0006h	DMA Ch-3 Base & Current Address register
0007h	DMA Ch-3 Base & Current Count register
0008h	DMA(0-3) Status register
0008h	DMA(0-3) Command register
0009h	DMA(0-3) Request register
000Ah	DMA(0-3) Write single mask bit
000Bh	DMA(0-3) Mode register
000Ch	DMA(0-3) Clear byte pointer
000Dh	DMA(0-3) Master Clear
000Eh	DMA(0-3) Clear Mask register
000Fh	DMA(0-3) Write all mask bits
000Fh	DMA(0-3) Mask Status register
0081h	DMA Ch 2 Low Page register
0082h	DMA Ch 3 Low Page register
0083h	DMA Ch 1 Low Page register

I/O Port Address	Register Description
0087h	DMA Ch 0 Low Page register
0089h	DMA Ch 6 Low Page register
008Ah	DMA Ch 7 Low Page register
008Bh	DMA Ch 5 Low Page register
008Fh	Refresh Low Page register
00C0h	DMA Ch 4 Base & Current Address register
00C2h	DMA Ch 4 Base & Current Count register
00C4h	DMA Ch 5 Base & Current Address register
00C6h	DMA Ch 5 Base & Current Count register
00CAh	DMA Ch 6 Base & Current Address register
00CAh	DMA Ch 6 Base & Current Count register
00CCh	DMA Ch 7 Base & Current Address register
00CEh	DMA Ch 7 Base & Current Count register
00D0h	DMA(4-7) Status register
00D0h	DMA(4-7) Command register
00D2h	DMA(4-7) Request register
00D4h	DMA(4-7) Write single mask bit register
00D6h	DMA(4-7) Mode register
00D8h	DMA(4-7) Clear byte pointer
00DAh	DMA(4-7) Master Clear
00DCh	DMA(4-7) Clear Mask register
00DEh	DMA(4-7) Write all mask bits register
00DEH	DMA(4-7) Mask Status register
0401h	DMA Ch 0 High Base & Current Count
0403h	DMA Ch 1 High Base & Current Count
0405h	DMA Ch 2 High Base & Current Count
0407h	DMA Ch 3 High Base & Current Count
0481h	DMA Ch 2 High Page register
0482h	DMA Ch 3 High Page register
0483h	DMA Ch 1 High Page register
0487h	DMA Ch 0 High Page register
0489h	DMA CH 6 High Page register
048Ah	DMA Ch 7 High Page register
048Bh	DMA Ch 5 High Page register
04C6h	DMA Ch 5 High Base & Current Count

I/O Port Address	Register Description
04CAh	DMA Ch 6 High Base & Current Count
04CEh	DMA Ch 7 High Base & Current Count
04D4h	DMA(4-7) Chaining Mode register
04D4h	DMA Chaining Mode Status register
04D6h	DMA(4-7) Extended Mode register
04E0h	DMA CH0 Stop register bits <7:2>
04E1h	DMA CH0 Stop register bits <15:8>
04E2h	DMA CH0 Stop register bits <23:16>
04E4h	DMA CH1 Stop register bits <7:2>
04E5h	DMA CH1 Stop register bits <15:8>
04E6h	DMA CH1 Stop register bits <23:16>
04E8h	DMA CH2 Stop register bits <7:2>
04E9h	DMA CH2 Stop register bits <15:8>
04EAh	DMA CH2 Stop register bits <23:16>
04ECh	DMA CH3 Stop register bits <7:2>
04EDh	DMA CH3 Stop register bits <15:8>
04EEh	DMA CH3 Stop register bits <23:16>
04F4h	DMA CH5 Stop register bits <7:2>
04F5h	DMA CH5 Stop register bits <15:8>
04F6h	DMA CH5 Stop register bits <23:16>
04F8h	DMA CH6 Stop register bits <7:2>
04F9h	DMA CH6 Stop register bits <15:8>
04FAh	DMA CH6 Stop register bits <23:16>
04FCh	DMA CH7 Stop register bits <7:2>
04FDh	DMA CH7 Stop register bits <15:8>
04FFh	DMA CH7 Stop register bits <23:16>

DMA Controller Description

For use with the 2935, the DMA controller operates in the master mode. In the master mode, the DMA controller generates the cycle control for DMA data transfers. The controller supplies the memory address and read/write signals for cycle execution. The DMA controller is in the master condition when any channels DAK signal is asserted. Refer to the EISA Bus Specification for a detailed description of the DMA controller operation.

Demand Transfer Mode

The 2935 utilizes the Demand Transfer mode of DMA operation. When a DMA channel is programmed for Demand Transfer, it performs a group of transfers for each arbitration cycle.

The Base Word Count register is programmed with the appropriate number of transfers to be performed. The Base Address register is loaded with the starting memory address for the DMA block. The DMA controller decrements the word count and increments the current address register after each data transfer. The transfer continues until the 2935 negates DRQ, the Current Word Count register reaches Terminal Count (the word count rolls over from 0 to $FFFFFF_h$), or an external end of process (EOP) is received. With the DMA controller in the auto initialize mode, Terminal Count (TC) or EOP causes the current registers to be loaded with the contents of the base registers.

The 2935 requests a Demand Mode Transfer by asserting the DRQ signal for its channel and holding DRQ in the true state until detecting DAK to be true. The 2935 holds DRQ true until it has no valid data in its FIFO (during read operations), or until its data FIFO is full (during write operations). DRQ is also negated when TC is detected. DMA transfers can be interrupted if another device requests the bus. This is important for such things as memory refresh. The 2935 requests the bus again by re-asserting or continuing to assert DRQ. Arbitration is performed and the winning channel DAK signal is asserted.

Auto Initialize

A channel, which is set for auto initialization, automatically loads the Current Page Address, Current Address, and Current Word Count registers from the Base Page Address, Base Address, and Base Word Count registers each time the DMA controller reaches terminal count or receives an EOP. By programming a bit in the Mode register, a channel can be set for Auto Initialization. The mask bit is not set at the end of the transfer when the channel is in this mode. After auto initialization, the channel is ready to perform another DMA operation without the need for CPU intervention.

The auto initialize mode is useful when operating the 3987 in the automatic mode. Successive list executions can occur and multiple DMA cycles can be executed without re-initializing the DMA controller.

EISA REGISTERS

Product Identification Byte 1 Address:0zC80$_h$

7	6	5	4	3	2	1	0
0	0	1	0	1	1	1	0

Product Identification Byte 2 Address:0zC81$_h$

7	6	5	4	3	2	1	0
0	1	1	0	0	0	1	1

Product Identification Byte 3 Address:0zC82$_h$

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Product Identification Byte 4 Address:0zC83$_h$

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Expansion Board Control Port Address:0zC84$_h$

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	CARD ENA

COMMUNICATION REGISTERS

Card Control/Status Register (CRDCSR) Offset:0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR	ABT	NU	RST IFC	TC IE	TC	NU	NU	DONE	LC	TCR ENA	FAST	CM	BLK	DIR	GO

Control/Status Register (CSR) Offset:2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EC 4	EC 2	EC 1	RST/ WDFB	ATTN I.E.	APND	NU	NU	LAM I.E.	DONE I.E.	TRIG 2	TRIG 1	FREQ 8	FREQ 4	FREQ 2	FREQ 1

Mode Control Register (MODE) Offset:4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	NU	NU	NU	NU	NU	CM	TM2	TM1	M2	M1	WS2	WS1	AD

CAMAC Command Register (CNAF) Offset:6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C2	C1	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

Data FIFO Register (DFR) Offset: 8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W 16	R/W 15	R/W 14	R/W 13	R/W 12	R/W 11	R/W 10	R/W 9	R/W 8	R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1
NOT USED FOR CAMAC HIGH DATA								R/W 24	R/W 23	R/W 22	R/W 21	R/W 20	R/W 19	R/W 18	R/W 17

Word Count Register (WCR) Offset:A_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WC 15	WC 14	WC 13	WC 12	WC 11	WC 10	WC 9	WC 8	WC 7	WC 6	WC 5	WC 4	WC 3	WC 2	WC 1	WC 0

LAMLO Register (LAML) Offset:C_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L 16	L 15	L 14	L 13	L 12	L 11	L 10	L 9	L 8	L 7	L 6	L 5	L 4	L 3	L 2	L 1

LAMHI Register (LAMH) Offset:E_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	NU	NU	NU	NU	NU	L 24	L 23	L 22	L 21	L 20	L 19	L 18	L 17

LAM Mask Lo Register (MASKL) Offset:10_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LM 16	LM 15	LM 14	LM 13	LM 12	LM 11	LM 10	LM 9	LM 8	LM 7	LM 6	LM 5	LM 4	LM 3	LM 2	LM 1

LAM Mask Hi Register (MASKH) Offset:12_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	NU	NU	NU	NU	NU	LM 24	LM 23	LM 22	LM 21	LM 20	LM 19	LM 18	LM 17

Command Memory Address Register (CMA) Offset:14_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

Command Memory Data Register (CM) Offset:16_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CD 15	CD 14	CD 13	CD 12	CD 11	CD 10	CD 9	CD 8	CD 7	CD 6	CD 5	CD 4	CD 3	CD 2	CD 1	CD 0

CAMAC Control/Status Register (CCSR) Offset:18_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLP	NU	OFF LINE	NU	NU	NU	LAM 24	NU	NU	READ INH	NU	NU	NU	SET INH	C	Z

Transfer Count Register (TCR) Offset:20_h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TC 15	TC 14	TC 13	TC 12	TC 11	TC 10	TC 9	TC 8	TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0