Model 2962

PCI Interconnect Highway Driver

Instruction Manual

February 5, 1999

Contents

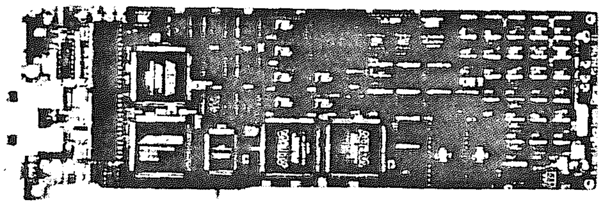
FIGURES

PCI Host Adapter for the Grand Interconnect

Allows a computer PCI bus to host the Grand Interconnect **2962**

Features

- **Provides a PCI interface for the Grand Interconnect highway**
- **Can be used with any combination of VXI or CAMAC chassis**
- **Provides access to 126 nodes**
- **Uses fiber-optic highway transmission**
- **Provides full throughput with up to two kilometers distance between fiber-optic nodes**
- **Exhibits 10 Mbytes/s highway throughput and 20 Mbytes/s PCI DMA burst rate**
- **Includes a high-speed command processor**
- **Includes multi-buffer functionality**



General Description *(Product specifications and descriptions subject to change without notice.)*

The Grand Interconnect (GI) connects multiple I/O chassis to a host computer. It provides high-throughput, deterministic data acquisition along with control capabilities. A complete GI system includes an Interconnect Host Adapter (IHA), a fiber-optic highway, and up to 126 I/O nodes that may include either or both VXI Slot-0 controllers and CAMAC crate controllers. The system supports distances between nodes of up to 2 kilometers (6560 ft).

The 2962 Interconnect Host Adapter is a single PCI (Peripheral Component Interface) card which provides the interface between the PCI bus and the Grand Interconnect highway. Communication between this IHA and the host computer is via a 32-bit data path that is used to configure the system and initiate highway operations. A DMA (direct memory access) mechanism is incorporated to transfer data over the highway using 32-bit data transfers. The 2962 IHA supports PCI DMA transfers, yielding a 20 Mbytes/s burst transfer rate.

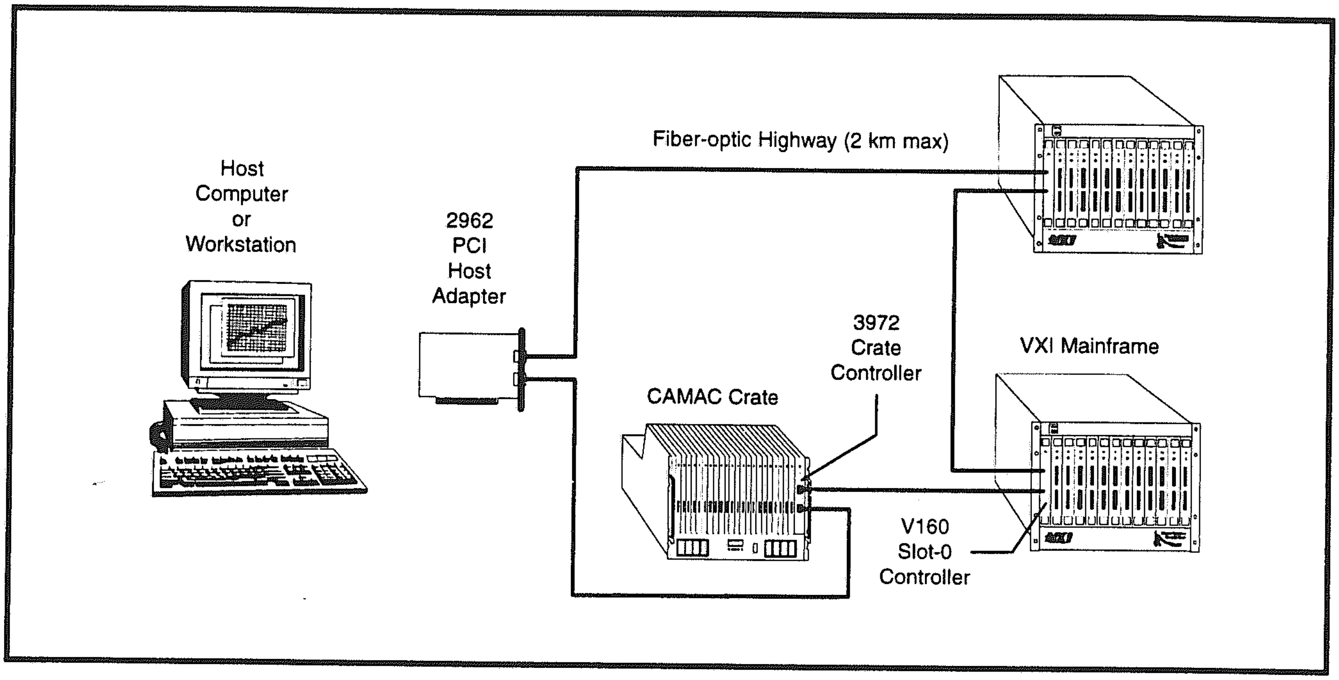
Data transfers to and from a VXI or CAMAC chassis are executed in a pipeline mode. These transfers will occur at full highway speed *if both the source and destination can maintain the data rate.* Full highway speed for the 2962 is 10 Mbytes/s over the interconnect highway. When transferring data to and from a CAMAC chassis, the 2962 provides the Q-Ignore, Q-Stop, Q-Repeat, and Q-Scan modes of operation.

The 2962 contains a 2048-word FIFO memory that stores asynchronous demand messages received from a chassis controller. These demand messages are generated from an interrupt in a VXI chassis or from a LAM (Look-At-Me) in a CAMAC chassis. The demand data identifies the chassis that sourced the demand message as well as the source of the interrupt or LAM within that chassis.

The Interconnect Host Adapter includes a command processor to execute a preloaded list of Interconnect operations. This list of operations is read from a 32K x 32 RAM memory and then executed. Command processing may be initiated by software control or by an internal, crystal-controlled, programmable counter/timer. The timer provides for the selection of triggering rates from 0.06 Hz to 500 kHz in 1-microsecond increments.

The 2962 uses host computer memory to implement multi-buffer functionality. The multi-buffer activity includes DMA data chaining and the setting of buffer segment flags.

System Configuration



Power Requirements

+5 volts: 4.4 A

Ordering Information

Model 2962-Z2A	PCI Host Adapter for the Grand Interconnect

Associated Products

Model 3972-Z1X	CAMAC Crate Controller, for use with the Grand Interconnect
Model V160-xxx2	VXI Slot-0 Controller, for use with the Grand Interconnect
Model AD21-NPA1	Software, Device Driver, Windows NT
Model AD21-UAA1	Software, Device Driver, Digital UNIX/Alpha AXP
Model AD21-VAA1	Software, Device Driver, Open VMS/Alpha AXP
Model 5802-Lxyz	Cable, 50 micrometer fiber-optic
Model 5802-Nxyz	Cable, 62.5 micrometer fiber-optic
Model 5857-Axyz	Cable, 1-contact LEMO to unterminated
Model 5857-Bxyz	Cable, 1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz	Cable, 1-contact LEMO to BNC shielded
Model 5910-Z1A	Connector, 1-contact LEMO

INTRODUCTION

The 2962 PCI Interconnect Highway Driver (IHD) is a full size PCI card which interfaces the PCI bus to the Interconnect Highway. The Interconnect Highway is a fiber-optic highway which allows serial access to up to 126 slave nodes. These slave nodes may be any combination of CAMAC Crate Controllers, VXI Chassis Controllers and VME Chassis Controllers. The maximum signaling distance between fiber-optic nodes is 2 kilometers. The highway runs at 125 Megabits-per-second using 12-bits per word, 8 of which are information bits and 4 of control. Therefore, the maximum bandwith of data transfers on the highway is 10 Megabytes-per-second.

The 2962 executes highway operations provided by a list of instructions preloaded into a 32K x 32 list memory. This memory is loaded prior to initiating operations by programmed I/O transfers. Once list processing is initiated, data transfers to/from the 2962 may occur using either DMA or programmed transfers. DMA operations to/from the 2962 are executed using a 32-bit word format.

The list processing element on the 2962 is composed of a hardware sequencer and a TMS320C25 Digital Signal Processor (DSP). The hardware sequencer is responsible for initially interrogating list elements and executing the data transfer instructions. If the sequencer encounters a non-data transfer instruction, it enables the DSP. The DSP then executes the non-data transfer instructions and returns control to the hardware sequencer.

The list may contain such instructions as Single Operations, Block Transfer Operations, Single Inline Write Operations, Generate Host Interrupts, Load Loop Counter, and Conditional/Unconditional Branches. These instructions allow for a very versatile list. The list instruction can be directed at either CAMAC or VXI/VME chassis. The format of the instruction varies depending on the type of slave node being accessed.

A Demand FIFO is provided to retain up to 2048 demand messages. These messages are generated by both CAMAC and VXI/VME slaves. For CAMAC slaves, these messages are typically sourced when a CAMAC Look-At-Me (LAM) occurs. VXI/VME slaves generate these messages in response to interrupt requests in the chassis. When these messages are received by the 2962, the chassis address and a demand identification byte are stored in the FIFO. Optionally, the receipt of a demand message may assert an interrupt request to the PCI bus.

INSTALLATION

The Model 2962 is designed to fit into any full size PCI expansion slot. After selecting the desired Highway Timeout value, the 2962 is ready to be installed in the computer.

Before the installation is initiated, turn off the power to the computer and remove the power cord. Remove the cover to the computer and locate an empty expansion slot. Remove the blank plate from the mounting rail of the selected slot. Insert the 2962 into the slot and secure the mounting plate with the screw that was removed from the blank plate. Replace the cover on the computer and then plug the power cord back into the unit.

After the card is installed in the computer, connect the fiber optic cables to the 2962. The top fiber optic connector on the 2962 is the highway output connector. The bottom fiber optic connector is the highway input connector. One fiber optic cable should run from the 2962 highway output connector (top) to the first chassis V160 Slot0 input connector (for VXI) or the 3972 input connector (for CAMAC). A second fiber optic cable should run from the bottom highway input fiber optic connector on the 2962 to the highway output connector on the V160 or 3972 in the last chassis on the highway.

HIGHWAY TIMEOUT SELECTION

The 2962 contains a strap selectable timer to control the timeout value for the highway. If the 2962 transmits a message on the highway and does not receive a reply message within the selected timeout period, an error is generated and the highway is reset. This timeout value ranges from 3 seconds to 10 seconds. The timeout may also be disabled to allow for an infinite timeout value. Please refer to Appendix B of this manual for the location and settings of the Highway Timeout.

PCI CONFIGURATION SPACE

The PCI Specification mandates a 64-byte Configuration Header that describes the requirements of add-in cards. The data contained in this region uniquely identifies the device and allows for generic control of the device. The configuration data indicates the memory requirements of the device along with other device specific information.

This section describes the 64 bytes of configuration space implemented by the 2962. The following diagram is a composite chart showing the configuration header.

	31	16	15	00
00	Device Identification		Vendor Identification	
04	Status		Command	
08	Class Code			Revision
0C	BIST	Header Type	Latency	Cache Size
10	Base Address Register #1			
14	Base Address Register #2			
18	Base Address Register #3			
1C	Base Address Register #4			
20	Base Address Register #5			
24	Base Address Register #6			
28	Reserved			
2C	Reserved			

30	Expansion ROM Base Address			
34	Reserved			
38	Reserved			
3C	Maximum Latency	Minimum Latency	Interrupt Pin	Interrupt Line

VENDOR IDENTIFICATION Field

The VENDOR IDENTIFICATION field contains read-only bits that identify the manufacturer of the device. The ID assigned to KineticSystems is 11F4 Hex.

DEVICE IDENTIFICATION Field

The DEVICE IDENTIFICATION field contains read-only bits which identify a particular device. The DEVICE ID field for this unit is 2962 Hex.

PCI COMMAND Register

The COMMAND field contains write/read bits used to configure basic PCI functions. The following diagram shows the COMMAND field as implemented by the 2962.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FST BTB	SER ENA	0	PER ENA	0	0	0	MAS ENA	MEM ENA	I/O ENA

<15:10> Not Used. These bits are not used and read as zeros.

<9> FAST BACK-TO-BACK is a write/read bit used to enable or disable the 2962 from executing "fast" back-to-back bus master cycles after completing a write cycle. Setting this bit to a one enables fast transfers and a zero disables the mode.

<8> SYSTEM ERROR ENABLE is a write/read bit used to enable and disable the 2962 from driving the PCI SYSTEM ERROR (SERR) signal. This signal is used by the 2962 to inform the host CPU of a parity error during an address or control portion of a bus operation. Setting this bit to a one enables the 2962 to assert SERR and disabled with a zero.

<7> Not Used. These bits are not used and read as zeros.

<6> PARITY ERROR ENABLE is a write/read bit used to enable and disable the 2962 from driving the PCI PARITY ERROR (PERR) signal. This signal is asserted by the 2962 when a parity error is detected during a data transfer to/from the 2962. The PERR function is enabled by setting this bit to a one and disabled with a zero.

<5:3> Not Used. These bits are not used and read as zeros.

<2> BUS MASTER ENABLE is a write/read bit which enables and disables the 2962 from executing bus master operations. Setting this bit to a one enables the 2962 to function as a bus master and a zero disables the master operation. Since the 2962 interface hardware actually controls bus master operations, this bit is not used.

<1> MEMORY SPACE ENABLE is a write/read bit that allows the 2962 to function in memory regions that may be defined in one of the base address registers. Since the 2962 is initially configured as an I/O device, this bit should be set to zero.

<0> I/O SPACE ENABLE is a write/read bit that allows the 2962 to function in I/O regions as defined in one of the base address registers. This bit is set to a one which allows the 2962 to function in I/O regions.

PCI STATUS Register

The PCI STATUS Register is used to record status information regarding PCI bus transfers. This register contains read-only bits and write/read bits. The following diagram shows the Status Register bits implemented by the 2962.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PAR DET	SIG SER	RCV MAB	RCV TAB	SIG TAB	DEV TM1	DEV TM0	DP RPT	1	0	0	0	0	0	0	0

<15> DETECTED PARITY ERROR is a write/read bit which is set whenever the 2962 detects a PCI parity error. This bit does not depend on the state of the PAR ENA bit in the PCI COMMAND Register. Once an error has been detected ,this may be cleared by writing a one to bit position 15.

<14> SIGNALED SYSTEM ERROR is a write/read bit which is set whenever the 2962 asserts the PCI SYSTEM ERROR (SERR) signal. Once this bit is set, it may be cleared by writing a one to bit position 14.

<13> RECEIVED MASTER ABORT is a write/read bit which is set when the 2962 is accessed as a target and the master aborts the transaction. This bit can be reset by writing a one to this bit position.

<12> RECEIVED TARGET ABORT is a write/read bit which is set when the 2962, acting as a bus master, has initiated a transfer and the addressed target aborts the transfer. This bit can be reset by writing a one to this bit position.

<11> SIGNALED TARGET ABORT is a write/read bit that is set when a bus master accesses the 2962 as a target and the 2962 aborts the cycle. This bit is reset when a one is written to this bit location.

<10:9> DEVICE SELECT TIMING 1 and 0 encode the timing of the PCI DEVSEL (Device Select) signal. This time reflects the slowest time that a device asserts DEVSEL for any bus command except Configuration Read and Configuration Write. Since the 2962 may be accesses in the fast mode, these bits are set to zero.

<8> DATA PARITY REPORTED is a write/read bit which is set when the 2962 detects a parity error when the 2962 is a bus master. This bit can be reset by writing a one to this bit position.

REVISION Field

The REVISION field contains read-only bits which reflect the current revision level of the 2962. The 2962 starts at revision one and subsequent revisions increment the number.

CLASS CODE Field

The CLASS CODE field actually contains three subfields that represent device characteristics. These three subfields are the BASE CLASS, the SUB-CLASS and the PROG I/F fields. These subfields define such parameters as network controllers, display controllers, video device, etc. The 2962 does not fit into any of the defined class codes. Therefore, the class code that the 2962 uses is FF0000 Hex which indicates that the 2962 class code is undefined by the PCI specification.

CACHE LINE SIZE Field

The CACHE LINE SIZE field is used by the system to define the cache line size. The 2962 does not use Memory Write and Invalidate PCI bus cycles when operating as a bus master and therefore sets this field to zero.

LATENCY TIMER REGISTER

The LATENCY TIMER REGISTER is only used when the 2962 is operating as a bus master. The values loaded in this register are the minimum number of PCI bus clocks that the 2962 can be guaranteed as a master. After the 2962 becomes bus master and asserts the PCI FRAME signal, the Latency Timer is decremented for each PCI bus clock. Subsequent to the timer decrementing to zero, the 2962 ignores the PCI bus grant signal and continues to transfer data until the timer expires. The value loaded into this register is in multiples of eight clock cycles since the low 3 bits of this field are hardwired to zero.

HEADER Field

The HEADER field establishes whether a PCI device contains a single function or multi-function PCI bus agent. Since the 2962 contains only a single function, this field is set to zero.

BUILD IN SELF TEST Field

This field is used to present Built In Self Test diagnostic results to a bus master. The 2962 does not implement BIST and returns a zero for this field.

BASE ADDRESS REGISTERS

The BASE ADDRESS REGISTERS are used to specify the memory or I/O requirements of add-in devices and also to configure the base addresses of these devices.

After power-up, system software can determine how much address space a particular device requires by writing all ones to a base address register and then reading that value back. The device returns zeros in all address bit locations that do not define the base address.

The least significant bit in each of the base address registers is used for specifying the region of address space for which the device is to reside. A value of zero specifies a memory region and a value of one specifies an I/O region. The 2962 is configured to operate in the I/O region.

The 2962 implements two of the Base Address registers. The first Base Address register is used to communicate with the PCI Interface Operational Registers (IOR) and the second is used to communicate with the Highway Operational Registers (HOR). The Interface Operational Registers require 16 longwords (64 bytes) of address space. A read of the first base address register, after a write of all ones, returns the value FFFFFFC1 Hex, indicating a request for 16 longwords of I/O space.

The Highway Operational Registers require 16 longwords (64 bytes) of address space. A read of the second base address register, after a write of all ones, returns the value FFFFFFC1 Hex, indicating a request for 16 longwords in I/O space.

After the system software has determined the total address space requirements of the system, it assigns the base addresses to memory and I/O devices by writing their Base Address Registers.

EXPANSION ROM BASE ADDRESS Register

This field is used to assign a physical memory address to expansion ROM in a system. The 2962 does not contain an expansion ROM and therefore does not require use of this field.

INTERRUPT LINE Field

This write/read field is used for communicating interrupt routing information and is configured by the PCI BIOS after power-up. The value in this field informs the system interrupt controller which pin of the controller the interrupt is connected to.

INTERRUPT PIN Field

The INTERRUPT PIN field is read-only and specifies which PCI interrupt pin that the 2962 is connected to. The 2962 returns a value of one in this field indicating that it uses the INTA interrupt.

MINIMUM GRANT Register

This write/read register is used by bus masters to specify the minimum amount of time the device needs for a period of burst transfers. Since the 2962 does not have this requirement, a value of zero must be used.

2962 Operational Registers

The 2962 PCI Interconnect Highway Driver (IHD) uses several I/O addressable registers to control and monitor operations. All data transfers to/from the 2962 must be executed using 32-bit data transfers. The 2962 does not accommodate byte or shortword accesses.

The 2962 incorporates a PCI Interface Controller manufactured by Applied Micro Circuits Corporation, the S5933. This device contains several PCI configuration registers and also some of the 2962 operational registers. The primary register that the 2962 uses is the bidirectional FIFO register. This FIFO is used in transferring data to/from slave nodes on the interconnect highway. A Control/Status register provides access to FIFO flags.

PCI Interface Operational Registers

The PCI Interface Operational Registers are contained in the PCI interface chip used on the 2962. This chip is the S5933 and is manufactured by Applied Micro Circuits Corporation. The base address of these registers is loaded by power-on BIOS routines and is contained in the Base Address Register #1 location of the PCI Configuration Registers.

Note: All references to Incoming and Outgoing are referred to the host. An Outgoing operation is a write operation from the host and an Incoming operation is a read operation from the 2962.

The following chart shows the various PCI Interface Registers along with their offsets from the base address.

Offset	Register	Access
0	Outgoing Mailbox #1	W/R
4	Outgoing Mailbox #2	W/R
8	Outgoing Mailbox #3	W/R
C	Outgoing Mailbox #4	W/R
10	Incoming Mailbox #1	R
14	Incoming Mailbox #2	R
18	Incoming Mailbox #3	R
1C	Incoming Mailbox #4	R
20	Data FIFO	W/R
24	Master Write Address	R
28	Master Write Transfer Count	R
2C	Master Read Address	R
30	Master Read Transfer Count	R
34	Mailbox Empty/Full Status	W/R
38	Interrupt Control/Status	W/R
3C	Bus Master Control/Status	W/R

Outgoing/Incoming Mailboxes

The Incoming and Outgoing Mailboxes are used by the KineticSystems software drivers to provide a communication mechanism between the DSP and the host CPU. The details of this communication scheme is beyond the scope of this manual.

Data FIFO Register

The Data FIFO Register is composed of two 8 x 32-bit FIFOs located in the PCI interface chip. When executing Interconnect Highway operations, all write and read data passes through these FIFOs. Data transfers to or from these FIFOs can be done by either programmed transfers executed by the host or by allowing the 2962 to become a bus master and transfer the data.

When executing write operations to the highway, the write data is first written to the Data FIFO Register. The data is then moved from the PCI interface chip to a 2K X 16-bit FIFO external to the chip in preparation for transmission onto the highway. When read operations from the highway are executed, the read data is initially stored in a 2K X 16 FIFO before transfer to the PCI interface chips' 8 X 32 FIFO.

Several status indicators are provided which indicate the amount of data contained in the PCI interface chip FIFOs and the external 2K X 32 FIFOs. The Bus Master Control/Status register contains 6 status bits that correspond to the PCI Interface chip internal FIFOs. Two status bits are provided in the Control/Status register of the Highway Operational registers for the two external 2K X 32 FIFOs. Both sets of status flags must be used in determining the amount of data contained in the write FIFO data path or the read FIFO data path.

Master Write Address Register

The Master Write Address Register is a read-only register that contains the last address that was accessed during a bus master write operation executed by the 2962. This address is actually pointing to one longword beyond the last address accessed since the memory address is incremented after each execution of a data transfer.

The Master Write Address Register can be written to by either the DSP or by programmed I/O through the Highway Operational Registers. When the Memory Address Register (MAR) of the Highway Operational Registers is written by programmed I/O or by the DSP, a hardware mechanism loads both the Master Write Address Register and the Master Read Address Register.

After a bus master operation completes, the current memory address minus 4 may be read from the Master Write Address Register. The initial memory address used for the bus master operation can be read through the Memory Address Register of the Highway Operational Registers.

Master Write Transfer Count Register

This register is not used by the 2962. When executing bus master operations, the 2962 uses the Total Transfer Count Register of the Highway Operational Registers to determine the number of bus operations to perform.

Master Read Address Register

The Master Read Address Register is a read-only register that contains the last address that was accessed during a bus master read operation executed by the 2962. This address is actually pointing to one longword beyond the last address accessed since the memory address is incremented after each execution of a data transfer.

The Master Read Address Register can be written to by either the DSP or by programmed I/O through the Highway Operational Registers. When the Memory Address Register (MAR) of the Highway Operational Registers is written by programmed I/O or by the DSP, a hardware mechanism loads both the Master Write Address Register and the Master Read Address Register.

After a bus master operation completes, the current memory address minus 4 may be read from the Master Read Address Register. The initial memory address used for the bus master operation can be read through the Memory Address Register of the Highway Operational Registers.

Master Read Transfer Count Register

This register is not used by the 2962. When executing bus master operations, the 2962 uses the Total Transfer Count Register of the Highway Operational Registers to determine the number of bus operations to perform.

Mailbox Empty/Full Status Register

The Empty/Full Status Register is used by the KineticSystems software driver to implement "special" functions. The communication scheme for the mailbox register used in the software driver is beyond the scope of this manual. The following shows the bit pattern for the Mailbox Empty/Full Status Register. The register is shown here for completeness only.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IMB 4D	IMB 4C	IMB 4B	IMB 4A	IMB 3D	IMB 3C	IMB 3B	IMB 3A	IMB 2D	IMB 2C	IMB 2B	IMB 2A	IMB 1D	IMB 1C	IMB 1B	IMB 1A
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
OMB 4D	OMB 4C	OMB 4B	OMB 4A	OMB 3D	OMB 3C	OMB 3B	OMB 3A	OMB 2D	OMB 2C	OMB 2B	OMB 2A	OMB 1D	OMB 1C	OMB 1B	OMB 1A

The IMB bits refer to the incoming mailbox registers. The OMB bits refer to the outgoing mailbox registers. The numbers 1 through 4 refer to the mailbox number and the letters D through A refer to the byte within the longword. Since the mailbox may only be written as longwords from either side, all byte indicators within a word will be either set or cleared.

PCI Interface Interrupt Control/Status Register

The PCI Interface Interrupt Control/Status Register of the PCI Interface Operational Registers is used to monitor and control interrupts generated by the PCI interface chip. Before an interrupt is sourced from the interface chip to the PCI bus, it must be enabled with the PCI INTERRUPT ENABLE bit in the Interrupt Control/Status Register of the Highway Operational Registers.

The following shows the bit pattern for the Interrupt Control/Status Register of the PCI Interface Operational Registers.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	INT REQ	0	TAR ABT	MAS ABT	RTC	WTC	IMB SRC	OMB SRC
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
RTC IE	WTC IE	0	IMB IE	IMB EMB	IMB EMA	IMB EBB	IMB EBA	0	0	0	OMB IE	OMB EMB	OMB EMA	OMB EBB	OMB EBA

<31:24> These 8 bits control endian conversion and must be set to zero for the 2962 to operate properly.

<23> INTERRUPT REQUEST is a read-only bit that is set when the PCI interface chip is requesting service. This bit reflects the interrupt output of the PCI chip and does not indicate that the PCI bus interrupt is asserted. If the PCI Interrupt Enable bit of the Interrupt Control/Status Register of the Highway Operational Registers is set to a one, this bit indicates that a PCI bus interrupt is requested.

<22> This bit is not used and is read as a zero.

<21> TARGET ABORT is a read/write-to-clear bit that indicates when the 2962 executes a bus master transfer and the addressed target aborts the transfer. An interrupt source is generated when this bit is set. This bit is cleared by writing a one to this bit position.

<20> MASTER ABORT is a read/write-to-clear bit that indicates when the 2962 executes a bus master operation and the addressed target does not respond. An interrupt source is generated when this bit is set. A write operation to this register with this bit set to a one clears the bit.

<19> READ TRANSFER COMPLETE is a read/write-to-clear bit that is set when the Master Read Transfer Count Register is decremented to zero. Since the 2962 does not use this register, the bit should never be set.

<18> WRITE TRANSFER COMPLETE is a read/write-to-clear bit that is set when the Master Write Transfer Count Register is decremented to zero. Since the 2962 does not use this register, the bit should never be set.

<17> INCOMING MAILBOX INTERRUPT SOURCE is a read/write-to-clear bit that is set to a one when the mailbox selected by bits 12 through 8 of this register are written by the DSP. An interrupt source is generated when this bit is a one. A write operation with this bit set to a one clears the bit.

<16> OUTGOING MAILBOX INTERRUPT SOURCE is a read/write-to-clear bit that is set to a one when the mailbox selected by bits 4 through 0 of this register is read by the DSP. An interrupt source is generated if this bit is set to a one. A write operation with this bit set to a one causes the bit to be cleared.

<15> READ TRANSFER COMPLETE INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of an interrupt when the read transfer count is exhausted. Since the 2962 does not used the Master Read Transfer Count, this bit should always be set to the disable state.

<14> WRITE TRANSFER COMPLETE INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of an interrupt when the write transfer

count is exhausted. Since the 2962 does not used the Master Write Transfer Count, this bit should always be set to the disable state.

<13> This bit is not used and is read as a zero.

<12> INCOMING MAILBOX INTERRUPT ENABLE is a write/read bit that is used to enable/disable the generation of an interrupt source when a preselected incoming mailbox register is written. Bits 11 through 8 of this register select which mailbox register write operation will generate the interrupt source.

<11:10> INCOMING INTERRUPT SELECT bits are used to select which incoming mailbox write operations are to generate an interrupt source. The binary combinations of these bits determine which mailbox to enable. Data 0 is mailbox #1, data 1 is mailbox #2, data 2 is mailbox #3 and data 3 is mailbox #4.

<9:8> INCOMING MAILBOX BYTE INTERRUPT SELECT bits are used to select which byte of the mailbox, selected by bits 11 and 10 of this register, are actually causing the interrupt source.

<7:5> These bits are not used and are read as zeros.

<4> OUTGOING MAILBOX INTERRUPT ENABLE is a write/read bit that is used to enable/disable the generation of an interrupt when a preselected outgoing mailbox register is written. Bits 3 through 0 of this register select which mailbox write operation will generate the interrupt source.

<3:2> OUTGOING INTERRUPT SELECT bits are used to select which outgoing mailbox write operations are to generate an interrupt source. The binary combinations of these bits determine which mailbox to enable. Data 0 is mailbox #1, data 1 is mailbox #2, data 2 is mailbox #3 and data 3 is mailbox #4.

<1:0> OUTGOING MAILBOX BYTE INTERRUPT SELECT bits are used to select which byte of the mailbox, selected by bits 3 and 2 of this register, are actually causing the interrupt source.

Bus Master Control/Status Register

The Bus Master Control/Status Register is used to monitor/control bus master operations and to check status of the two PCI interface chip FIFOs. The following diagram shows the bit pattern for the Bus Master Control/Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	MBX RST	INF RST	OTF RST	AON RST	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	IFE MT	IFI 4+	IFI FUL	OTF MT	OTF 4+	OTF FUL

The bits shown as zeros in the preceding bit layout must be set to zeros when writing to the Bus Master Control/Status Register. The bits that have non-zero indications are the only useful bits in this register. The remaining bits are reserved for diagnostic purposes. Even though some of these bits are shown as zeros, they may eventually be read as ones. Note that the Inbound FIFO refers to the internal PCI controller interface chips' FIFO for executing highway read operations and the Outbound FIFO refers to highway write operations.

<31:28> These bits are not used but must be written to zero.

<27> MAILBOX FLAG RESET is a write-only bit which resets all of the mailbox status flags.

<26> INBOUND FIFO RESET is a write-only bit which clears the inbound FIFO, Inbound FIFO +4 bit, Inbound FIFO Full and sets the Inbound FIFO Empty flag.

<25> OUTBOUND FIFO RESET is a write-only bit which clears the outbound FIFO, Outbound FIFO +4 bit, Outbound FIFO Full and sets the Outbound FIFO Empty bit.

<24> ADD-ON RESET is a write-only bit which, when set to a one, resets all of the Highway Operational Registers.

<23:6> These bits are not used but must be written to zero.

<5> INBOUND FIFO EMPTY is a read-only bit which is set when the inbound FIFO contains no data.

<4> INBOUND FIFO +4 is a read-only bit and is set to a one as long as there are at least 4 longwords of data in the inbound FIFO.

<3> INBOUND FIFO FULL is a read-only bit that is set when the incoming FIFO is full.

<2> OUTBOUND FIFO EMPTY is a read-only bit which is set when the outbound FIFO contains no data.

<1> OUTBOUND FIFO +4 SPACES is a read-only bit and is set to a one as long as there are at least 4 empty longwords in the outbound FIFO.

<0> OUTBOUND FIFO FULL is a read-only bit that is set when the outbound FIFO is full.

HIGHWAY OPERATIONAL REGISTERS

The following section describes the registers used to control operations directed toward the Interconnect Highway. The base address of these registers is set dynamically when the computer is powered-up and the PCI BIOS is executed. The PCI BIOS determines the resources required by each add-in card and allocates memory and I/O addresses accordingly. After the setup has been completed, the Base Address Register #2 from the PCI Interface Registers may be read to determine the address allocated to the 2962 by the PCI BIOS.

Address	Register Description	Mnemonic
Base + 00	Control/Status Register	CSR
Base + 04	Interrupt Control/Status Register	ICSR
Base + 08	Timer Control Register	ICR
Base + 0C	Command Memory Address Register	CMA
Base + 10	Command Memory Data Register	CMD
Base + 14	List Transfer Count Register	LTCR
Base + 18	Total Transfer Count Register	TTCR
Base + 1C	Memory Address Register	MAR
Base + 20	Buffer Interval Counter	BIC
Base + 24	Multi-Buffer Control Register	MBMCT
Base + 28	Demand FIFO Register	DFR
Base + 2C	Reset Interface	RSTIFC
Base + 30	Reset Demand FIFO	RSTDFR
Base + 34 through Base + 3F	Reserved	

Appendix A contains a composite register layout chart for the 2962.

Model 2962

Control/Status Register(CSR)

Write Operations:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
0	0	0	0	0	0	0	0	0	0	APND STA	RLD ENA	DMA DIR	DMA ENA	SUSP	GO

Read Operations:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR CD3	ERR CD2	ERR CD1	ERR CD0	VXI TMO	QTMO	N>23	ILLG CMD	RMT PER	NO SYNC	0	PAR ERR	TMO	ADNR	NOX	NOQ
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
0	0	LIST INT	DMD OFLO	DMD PND	0	XMT FULL	RCV DAV	DONE	0	APND STAT	RLD ENA	DMA DIR	DMA ENA	SUSP	0

<31:28> ERROR CODE3 through 0 are read-only bits which encode the source of a 2962 error. The following chart shows the error code hex pattern along with the source of the error. The error sources are encoded by a priority encoder resulting in the highest priority error being displayed in the case where multiple errors are encountered. Individual bits in the CSR may be read to determine other error sources that may have occurred along with the highest priority error encoded.

Error Code	Error Source
F	Reserved.
E	Reserved.
D	PARITY ERROR. The 2962 highway receiver detected a parity error on the incoming message.
C	ADDRESS_NOT_RECOGNIZED. An addressed highway command message was transmitted by the 2962 and then received by the 2962 indicating that the addressed slave did not accept the message.
B	TIMEOUT. A highway command message was transmitted by the 2962 and a reply message was not received within the preselected timeout period.
A	VXI TIMEOUT. A VXI bus timeout occurred in the VXI chassis addressed during the last highway operation.
9	Reserved.
8	N GREATER THAN 23. N>23 indicates that a Q-Scan operation in a CAMAC chassis resulted in the station number incrementing beyond 23.

7	Q-REPEAT TIMEOUT. This error code is generated when a Q-Repeat operation in the addressed CAMAC chassis did not receive a CAMAC Q-response of one within the 200 millisecond timeout period.
6	NO-X. A highway operation to an addressed CAMAC chassis resulted in a CAMAC X-response of zero.
5	NO-Q. A highway operation to an addressed CAMAC chassis resulted in a CAMAC Q-response of zero.
4	ILLEGAL COMMAND. This error code is generated when an attempt is made at accessing a non-existent location within a CAMAC or VXI controller.
3	REMOTE PARITY ERROR. This code is generated when an addressed slave receives a parity error.

Error Code	**Error Source**
2	Reserved.
1	Reserved.
0	NO ERROR. There are no errors to report from the 2962.

< 27> VXI/VME TIMEOUT is a read-only bit that is set when an operation in an addressed VXI/VME chassis resulted in a bus timeout.

< 26> Q-REPEAT TIMEOUT is a read-only bit that is set when a Q-Repeat operation in an addressed CAMAC chassis failed to receive a CAMAC Q-response of one within the 200 millisecond timeout period.

< 25> N GREATER THAN 23 is a read-only bit that is set when a Q-Scan operation in an addressed CAMAC chassis terminated due to the CAMAC station number incrementing beyond 23.

< 24> ILLEGAL COMMAND is a read-only bit that is set when an attempt is made to access a non-existent address location within a CAMAC or VXI controller.

< 23> REMOTE PARITY ERROR is a read-only bit which is set when an addressed slave receives a parity error.

< 22> NO SYNC is a read-only bit that is set when the 2962 highway driver is not receiving a synchronization message from the highway. When no list processing operations are occurring, the 2962 sends a synchronization message around the highway, expecting to see it returned. The SYNC LED may not be lit during large block transfer operations since the sync message is not inserted during large data transfers. A loss of the SYNC signal during large data transfers does not set any NO SYNC error conditions.

< 21> This bit is not used and is read as a zero.

< 20> PARITY ERROR is a read-only bit which is set when the 2962 receives a message that contains a parity error.

<19> TIMEOUT is a read-only bit that is set when the 2962 transmits a command message to a slave and the slave does not respond within the selectable timeout period. This period can range from 3 to 10 seconds.

< 18> ADDRESS_NOT_RECOGNIZED is a read-only bit that is set when the 2962 transmits a command message to a slave and receives the message back indicating that the addressed slave did not respond.

< 17> NO-X is a read-only bit which is set when an addressed CAMAC chassis operation resulted with a CAMAC X-response of zero.

< 16> NO-Q is a read-only bit which is set when an addressed CAMAC chassis operation resulted with a CAMAC Q-response of zero.

<15:14> These bits are not used and are read as zeros.

<13 > LIST INTERRUPT is a read-only bit that is set when the list processing DSP asserts an interrupt to the host computer. This bit also appears in the Interrupt Control/Status Register.

< 12> DEMAND OVERFLOW is a read-only bit that is set when the 2962 has 2048 demands pending in the Demand FIFO Register and a subsequent demand message is received. This bit may be cleared by a write operation to the Clear Demand FIFO Register address.

< 11> DEMAND PENDING is a read-only bit which is set when at least one demand message is contained in the Demand FIFO Register.

< 10> This bit is not used and is read as a zero.

< 9> TRANSMIT FULL is a read-only bit that reflects the status of the highway transmitter write data FIFO. The full flag is used to determine if the FIFO may accept additional write data words when executing programmed I/O highway operations. As long as this bit is zero, the FIFO may be written.

< 8> RECEIVE DATA AVAILABLE is a read-only bit which is set to a one as long as highway read data is contained in the read data FIFO. This bit is used for programmed I/O read operations for determining data availability.

< 7> DONE is a read-only bit which indicates when the 2962 is not executing any list operations. Once a list operation is initiated, the DONE bit is set to a zero until the operation is completed.

<6> This bit is not used and is read as a zero.

<5> APPEND STATUS is a write/read bit that enables and disables the appending of a status word after a list execution terminates. Setting this bit to a one enables the status append and a zero disables the function. Refer to the Append Status section of this manual for additional information.

<4> RELOAD ENABLE a write/read bit used to control the automatic reloading of the Memory Address and Total Transfer Count Registers once the transfer count register is exhausted. Setting this bit to a one enables reloading and a zero disables reloading.

<3> DMA DIRECTION is a write/read bit that specifies the direction of DMA transfers. A direction of zero specifies DMA transfers from host memory to the 2962 (write operations). A one specifies DMA transfers from the 2962 to host memory (read operations).

< 2> DMA ENABLE is a write/read bit that is used to enable/disable DMA activity. Setting this bit to a one enables DMA operations to occur when the list processor requests data transfers. A zero allows for programmed I/O transfers and disables DMA operations.

< 1> SUSPEND is a write/read bit used to suspend list processing operations in the 2962. After SUSPEND is set to a one, the host must wait for the DONE bit to be set before using the 2962 for other operations. After the DONE bit has been set, the SUSPEND bit may then be written back to a zero.

< 0> GO is a write-only bit that is used to initiate list processing operations at the address specified in the List Memory Address Register.

Interrupt Control/Status Register

The Interrupt Configuration Register (ICSR) is a write/read register located at an offset of 4 from the selected base address. This register is used to enable/disable the various sources of interrupts on the 2962. Status bits are also in this registers reflecting the state of the interrupt sources. Once enabled and sourced, the 2962 asserts the PCI INTA signal to the host.

The 2962 has five sources of interrupts as follows:

1.) List Processing Done
2.) List Interrupt
3.) Demand
4.) Multi-Buffer Interrupt.
5.) A PCI Interface Controller Interrupt.

The ICSR contains individual enables and status bits for each of the five sources. To allow an interrupt status bit to be enabled in the ICSR, the corresponding enable bit must be set to a one. Interrupt sources are disabled by setting the bit to a zero. In the case where polling is used instead of interrupt generation, the interrupt source bits may be cleared by writing to the ICSR with the data set equal to the source bit to be cleared.

The following diagram shows the bit layout of the Interrupt Control/Status Register.

Interrupt Control/Status Register (ICSR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	PCI INT	MBM INT	DMD INT	LIST INT	DONE INT	PCI IE	MBM IE	DMD IE	LIST IE	DONE IE

<31:10> These bits are not used and read as zero.

< 9> PCI INTERFACE INTERRUPT SOURCE is a read only bit which reflects the status of the PCI interface chips' interrupt source. The actual source of these interrupts may be found in the PCI Interrupt Control/Status Register.

< 8> MULTIBUFFER MEMORY INTERRUPT SOURCE is a read/write-to-clear bit that is set when the Buffer Interval Counter overflows and this interrupt source is enabled. A write of this bit with data set to one clears the source. The MBM IE bit in this register must be set to a one to enable this source.

< 7> DEMAND INTERRUPT SOURCE is a read/write-to-clear bit that is set whenever a demand message is received by the 2962 and this interrupt source is enabled. A write of this bit with data set to one clears the source. The DMD IE bit in this register must be set to a one to enable this interrupt source.

< 6> LIST INTERRUPT SOURCE is a read/write-to-clear bit that is set when the list processor executes a Generate Host Interrupt instruction. A write of this bit with data set to one clears the source. The LIST IE bit in this register must be set to a one to enable this interrupt source.

< 5> DONE INTERRUPT SOURCE is a write/read bit that is set when the 2962 completes execution of a list and this interrupt source is enabled. A write of this bit with data set to a one clears the source. The DONE IE bit in this register must be set to a one to enable this source.

< 4> PCI INTERFACE INTERRUPT ENABLE is a write/read bit that is used to enable/disable the generation of a PCI interrupt request when the PCI Interface chip requires service. Setting this bit to a one enables the interrupt source and a zero disables the source.

< 3> MULTIBUFFER MEMORY INTERRUPT SOURCE ENABLE is a write/read bit that enables/disables the assertion of an interrupt source when the Buffer

Interval Counter overflows during multibuffer operations. Setting this bit to a one enables this interrupt source and disabled with a zero.

< 2> DEMAND INTERRUPT SOURCE ENABLE is a write/read bit that enables/disables the generation of an interrupt source when the 2962 receives a demand message from the highway. Setting this bit to a one enables the interrupt source and a zero disables the source.

<1 > LIST INTERRUPT SOURCE ENABLE is a write/read bit used to enable/disable the assertion of an interrupt source when the list processor executes a Generate Host Interrupt instruction. Setting this bit to a one enables the interrupt source and a zero disables the source.

<0> DONE INTERRUPT SOURCE ENABLE is a write/read bit used to enable/disable the generation of an interrupt source when a list processing operation completes. Setting this bit to a one enables the interrupt source and a zero disables the source.

Timer Control Register

The Timer Control Register (TCR) is a write/read register located at an offset of 08 hex from the selected base address. This register is used to specify the frequency at which list execution is initiated during timer initiated list processing operations.

The timer frequency can range from 250 Kilohertz to .059 hertz. This range yields 'tic' rates (periods) from 40 microseconds to 16.777 seconds in 1 microsecond increments. This timer rate specification does not refer to the interval at which each element in the list is executed but the rate at which the entire list is initiated. This automatic mode is enabled with bit 24 in this register.

The 2962 provides for an external clock input that control the rate at which the list is started. This input is routed through the external clock LEMO connector mounted on the front panel of the 2962. The clock period may range from 250 kHz to DC. The input signal is low true and must have a minimum pulse width of 200 nanoseconds and a maximum of 1 microsecond.

If the timer rate selected for list execution is faster than the time it takes to execute the entire list, the clock transitions that occur while the list is executing are ignored.

The data for this register is calculated as follows:

$$((1/\text{Desired Frequency})/1 \text{ X } 10^{-6}) -1$$

The following diagram shows the bit layout of the Timer Control Register.

Timer Control Register (TCR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	CLK SRC	TMR ENA	TCR 23	TCR 22	TCR 21	TCR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

<31:26> These bits are not used and are read as zeros.

<25> CLOCK SOURCE is a write/read bit that selects the source of the timing signal that initiates list execution when the TMR ENA bit is set to a one. Setting the CLK SRC bit to a one selects the external clock input and a zero selects the internal timer.

<24> TIMER ENABLE is a write/read bit that is used to enable/disable timer initiated list processing operations. Setting this bit to a one enables timer initiated operations and a zero disables timer operations.

<23:0> TIMER CONTROL RATE23 through 0 are write/read bits that are used to select the rate at which list processing operations are initiated when the timer operations are enabled. The least significant bit of this field corresponds to a 1 microsecond interval. The data loaded in this register is actually one less than the desired interval. For example, to select a 250 microsecond interval, load the value 249 into this register.

Command Memory Address Register

The Command Memory Address Register (CMA) is a write/read register located at an offset of 0C Hex from the selected base address. This register is used for several purposes. The CMA is used to specify the start address for list processing, specify the memory address at which subsequent write/read operations to the Command Memory Data Register occur, and to read the last address that the list processor accessed during a list processing operation.

The Command Memory Data Register (CMD) is a 32K X 32 memory that is used to hold the list processing instructions to be executed. The CMD is loaded by executing programmed I/O write operations to offset 10 Hex. Prior to executing the initial write to the memory, the CMA must first be loaded with the first address location to access. The valid address range is 0 to 7FFF Hex. After the CMA is loaded, the first CMD data word may then be written. After a write operation to the CMD, the CMA is automatically incremented to the next address location. This allows the CMD to be loaded without having to write the CMA for every CMD write operation.

If it is necessary to read the CMD, the CMA must first be loaded with the initial address to be accessed. After a word of data is read from the CMD, the CMA is automatically incremented to the next address location.

A bit in this register is also provided which initiates a single list processing operation. Setting this bit causes the same operation as setting the GO bit in the Control/Status Register.

The format of the Command Memory Address Register is shown in the following diagram.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	**14**	**13**	**12**	**11**	**10**	**09**	**08**	**07**	**06**	**05**	**04**	**03**	**02**	**01**	**00**
LIST GO	CMA 14	CMA 13	CMA 12	CMA 11	CMA 10	CMA 9	CMA 8	CMA 7	CMA 6	CMA 5	CMA 4	CMA 3	CMA 2	CMA 1	CMA 0

<31:16> These bits are not used and are read as zeros.

<15> LIST GO is a write-only bit which is set to a one to initiate a list processing operation. Setting this bit has the same effect as setting the GO bit in the CSR. This bit is not latched.

<14:0> COMMAND MEMORY ADDRESS14 through 0 are used for specifying the initial address for CMD write/read operations, the initial address for list execution, and for determining where the list processor halted after list processing.

Command Memory Data Register

The Command Memory Data Register (CMD) is a write/read register located at an offset of 10 Hex from the selected base address. This register is used to load the instructions for the list processor. The format of these instructions/commands may be found in the Command Memory Instructions section of this manual.

The Command Memory is a 32K X 32 memory which is accessed by programmed I/O. Before initial words may be written to the CMD, the Command Memory Address Register (CMA) must be loaded. After the CMA is loaded with the first address of the CMD to access, the CMD may then be written. After a write operation to the CMD, the CMA is automatically incremented to the next sequential address location. This eliminates the need to reload the CMA for every access to the CMD.

If necessary, the CMD may be read to verify its contents. As with write operations to the CMD, the CMA must be loaded prior to the initial access to the CMD. After a read operation is executed to the CMD, the CMA is automatically incremented.

The format of the Command Memory Data Register is shown in the following diagram.

Command Memory Data Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMD 31	CMD 30	CMD 29	CMD 28	CMD 27	CMD 26	CMD 25	CMD 24	CMD 23	CMD 22	CMD 21	CMD 20	CMD 19	CMD 18	CMD 17	CMD 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMD 15	CMD 14	CMD 13	CMD 12	CMD 11	CMD 10	CMD 9	CMD 8	CMD 7	CMD 6	CMD 5	CMD 4	CMD 3	CMD 2	CMD 1	CMD 0

<31:0> COMMAND MEMORY DATA31 through 0 are write/read bits used to load/read the 32K X 32 Command Memory.

List Transfer Count Register

The List Transfer Count Register (LTCR) is a read-only register located at an offset of 14 Hex from the selected base address. This register returns the two's complement of the number of transfers remaining during a block transfer mode of operation. When the list processor encounters a block transfer instruction, it loads the 32-bit List Transfer Count Register with the count specified in the instruction. This value is the two's complement of the maximum number of transfers that are to occur for the block transfer operation. When this counter is incremented to zero, the block transfer operation terminates and the next instruction in the list is interpreted. If an error occurs during the block operation, the LTCR may then be read to determine the number of transfers remaining.

The Transfer Count reflects the number of transfers without regard to the data word size.

The following diagram shows the bit pattern for the List Transfer Count Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 31	LTC 30	LTC 29	LTC 28	LTC 27	LTC 26	LTC 25	LTC 24	LTC 23	LTC 22	LTC 21	LTC 20	LTC 19	LTC 18	LTC 17	LTC 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LTC 15	LTC 14	LTC 13	LTC 12	LTC 11	LTC 10	LTC 9	LTC 8	LTC 7	LTC 6	LTC 5	LTC 4	LTC 3	LTC 2	LTC 1	LTC 0

<31:0> LIST TRANSFER COUNT31 through 0 are read-only bits Which reflect the number of transfers remaining after a block transfer operation concludes. This data is in two's complement format.

Total Transfer Count Register

The Total Transfer Count Register (TTCR) is a write/read register located at an offset of 18 Hex from the selected base address. This register is used to specify the maximum number of DMA transfers that are to occur. Before a list operation is executed where data transfers to/from the highway occur using Direct Memory Access (DMA), the Total Transfer Count Register must be loaded with the two's complement of the maximum number of transfers. In case that the list terminates prematurely, the TTCR may be read to determine the number of transfers remaining to be executed.

Along with write access to the TTCR from the host by programmed I/O, the TTCR may also be loaded by using a list instruction. When the list processor encounters this instruction, the contents of the count specification are loaded into the TTCR.

The TTCR is incremented once for every DMA write or read access to PCI. When the counter increments to zero, the transfer is considered complete.

The following diagram shows the bit layout for the Total Transfer Count Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TTCR 31	TTCR 30	TTCR 29	TTCR 28	TTCR 27	TTCR 26	TTCR 25	TTCR 24	TTCR 23	TTCR 22	TTCR 21	TTCR 20	TTCR 19	TTCR 18	TTCR 17	TTCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TTCR 15	TTCR 14	TTCR 13	TTCR 12	TTCR 11	TTCR 10	TTCR 9	TTCR 8	TTCR 7	TTCR 6	TTCR 5	TTCR 4	TTCR 3	TTCR 2	TTCR 1	TTCR 0

<31:0> TOTAL TRANSFER COUNT31 through 0 are write/read bits which specify the maximum number of DMA transfers to execute. A read of this register returns the two's complement of the number of transfer remaining.

Memory Address Register

The Memory Address Register (MAR) is a write/read register located at an offset of 1C Hex from the selected base address. This register is used to specify the initial Direct Memory Access (DMA) address. Before any DMA operations are executed by the 2962, the MAR must be loaded with the first address to be accessed during DMA write or read operations. After the 2962 executes the first DMA operation, the MAR is automatically incremented to the next sequential longword address. Note that all DMA MAR specifications must be longword aligned.

When the RELOAD ENABLE bit in the CSR is enabled, the MAR may automatically reload itself after the Total Transfer Count Register is incremented to zero. The value that is reloaded is contained in the MAR. This feature allows the 2962 to DMA data to a circular buffer.

Along with write access to the MAR from the host by programmed I/O, the MAR may also be loaded by using a list instruction. When the list processor encounters this instruction, the contents of the count specification are loaded into the MAR.

DMA operations to/from the 2962 are always 32-bits in length. Therefore, the MAR specification must be on a longword boundary.

The following diagram shows the bit pattern for the Memory Address Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR 31	MAR 30	MAR 29	MAR 28	MAR 27	MAR 26	MAR 25	MAR 24	MAR 23	MAR 22	MAR 21	MAR 20	MAR 19	MAR 18	MAR 17	MAR 16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MAR 15	MAR 14	MAR 13	MAR 12	MAR 11	MAR 10	MAR 9	MAR 8	MAR 7	MAR 6	MAR 5	MAR 4	MAR 3	MAR 2	0	0

<31:2> MEMORY ADDRESS31 through 2 are write/read bits used to specify the initial DMA Memory Address.

<1:0> These bits are not used and are read as zeros.

Buffer Interval Counter

The Buffer Interval Counter (BIC) is a write/read register located at an offset of 20 Hex from the selected base address. This counter is used to define the number of DMA transfers that the 2962 executes before a multibuffer flag bit is set and an interrupt is generated. The BIC allows the 2962 to use host computer memory to simulate a multibuffer memory. When using this mode, the 2962 is continuously acquiring data and transferring the read data to memory via DMA. When a predetermined number of DMA transfers have occurred, a multibuffer flag is set and optionally an interrupt generated. When the host sees the flag set, it may then read the buffer of data received. As additional words are transferred to memory, subsequent multibuffer flags are set.

When the Total Transfer Count Register is incremented to zero, the Memory Address Register and Total Transfer Register are reloaded, creating a circular buffer. The reloading of the Memory Address Register and the Total Transfer Count Register is controlled through the RELOAD ENABLE bit in the Control/Status Register. As long as the RELOAD ENABLE bit is set, this data acquisition sequence continues until the 2962 is disabled.

Refer to the Multibuffer Operation section of this manual for additional information.

The following diagram shows the bit pattern for the Buffer Interval Counter.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIC 31	BIC 30	BIC 29	BIC 28	BIC 27	BIC 26	BIC 25	BIC 24	BIC 23	BIC 22	BIC 21	BIC 20	BIC 19	BIC 18	BIC 17	BIC 16
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BIC 15	BIC 14	BIC 13	BIC 12	BIC 11	BIC 10	BIC 9	BIC 8	BIC 7	BIC 6	BIC 5	BIC 4	BIC 3	BIC 2	BIC 1	BIC 0

<31:0> BUFFER INTERVAL COUNTER31 through 0 are write/read bits used to specify the number of DMA transfers that the 2962 executes before a multibuffer flag is set during multibuffered data acquisition.

Multibuffer Memory Control Register

The Multibuffer Memory Control Register (MBMCT) is a write/read register located at an offset of 24 Hex from the selected base address. This register is used to enable the multibuffer flags and to monitor the status of the flags.

Once multibuffer activity has been enabled, the multibuffer flags are incrementally set in this register as the Buffer Interval Counter (BIC) expires. The BIC is decremented as the 2962 executes each DMA operation. When the BIC is exhausted, the next sequential flag bit is set. After the fourth flag is set, the next expiration of the BIC causes the first flag to be set. If the host computer has not cleared a flag, via programmed I/O, before the 2962 loops around to set it again, the flag overflow bit is set. Refer to the Multibuffer Operation section of this manual for additional information.

The following diagram shows the bit pattern for the Multibuffer Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	MBM ENA	FLG OFLO	FLG 3	FLG 2	FLG 1	FLG 0

<31:6> These bits are not used and are read as zeros.

<5> MULTIBUFFER ENABLE is a write/read bit used to enable/disable the generation of the flag bits that correspond to the expiration of the Buffer Interval Counter (BIC). Setting this bit to a one enables the flags and disabled by a zero.

<4> FLAG OVERFLOW is a read/write-to-clear bit which is used to signify an overflow condition. This bit is set whenever the 2962 needs to set a multibuffer flag and the flag is already set; indicating that a buffer of data is being overwritten before the host could read the buffer and clear the flag. A write operation with this bit set to a one causes the overflow condition to be cleared.

<3:0> MULTIBUFFER FLAG3 through 0 are read/write-to-clear bits that are sequentially set as the Buffer Interval Counter expires during multibuffer data acquisition. A write operation to these bits with any bit set to a one causes the flag to be cleared.

Demand FIFO Register

The Demand FIFO Register (DFR) is a read-only register located at an offset of 28 Hex from the selected base address. This register is loaded with demand message data received from the highway. When a slave chassis requires service, it may generate an asynchronous demand message on the highway. When the 2962 receives these demands, they are placed in a 2K X 16 FIFO. Optionally, the 2962 may assert a PCI interrupt when the 2962 receives a demand message. The FIFO data contains the node address of the chassis that generated the demand message along with an 8-bit identifier. Please refer to the individual slave module manuals for details on the sources of the identifiers.

As long as there is at least one demand message contained in the Demand FIFO Register the DEMAND PENDING (DMD PND) bit in the CSR is set to a one. If the DFR is full (2048 demands) and an additional demand message is received from the highway, the DEMAND OVERFLOW (DMD OFL) bit in the CSR is set to a one. The Demand FIFO Register and the DEMAND OVERFLOW bit are cleared by power-up, a write to the Reset Interface address, and by a write to the Reset Demand FIFO address.

The following diagram shows the bit pattern for the Demand FIFO Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	DID 7	DID 6	DID 5	DID 4	DID 3	DID 2	DID 1	DID 0

<31:15> These bits are not used and are read as zeros.

<14:8> NODE ADDRESS64 through 1 are read-only bits which indicates the chassis' node address that generated the demand message.

<7:0> DEMAND IDENTIFIER7 through 0 are read-only bits which indicate the chassis' internal demand source.

Reset Interface

The Reset Interface (RSTIFC) is a write-only address location located at an offset of 2C Hex from the selected base address. A write operation to this address with any data pattern causes the 2962 to be reset to an initial state.

Reset Demand FIFO Register

The Reset Demand FIFO Register is a write-only address location located at an offset of 30 Hex from the selected base address. A write operation to this address with any data pattern causes the Demand FIFO Register and the DEMAND OVERFLOW bit to be cleared.

PROGRAMMED TRANSFERS

Programmed transfers are used to setup and initiate highway operations. Once these operations are started, data transfer to/from the Data FIFO Registers may occur under programmed transfer or by Direct Memory Access (DMA). DMA transfers have a significant speed advantage over programmed transfers. The DMA transfers to the 2962 occur without any software overhead once the transfer is setup.

When using programmed transfers, the software must examine the FIFO flags in order to determine whether to transfer data to/from the Data FIFO Resister (FIFO). These flags are located in the Control/Status Register of the Highway Operational Registers and the Bus Master Control/Status Register of the PCI Interface Registers. Before a write operation to the 2962 FIFOs may occur, the software must read the Control/Status Register (CSR) to determine if there is room in the FIFO for another piece of write data. If either the TRANSMIT FIFO FULL bit in the Control/Status Register is set or the OUTBOUND FIFO FULL bit in the Bus Master Control/Status Register is set, the software must suspend the write operation until both bits are negated. When read commands are executed, the software must first check the INBOUND FIFO EMPTY bit in the Bus Master Control/Status Register before the data may be retrieved. If this bit is set, the software must loop on reading these registers until the bit is asserted. These procedures must be followed when executing programmed transfer operations to the FIFO while list processing is in progress.

The following is a basic example of how to execute a programmed transfer list operation. For this example, the direction of data transfer is from the 2960 to a highway slave device.

1.) Set the Command Memory Address Register to zero.
2.) Load the Command Memory Data Register with the instructions required to execute the write operation. Make sure that the last element in the list is a HALT instruction.
3.) Set the Command Memory Address Register to zero.
4.) Set the GO bit in the Control/Status Register.
5.) Read the Control/Status Register and loop on this step until the TRANSMIT FIFO FULL bit is false.
6.) Read the Bus Master Control/Status Register and loop on this step until the OUTBOUND FIFO FULL bit is false.
7.) Write the Data FIFO Register with the data to be transmitted. Return to step 5 until all the transmit data words have been loaded into the 2962.
* 8.) Wait for the DONE bit in the Control/Status Register to be asserted, indicating that the operation is complete.
9.) Read the Control/Status Register and Error/Status Register to check for any errors.

The following example shows the steps required to execute a programmed transfer operation that transfers data from a highway slave device to the 2960.

1.) Set the Command Memory Address Register to zero.
2.) Load the Command Memory Data Register with the instructions required to execute the write operation. Make sure that the last element in the list is a HALT instruction.
3.) Set the Command Memory Address Register to zero.
4.) Set the GO bit in the Control/Status Register.
5.) Loop on reading the Control/Status Register until the Bus Master Control/Status Register until the INBOUND FIFO EMPTY bit is set.
6.) Read the data from the Data FIFO Register and return to step 5 until all data words have been read.
* 7.) Wait for the DONE bit in the Control/Status Register to be asserted indicating that the operation is complete.
8.) Read the Control/Status Register and the Error/Status Register to check for any errors.

* When using the 2962 with the Done Interrupt enabled, the steps that include waiting for DONE may be removed since the assertion of the DONE bit generates an interrupt.

DMA TRANSFERS

Direct Memory Access (DMA) transfers provide the most efficient mechanism of transferring data to/from the 2962 during list processing operations. Minimal programming is required to setup the DMA mechanism.

Before a DMA operation begins, the 2962 must have the Memory Address loaded with the initial host memory address to access during the operation. After the 2962 accesses the specified location, the memory address is incremented to the next longword address. Note that the address specification must be longword aligned. As the DMA operations progresses, the Memory Address is incremented until the DMA operation is complete.

The maximum number of transfers that the 2962 is to executed must be loaded in the Total Transfer Count Register prior to enabling DMA. This register is loaded with the two's complement of the number of transfers to occur during the DMA operation. This value must take into account all data transfer instructions in the list, excluding the Single Inline Write operation. As each data word is transferred to/for host memory, the transfer count is incremented. When the count is incremented to zero, the DMA operation is complete.

The RELOAD ENABLE bit in the Control/Status Register is used to establish a circular buffer in host memory for repetitive operations. When the reload is enabled, the Total Transfer Count Register and the Memory Address Register are reloaded with the initial data after the Total Transfer Count expires. The Memory Address and Total Transfer Count Registers may also be loaded by the list processor by inserting the appropriate instructions in the list. The DMA direction may also be changed by list instructions.

COMMAND MEMORY INSTRUCTION FORMATS

The 2962 contains a 32K x 32 word memory used to hold the list processing instructions to be executed by the hardware list processor or the DSP. When list processing is initiated, the hardware list processor examines the header instruction of the first list instruction. If the header indicates that the instruction is a data transfer instruction to a CAMAC or VXI/VME chassis, the hardware processor forms the necessary command to transmit on the highway. After the highway transaction is complete, the Command Memory Address is incremented and the next instruction interpreted.

If the hardware list processor encounters a "special" instruction, one that does not require a highway operation, the DSP is enabled. The DSP then executes the "special" instruction and continues processing until a HALT instruction is found or another data transfer operation is requested.

The lower 16-bits of the first longword of a command instruction specifies the type of the instruction. This 16-bit word is referred to as the instruction header. The following diagram shows the format of the instruction header.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CM 1	CM 0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	TM 2	TM 1	AM 2	AM 1	WS 2	WS 1	AD

Bits 15 and 14 of the instruction header specify the type of instruction as follows:

CM1	CM0	Instruction Type
0	0	CAMAC Instruction
0	1	VXI/VME Instruction
1	0	Special Instruction
1	1	Reserved

If the CM1 bit is a zero, indicating that highway data transfers are to occur, bits 13 through 7 specify the node address at which the addressed command is directed. For special instructions, these bits may take on other definitions. The bits 13 through 7 for data transfer instructions allow a node address value from zero to 127. Even though node address 0 and 127 are valid, they are reserved for future expansion.

The definitions of the remaining bits in the instruction header vary depending on the type of command. The next two sections fully define bits 6 through 0 of the instruction header.

Subsequent words in a command instruction are dependant on the command type. For example, a CAMAC header is followed by the Station Number, Function Code, and Subaddress whereas VXI/VME headers are followed by the 32-bit VME address.

The next two sections of this manual describe the various CAMAC and VXI/VME instructions.

CAMAC Instructions

For all CAMAC instructions, the instruction header has bits 15 and 14 set to zeros. Bits 13 through 7 are used to specify the node address of the CAMAC chassis to access during the operation. Other bits in this word define the Transfer Mode, Access Mode, and Data Word Size.

The following diagram shows the instruction header for CAMAC instructions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	TM 2	TM 1	AM 2	AM 1	WS 2	WS 1	AD

Bits 15 and 14 of the CAMAC instruction header must be set to zeros.

Bits 13 through 7 are used to specify the node address of the CAMAC chassis to access.

Bits 6 and 5 are the Transfer Mode bits and specify the CAMAC transfer protocol as follows:

TM2	TM1	Transfer Mode
0	0	Single Operation
0	1	Block Transfer Operation
1	0	Single Inline Write Operation
1	1	Reserved

The Single Operation Transfer Mode simply transfers one data word to/from the CAMAC chassis for the specified CAMAC command. These operations may include write, read and control operations.

Block Transfer Operations move blocks of data to/from a CAMAC chassis for each block instruction. The number of data words to transfer during Block Transfer operations are found in additional words accompanying this instruction. These operations may include either CAMAC write or read operations.

Single Inline Write Operations are single transfer CAMAC write operations that have the CAMAC write data embedded in the list. These commands are useful for initializing modules and also allow CAMAC write operations to occur in a read command list.

The Access Mode bits, AM2 and AM1, specify the access method to be used during the requested transfer. The Access Modes provided are as follows.

AM2	AM1	Access Mode
0	0	Q-Stop Mode
0	1	Q-Ignore Mode
1	0	Q-Repeat Mode
1	1	Q-Scan Mode

The Access Modes for CAMAC provide a mechanism for controlling the data transfer based on the CAMAC Q-response received after every Dataway cycle. These modes include stopping when a Q=0 response is found, repeating a CAMAC command until a Q=1 response is found, or scanning through a CAMAC chassis. Please refer to the CAMAC Access Modes section of this manual for additional information.

The Word Size bits, WS2 and WS1, are used to specify the size of the CAMAC data word accessed in the CAMAC chassis. The following chart shows the available CAMAC data word size selections.

WS2	WS1	Data Word Size
0	0	32-Bits
0	1	24-Bits
1	0	16-Bits
1	1	8-Bits

Even though 32-bit transfers are not supported by CAMAC, this data word size was included for compatibility with VXI/VME data word sizes. If 32-bit data word sizes are selected, they are treated as 24-bit transfers.

The last bit in the instruction header, ABORT DISABLE, is used to enable or disable the termination of an operation when an X-response of zero occurs. Setting this bit to a one enables the termination due to a X=0 response from a CAMAC module and a zero enables the X=0 termination.

CAMAC NAF Word

The second 16-bit word for a CAMAC instruction contains the CAMAC Station Number (N), Subaddress (A), and the Function Code (F). This second 16-bit word is the high 16-bits of the first 32-bit Command Memory Data word. The following diagram shows the format of the second instruction word containing the CAMAC NAF specification.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

Bits 31 and 30 are not used and must be set to zero.

The Station Number 16 through 1 bits are used to specify the CAMAC Station Number to be used for the addressed operation. This allows for a CAMAC Station Number specification in the range of 0 through 31. Valid CAMAC Station Numbers that specify actual slots within the chassis are 1 through 23. Station Number 30 is a pseudo-address and is used to access the internal registers of the 3972. Station Numbers 24 through 29 and 0 are reserved. Please refer to the 3972 CAMAC Crate Controller for additional information on internal controller registers.

The Subaddress 8 through 1 bits are used to specify the CAMAC Subaddress to be accessed during the addressed CAMAC operation. Valid Subaddresses range from 0 to 15.

The Function Code 16 through 1 bits are used to specify the CAMAC Function Code to be used during the addressed CAMAC operation. The binary combination of the F16 and F8 bits determine the type of operation as follows.

F16	F8	Operation
0	0	CAMAC Read
0	1	CAMAC Control *
1	0	CAMAC Write
1	1	CAMAC Control *

* CAMAC Control operations are dataless operations. A Dataway cycle is executed for these commands but no data is transferred.

CAMAC Single Transfer Instructions

The Header Word and CAMAC NAF specification are common for all CAMAC instructions. This information occupies an entire 32-bit Command Memory Data word. For CAMAC Single Operations, this is the only data required. For each Single Transfer instruction encountered in the list, only one data word is transferred. The direction of the transfer is based on the CAMAC Function Code specified for the command. This instruction format may also be used to execute CAMAC control operations. To transfer multiple data words to/from a CAMAC chassis with one instruction, the CAMAC Block Transfer instruction must be used.

The following diagram shows the composite format for the CAMAC Single Operation instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	0	0	AM2	AM1	WS2	WS1	AD

CAMAC Block Transfer Instructions

CAMAC Block Transfer instructions allow multiple data words to be transferred to/from a CAMAC chassis with one instruction. This provides an efficient method for transferring a block of data to/from a particular CAMAC NAF.

Associated with each Block Transfer instruction is a Transfer Count. The Transfer Count, which is 32-bits in length, is the two's complement of the maximum number of CAMAC words to transfer during the block operation. This transfer count specifies the number of data words to transfer, regardless of the CAMAC Data Word Size.

When the list processor finds a Block Transfer instruction in the Command Memory, it loads the List Transfer Count Register on the 2962 with the Transfer Count data found in the list. The List Transfer Count Register is then incremented as each data word is transferred to/from the CAMAC chassis. The Block Transfer operation continues until the List Transfer Count is exhausted or an error occurs. If the transfer terminates prematurely, the List Transfer Count Register may then be read to determine the number of data words remaining to transfer.

The format of the CAMAC Block Transfer instruction is shown in the following diagram.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	0	1	AM2	AM1	WS2	WS1	AD

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCR 31	TCR 30	TCR 29	TCR 28	TCR 27	TCR 26	TCR 25	TCR 24	TCR 23	TCR 22	TCR 21	TCR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

CAMAC Single Inline Write Instruction

The Single Inline Write instruction allows a predetermined data word to be placed in the list and written to the specified NAF. Most often, this type of instruction is used for module initialization or as a mechanism to execute a CAMAC write operation in a read list.

The format of the CAMAC Single Inline Write instruction is shown in the following diagram.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	1	0	AM2	AM1	WS2	WS1	AD

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	W23	W22	W21	W20	W19	W18	W17	W16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0

If it is necessary to embed a CAMAC control operation in the list, the Single Inline Write format may be used. Since CAMAC control operations are dataless, the 2nd Word may be filled with any data pattern. Even though the data portion is not used, it must still be included.

VXI/VME Instructions

For all VXI/VME instructions, the instruction header has bits 15 set to a zero and bit14 set to a one. Bits 13 through 7 are used to specify the node address of the VXI/VME chassis to access during the operation. Other bits in this word define the Transfer Mode, Access Mode, and Data Word Size. The following diagram shows the instruction header for VXI/VME instructions.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	TM2	TM1	AM2	AM1	WS2	WS1	AD

Bits 15 must be set to a zero and bit 14 to a one.

Bits 13 through 7 are used to specify the node address of the VXI/VME chassis to access.

Bits 6 and 5 are the Transfer Mode bits and specify the VXI/VME transfer protocol as follows:

TM2	TM1	Transfer Mode
0	0	Single Operation
0	1	Block Transfer Operation
1	0	Single Inline Write Operation
1	1	Reserved

The Single Operation Transfer Mode simply transfers one data word to/from the VXI/VME chassis for the specified VXI/VME command. These operations may include write or read operations.

Block Transfer Operations move blocks of data to/from a VXI/VME chassis for each block instruction. The number of data words to transfer during Block Transfer operations are found in additional words accompanying this instruction. These operations may include either VXI/VME write or read operations.

Single Inline Write Operations are single transfer VXI/VME write operations that have the write data embedded in the list. These commands are useful for initializing modules and also allow VXI/VME write operations to occur in a read command list.

The Access Mode bits, AM2 and AM1, specify the access method to be used during the requested transfer. This mode concerns the addressing of the VXI/VME chassis. After the initial VXI/VME transfer is executed during block transfers, the address may be either incremented or left the same for subsequent transfers of the block. The Access Modes provided are as follows.

AM2	AM1	Access Mode
0	0	Increment Address
0	1	Reserved
1	0	Address Unchanged
1	1	Reserved

The Word Size bits, WS2 and WS1, are used to specify the size of the VXI/VME data word accessed in the addressed chassis. The following chart shows the available VXI/VME data word size selections.

WS2	WS1	Data Word Size
0	0	32-Bits
0	1	Reserved
1	0	16-Bits
1	1	8-Bits

The last bit in the instruction header, ABORT DISABLE, is used to enable or disable the termination of an operation when an a VXI Timeout is encountered. Setting this bit to a one allows an operation to run to completion without regard to the bus timeouts. Setting this bit to a zero causes an operation to terminate when a bus error occurs.

VXI/VME Address

The second 16-bit word for VXI/VME instructions contains the VME Address Modifier, a bit indicating the direction of the transfer (write or read), and a bit that is set to execute operations within the chassis controller. This second 16-bit word is the high 16-bits of the first 32-bit Command Memory Data word. The following diagram shows the second instruction word for VXI/VME instructions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT	DIR	0	0	0	0	0	0	0	0	AMD 5	AMD 4	AMD 3	AMD 2	AMD 1	AMD 0

The INTERNAL bit, bit 31, is used to indicate whether the addressed command is to be executed internal to the chassis controller or external. Setting this bit to a one specifies that the operation is executed internal to the chassis controller. For operations to occur on the VXI/VME backplane, this bit must be set to a zero.

The DIRECTION bit, bit 30, is used to define the direction of the transfer. When DIRECTION is set to zero, the direction of the transfer is from the 2962 to the VXI/VME chassis controller (write operations). This bit is set to a one for transferring data from the addressed VXI/VME chassis to the 2962 (read operations).

Bits 29 through 22 are not used and must be set to zeros.

The ADDRESS MODIFIER bits, AMD5 through AMD0, are used to specify the VME address modifier that the addressed chassis controller is to use for the VXI/VME bus cycle. The following chart is a subset of the VME address modifiers.

Address Modifier Data (Hex)	Function
3F	Standard (A24) Supervisory Block Transfer
3E	Standard (A24) Supervisory Program Access
3D	Standard (A24) Supervisory Data Access
3B	Standard (A24) Nonprivleged Block Transfer
3A	Standard (A24) Nonprivleged Program Access
39	Standard (A24) Nonprivleged Data Access
2D	Short (A16) Supervisory Access
29	Short (A16) Nonprivleged Access
0F	Extended (A32) Supervisory Block Transfer
0E	Extended (A32) Supervisory Program Access
0D	Extended (A32) Supervisory Data Access
0B	Extended (A32) Nonprivleged Block Transfer
0A	Extended (A32) Nonprivleged Program Access
09	Extended (A32) Nonprivleged Data Access

The next longword (32-bits) of any VXI/VME instruction is the physical address. The following diagram shows the bit pattern for the 2nd longword of a VXI/VME instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

VXI/VME Single Transfer Instructions

The Header Word, Address Modifier, and Address specification are common for all VXI/VME instructions. This information occupies two 32-bit Command Memory Data words. For VXI/VME Single Operations, this is the only data required. For each Single Transfer instruction encountered in the list, only one data word is transferred. The direction of the transfer is controlled by the DIRECTION bit. To transfer multiple data words to/from a VXI/VME chassis with one instruction, the VXI/VME Block Transfer instruction must be used.

The following diagram shows the composite format for the VXI/VME Single Operation instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT	DIR	0	0	0	0	0	0	0	0	AMD 5	AMD 4	AMD 3	AMD 2	AMD 1	AMD 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	0	0	AM2	AM1	WS2	WS1	AD

VXI/VME Block Transfer Instructions

VXI/VME Block Transfer instructions allow multiple data words to be transferred to/from a VXI/VME chassis with one instruction. This provides an efficient method for transferring a block of data to/from a particular module(s).

Associated with each Block Transfer instruction is a Transfer Count. The Transfer Count, which is 32-bits is length, is the two's complement of the maximum number of VXI/VME words to transfer during the block operation. This transfer count specifies the number of data words to transfer, regardless of the Data Word Size.

When the list processor finds a Block Transfer instruction in the Command Memory, it loads the List Transfer Count Register on the 2962 with the Transfer Count data found in the list. The

List Transfer Count Register is then incremented as each data word is transferred to/from the VXI/VME chassis. The Block Transfer operation continues until the List Transfer Count is exhausted or an error occurs. If the transfer terminates prematurely, the List Transfer Count Register may then be read to determine the number of data words remaining to transfer.

The format of the VXI/VME Block Transfer instruction is shown in the following diagram.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT	DIR	0	0	0	0	0	0	0	0	AMD 5	AMD 4	AMD 3	AMD 2	AMD 1	AMD 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	0	1	AM2	AM1	WS2	WS1	AD

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

3rd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TCR 31	TCR 30	TCR 29	TCR 28	TCR 27	TCR 26	TCR 25	TCR 24	TCR 23	TCR 22	TCR 21	TCR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

VXI/VME Single Inline Write Instruction

The Single Inline Write instruction allows a predetermined data word to be placed in the list and written to the specified VXI/VME address. Most often, this type of instruction is used for module initialization or as a mechanism to execute a VXI/VME write operation in a read list.

The format of the VXI/VME Single Inline Write instruction is shown in the following diagram.

Model 2962

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
INT	DIR	0	0	0	0	0	0	0	0	AMD 5	AMD 4	AMD 3	AMD 2	AMD 1	AMD 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	1	0	AM2	AM1	WS2	WS1	AD

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

3rd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
W31	W30	W29	W28	W27	W26	W25	W24	W23	W22	W21	W20	W19	W18	W17	W16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W0

Special Instructions

There are several special instructions implemented by the 2962. These instructions are not handled by the hardware list processor. When the hardware list processing mechanism encounters any special instructions, it sends a signal to the DSP. The DSP then examines the special instruction and executes the operation.

The only required special instruction that must be used is the HALT instruction. The HALT must be the last list instruction loaded following a valid list.

The following chart shows the special instructions implemented by the 2962. The hex data shown corresponds to the first 16-bit word of the special instruction (header).

Special Instruction (hex)	Function
8000	Halt
8040	Addressed Slave Trigger
8041	Broadcast Trigger
8043	Generate Host Interrupt
8070	Load Memory Address Register
8071	Load Transfer Count Register
8072	Set DMA Direction (Reads)
8073	Clear DMA Direction (Writes)
8100	Write Reply FIFO Short
8101	Write Reply FIFO Long

Halt Instruction

The Halt instruction has a value of 8000 hex and must be placed at the end of a list sequence. This special instruction informs the list processor to cease processing until retriggered. The following diagram shows the bit pattern for the Halt instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Addressed Slave Trigger Instruction

The Addressed Slave Trigger instruction has an opcode of 8040 hex and is used to initiate a trigger at an addressed slave. The data sent to the addressed slave is contained in the list instruction. The addressed slave takes the write data and strobes it into the Trigger Source Register. Refer to the individual slave device manuals for further information on the Trigger Source Register.

The following is the format of the Addressed Slave Trigger instruction.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

NODE ADDRESS 64 through 1 specify the node address to be accessed.

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TD15	TD14	TD13	TD12	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

TRIGGER DATA 15 through 0 is the data to be written into the addressed slave Trigger Source Register.

Broadcast Trigger Instruction

The Broadcast Trigger Instruction has an opcode of 8041 hex and is used to generate a Broadcast Trigger Message on the highway. This message is received by all slave devices on the highway. Once a slave device receives this message, it takes the data preloaded in the Broadcast Trigger Mask Register and applies the data to the Trigger Source Register. Any bit that is set to a one in the Broadcast Trigger Mask Register causes the corresponding local trigger to be asserted. Please refer to the individual slave devices operating manual for additional information.

The following shows the format of the Broadcast Trigger instruction.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Generate Host Interrupt Instruction

The Generate Host Interrupt Instruction has an opcode of 8043 hex and is used to generate an interrupt to the host computer. In order for this instruction to generate an interrupt to the PCI bus, it must be first enabled in the Interrupt Control/Status Register. If polling is desired, the LIST INTERRUPT bit in the Control/Status Register can be used.

The following shows the format for the Generate Host Interrupt instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1

Load Memory Address Register Instruction

The Load Memory Address Register instruction has an opcode of 8070 hex and is followed by a longword that contains the data to be loaded. This instruction loads the Memory Address

Register used for Direct Memory Accesses (DMA) through the list processor. When the DSP encounters this instruction, it makes sure that all the current DMA activity is complete before loading the data into the Memory Address Register.

The following shows the format for the Load Memory Address Register instruction.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR 31	MAR 30	MAR 29	MAR 28	MAR 27	MAR 26	MAR 25	MAR 24	MAR 23	MAR 22	MAR 21	MAR 20	MAR 19	MAR 18	MAR 17	MAR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MAR 15	MAR 14	MAR 13	MAR 12	MAR 11	MAR 10	MAR 9	MAR 8	MAR 7	MAR 6	MAR 5	MAR 4	MAR 3	MAR 2	0	0

MEMORY ADDRESS 31 through 2 is the data to be loaded into the Memory Address Register.

Load Total Transfer Count Register Instruction

The Load Total Transfer Count Register instruction has an opcode of 8071 hex and is followed by a longword that contains the data to be loaded. This instruction loads the Total Transfer Count Register used for Direct Memory Accesses (DMA) through the list processor. When the DSP encounters this instruction, it makes sure that all the current DMA activity is complete before loading the data into the Total Transfer Count Register.

The following shows the format for the Load Total Transfer Count Register instruction.

1st Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1

2nd Longword:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TTCR 31	TTCR 30	TTCR 29	TTCR 28	TTCR 27	TTCR 26	TTCR 25	TTCR 24	TTCR 23	TTCR 22	TTCR 21	TTCR 20	TTCR 19	TTCR 18	TTCR 17	TTCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TTCR 15	TTCR 14	TTCR 13	TTCR 12	TTCR 11	TTCR 10	TTCR 9	TTCR 8	TTCR 7	TTCR 6	TTCR 5	TTCR 4	TTCR 3	TTCR 2	TTCR 1	TTCR 0

TOTAL TRANSFER COUNT 31 through 0 is the data to be loaded into the Total Transfer Count Register.

Set DMA Direction Instruction

The Set DMA Direction instruction has an opcode of 8072 hex and is used to set the DMA DIRECTION in the Control/Status Register to a one. Setting this bit to a one sets the direction of DMA transfer from the 2962 to computer memory (reads). When the DSP encounters this instruction, it makes sure that all the current DMA activity is complete before setting the direction bit.

The following shows the format for the Set DMA Direction instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0

Clear DMA Direction Instruction

The Clear DMA Direction instruction has an opcode of 8073 hex and is used to clear the DMA DIRECTION in the Control/Status Register. Clearing this bit to a zero sets the direction of DMA transfer from the computer memory to the 2962 (writes). When the DSP encounters this instruction, it makes sure that all the current DMA activity is complete before clearing the direction bit.

The following shows the format for the Clear DMA Direction instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1

Write Reply FIFO Short Instruction

The Write Reply FIFO Short instruction has an opcode of 8100 hex and is used to write 16-bits of data to the Reply FIFO on the 2962. The second longword associated with this command contains the data to write to the FIFO. The Reply FIFO holds all the data received from the highway during read operations on the highway. If desired, the list processor may be instructed to insert a data pattern into the read data path. This can be used to tag data when a branch instruction is used or to realign a read data buffer to longwords. Since the 2962 forms 32-bit read data words before transferring the data to the output FIFO, it may be necessary to include a Write Reply FIFO Short instruction in a list to make sure longword alignment is maintained. For example, if a list operation resulted in an odd number of 16-bit words being transferred, the user must include a Write Reply FIFO Short instruction to ensure that the last 16-bit word is not "stuck" in the 2962.

The following diagram shows the format for the Write Reply FIFO Short instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RFD 15	RFD 14	RFD 13	RFD 12	RFD 11	RFD 10	RFD 9	RFD 8	RFD 7	RFD 6	RFD 5	RFD 4	RFD 3	RFD 2	RFD 1	RFD 0

Write Reply FIFO Long Instruction

The Write Reply FIFO Long instruction has an opcode of 8101 hex and is used to write 32-bits of data to the Reply FIFO on the 2962. The second longword associated with this command contains the data to write to the FIFO. The Reply FIFO holds all the data received from the highway during read operations on the highway. If desired, the list processor may be instructed to insert a data pattern into the read data path. This can be used to tag data when a branch instruction is used.

The following diagram shows the format for the Write Reply FIFO Long instruction.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFD 31	RFD 30	RFD 29	RFD 28	RFD 27	RFD 26	RFD 25	RFD 24	RFD 23	RFD 22	RFD 21	RFD 20	RFD 19	RFD 18	RFD 17	RFD 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RFD 15	RFD 14	RFD 13	RFD 12	RFD 11	RFD 10	RFD 9	RFD 8	RFD 7	RFD 6	RFD 5	RFD 4	RFD 3	RFD 2	RFD 1	RFD 0

CAMAC ACCESS MODES

There are four CAMAC Access Modes available for accessing a CAMAC chassis. These modes include Q-Ignore, Q-Stop, Q-Repeat and Q-Scan. When a CAMAC chassis is addressed, the two Access Mode bits, AM2 and AM1, are passed to the chassis controller. The Q-modes operations are actually performed in the chassis controller, not the highway driver.

The following chart shows the various Access Modes based on the binary combinations of the AM bits.

Access Mode 2	Access Mode 1	Access Mode
0	0	Q-Stop
0	1	Q-Ignore
1	0	Q-Repeat
1	1	Q-Scan

The following sections detail the four access modes.

CAMAC Q-Stop Access Mode

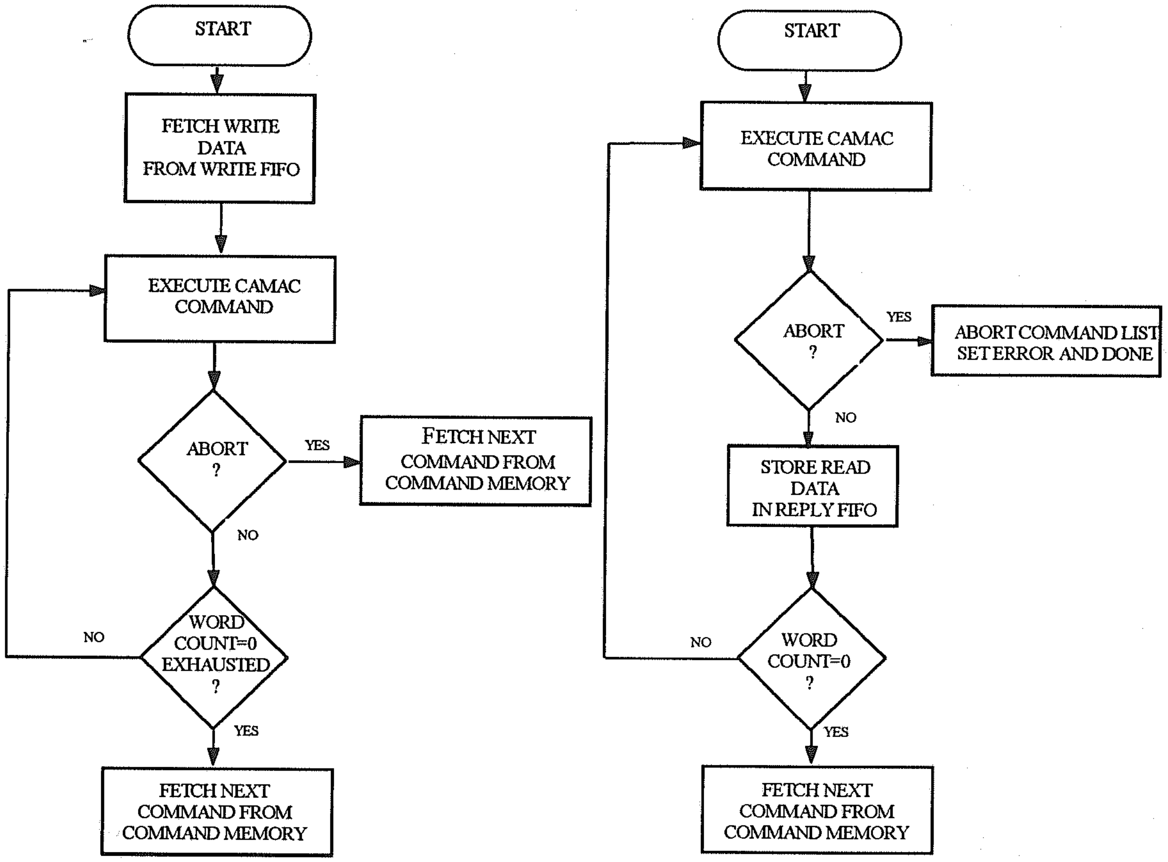
The CAMAC Q-Stop Access Mode is selected by setting both the access mode bits to zeros. During Q-Stop operations, the CAMAC command (NAF) specified is repeated until a CAMAC Q-response of zero is received or the transfer count is exhausted. This provides an efficient mechanism to transfer data to/from a CAMAC NAF without actually knowing the amount of room available within the module. Therefore, the transfer count specification is set large enough to write the entire buffer. If the entire buffer is not sent, due to a NO-Q condition, the transfer count registers on the 2962 and 3972 may be evaluated to determine the number of transfers that did not occur.

The transfer will also terminate if an error is encountered. The definition of an error for this mode is as follows:

$$\begin{aligned} \text{ERROR} = {} & \text{NO-Q} \\ & + \text{NO-X} * \overline{\text{AD}} \end{aligned}$$

The following is a simplified flow diagram showing the sequences the CAMAC Chassis Controller uses to execute Q-Stop write and read transfers.

Q-Stop/Q-Ignore Flow Diagram


START
FETCH WRITE DATA FROM WRITE FIFO
EXECUTE CAMAC COMMAND
ABORT ?
YES
FETCH NEXT COMMAND FROM COMMAND MEMORY
NO
WORD COUNT=0 EXHAUSTED ?
NO
YES
FETCH NEXT COMMAND FROM COMMAND MEMORY
START
EXECUTE CAMAC COMMAND
ABORT ?
YES
ABORT COMMAND LIST SET ERROR AND DONE
NO
STORE READ DATA IN REPLY FIFO
WORD COUNT=0 ?
NO
YES
FETCH NEXT COMMAND FROM COMMAND MEMORY

IGNORE - Q WRITE COMMANDS

IGNORE - Q READ COMMANDS

CAMAC Q-Ignore Access Mode

The CAMAC Q-Ignore Access Mode is selected by setting the AM2 bit to zero and the AM1 bit to a one. During Q-Ignore operations, the CAMAC command (NAF) specified is repeated for each data word until the transfer count is exhausted. This mode does not examine the CAMAC Q-response from the previous transfer to determine if the operation should be terminated. The transfer will terminate if an error is encountered during the operation. The definition of an error for this mode is as follows:

$$\text{ERROR} = \text{NO-X} * \overline{\text{AD}}$$

The previous flow diagram shows the sequences the CAMAC Chassis Controller uses for executing Q-Ignore write and read transfers.

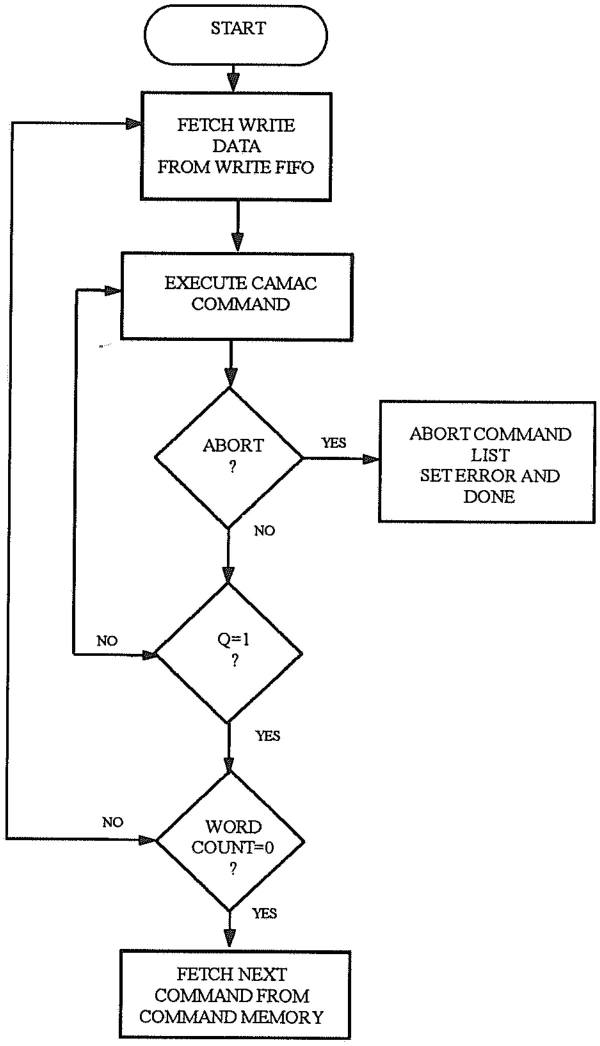
CAMAC Q-Repeat Access Mode

The CAMAC Q-Repeat Access Mode is selected by setting the AM2 bit to a one and the AM1 bit to a zero. During Q-Repeat operations, the CAMAC command (NAF) specified is repeated for each data word until a CAMAC Q-response of one is returned. A Q-response of one either causes new write data to be fetched or read data to be stored. The command is repeated for each data word until the transfer count is exhausted. If a Q-response of one is not obtained within the 200 millisecond timeout period, the transfer terminates with a Q-Repeat Timeout. The following describes an error when executing commands in the Q-repeat mode.

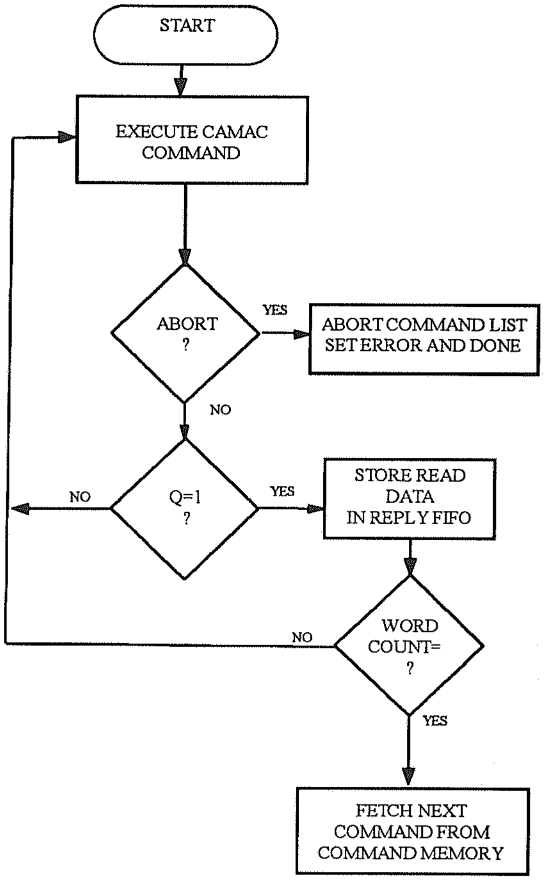
$$\begin{aligned}\text{ERROR} = {} & \text{Q-REPEAT TIMEOUT} \\ & + \text{NO-X} * \overline{\text{AD}}\end{aligned}$$

The following simplified flow chart shows the sequences the CAMAC Chassis Controller used for executing Q-Repeat write and read transfers.

Q-Repeat Write and Read Transfers


START
FETCH WRITE DATA FROM WRITE FIFO
EXECUTE CAMAC COMMAND
ABORT ?
YES
ABORT COMMAND LIST SET ERROR AND DONE
NO
Q=1 ?
NO
YES
WORD COUNT=0 ?
NO
YES
FETCH NEXT COMMAND FROM COMMAND MEMORY

Q-REPEAT WRITE COMMANDS


START
EXECUTE CAMAC COMMAND
ABORT ?
YES
ABORT COMMAND LIST SET ERROR AND DONE
NO
Q=1 ?
NO
YES
STORE READ DATA IN REPLY FIFO
WORD COUNT= ?
NO
YES
FETCH NEXT COMMAND FROM COMMAND MEMORY

Q -REPEAT READ COMMANDS

CAMAC Q-Scan Access Mode

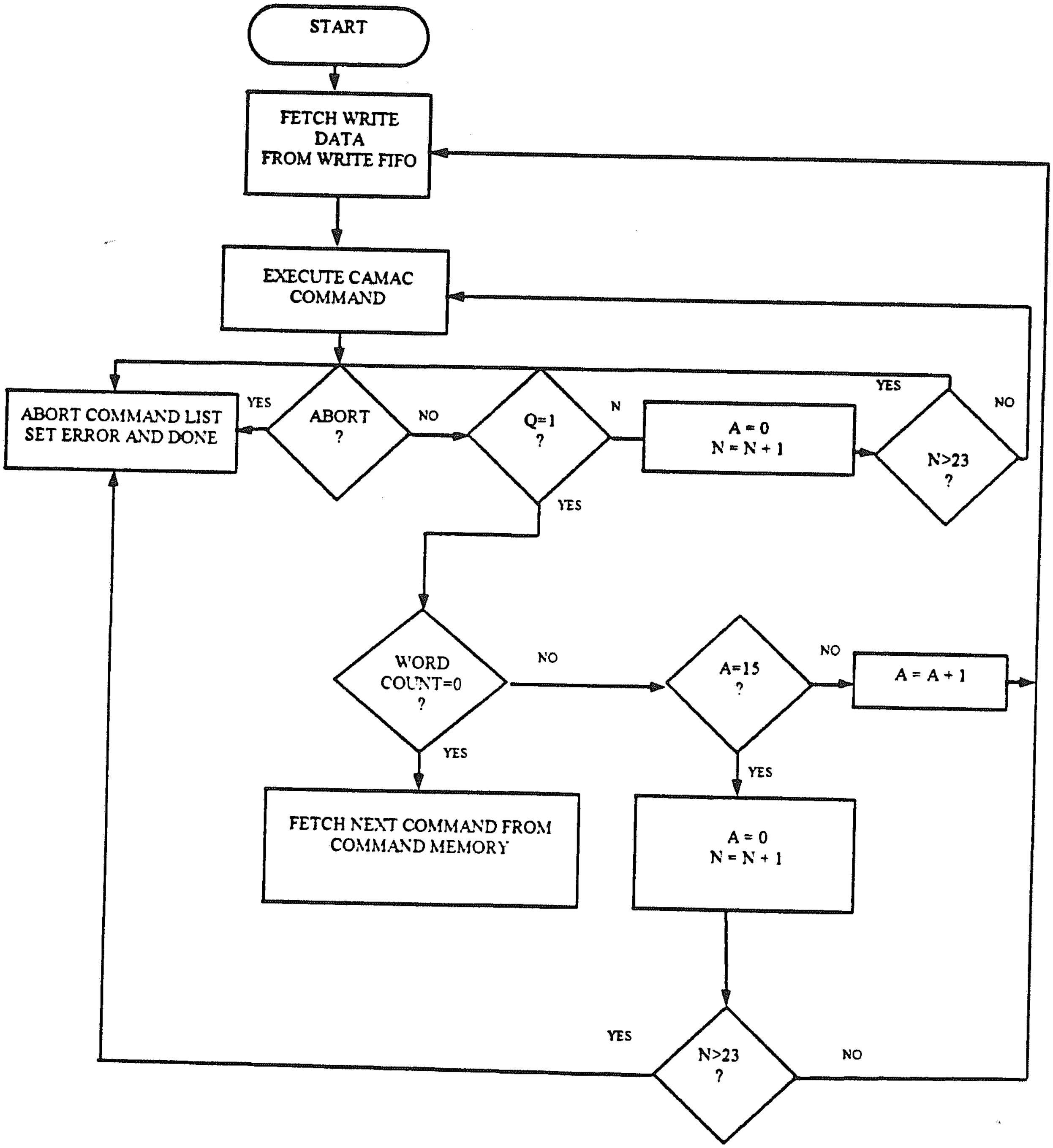
The CAMAC Q-Scan Access Mode is selected by setting the AM2 and AM1 bits to a one. During Q-Scan operations, the CAMAC Chassis Controller uses the Q-response from the previously executed CAMAC command to determine the Station Number (N) and Subaddress (A) for the next operation. A Q-response of zero indicates that the last valid Subaddress of the current Station Number has been accessed. The CAMAC controller responds to the Q=0 response by incrementing the Station Number and resetting the Subaddress to zero. A Q=1 response indicates that the last CAMAC command was executed to a valid address. The controller responds to the Q=1 by either storing the read data or retrieving the next write data word. After the Q=1 is received, the controller updates the CAMAC address as follows: the Subaddress is incremented or, if the Subaddress was 15, it is reset to zero and the Station Number is incremented.

If, due to a programming error, the Station Number is incremented beyond Station Number 23, the transfer is terminated and an error condition indicated. The following equation describes an error during Q-Scan operations.

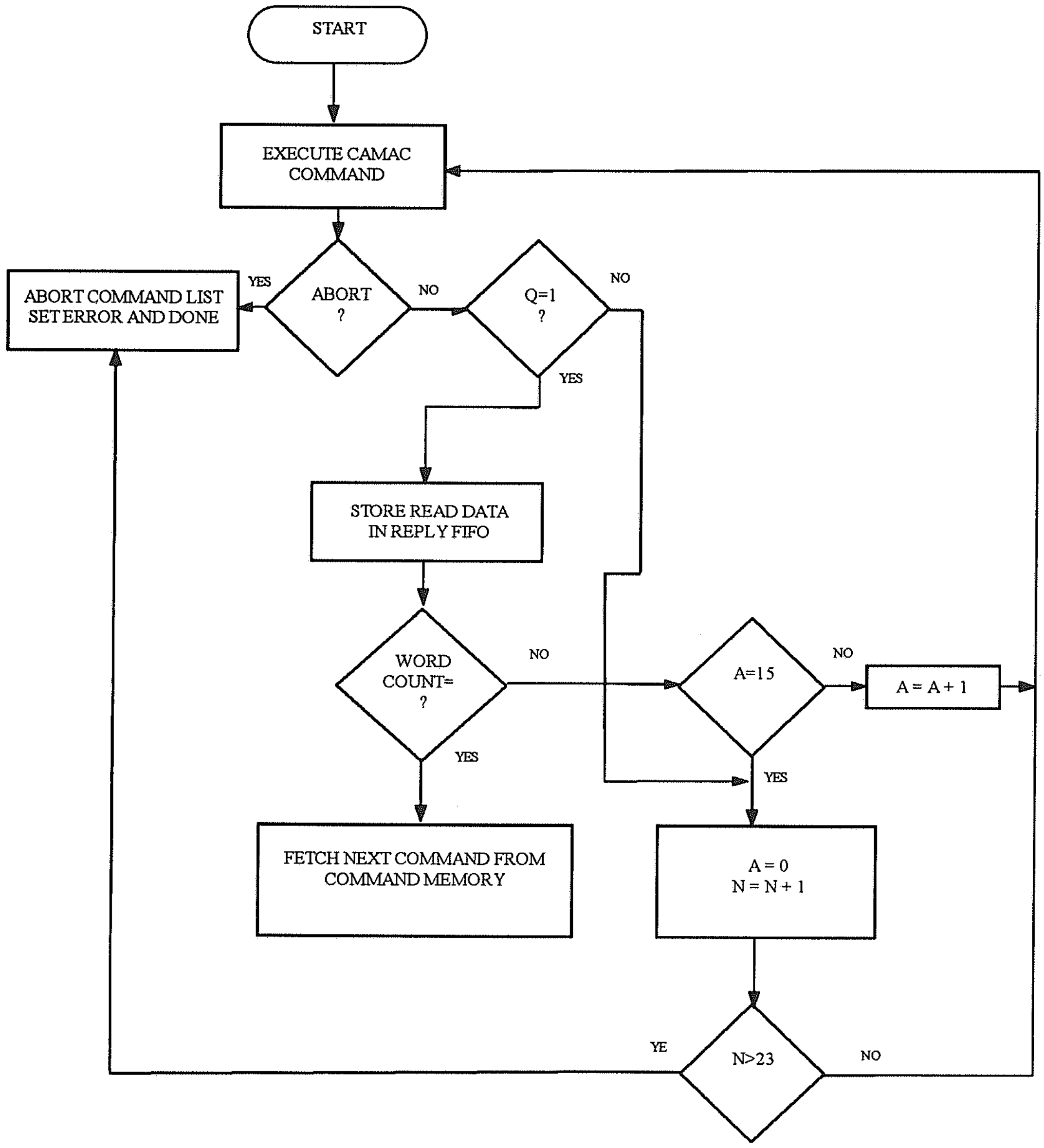
$$\text{ERROR} = N > 23$$

The following diagrams show the basic flow for Q-Scan write and read operations.

Q-Scan Write Operations



Q-Scan Read Operations



Q-SCAN READ OPERATIONS

CAMAC LIST PROCESSING EXAMPLE

As an example, assume it is desired to read a two channel analog-to-digital converter (ADC) located in chassis number 3 slot 6. 1024 samples of the analog data are to be taken from each channel. The ADC module is accessed by the following commands:

F(2) A(0) - Reads the digitized data. Q-response of 1 indicates valid data.
F(17) A(0) - Selects the channel to read.

Data = 1 selects channel 1.
Data = 2 selects channel 2.

F(24) A(0) - Disables ADC conversions.
F(26) A(0) - Enables ADC conversions.

For this application example, an F(17) A(0) with data = 1 is first executed to select the desired channel. An F(26) A(0) is then executed to enable conversions. A Standard CAMAC Block Transfer operation is executed in the Q-Repeat mode to read the 1024 converted samples. After the samples are read, an F(24) A(0) command is executed to disable the conversions. These steps are then repeated for channel number 2.

For this example, the following commands are executed :

Single Inline CAMAC Write	Node(3) N(6) F(17) A(0) DATA(1)
Single Inline CAMAC Write	Node(3) N(6) F(26) A(0) DATA (not required for Control)
CAMAC Block Transfer	Node(3) N(6) F(2) A(0) WORD COUNT(1024)
Single Inline CAMAC Write	Node(3) N(6) F(24) A(0) DATA (not required for Control)
Single Inline CAMAC Write	Node(3) N(6) F(17) A(0) DATA(2)
Single Inline CAMAC Write	Node(3) N(6) F(26) A(0) DATA (not required for Control)
CAMAC Block Transfer	Node(3) N(6) F(2) A(0) WORD COUNT(1024)
Single Inline CAMAC Write	Node(3) N(6) F(24) A(0) DATA(not required for Control)

After the list is formed with the above parameters, the actual list is as follows:

Hex Instruction Data	List Entry Contents
0C1101C2	N(6) A(0) F(17) Single Inline Write Node (3) Q-Ignore 24-Bit
00000001	DATA(1)
0C1A01C2	N(6) A(0) F(26) Single Inline Write Node (3) Q-Ignore 24-Bit
00000000	DATA (0)
0C0201B2	N(6) A(0) F(2) Block Transfer Node(3) Q-Repeat 24-Bit
FFFFFC00	Transfer Count (-1024)
0C1801C2	N(6) A(0) F(24) Single Inline Write Node (3) Q-Ignore 24-Bit
00000000	DATA (0)
0C1101C2	N(6) A(0) F(17) Single Inline Write Node(3) Q-Ignore 24-Bit
00000002	DATA (2)
0C1A01C2	N(6) A(0) F(26) Single Inline Write Node(3) Q-Ignore 24-Bit
00000000	DATA (0)
0C0201B2	N(6) A(0) F(2) Block Transfer Node(3) Q-Repeat 24-Bit
FFFFFC00	Transfer Count (-1024)
0C1801C2	N(6) A(0) F(24) Single Inline Write Node(3) Q-Ignore 24-Bit
00000000	DATA (0)
00008000	HALT

VXI LIST PROCESSING EXAMPLE

As an example, assume it is desired to setup, enable, and read a block of 20000 32-bits words from a VXI module. For this example, the following parameters exist:

Node Address = 16
Logical Address = 2
A32 Device
Readout address for data is at base address for A32 space

For this example, two Single VXI Inline Write operations are executed to setup the modules Offset Register in A16 address space and then enable the module by setting the A24/A32 enable bit in the Status/Control Register. The module will be set to occupy address 30000000 in A32 address space. After setup, a VXI Block Transfer instruction is executed to read the data.

With a Logical Address of 2, the modules' Status/Control Register is located at C084 hex and the Offset Register is at address C086 hex. Both of these registers are located in A16 address space and may be accessed with an address modifier of 2D hex.

For this example, the following instructions are executed.

Single Inline VXIWrite	Address(C086)	Address Modifier (2D)	Data(3000)
Single Inline VXIWrite	Address (C084)	Address Modifier (2D)	Data (8000)
Block VXI Read	Address (30000000)	Address Modifier (D)	Transfer Count (-20000)

After the list elements are formed, the actual list is as follows:

Hex Instruction Data	List Entry Contents
002D4840	Address Modifier (2D) VXI Single Inline Write 32-Bit
0000C086	Address (C086)
00003000	DATA(00003000)
002D4840	Address Modifier (2D) VXI Single Inline Write 32-Bit
0000C084	Address (0000C084)
00008000	DATA(00008000)
400D4820	Read, Address Modifier (D) VXI Block Transfer Increment Address 32-Bit
30000000	Address (30000000)
FFFFB1E0	Transfer Count (-20000)
00008000	HALT

INTERRUPTS

The 2962 may generate interrupts to the PCI bus from any of five sources. These sources include the assertion of the DONE, the presence of a Demand Message in the Demand FIFO Register, the list processor encountering the Generate Host Interrupt instruction, the PCI interface chip, or by the Buffer Interval Counter overflowing during multibuffer read operations.

These sources are individually enabled in the Interrupt Control/Status Register. The level at which the 2962 interrupts the host computer is based on the computer architecture and the mapping of the 2962 PCI interrupt to the host computer bus interrupt. The 2962 interrupts on the PCI bus by asserting the INTA signal.

The DONE interrupt source is generated when a list processing operation is completed and the DONE, bit 7, in the Control/Status Register is set to a one. The DONE INTERRUPT ENABLE, bit 0, in the Interrupt Control/Status Register must be set to a one in order to generate an PCI interrupt.

If enabled, the receipt of a Demand Message from the highway can generate an PCI interrupt. The interrupt is enabled in the Interrupt Control/Status Register using the DEMAND INTERRUPT ENABLE bit, bit 2. When this interrupt source is generated, the entire contents of the Demand FIFO Register should be read in order to allow additional interrupts to occur.

The list processor may also generate an interrupt to the PCI bus. The Generate Host Interrupt instruction asserts the interrupt source and must be enabled using the LIST INTERRUPT ENABLE bit in the Interrupt Control/Status Register.

Another interrupt source from the 2962 is generated during multibuffer read operation. During multibuffer read operations, the Buffer Interval Counter is used to indicate when a segment of the read data buffer has been filled. When this occurs, an interrupt may be generated. This interrupt source is enabled using the MULTIBUFFER INTERRUPT ENABLE bit in the Interrupt Control/Status Register. Please refer to the Multibuffer Operations section of this manual for additional information.

The last interrupt source from the 2962 may be generated from the PCI interface chip. To enable this source, the PCI INTERRUPT ENABLE bit in the Interrupt/Control/Status Register must be set to a one. Refer to the PCI Interface Interrupt Control/Status Register section of this manual for additional information on the PCI interface chip interrupts.

Once an interrupt is asserted, it remains asserted until cleared by writing to the Interrupt Control/Status Register with the data that matches the interrupt sources to clear.

DEMANDS

Demands are asynchronous messages received from devices on the interconnect highway. These messages provide a means of informing the 2962 that the device sourcing the message requires attention. The Demand Message contains the chassis address of the node requesting service along with an 8-bit Demand Identification byte. For the definition of the Demand Identification bits, refer to the manual for the slave device.

After a Demand Message is received by the 2962, it is stored in a 2048 word FIFO. As long as there is at least one demand in the FIFO, the DEMAND PENDING bit in the Control/Status Register is set to a one. After all demand words are read from the FIFO, the bit is reset to a zero.

If the Demand FIFO is full and another Demand Message is received by the 2960, the message is lost and the DEMAND OVERFLOW bit in the Control/Status Register is set to a one. After the overflow occurs, the DEMAND FIFO OVERFLOW bit can be cleared by executing a write to the Demand FIFO Reset Register address.

MULTIBUFFER OPERATIONS

The 2962 may be configured to execute highway read operations automatically and notify the host computer when a buffer a data is available. When the host is reading data from one buffer segment, the 2962 may be filling another. This is referred to as multibuffering.

The highway operations can be executed automatically by enabling the on-board timer through the Timer Control Register. This register controls the frequency at which the list is executed. This rate is referred to as the 'tic' rate. After selecting the frequency in this register, the timer must be enabled.

When multibuffer operations are executed, the read data received from the highway is transferred to the host computer memory via Direct Memory Access (DMA). The DMA operation is initially set up through programmed I/O transfer to the 2962. This establishes the initial DMA address as well as the total number of PCI transfers to be executed before reloading the address and transfer count registers. The reloading of the memory address and transfer count registers is enabled with the RELOAD ENABLE bit in the Control/Status Register. When the reloading is enabled, the host computer memory is used as a circular buffer. When the entire DMA buffer has been filled, the 2962 reloads its memory address and transfer count registers.

Before the multibuffer operation is initiated, the Buffer Interval Counter must be loaded with the count indicating the number of PCI transfers that are to occur before setting a multibuffer flag. As an example, assume that the transfer count specification for the 2962 is 1000. This creates a circular buffer in the host memory of 1000 words. The buffer is to be split into four equal segments. Therefore, the Buffer Interval Counter (BIC) is loaded with 1000/4. Every time the BIC is exhausted, a multibuffer flag bit is set. The flag bits are incrementally set until the transfer count expires and the internal pointer is set to the first flag bit.

When the host sees a flag bit on, it reads out the corresponding segment of data from the buffer and clears the appropriate multibuffer flag by executing a write to the Multibuffer Flag Register. The data for this write must correspond with the flag to clear.

If a flag is set and readout of the buffer segment is not complete by the time the 2962 loops around to the buffer segment again, the FLAG OVERFLOW bit in the Multibuffer Control Register. This is typically caused by the memory buffer being readout too slow.

APPEND STATUS

The 2962 may be enabled to append a status byte onto the end of a highway read operation by enabling the APPEND STATUS bit in the Control/Status Register. Setting this bit to a one enables the feature.

After a read list operation is ended by the list processor encountering a HALT instruction, the APPEND STATUS bit is examined to see if an additional word of data is to be written into the highway read reply FIFO. If the bit is set to a one, the list processor reads a status word from internal registers and writes the data to the read reply FIFO. If append status is used, care must be taken to allocate the additional 32-bit data word in the read data block. The first 16-bit word contains the status and the second 16-bit word contains zero.

The following diagram shows the bit layout for the returned appended status word. The Error/Status Register section of this manual should be consulted for a detailed description of these bits.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	DMD PND	VXI TMO	QRPT TMO	N>23	0	RMT PERR	PERR	TMO	ADNR	NOX	NOQ	0

EXTERNAL CLOCK INPUT

If the clock rate selections on the 2962 do not meet an application requirement for timer initiated list processing, an external clock source may be connected to the 2962. This input is fed into the 2962 through the LEMO connector located on the rear panel. This input provided to the 2962 must be TTL compatible. The list is triggered by the high to low transition of the input, and must have a minimum pulse width of 300 nanoseconds.

To enable the external clock input, the Timer Control Register must have both the CLOCK SOURCE and TIMER ENABLE bits set to a one. Refer to the Timer Control Register section of this manual for additional information.

LEDs

Two LEDs are mounted on the 2962. One LED is used as an indication of highway synchronization and the other indicates when a list processing operation is in progress. As viewed from the 2962 front panel bracket, the left-most LED is illuminated when the highway is in sync. This is a red LED. The green LED is illuminated as long as the list processor is busy.

APPENDIX A - 2962 Composite Register Layout

Control/Status Register Offset 00 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ERR CD3	ERR CD2	ERR CD1	ERR CD0	VXI TMO	QTMO	N>23	ILLG CMD	RMT PER	NO SYNC	0	PAR ERR	TMO	ADNR	NOX	NOQ

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	LIST INT	DMD OFLO	DMD PND	0	XMT FULL	RCV DAV	DONE	0	APND STAT	RLD ENA	DMA DIR	DMA ENA	SUSP	GO

Interrupt Control/Status Register Offset 04 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	PCI INT	MBM INT	DMD INT	LIST INT	DONE INT	PCI IE	MBM IE	DMD IE	LIST IE	DONE IE

Timer Control Register Offset 08 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	CLK SRC	TMR ENA	TCR 23	TCR 22	TCR 21	TCR 20	TCR 19	TCR 18	TCR 17	TCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TCR 15	TCR 14	TCR 13	TCR 12	TCR 11	TCR 10	TCR 9	TCR 8	TCR 7	TCR 6	TCR 5	TCR 4	TCR 3	TCR 2	TCR 1	TCR 0

Command Memory Address Register Offset 0C hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LIST GO	CMA 14	CMA 13	CMA 12	CMA 11	CMA 10	CMA 9	CMA 8	CMA 7	CMA 6	CMA 5	CMA 4	CMA 3	CMA 2	CMA 1	CMA 0

Command Memory Data Register Offset 10 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CMD 31	CMD 30	CMD 29	CMD 28	CMD 27	CMD 26	CMD 25	CMD 24	CMD 23	CMD 22	CMD 21	CMD 20	CMD 19	CMD 18	CMD 17	CMD 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CMD 15	CMD 14	CMD 13	CMD 12	CMD 11	CMD 10	CMD 9	CMD 8	CMD 7	CMD 6	CMD 5	CMD 4	CMD 3	CMD 2	CMD 1	CMD 0

List Transfer Count Register Offset 14 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 31	LTC 30	LTC 29	LTC 28	LTC 27	LTC 26	LTC 25	LTC 24	LTC 23	LTC 22	LTC 21	LTC 20	LTC 19	LTC 18	LTC 17	LTC 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
LTC 15	LTC 14	LTC 13	LTC 12	LTC 11	LTC 10	LTC 9	LTC 8	LTC 7	LTC 6	LTC 5	LTC 4	LTC 3	LTC 2	LTC 1	LTC 0

Total Transfer Count Register Offset 18 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TTCR 31	TTCR 30	TTCR 29	TTCR 28	TTCR 27	TTCR 26	TTCR 25	TTCR 24	TTCR 23	TTCR 22	TTCR 21	TTCR 20	TTCR 19	TTCR 18	TTCR 17	TTCR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TTCR 15	TTCR 14	TTCR 13	TTCR 12	TTCR 11	TTCR 10	TTCR 9	TTCR 8	TTCR 7	TTCR 6	TTCR 5	TTCR 4	TTCR 3	TTCR 2	TTCR 1	TTCR 0

Memory Address Register Offset 1C hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MAR 31	MAR 30	MAR 29	MAR 28	MAR 27	MAR 26	MAR 25	MAR 24	MAR 23	MAR 22	MAR 21	MAR 20	MAR 19	MAR 18	MAR 17	MAR 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MAR 15	MAR 14	MAR 13	MAR 12	MAR 11	MAR 10	MAR 9	MAR 8	MAR 7	MAR 6	MAR 5	MAR 4	MAR 3	MAR 2	0	0

Buffer Interval Counter   Offset 20 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIC 31	BIC 30	BIC 29	BIC 28	BIC 27	BIC 26	BIC 25	BIC 24	BIC 23	BIC 22	BIC 21	BIC 20	BIC 19	BIC 18	BIC 17	BIC 16

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BIC 15	BIC 14	BIC 13	BIC 12	BIC 11	BIC 10	BIC 9	BIC 8	BIC 7	BIC 6	BIC 5	BIC 4	BIC 3	BIC 2	BIC 1	BIC 0

Multibuffer Control Register   Offset 24 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

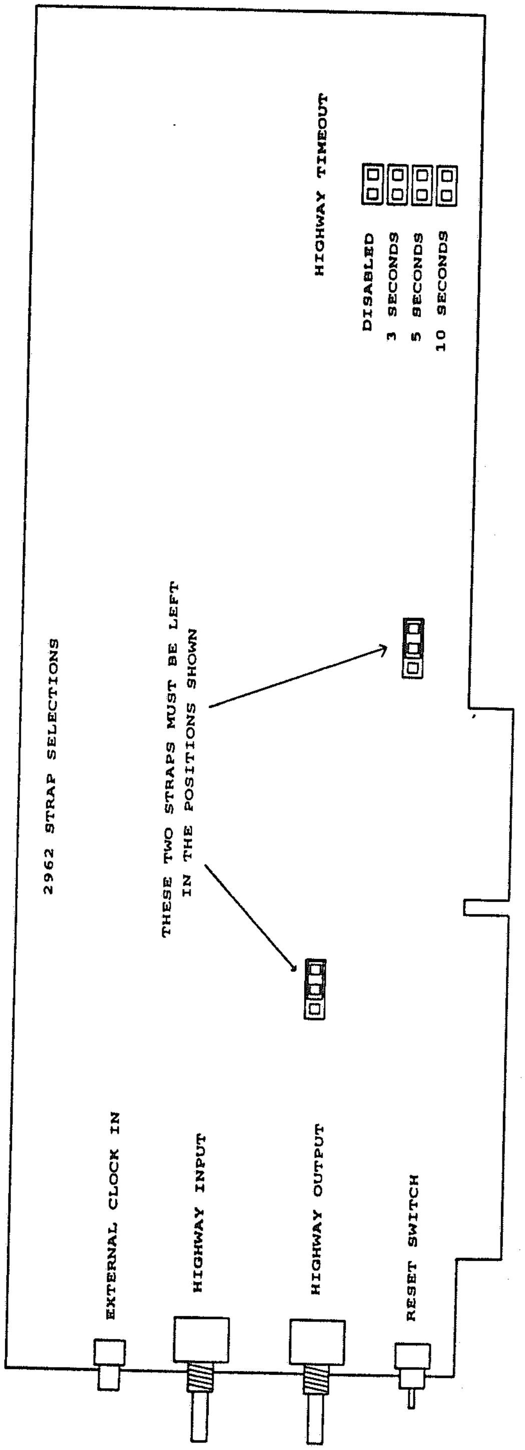
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	MBM ENA	FLG OFLO	FLG 3	FLG 2	FLG 1	FLG 0

Demand FIFO Register   Offset 28 hex

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	NDA 64	NDA 32	NDA 16	NDA 8	NDA 4	NDA 2	NDA 1	DID 7	DID 6	DID 5	DID 4	DID 3	DID 2	DID 1	DID 0

APPENDIX B - 2962 Strap Locations



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2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com