

Model 3063-A1A
16-bit Input Gate/Output Register
INSTRUCTION MANUAL

February, 1987

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Lockport, Illinois
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*****Special Option*****

Model 3063-S003

16-bit Input Gate/Output Register

Revised May, 1991

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*****Special Option*****

Model 3063-S003

The Model 3063-S003 is the same as the 3063-A1A except that the time constant of the input filter has been modified to be 1 ms.

The factory selected pulsed outputs for the 3063-S003 are:

Designation	Command	Output State
ON A	F(25)A(0)	LOW when pulsed
ON B	F(25)A(1)	LOW when pulsed
ON C	F(25)A(2)	LOW when pulsed
ON D	F(25)A(3)	LOW when pulsed

NPD:rem(WP)
Revised May 8, 1991

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DATA INPUT GATE

The data input gate contains 16 bits. These are read by an F(0)·A(0) command (Read lines R1 to R16). A read staticize register is provided to prevent data from changing early in the Dataway cycle. The signals are low-true at either HTL or TTL level. The input gate can be used without handshaking, if desired. Handshaking can be used to coordinate the data exchange from the peripheral device.

INPUT TRANSFER TIMING (HANDSHAKE SIGNALS USED)

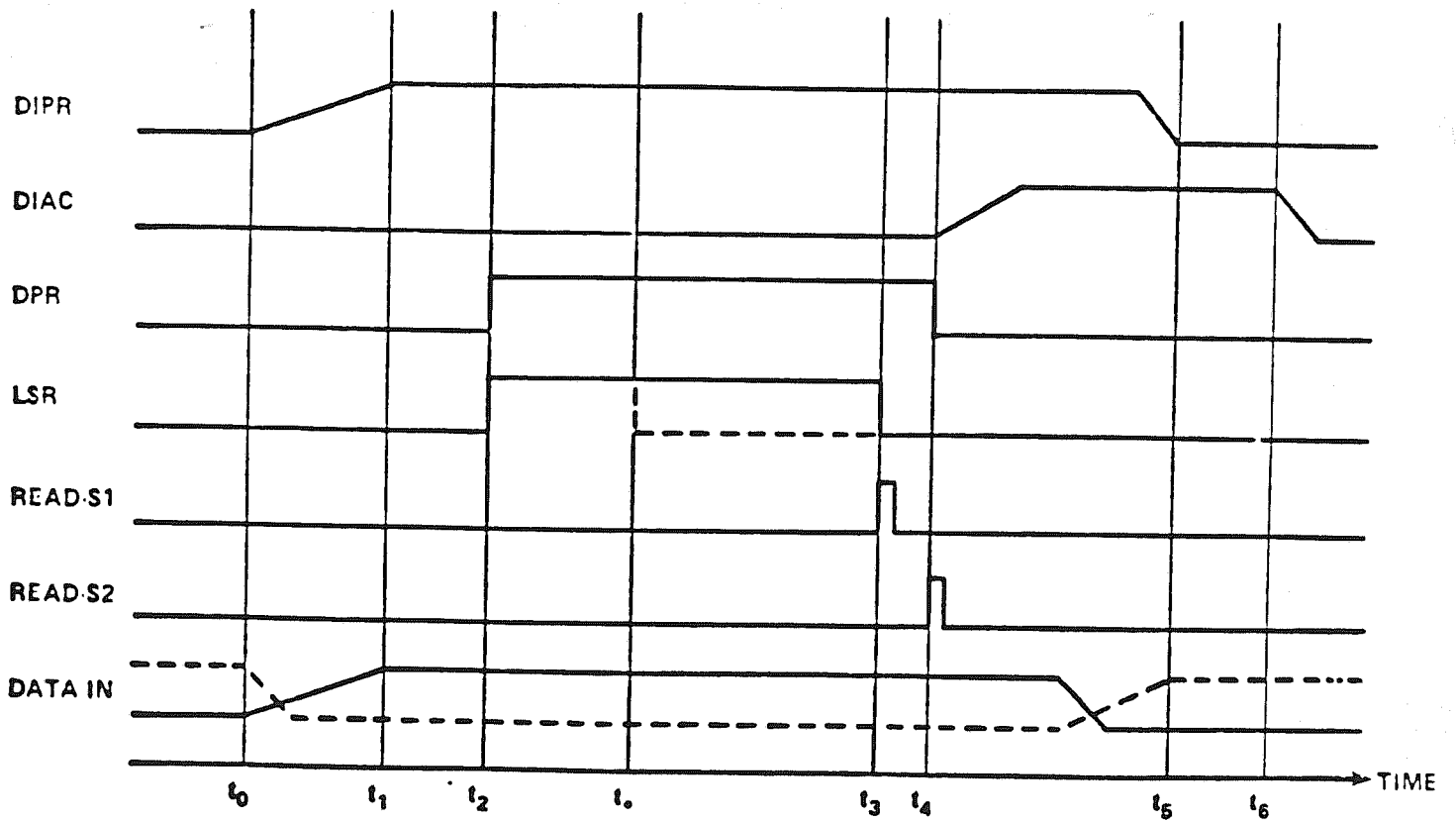
Two high-true handshake signals are provided for input data. Data Input Present (DIPR) is set high by the external device, indicating that new data is present on the Data Input (DI) lines. When the data is read by the F(0)·A(0) command, the module asserts Data Input Accepted (DIAC), indicating that it has accepted the data and is ready for another data word.

At time t_0 the peripheral device generates a "Data In" word, indicating this by DIPR = high. At time t_1 the CAMAC module detects DIPR = high. (Due to high impedance pull-up resistors and low impedance open-collector drivers, the rise time of a signal will be longer than the fall time. DIPR and all other timing signals match the worse case when they are high-true). At time t_2 , after a delay of $10\mu\text{s}$ (typical) for skew compensation, the LAM source DPR and the Read LAM status (LSR) become Logic 1, indicating that the data is established.

At time t_3 the data is read by a Dataway operation, and the LAM status is cleared. (The LAM status may be cleared earlier at time t_* by a clear-LAM operation.) At time t_4 DIAC = high is generated, indicating that the data has been read and may change. The LAM source DPR becomes Logic 0.

When the peripheral device detects DIAC = high, it may change the data and responds with generating DIPR = low.

At time t_5 , the CAMAC module receives DIPR = low and generates DIAC = low after a delay of $15\mu\text{s}$ (typical) at time t_6 . Then the next transfer cycle may be started by the peripheral device.



LAM AND HANDSHAKE TEST COMMANDS - INPUT

The F(26)·A(0) command enables the Read LAM request (allows the Read LAM status to assert the L-line). An F(24)·A(0) disables this LAM request. When a new word of input data is present and stable (DPR = 1), the Read LAM Status (LSR) is set. This is cleared by a Read command or clear LAM operation.

In a polling environment, the F(27)·A(0) command is used to determine if stable data is present (DP = 1) and the data has not yet been read. This returns Q = 1 (Q = 0 otherwise).

DATA OUTPUT REGISTER

The data output register contains 16 bits. These are written by various F(16) commands. After the data is written, the data output lines remain in the selected pattern until the next write operation. When the 3063 is used to drive a single device with up to 16 bits, an F(16)·A(1) command is used to write the data word.

In some cases, it is desirable to control two separate devices (8 bits each). For these applications, the F(16)·A(2) command writes the lower 8 bits and the F(16)·A(3) command the upper 8 bits. To drive 4-bit devices, the F(16)·A(8) through F(16)·A(11) commands are used. See the FUNCTION CODE chart on page 2 for details. Note that the byte and nibble commands affect only the desired bits and leave all other bits unchanged. Also, the write line to data output bit mapping is the same for all commands. For example, the F(16)·A(10) command writes D09 to D12 from W9 to W12.

The output signals are low true at either HTL or TTL level. The output register can be used without handshaking, if desired. Handshaking can be used to coordinate the data exchange to the peripheral device.

OUTPUT TRANSFER TIMING (HANDSHAKE SIGNALS USED)

Two high-true handshake signals are provided for output data. Data Output Present (DOPR) is set high by the module, indicating that a new data word has been established by the CAMAC write command. The peripheral device then sets Data Output Accepted (DOAC) high to indicate that it has accepted the data and is ready for another data word. Note that only one pair of output handshake signals are available; for byte and nibble addressing, the handshake signals are not generally used.

At time t_0 the CAMAC module receives DOAC = low, indicating that the preceding write cycle has been completed. The LAM source TC and the LAM status LSW become Logic 1, indicating that the next data word can be transferred.

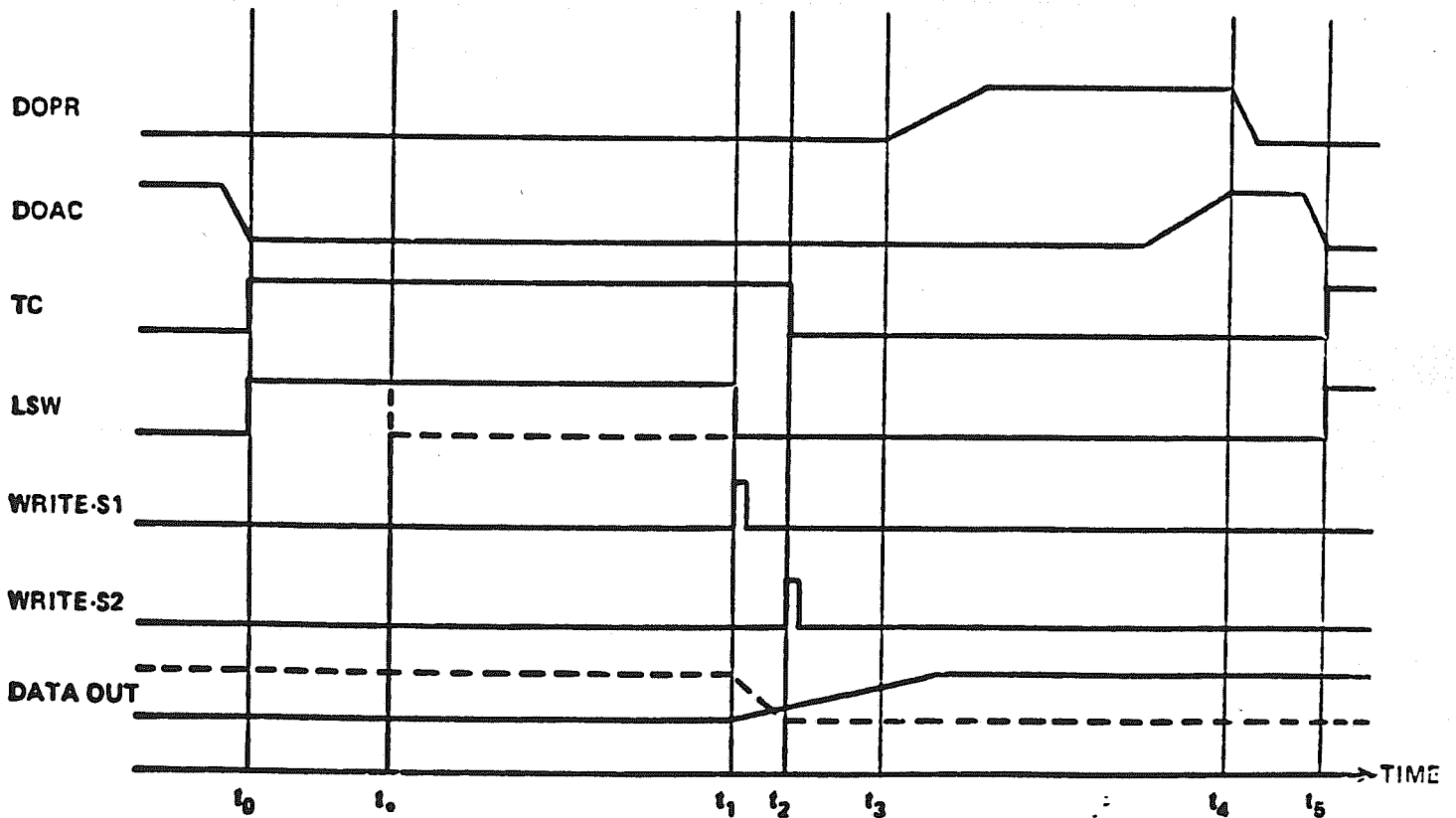
At time t_1 the data word is written into the CAMAC module by a Dataway write operation, the LAM status is cleared (the LAM status may be cleared earlier at time t_8 by a clear-LAM operation), and the status of the Data Out lines start to

Model 3063

change. At time t_2 the LAM source TC becomes Logic 0, and at time t_3 , after a delay of $10\mu\text{s}$ (typical) for skew compensation, DOPR = high is generated, indicating to the peripheral device that a new data word has been established. Having received DOPR = high, the peripheral device starts to accept the established data word and responds with generating DOAC = high.

At time t_4 the CAMAC module receives DOAC = high and generates DOPR = low but keeps the data word established until it receives DOAC = low.

DOAC = low is detected at time t_5 , the transfer cycle is completed, and a new data word may be established.



LAM AND HANDSHAKE TEST COMMANDS - OUTPUT

The F(26)A(1) command enables the Write LAM request (allows the Write LAM status to assert the L-line). An F(24)A(1) command disables this LAM request. When a word of data has been accepted by the peripheral device (it is ready for the next word), the Write LAM status is set. This is cleared by a Write command or clear LAM operation.

In a polling environment, the F(27)A(1) command is used to determine if the peripheral device is ready for a new word (transfer complete). This returns Q = 1 (Q = 0 otherwise).

STATUS INPUT BIT

In addition to the 16-bit input gate, a single bit is provided (TST input). This has general purpose use. For example, it may indicate if a peripheral device is in the ON or OFF state. This low-true signal can be HTL or TTL by module option. If the input is LOW, and F(27)A(2) command will return Q = 1; if HIGH, Q = 0.

PULSED OUTPUT CONTROL

Four pulsed control outputs are provided. These outputs are open-collector and diode-clamped to +24 volts. No pull-up resistors are provided on the module. They can drive loads up to 100 mA and +24 volts. These outputs are generally used to turn peripheral devices ON or OFF. They are as follows:

<u>Designation</u>	<u>Command</u>	<u>Output State</u>
ON A	F(25)A(0)	LOW when pulsed
OFF B	F(25)A(1)	HIGH when pulsed
ON C	F(25)A(2)	LOW when pulsed
OFF D	F(25)A(3)	HIGH when pulsed

The above indicates the factory-selected outputs. Strap options are provided to allow any of these outputs to be LOW (conducting) or HIGH (non-conducting) when pulsed.

The control pulse outputs are active for 0.5 seconds, typical. They are retriggerable and respond with Q = 0 if that particular pulse were still true when commanded to pulse again.

HTL OR TTL INPUT SIGNAL STANDARDS

For the HTL option, all data inputs (DI and TST) are low true with logic 1 = 0 to 6 volts and logic 0 = 8 to 15 volts. The two handshake signals that are IN to the module have Schmitt trigger action with logic 0 = 0 to 3.5 volts, logic 1 = 11 to 15 volts and $V_{hyst} \geq 3.5$ volts. Each input has a 10 K ohm pull-up to +15 volts.

For the TTL option, all data inputs are low true with logic 1 = 0 to 0.6 volts and logic 0 = 2 to 5 volts. The two Schmitt trigger handshake signals that are IN to the module, logic 0 = 0 to 0.6 volts, logic 1 = 2 to 5 volts, with a minimum hysteresis of 0.4 volts. Each input has a 10 K ohm pull-up to +5 volts.

HTL OR TTL OUTPUT SIGNAL STANDARDS

For the HTL option, the data output and handshake OUT signals (DO, DOPR, DIAC) are open-collector and are diode-clamped to +15 volts. They have a drive capability of 30 mA maximum.

For the TTL option, the data output and handshake OUT signals (DO, DOPR, DIAC) are open-collector and contain internal 4076 ohm pull-up resistors to +5 volts.

MODULE ID COMMAND

An F(1)·A(15) command will return a unique identification pattern, indicating the module type and serial number. The pattern is as follows:

READ BIT	STATE	MEANING
16	1	} Indicates that this is a 3063 IGOR module.
15	0	
14	0	
13	0	
12	0	
11 - 1	As Req'd	Represents the binary value of the module serial number.

For example a 3063 module with serial number 31 would have bits 16, 5, 4, 3, 2, 1 = 1 and all others = 0.

FRONT PANEL

LED Indicator

N Flashes whenever a command is accepted.

I/O Connector

I/O Port I/O Connector (Cannon DD-50P or Amphenol 50-contact ribbon).

A jackscrew is provided which functions both in insertion and extraction of the module.

POWER FOR REMOTE DEVICES

A +24-volt output is provided on the connector to power relays, etc. for the control outputs. This source is fused at 0.5 amp.

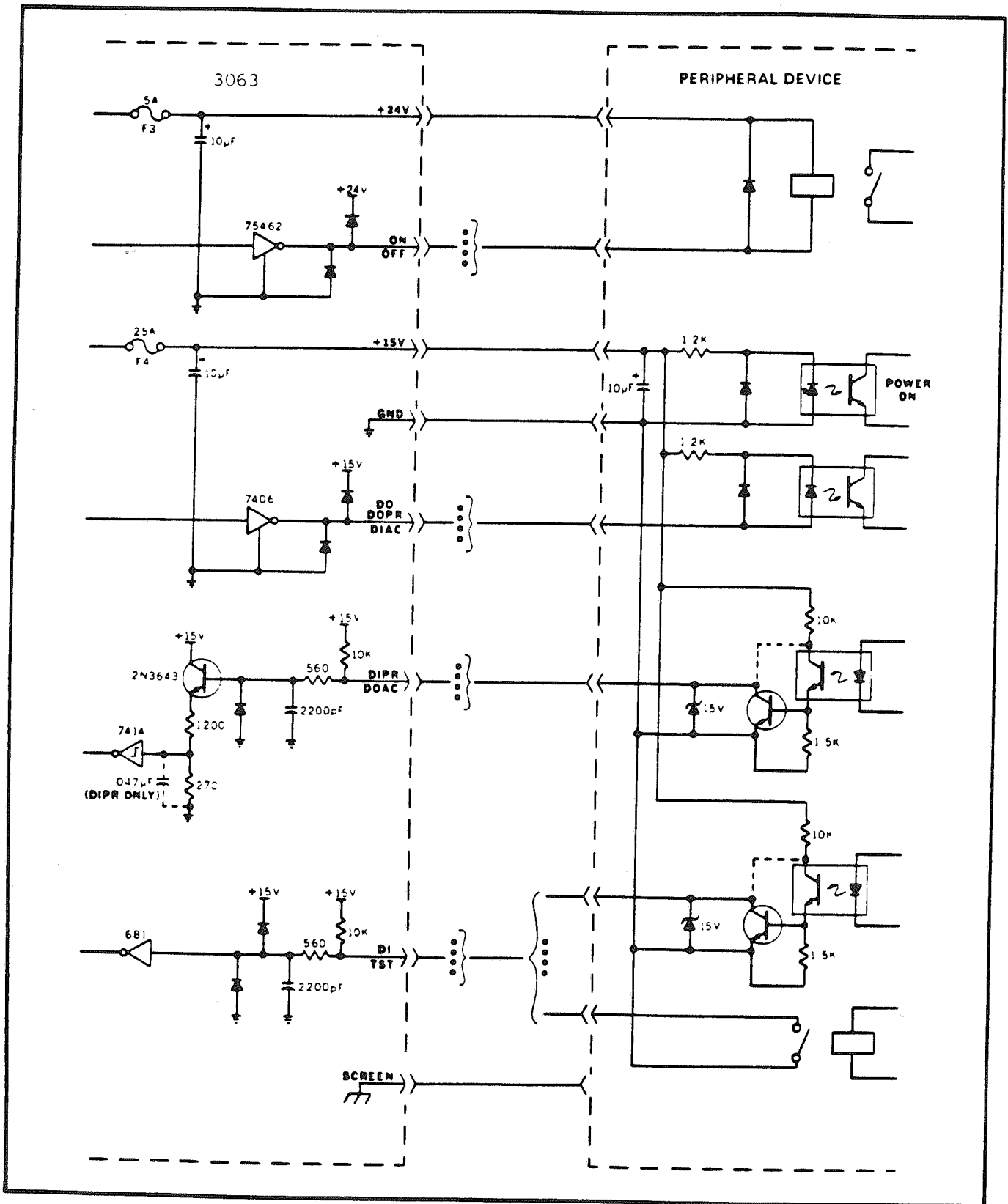
A +15-volt output is provided on the connector to power optically isolated interfaces, etc. in the peripheral device. This source is fused at 0.25 amp (+5 volts fused at 1 amp).

POWER-UP INITIALIZE

Power-up, initialize (Z), or an F(9)·A(0) command clear write data, disable LAM requests, and stop the control pulse generation. In addition, DIAC = high is generated; thus a read transfer from the peripheral device may be completed, and DOPR = high is generated. This starts a write transfer to the peripheral device and data equal to zero.

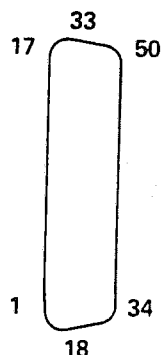
During power-up, DIAC = high and DOPR = high are maintained for a duration of 500 msec (typical) regardless of the state of DIPR and DOAC. Within that time, the handshake featured in the peripheral device must be set to the initial state generating DIPR = low and DOAC = high (unless the timing signals are not used).

INTERFACING PERIPHERAL EQUIPMENT WITH OPTICAL ISOLATION, HTL OPTIONS



NOTES:

- Value shown is for HTL version (3063-E1A); for TTL version (3063-E1B), a +5 volt, 1A. signal is provided.



FACE VIEW

Pin/Wire List

Model 3063-E1A,-E1B

50 PIN 'D'

PIN NO.

17	DI 16
16	DI 15
15	DI 14
14	DI 13
13	DI 12
12	DI 11
11	DI 10
10	DI 9
9	DI 8
8	DI 7
7	DI 6
6	DI 5
5	DI 4
4	DI 3
3	DI 2
2	DI 1
1	GND (0V)

PIN NO.

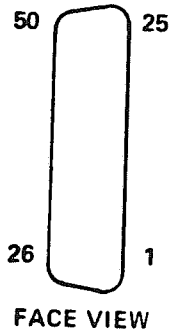
33	DO 16
32	DO 15
31	DO 14
30	DO 13
29	DO 12
28	DO 11
27	DO 10
26	DO 9
25	DO 8
24	DO 7
23	DO 6
22	DO 5
21	DO 4
20	DO 3
19	DO 2
18	DO 1

PIN NO.

50	GND
49	+24V, 0.5A
48	+15V, 0.25A (NOTE 1)
47	OFF D
46	ON C
45	OFF B
44	ON A
43	GND
42	DOAC
41	GND
40	DOPR
39	GND
38	DIAC
37	GND
36	DIPR
35	GND
34	Status Bit (TST)

Connector: Cannon DD-50P or equivalent type with fixing screw
 (Mating, floating member Cannon DD-50S, or equivalent type)
 or Amphenol 50-20500 (Mating, Amphenol 105000-7)

Socket/Wire List



50 SOCKET RIBBON CONN.

Model 3063-A1A, A1B

NOTES:

1) Value shown is for HTL version (3063-A1A); for TTL version (3063-A1B), a +5 volt, 1 Amp signal is provided.

SOCKET NO.

50	GND
49	+24V, 0.5A
48	+15V, 0.25 A (Note 1)
47	OFF D
46	ON C
45	OFF B
44	ON A
43	GND
42	DOAC
41	GND
40	DOPR
39	GND
38	DIAC
37	GND
36	DIPR
35	GND
34	STATUS BIT (TST)
33	DO 16
32	DO 15
31	DO 14
30	DO 13
29	DO 12
28	DO 11
27	DO 10
26	DO 9

SOCKET NO.

25	DO 8
24	DO 7
23	DO 6
22	DO 5
21	DO 4
20	DO 3
19	DO 2
18	DO 1
17	DI 16
16	DI 15
15	DI 14
14	DI 13
13	DI 12
12	DI 11
11	DI 10
10	DI 9
9	DI 8
8	DI 7
7	DI 6
6	DI 5
5	DI 4
4	DI 3
3	DI 2
2	DI 1
1	GND (0.0V)

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STRAP OPTIONS

Operation is described earlier covers the module strap options as set by the factory. Field options are described in Figure 1. NOTE THAT THE MODULE CANNOT READILY BE CONVERTED BETWEEN TTL AND HTL -- THIS IS A FACTORY ORDERING OPTION.

