Model 3063-A1X

16-bit Input Gate/Output Register

INSTRUCTION MANUAL

February, 1987

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16-bit Input Gate/Output Register

Provides general-purpose interfacing of TTL or HTL signals

3063

Features

- **16-bit Input Gate/Output Register (IGOR) with handshaking**
- **Four control pulses and one status bit**
- **Complete interrupt capability**
- **HTL and TTL signal options available**

Typical Applications

- **General-purpose input/output register**
- **Communication link between CAMAC systems**
- **Device interfaces**
- **Power supply interfaces**

General Description

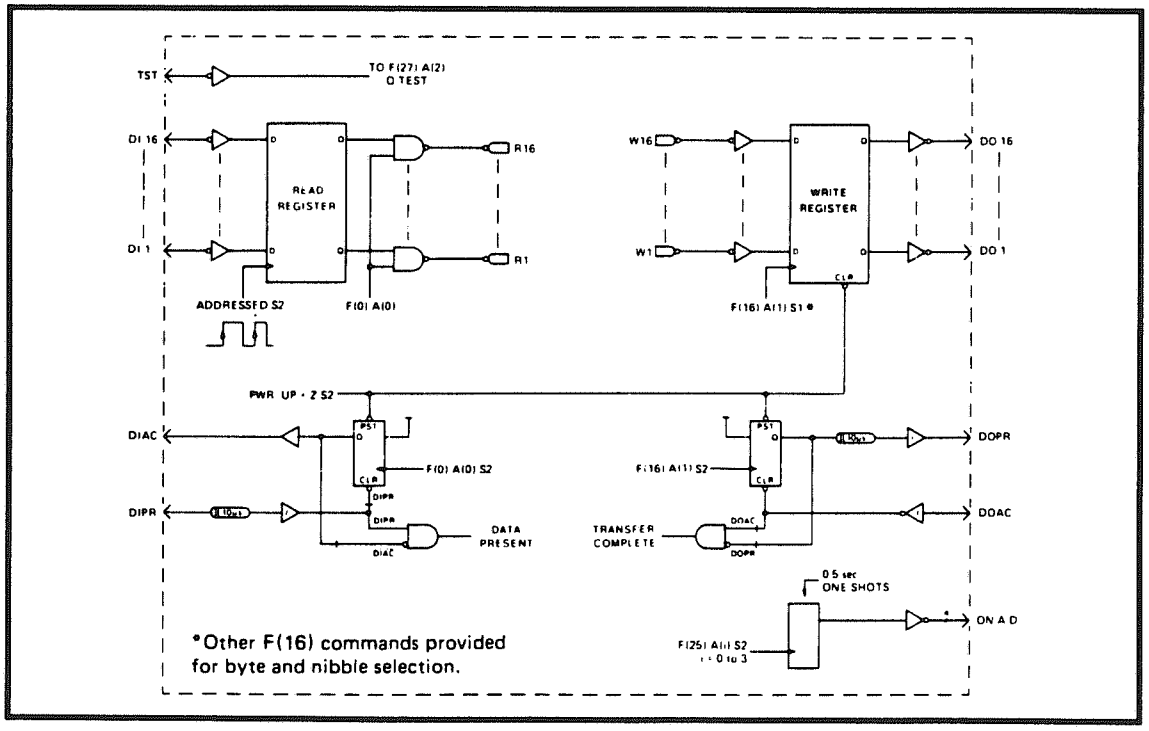
The 3063 is a single-width module containing a 16-bit input gate, a 16-bit output register, a 1-bit status input, and four 0.5-second pulse outputs. Full handshaking is provided for the input gate and output register. The handshake signals can be tested; they also can generate a LAM. The module can be used without handshaking, if desired.

The four pulsed control outputs can drive loads up to 100 milliamperes and +24 volts. This module can be ordered with all other I/O signals using either high threshold logic (HTL) or TTL. With the HTL option, the data and status inputs recognize logic one from 0 to 6 volts and logic zero from 8 to 15 volts.

Commands are included to write the entire 16-bit output register, to write eight bits at a time, as well as to write four bits at a time. This allows the module to drive independent 4-bit or 8-bit devices.

The 3063 is available with a 50-pin "D" or 50-contact Amphenol ribbon connector.

Simplified Block Diagram



Function Codes

Command		Q	Action
F(0)·A(0)	RD1	1	Reads the input data and clears the Read LAM status.
F(1)·A(15)	RD2	1	Reads the module identifing number. ($3063 = 5767_8$).
F(8)·A(0)	TLM	LRR	Tests the Read LAM request.
F(8)·A(1)	TLM	LRW	Tests the Write LAM request.
F(8)·A(15)	TLM	LR	Tests whether a LAM request is present.
F(9)·A(0)	CL1	1	Clears the LAM status bits, disables all LAM requests, sets DIAC and DOPR true.
F(9)·A(1)	CL1	1	Same as F(9)·A(0). (See Note 3.)
F(10)·A(0)	CLM	1	Clears the Read LAM status.
F(10)·A(1)	CLM	1	Clears the Write LAM status.
F(16)·A(1)	WT1	1	Writes the Output Data register word (DO1 to DO16) and clears the Write LAM status.
F(16)·A(2)	WT1	1	Writes the Output Data register byte 1 (DO1 to DO8) and clears the Write LAM status.
F(16)·A(3)	WT1	1	Writes the Output Data register byte 2 (DO9 to DO16) and clears the Write LAM status.
F(16)·A(8)	WT1	1	Writes the Output Data register nibble 1 (DO1 to DO4) and clears the Write LAM status.
F(16)·A(9)	WT1	1	Writes the Output Data register nibble 2 (DO5 to DO8) and clears the Write LAM status.
F(16)·A(10)	WT1	1	Writes the Output Data register nibble 3 (DO9 to DO12) and clears the Write LAM status.
F(16)·A(11)	WT1	1	Writes the Output Data register nibble 4 (DO13 to DO16) and clears the Write LAM status.
F(24)·A(0)	DIS	1	Disables the Read LAM request.
F(24)·A(1)	DIS	1	Disables the Write LAM request.
F(25)·A(0)	XEQ	A $\overline{\text{ACTIVE}}$	Executes Pulse A (0.5 seconds).
F(25)·A(1)	XEQ	B $\overline{\text{ACTIVE}}$	Executes Pulse B (0.5 seconds).
F(25)·A(2)	XEQ	C $\overline{\text{ACTIVE}}$	Executes Pulse C (0.5 seconds).
F(25)·A(3)	XEQ	D $\overline{\text{ACTIVE}}$	Executes Pulse D (0.5 seconds).
F(26)·A(0)	ENB	1	Enables the Read LAM request.
F(26)·A(1)	ENB	1	Enables the Write LAM request.
F(27)·A(0)	TST	DP	Tests whether the Data Present LAM source is true.
F(27)·A(1)	TST	TC	Tests whether the Transfer Complete LAM source is true.
F(27)·A(2)	TST	TST	Tests whether the TST input is true.
Z	CZ	0	Clears the LAM status bits, disables all LAM requests, sets DIAC and DOPR true.

Notes: 1. X = 1 for all valid addressed commands.
2. The Execute commands return Q = 0 if that Execute Pulse is still true from a previous command.
3. Command provided for special application, not needed for standard 3063.

Power Requirements (not including external loads)

+6 volts:	550 mA
+24 volts:	50 mA (no internal +24-volt load for TTL versions)

Ordering Information

Model 3063-A1A	Input Gate/Output Register, 16 bits, with HTL I/O, 50S Amphenol Ribbon connector
Model 3063-A1B	Input Gate/Output Register, 16 bits, with TTL I/O, 50S Amphenol Ribbon connector
Model 3063-E1A	Input Gate/Output Register, 16 bits, with HTL I/O, 50P "D" connector
Model 3063-E1B	Input Gate/Output Register, 16 bits, with TTL I/O, 50P "D" connector

Related Products

For Model	Mating Connector	I/O Cable (one end unterminated)
3063-A1A, A1B	5950-Z1A	5853-Axyz
3063-E1A, E1B	5934-Z1A	5851-Bxyz

DATA INPUT GATE

The data input gate contains 16 bits. These are read by an F(0)·A(0) command (Read lines R1 to R16). A read staticize register is provided to prevent data from changing early in the Dataway cycle. The signals are low-true at either HTL or TTL level. The input gate can be used without handshaking, if desired. Hand-shaking can be used to coordinate the data exchange from the peripheral device.

INPUT TRANSFER TIMING (HANDSHAKE SIGNALS USED)

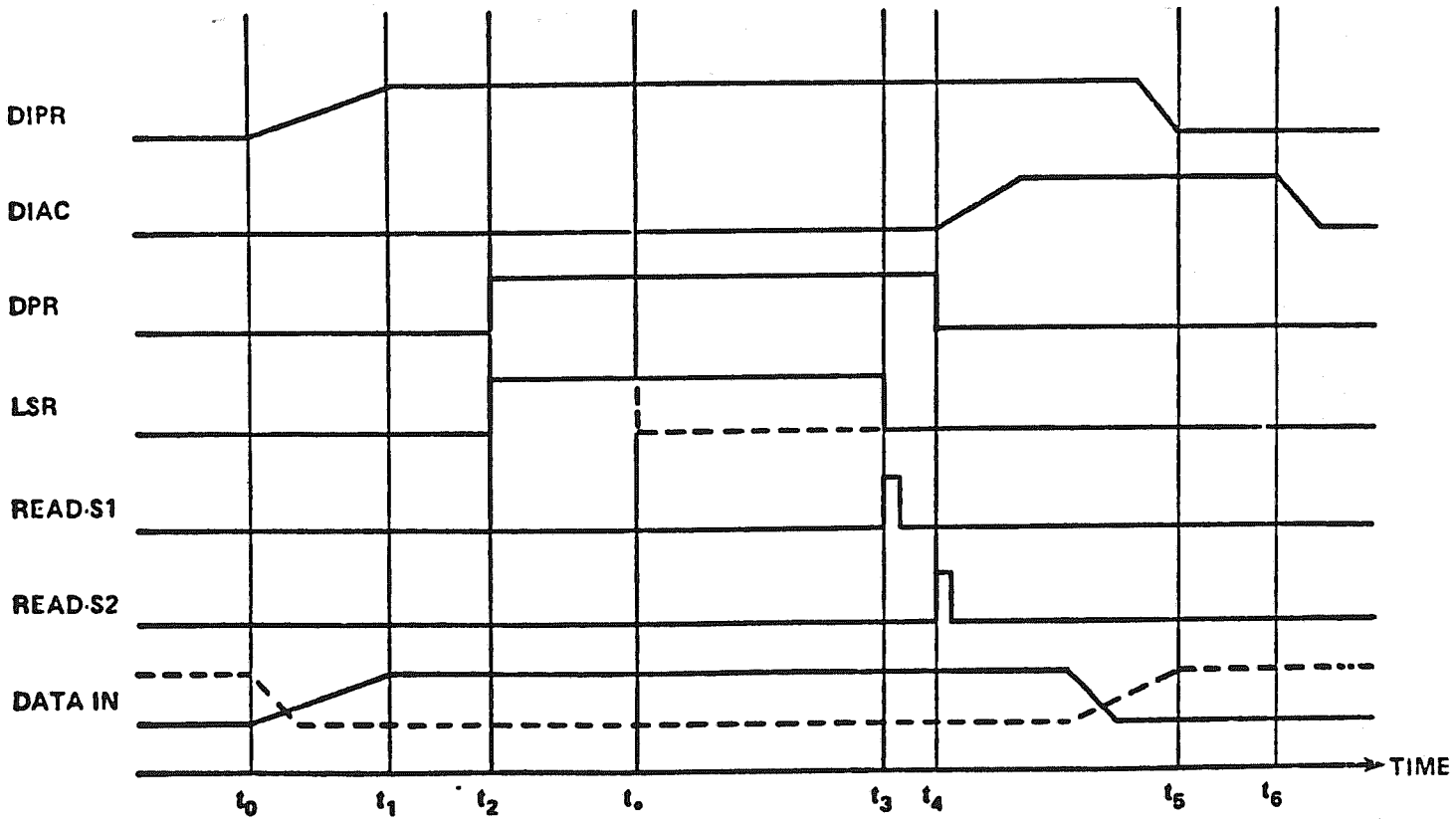
Two high-true handshake signals are provided for input data. Data Input Present (DIPR) is set high by the external device, indicating that new data is present on the Data Input (DI) lines. When the data is read by the F(0)·A(0) command, the module asserts Data Input Accepted (DIAC), indicating that it has accepted the data and is ready for another data word.

At time t_0 the peripheral device generates a "Data In" word, indicating this by DIPR = high. At time t_1 the CAMAC module detects DIPR = high. (Due to high impedance pull-up resistors and low impedance open-collector drivers, the rise time of a signal will be longer than the fall time. DIPR and all other timing signals match the worse case when they are high-true). At time t_2, after a delay of 10us (typical) for skew compensation, the LAM source DPR and the Read LAM status (LSR) become Logic 1, indicating that the data is established.

At time t_3 the data is read by a Dataway operation, and the LAM status is cleared. (The LAM status may be cleared earlier at time $t*$ by a clear-LAM operation.) At time t_4 DIAC = high is generated, indicating that the data has been read and may change. The LAM source DPR becomes Logic 0.

When the peripheral device detects DIAC = high, it may change the data and responds with generating DIPR = low.

At time t_5, the CAMAC module receives DIPR = low and generates DIAC = low after a delay of 15us (typical) at time t_6. Then the next transfer cycle may be started by the peripheral device.


DIPR
DIAC
DPR
LSR
READ·S1
READ·S2
DATA IN
TIME
t_0
t_1
t_2
t_3
t_4
t_5
t_6

LAM AND HANDSHAKE TEST COMMANDS - INPUT

The F(26)·A(0) command enables the Read LAM request (allows the Read LAM status to assert the L-line). An F(24)·A(0) disables this LAM request. When a new word of input data is present and stable (DPR = 1), the Read LAM Status (LSR) is set. This is cleared by a Read command or clear LAM operation.

In a polling environment, the F(27)·A(0) command is used to determine if stable data is present (DP = 1) and the data has not yet been read. This returns Q = 1 (Q = 0 otherwise).

DATA OUTPUT REGISTER

The data output register contains 16 bits. These are written by various F(16) commands. After the data is written, the data output lines remain in the selected pattern until the next write operation. When the 3063 is used to drive a single device with up to 16 bits, an F(16)·A(1) command is used to write the data word.

In some cases, it is desirable to control two separate devices (8 bits each). For these applicatons, the F(16)·A(2) command writes the lower 8 bits and the F(16)·A(3) command the upper 8 bits. To drive 4-bit devices, the F(16)·A(8) through F(16)·A(11) commands are used. See the FUNCTION CODE chart on page 2 for details. Note that the byte and nibble commands affect only the desired bits and leave all other bits unchanged. Also, the write line to data output bit mapping is the same for all commands. For example, the F(16)·A(10) command writes D09 to D012 from W9 to W12.

The output signals are low true at either HTL or TTL level. The output register can be used without handshaking, if desired. Handshaking can be used to coordinate the data exchange to the peripheral device.

OUTPUT TRANSFER TIMING (HANDSHAKE SIGNALS USED)

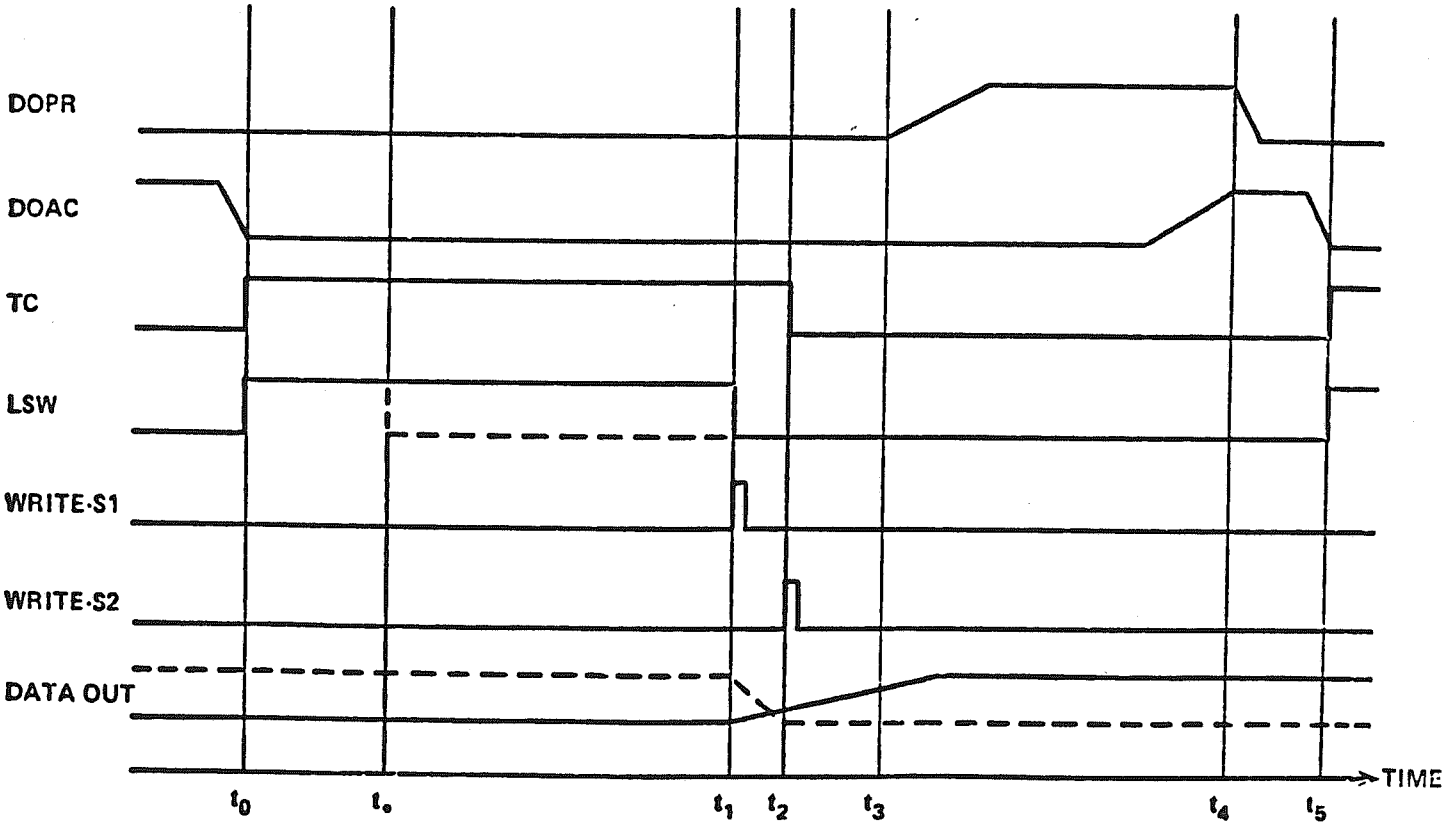
Two high-true handshake signals are provided for output data. Data Output Present (DOPR) is set high by the module, indicating that a new data word has been established by the CAMAC write command. The peripheral device then sets Data Output Accepted (DOAC) high to indicate that it has accepted the data and is ready for another data word. Note that only one pair of output handshake signals are available; for byte and nibble addressing, the handshake signals are not generally used.

At time t_0 the CAMAC module receives DOAC = low, indicating that the preceding write cycle has been completed. The LAM source TC and the LAM status LSW become Logic 1, indicating that the next data word can be transferred.

At time t_1 the data word is written into the CAMAC module by a Dataway write operation, the LAM status is cleared (the LAM status may be cleared earlier at time t_8 by a clear-LAM operation), and the status of the Data Out lines start to change. At time t_2 the LAM source TC becomes Logic 0, and at time t_3, after a delay of 10us (typical) for skew compensation, DOPR = high is generated, in-dicating to the peripheral device that a new data word has been established. Having received DOPR = high, the peripheral device starts to accept the estab-lished data word and responds with generating DOAC = high.

At time t_4 the CAMAC module receives DOAC = high and generates DOPR = low but keeps the data word established until it receives DOAC = low.

DOAC = low is detected at time t_5, the transfer cycle is completed, and a new data word may be established.



LAM AND HANDSHAKE TEST COMMANDS - OUTPUT

The F(26)A(1) command enables the Write LAM request (allows the Write LAM status to assert the L-line). An F(24)A(1) command disables this LAM request. When a word of data has been accepted by the peripheral device (it is ready for the next word), the Write LAM status is set. This is cleared by a Write command or clear LAM operation.

In a polling environment, the F(27)A(1) command is used to determine if the peripheral device is ready for a new word (transfer complete). This returns Q = 1 (Q = 0 otherwise).

STATUS INPUT BIT

In addition to the 16-bit input gate, a single bit is provided (TST input). This has general purpose use. For example, it may indicate if a peripheral device is in the ON or OFF state. This low-true signal can be HTL or TTL by module option. If the input is LOW, and F(27)A(2) command will return Q = 1; if HIGH, Q = 0.

PULSED OUTPUT CONTROL

Four pulsed control outputs are provided. These outputs are open-collector and diode-clamped to +24 volts. No pull-up resistors are provided on the module. They can drive loads up to 100 mA and +24 volts. These outputs are generally used to turn peripheral devices ON or OFF. They are as follows:

Designation	Command	Output State
ON A	F(25)A(0)	LOW when pulsed
OFF B	F(25)A(1)	HIGH when pulsed
ON C	F(25)A(2)	LOW when pulsed
OFF D	F(25)A(3)	HIGH when pulsed

The above indicates the factory-selected outputs. Strap options are provided to allow any of these outputs to be LOW (conducting) or HIGH (non-conducting) when pulsed.

The control pulse outputs are active for 0.5 seconds, typical. They are retriggerable and respond with Q = 0 if that particular pulse were still true when commanded to pulse again.

HTL OR TTL INPUT SIGNAL STANDARDS

For the HTL option, all data inputs (DI and TST) are low true with logic 1 = 0 to 6 volts and logic 0 = to 8 to 15 volts. The two handshake signals that are IN to the module have Schmitt trigger action with logic 0 = 0 to 3.5 volts, logic 1 = 11 to 15 volts and V_{hyst} __ 3.5 volts. Each input has a 10 K ohm pull-up to +15 volts.

For the TTL option, all data inputs are low true with logic 1 = 0 to 0.6 volts and logic 1 = 2 to 5 volts. The two Schmitt trigger handshake signals that are IN to the module, logic 0 = 0 to 0.6 volts, logic 1 = 2 to 5 volts, with a minimum hysterisis of 0.4 volts. Each input has a 10 K ohm pull-up to +5 volts.

HTL OR TTL OUTPUT SIGNAL STANDARDS

For the HTL option, the data output and handshake OUT signals (DO, DOPR, DIAC) are open-collector and are diode-clamped to +15 volts. They have a drive capa-bility of 30 mA maximum.

For the TTL option, the data output and handshake OUT signals (DO, DOPR, DIAC) are open-collector and contain internal 4076 ohm pull-up resistors to +5 volts.

MODULE ID COMMAND

An F(1)·A(15) command will return a unique identification pattern, indicating the module type and serial number. The pattern is as follows:

READ BIT	STATE	MEANING
16	1	
15	0	
14	0	Indicates that this is a 3063 IGOR module.
13	0	
12	0	
11 - 1	As Req'd	Represents the binary value of the module serial number.

For example a 3063 module with serial number 31 would have bits 16, 5, 4, 3, 2, 1 = 1 and all others = 0.

FRONT PANEL

LED Indicator

N	Flashes whenever a command is accepted.

I/O Connector

I/O Port	I/O Connector (Cannon DD-50P or Amphenol 50-contact ribbon).

A jackscrew is provided which functions both in insertion and extraction of the module.

POWER FOR REMOTE DEVICES

A +24-volt output is provided on the connector to power relays, etc. for the control outputs. This source is fused at 0.5 amp.

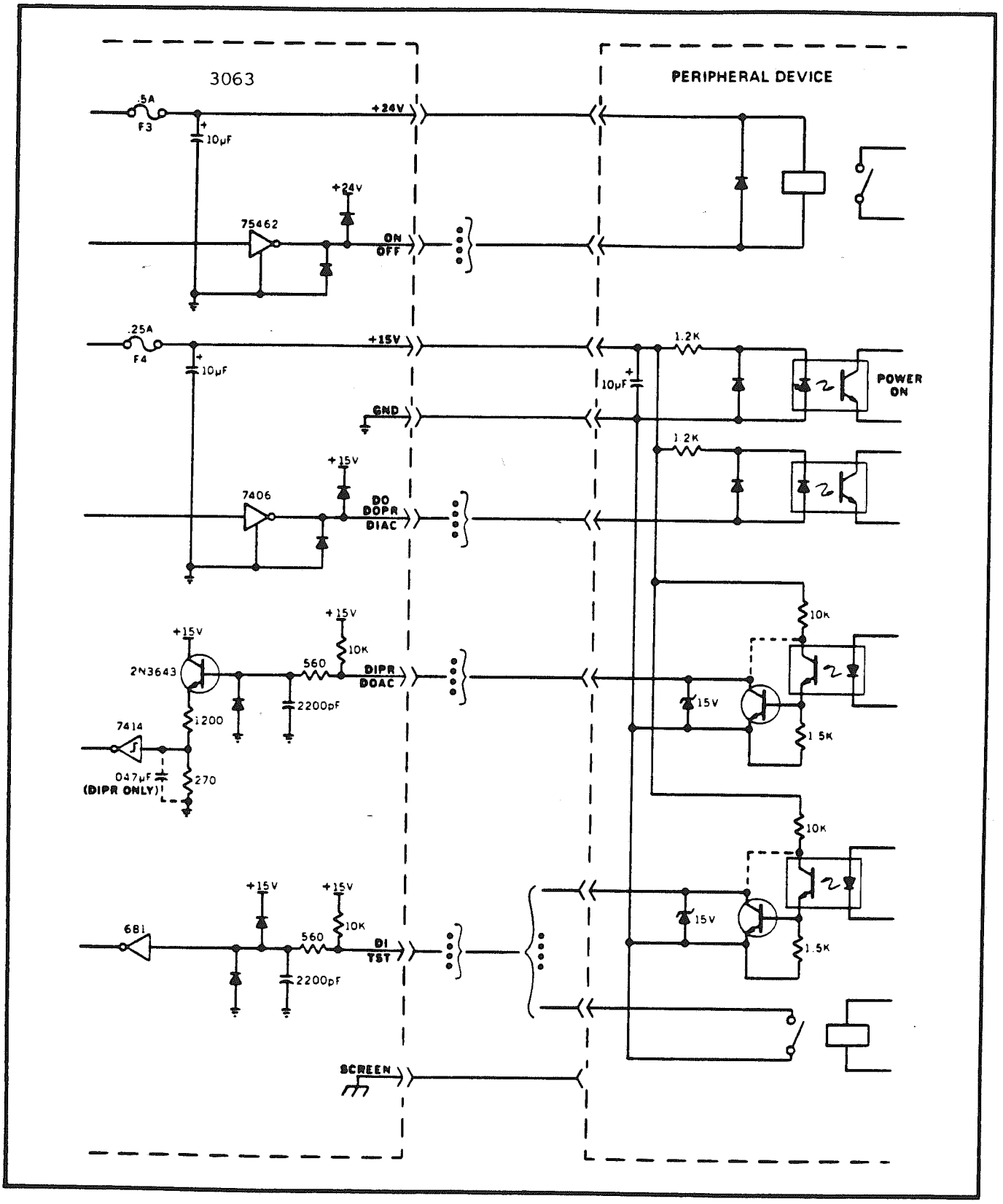
A +15-volt output is provided on the connector to power optically isolated interfaces, etc. in the peripheral device. This source is fused at 0.25 amp (+5 volts fused at 1 amp).

POWER-UP INITIALIZE

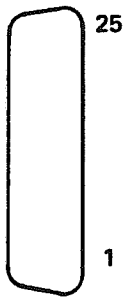
Power-up, initialize (Z), or an F(9)·A(0) command clear write data, disable LAM requests, and stop the control pulse generation. In addition, DIAC = high is generated; thus a read transfer from the peripheral device may be completed, and DOPR = high is generated. This starts a write transfer to the peripheral device and data equal to zero.

During power-up, DIAC = high and DOPR = high are maintained for a duration of 500 msec (typical) regardless of the state of DIPR and DOAC. Within that time, the handshake featured in the peripheral device must be set to the initial state generating DIPR = low and DOAC = high (unless the timing signals are not used).

INTERFACING PERIPHERAL EQUIPMENT WITH OPTICAL ISOLATION, HTL OPTIONS



Model 3063-
A1X,-A1Y



FACE VIEW

Socket/Wire List

50 SOCKET RIBBON CONN.

3063-A1X,-A1Y

Note:

Value shown is for HTL version (3063-A1X); for TTL version (3063-A1Y), a +5 volt, 1 Amp signal is provided.

SOCKET NO.		SOCKET NO.	
50	GND	25	DI 16
49	DO 16	24	+ 24 V, 0.5 A
48	DI 15	23	DO 15
47	+ 15, 0.25 A (Note)	22	DI 14
46	DO 14	21	OFF D
45	DI 13	20	DO 13
44	ON C	19	DI 12
43	DO 12	18	OFF B
42	DI 11	17	DO 11
41	ON A	16	DI 10
40	DO 10	15	GND
39	DI 9	14	DO 9
38	DOAC	13	DI 8
37	DO 8	12	GND
36	DI 7	11	DO 7
35	DOPR	10	DI 6
34	DO 6	9	GND
33	DI 5	8	DO 5
32	DIAC	7	DI 4
31	DO 4	6	GND
30	DI 3	5	DO 3
29	DIPR	4	DI 2
28	DO 2	3	GND
27	DI 1	2	DO 1
26	Status Bit (TST)	1	GND

STRAP OPTIONS

Operation is described earlier covers the module strap options as set by the factory. Field options are described in Figure 1. NOTE THAT THE MODULE CANNOT READILY BE CONVERTED BETWEEN TTL AND HTL -- THIS IS A FACTORY ORDERING OPTION.

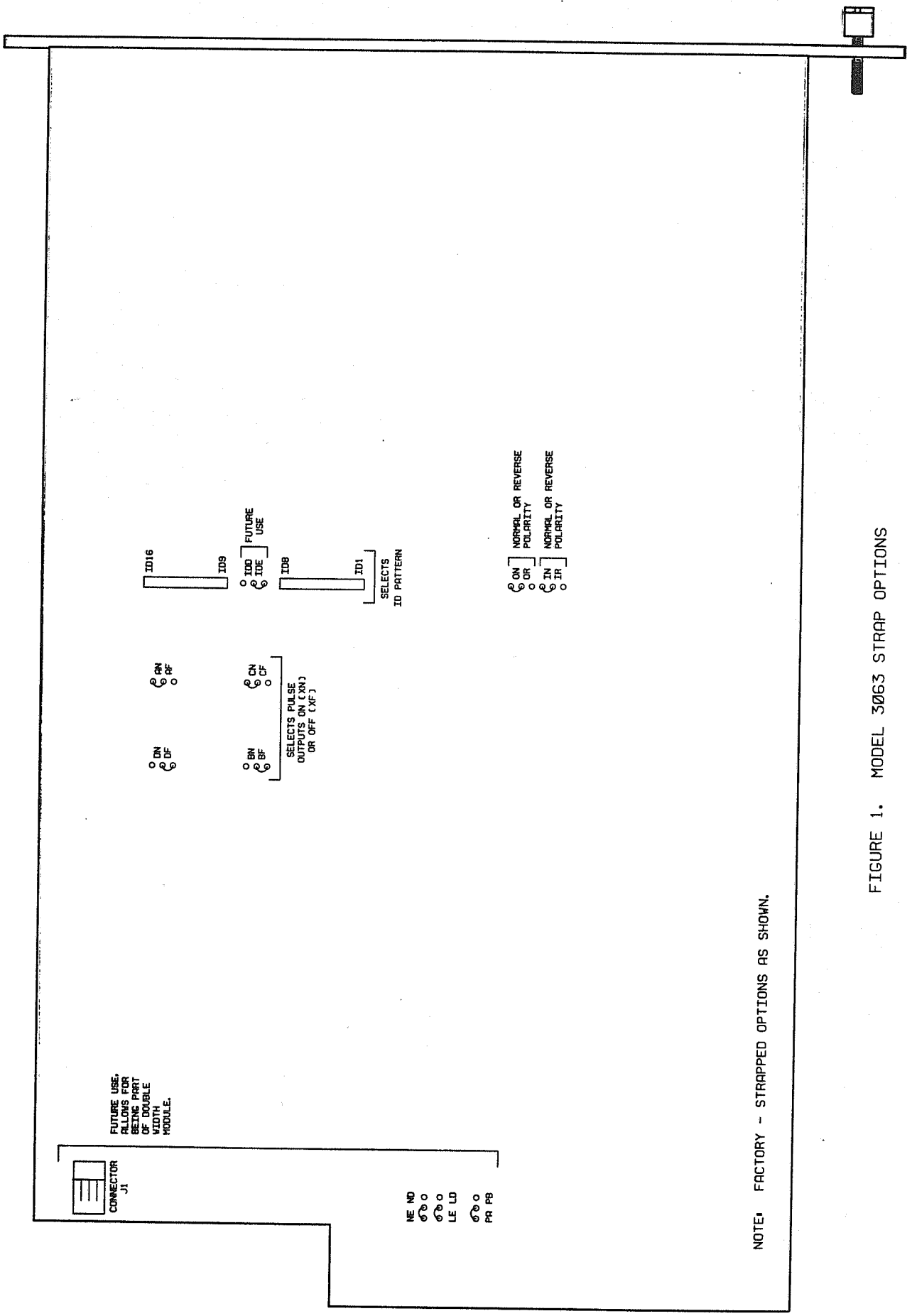


FIGURE 1. MODEL 3063 STRAP OPTIONS