Model 3115-L3A

Timed D/A Converter

INSTRUCTION MANUAL

December, 1993

CONTENTS

Features and Applications 1
General Description 1
Function Codes 2
Simplified Block Diagram (single channel) 2
Power Requirements & Weight 2
Ordering Information 2

OPERATION 3

CLOCK CONTROL REGISTER 4

MASTER/SLAVE OPERATION 4

EXTERNAL CLOCK INPUT 5

EXTERNAL CLOCK OUTPUT 5

STOP TRIGGER INPUT 5

LAM REQUEST 5

RECYCLE FEATURE 6

D/A CALIBRATION 6

OFFSET ADJUSTMENT 7

GAIN ADJUSTMENT 7

DAC-80 DATA SHEET

FIGURES

FIGURE 1 - RANGE STRAPS 8
FIGURE 2 - OFFSET/GAIN CONTROLS 9

Schematic Drawing #022191-D-5044

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Warranty
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6-Channel Timed D/A Converter

Generates arbitrary waveforms with an internal or external clock **3115**

Features

- **6 analog output channels**
- **12-bit memory driving each channel**
- **1K, 2K & 4K memory options**
- **Programmable clock rates**
- **External clock option**
- **Programmable recycle feature**
- **LAM request generation when memory readout reaches half-way point**
- **Selectable output voltage ranges**

Typical Applications

- **Analog waveform generation**
- **Reconstruction of digitized transients**
- **Simulation**

General Description *(Product specifications and descriptions subject to change without notice.)*

The 3115 is a single-width CAMAC module that generates six output voltages that can dynamically change in a predetermined way. Each channel contains a 12-bit D/A converter that receives data from a 1K-, 2K- or 4K-word First-In, First-Out (FIFO) memory. Data is clocked out of the FIFO and transformed to an analog voltage signal by the D/A converter. Strap options are provided so that the output range of each channel can be independently set by the user to ±2.5 volts, ±5 volts, ±10, 0 to 5 volts, or 0 to +10 volts. The module uses two's complement format to represent the data in the bipolar ranges and straight binary for the unipolar ranges.

FIFO clocking is common for all channels on the module. The rate is determined by the clock control register. The eight clock rates, selected from an on-board, crystal-controlled source, are 10, 5, 2.5, and 1 kilohertz, and 500, 250, 100, and 50 hertz. An external clock input and a clock output connection are also provided so that one 3115 can act as the master clock source for other modules. The maximum external clock frequency is 200 kilohertz; the maximum length of the data stream is 1024, 2048 or 4096 points, depending on the option chosen.

Any channel can generate a LAM request signal when the FIFO reaches the half-full point. This signal can be used to interrupt the controlling computer to load additional waveform data.

The recycle feature allows retransmission of FIFO data to generate repetitive waveforms. This feature is common to all channels and must be separately enabled from the Dataway. It is disabled if any channel is rewritten with new data. While the enabling of this feature is common to all channels, the recycling in any channel is controlled by end-of-data for that channel. Waveform periods can therefore vary from channel to channel.

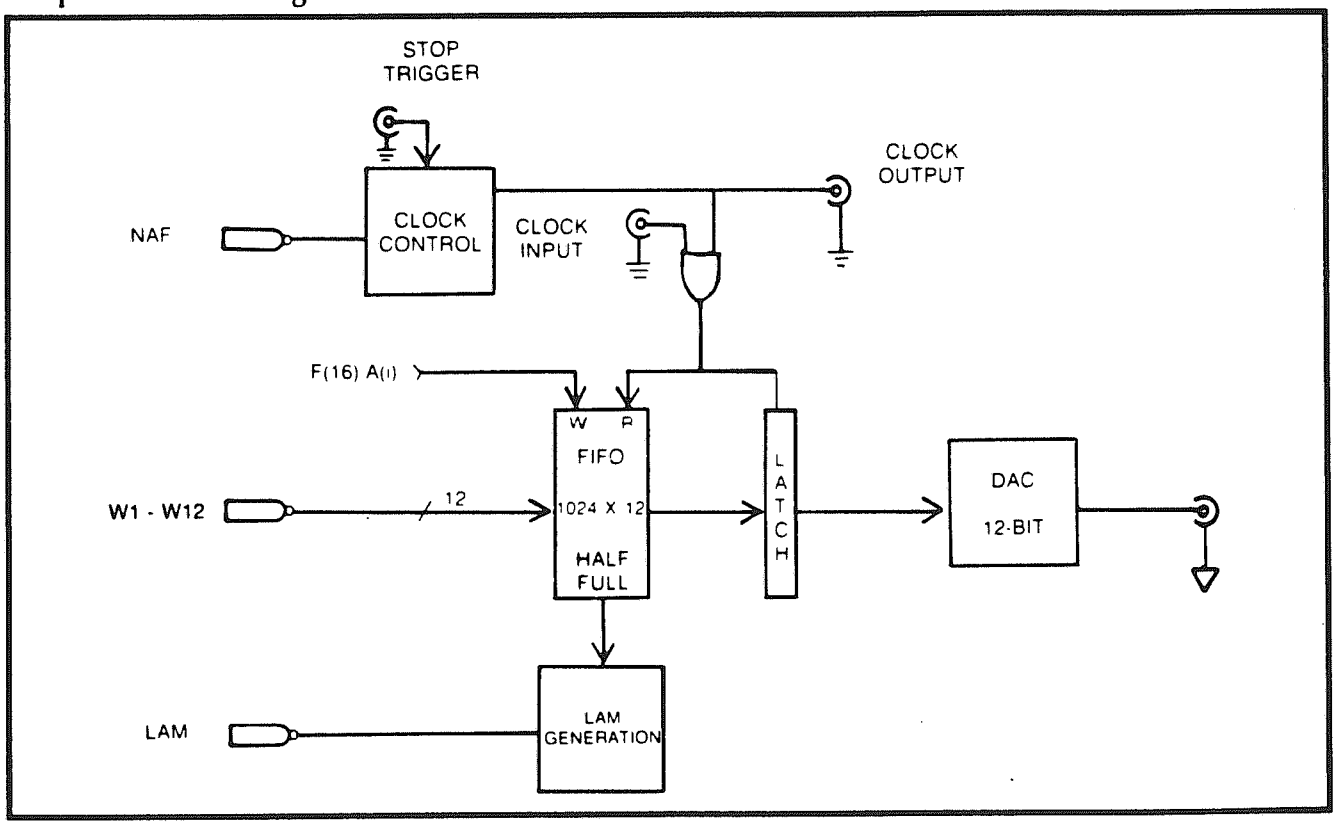
All analog outputs are available on the 3115's front panel via single-contact LEMO connectors, as are TTL level clock input and output connections. Front-panel LEDs indicate: (A) when the module is addressed, (B) whether or not the module is in the sample state, and (C) the presence of a LAM condition.

Function Codes

Command		Q	Action
F(1)·A(12)	RD2	1	Reads the LAM status pattern.
F(8)·A(15)	TLM	LR	Tests for the presence of a LAM request.
F(9)·A(0)	CL1	1	Aborts the sampling cycle and sets the analog output levels to zero volts.
F(9)·A(1)	CL1	1	Aborts the sampling cycle, leaving the analog output levels at the values last sampled.
F(9)·A(2)	CL1	1	Resets FIFO memory pointers.
F(11)·A(12)	CL2	1	Clears the LAM status bits.
F(16)·A(i)	WT1	$\overline{\text{Full}}$	Writes data into the selected channel's FIFO. (See Note 2.)
F(17)·A(0)	WT2	1	Writes the Clock Control register.
F(17)·A(13)	WT2	1	Writes the LAM Mask register.
F(24)·A(0)	DIS	1	Disables the recycle feature.
F(25)·A(0)	XEQ	1	Sets the FIFO Read pointers to the first valid data entry and (at S2) initializes the sampling cycle.
F(25)·A(1)	XEQ	1	Initializes the sampling cycle from the current positions of FIFO Read pointers.
F(26)·A(0)	ENB	1	Enables the recycle feature.

Notes: 1. X = 1 for all valid addressed commands.
2. i can range from 0 to 5.

Simplified Block Diagram



Power Requirements

+6 volts: 1.51 A +24 volts: 47 mA -24 volts: 130 mA

Ordering Information

Model 3115-L1A Timed D/A Converter, 6 channels, 12 bits, 1K x 12 FIFO, six 1-contact LEMO connectors
Model 3115-L2A Timed D/A Converter, 6 channels, 12 bits, 2K x 12 FIFO, six 1-contact LEMO connectors
Model 3115-L3A Timed D/A Converter, 6 channels, 12 bits, 4K x 12 FIFO, six 1-contact LEMO connectors

Related Products

Model 5910-Z1A Mating Connector
Model 5857-Axyz and -Bxyz LEMO Cable Assemblies

OPERATION

The operation of the Model 3115 is as follows:

1. Data is first written to the selected channel's FIFO memory via F(16) commands. Each channel holds up to 4096 12-bit data words. Each of the F(16) commands responds with Q=1 indicating that the FIFO is not full and that data has been accepted.

2. Once data is loaded into the respective channel or channel's FIFO memory, the rate at which the digital-to-analog conversions are to take place is selected by writing the Clock Control Register with an F(17)A(0) command.

3. At this point, two options are available which affect the output cycle of the Model 3115.

   A. The module may be used to produce a repetitive waveform by retransmitting the stored data pattern once the FIFO memory reaches the "Empty" state. You may enable this recycle feature with an F(26)A(0) command.

   B. The module may be used to transmit a continuously varying data pattern. Once the FIFO memory data has been transferred to the output, new data may be written to the module with additional F(16) commands. To avoid a dead band in the output signals, a LAM request may be generated when any channel's FIFO is less that half-full. Refer to the discussion of LAM Requests (page 5) for further details on this option.

4. Sampling is referred to as the transfer of data from the FIFO memory to the D/A converters. The F(25) A(0) command resets the FIFO read pointers to the first valid data entry and initiates the sampling cycle.

   If sampling is terminated after 4096 pieces of data is written to a channel, then it is necessary to clear or reset the FIFOs with an F(9)A(2) command before inputting another 4096 pieces of data and using the F(25)A(0) command to initiate a new sample.

   No CLEAR is necessary when using 4095 pieces or less. Also, no CLEAR is necessary if data is continually written and sampling is not stopped.

5. If a LAM request is enabled, the module will generate a LAM request signaling for more data once the FIFO reaches the half-full state. The F(8)A(15) command can be used to test for this condition. If the FIFO reaches empty, the analog output remains at the last value sampled until additional data is received.

6. The F(9)A(1) and the Stop Trigger Input will abort the sampling cycle, leaving the analog outputs at the values last sampled. The F(25)A(1) command will resume the sampling cycle from the current positions of the FIFO pointers. The F(9)A(0) aborts the sampling cycle, sets the analog outputs to 0 volts, and disables the recycle feature. (See the section on the Recycle Feature.)

CLOCK CONTROL REGISTER

This register is used to select the rate at which the digital-to-analog conversions are to occur. This register is written with an F(17)A(0) command with data in the following format:

W5				W1	
SLV	EXT	S3	S2	S1	F(17)A(0)

SLV - **Slave Mode Bit.** When set to "1", the module functions as a slave. When set to "0", the module functions independently. Setting this bit to a "1" overrides the setting of all other bits in the register.

EXT - **External Clock Bit.** When set to "1", the module will use the External Clock Input as a clock source. When set to "0", the module uses the internal, programmable clock source.

S3-S1 - **Clock Select Bits.** These bits are used to select an internal sampling clock rate.

S3	S2	S1	RATE
0	0	0	50 Hz
0	0	1	100 Hz
0	1	0	250 Hz
0	1	1	500 Hz
1	0	0	1 KHz
1	0	1	2.5 KHz
1	1	0	5 KHz
1	1	1	10 KHz

These bits are ignored if the SLV or EXT bits are set.

MASTER/SLAVE OPERATION

The slave bit in the Clock Control Register enables the Model 3115 to function as a slave when chaining two or more modules together. When the slave bit is set, the module samples under the control of its external clock input. All sampling control commands must be directed to the master module.

If the recycle feature is disabled, the slave's LAM circuitry can still be used to indicate that a channel is less than half-full and is ready for more data.

If the recycle feature is enabled, the slave module will respond to an F(9)A(0) command by aborting the recycle mode and setting all its analog outputs to zero volts. The F(24)A(0) command will disable the recycle mode by sampling the remaining FIFO data, provided that the Master Clock is active, to allow the remaining samples to take place. Rewriting data to any channel while the slave is sampling in the recycle mode is restricted.

EXTERNAL CLOCK INPUT

An External Clock Input is provided for sampling at rates other than the selectable frequencies. This clock must be a TTL Level Clock and should not exceed 200 Kilohertz. All analog outputs synchronously update on the high-to-low transition of the clock input signal. This input is also used when chaining of two or more modules is desired. (See section on Master/Slave Operation.)

EXTERNAL CLOCK OUTPUT

The sampling clock is made available at the External Clock Output providing a means of channel expansion. By choosing one Model 3115 as a master, successive modules can be chained together by feeding the clock output of the master to the clock inputs of the preselected slave modules.

STOP TRIGGER INPUT

The Stop Trigger Input provides a means of externally aborting the sampling cycle, leaving the analog outputs at the values last sampled. This input responds to a one microsecond TTL level pulse which is strap selectable allowing pulses to be HIGH- or LOW-TRUE. (See Figure 2) This strap must be in the LOW-TRUE position when the input is not being used.

LAM REQUEST

The Model 3115 LAM Request is used to indicate when a respective channel's FIFO memory has been decremented beyond the half-full point. This provides a means of signaling the host computer to load additional waveform data when generating waveforms consisting of more than 4096 data points. The LAM circuitry consists of a LAM Status Register, LAM Mask Register, and a LAM Request Signal.

The LAM Status Register is a 6-bit Read-Only Register containing a less-than-half-full status bit for each channel. The respective bit will be set to a "1" when the channel's FIFO memory pointer decrements from 2049 to 2048 words. This bit will not be set unless the FIFO memory has been written beyond the half-full position (which is defined as 2049 data words). The respective bits will be reset to "0" following the first Write to the channel's FIFO memory. All bits can be cleared via F(11)A(12) command or by a crate initialization. This register is read by a F(1)A(12) command and returns the data in the following format:

R6					R1	
HF6	HF5	HF4	HF3	HF2	HF1	F(1)A(12)

The LAM Mask Register is a 6-bit Write-Only Register containing a LAM enable bit for each channel. Setting any combination of these bits to "1" will enable the respective channel or channels to generate a LAM request. This register is reset to "0" upon crate initialization and is written with an F(17)A(13) command with data in the following format:

R6					W1	
LE6	LE5	LE4	LE3	LE2	LE1	F(17)A(13)

The LAM Request Signal is generated when both the LAM Mask bit and the corresponding LAM Status bit are set to "1". This condition can be tested with an F(8)A(15) command using Q=1 to indicate the presence of a LAM request.

RECYCLE FEATURE

The recycle feature allows for the retransmission of FIFO data once all data have been read out. This allows the module to generate repetitive waveforms. Although this feature is common to all channels on the module, it is independent of the amount of data in each channel's FIFO, thus allowing varying lengths of waveforms, to the maximum size of 4096 points per channel. After all data have been loaded and a clock rate has been selected, executing an F(26)A(0) command followed by an F(25)A(0) command enables the recycle feature and starts the sampling cycle. The F(24)A(0) command will disable recycling by sampling the remaining FIFO data in each of the active channels, thus completing the current waveform cycle. Recycle is also disabled by an F(9)A(0) command or if any channel is rewritten with new data, simultaneously aborting the sampling cycle and setting the analog outputs to zero volts. When recycle is enabled, the LAM circuitry is disabled.

D/A CALIBRATION

The Model 3115 is strapped and calibrated at the factory for an output range of ± 10 volts. Output ranges of ± 5 volts, ± 2.5 volts, 0 to +10 volts, and 0 to +5 volts can be achieved by repositioning the range straps according to the chart shown below (See Figure 1 for the location of the Option Straps.) All channels need not be strapped the same.

OUTPUT RANGE	STRAP POSITION
0 TO + 5 volts	A, C, E, U
0 to +10 volts	A, E, U
± 2.5 volts	B, E, F, B
± 5 volts	B, E, B
± 10 volts	B, D, B

If field calibration is required, offset and gain controls are provided for each D/A converter (See Figure 2) The offset potentiometer adjusts the unit for unipolar zero or bipolar, negative full-scale outputs, and the gain potentiometer adjusts the unipolar and bipolar positive full-scale outputs.

To perform calibration, initialize the Model 3115 with a crate Z cycle. Executing an F(25)A(0) command will put the Model 3115 in a continuous sampling state and allow the selected D/A analog output to update upon being written. Calibration is as follows:

OFFSET ADJUSTMENT

Write the offset data to the channel being calibrated and adjust the offset potentiometer to the analog output level according to the selected operating range shown below:

OUTPUT RANGE	OFFSET DATA	OUTPUT LEVEL
0 to + 5 volts	000 H	0.0000 volts
0 to +10 volts	000 H	0.0000 volts
± 2.5 volts	800 H	-2.5000 volts
± 5 volts	800 H	-5.0000 volts
± 10 volts	800 H	-10.0000 volts

GAIN ADJUSTMENT

OUTPUT RANGE	GAIN DATA	OUTPUT LEVEL
0 to + 5 volts	FFF H	+4.9988 volts
0 to +10 volts	FFF H	+9.9976 volts
± 2.5 volts	7FF H	+2.4988 volts
± 5 volts	7FF H	+4.9976 volts
± 10 volts	7FF H	+9.9951 volts

NOTE: Changes in the gain adjustment may affect the offset; therefore, it is advisable to repeat the calibration procedure.

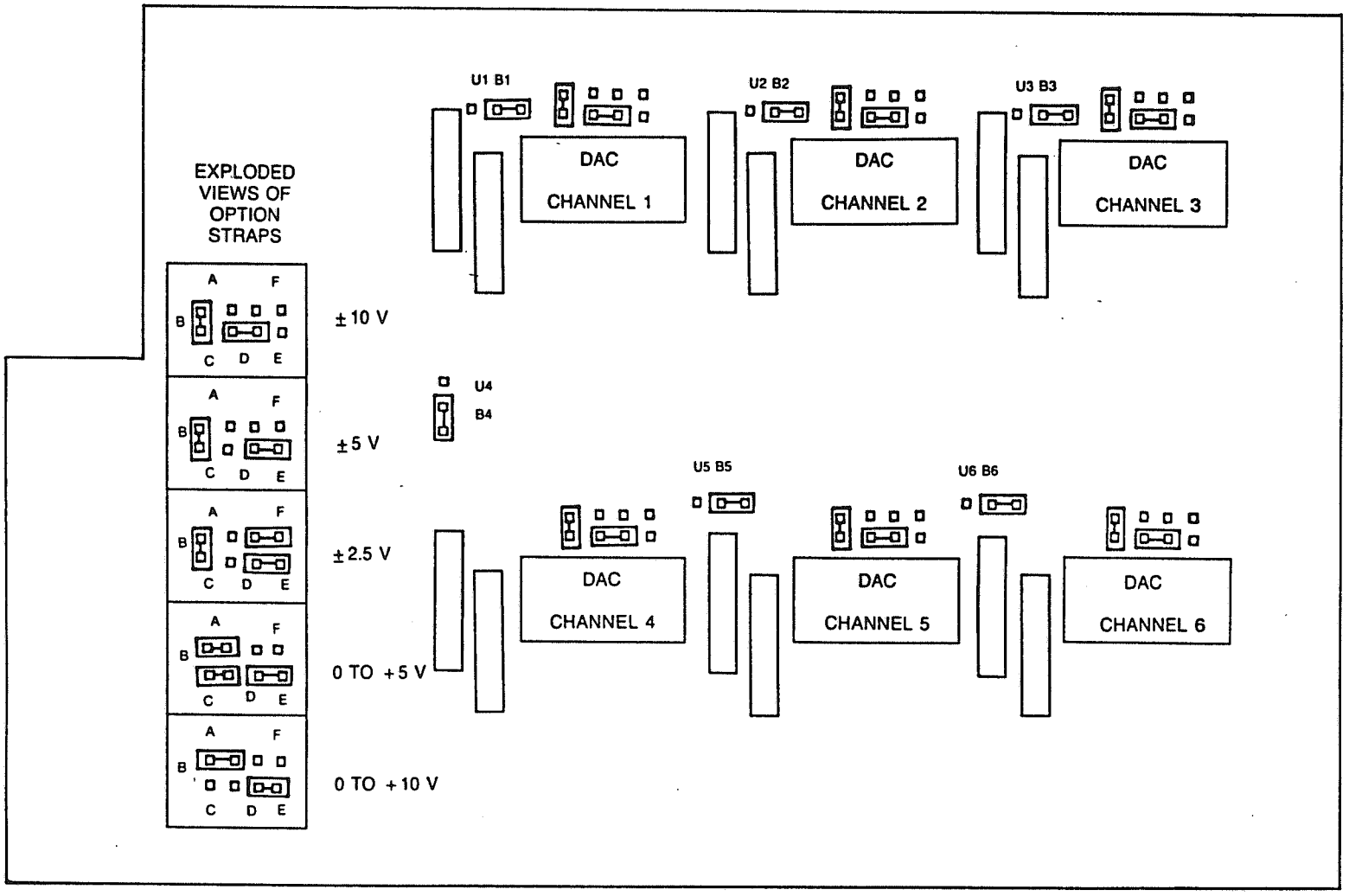


FIGURE 1 - RANGE STRAPS

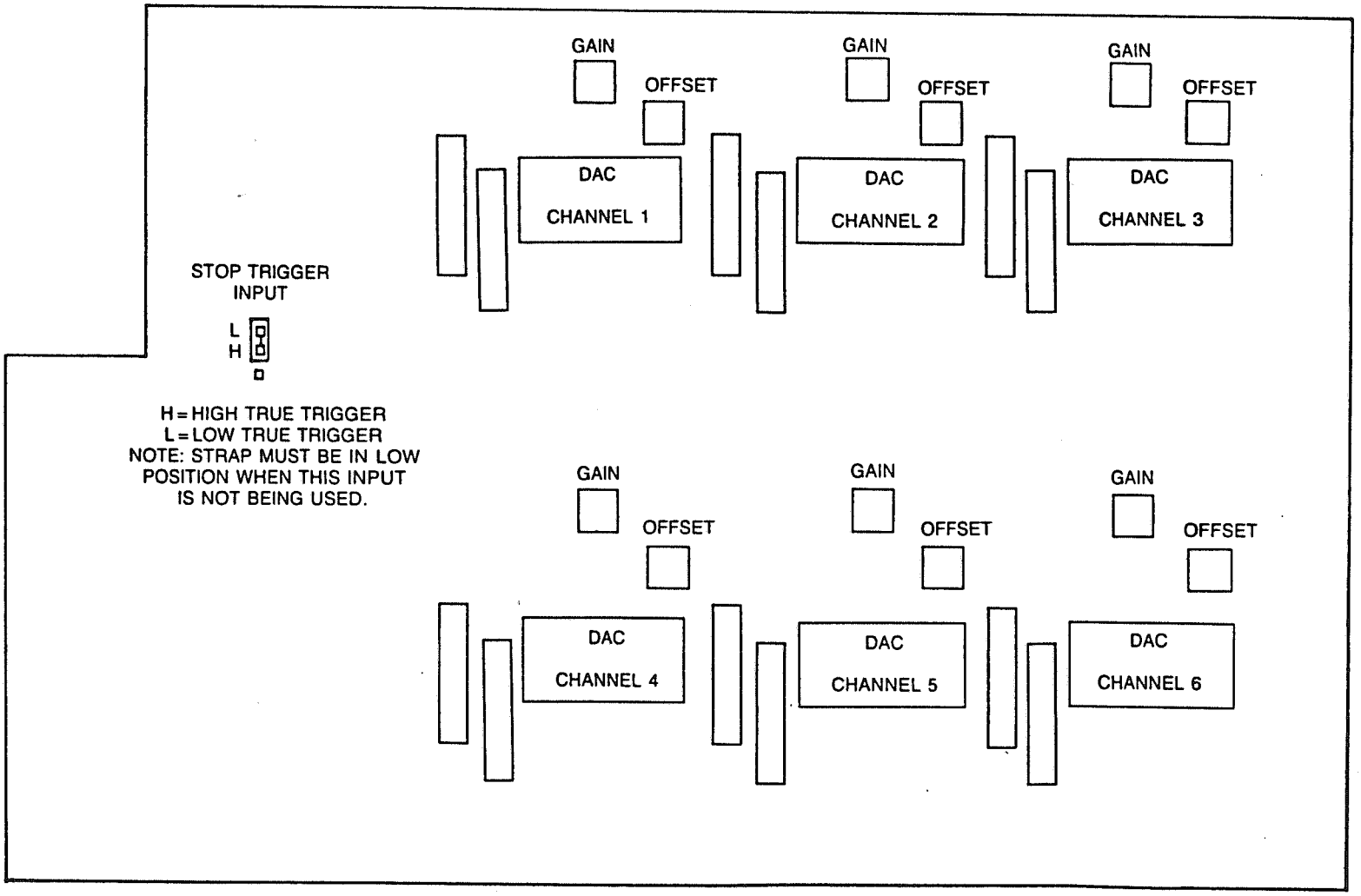


FIGURE 2 - OFFSET/GAIN CONTROLS