Model 3196-Z1A

16-Channel, 16-Bit Multiplying
DAC Attenuator

INSTRUCTION MANUAL

November, 1995

CONTENTS

16-channel, 16-bit Multiplying DAC

Provides digitally controlled attenuation with 16-bit resolution

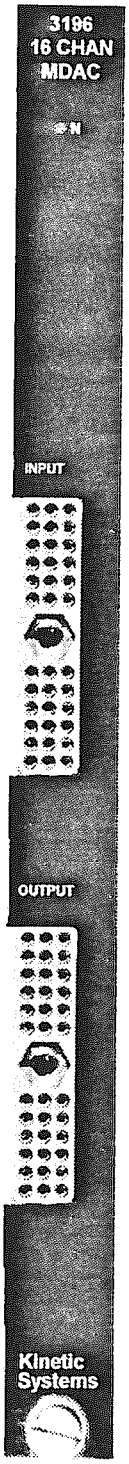
3196

Features

- **16 channels of 16-bit multiplying digital-to-analog converters**
- **Excellent gain stability**
- **Full four-quadrant multiplication**
- **16-bit resolution of digitally controlled gain from -1 to +1**
- **Channel-by-channel programmable pre-gain (1 or 100)**
- **Independent differential inputs for each channel**
- **Input and output full-scale range of ±10 V**

Typical Applications

- **Magnetic modeling**
- **Applications requiring precision computer control of signal attenuation**



General Description

The 3196 is a single-width CAMAC module that functions as a programmable digital attenuator for 16 differentially-received analog inputs. Each channel contains a four-quadrant, multiplying digital-to-analog converter that provides 16-bit (one part in 65,536) resolution in gain from -1 to +1. In addition, a channel-by-channel programmable pre-gain of 100 may be selected.

The data for channels 1 through 16 are written as 16-bit 2's complement words using function codes F(16)·A(0) through F(16)·A(15), respectively. On power-up or in response to an Initialize command, the MDACs are cleared to provide a nominal gain of zero. Two 36-contact AMP front-panel connectors are provided, one for the input signals and one for the output signals. For maximum noise immunity, twisted pair cables should be used for both inputs and outputs. Individual shields or common shields for each connector are acceptable.

A front panel "N" LED indicates when the module is addressed.

Function Codes

Command		Q	Action
F(0)·A(0)	RD1	RDY	Reads the last data word sent by an F(16) command (Note 1)
F(1)·A(0)	RD2	1	Reads the 16-bit Pre-gain register for all channels. Bit "x"=1 indicates a gain of 100 on Chan. "x"
F(16)·A(i)	WT1	RDY	Writes the Gain Multiplier data for channel i+1 (Notes 2, 3)
F(17)·A(0)	WT2	1	Writes the Pre-gain Register for all channels. Bit "x"=1 indicates a gain of 100 on Chan. "x."
F(27)·A(0)	TST	RDY	Tests (through the "Q" response) if the module is ready for further commands
Z·S2	CZ	0	Clears the DAC data (0 x Vin for all channels) and clears the Pre-gain register

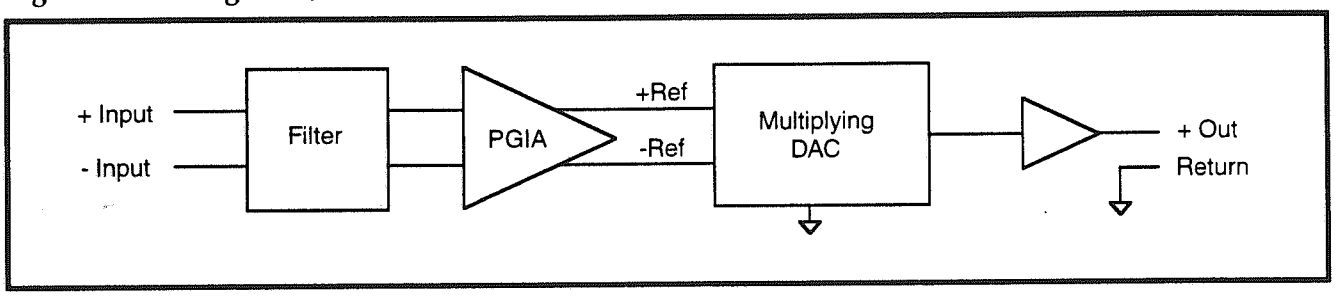
Notes:
1. This command is only operational when the /TST strap is removed (for factory diagnostic purposes only).
2. Channels 1 to 16 correspond to i = 0 to 15.
3. This command requires approximately 5 us to execute and produces a Not Ready (/RDY) condition until it is completed.

Signals and Connectors

J1 Differential analog channel inputs (ESD and overvoltage protected)
Up to ±10 volt signal range (depending on setting of channel gain)
Connector type: 36-socket rectangular AMP connector

J2 Differential analog channel outputs
Up to ±10 volt signal range
Connector type: 36-socket rectangular AMP connector

Signal Flow Diagram (one channel shown)



Specifications

Item	Specification
Number of inputs	16
Type of input	Differential
Input impedance	10^{10} Ω ll 35 pF minimum
Full-scale input range	+10 V @ unity gain, +0.1 V @ pre-gain of 100
Full-scale output range	±10 V
Output current capability	40 mA maximum over full-scale voltage range
Resolution	16 bits
Missing codes	None
Programmable pre-gain	1 or 100 +0.025%
Pre-gain change settling time	140 µs to 0.01%
Offset drift error	±0.4 + 3/G µV/°C typical
Common-mode rejection ratio	100 dB typical, 0 to 60 Hz
Effective bandwidth (-3 dB)	4 kHz

Power Requirements

+6 volts: 835 mA
+24 volts: 220 mA + load current
-24 volts: 190 mA + load current

Ordering Information

Model 3196-Z1A Multiplying DAC, 16 channels, 16 bits

Related Products

Model 5944-Z1A 36-pin AMP Rectangular Mating Connector
Model 1865-Z1A Rack-mount Termination Panel
Model 5855-Bxyz 50-socket Ribbon to 36-pin AMP Rectangular Connector Cable

3196 STRAP OPTIONS

There is only one strap option on the Model 3196. This **/TST** strap is only to be removed for in-factory testing and should ALWAYS remain in place during normal module use. Its removal allows the Attenuation Multiplier words written by F(16)A(I) commands to be read back by an F(0)A(0) command for testing of the digital pathways. When the strap is in the normal "in place" position, the F(0)A(0) command is invalid and not accepted; that is, a "No X" and "No Q" response will be returned.

REGISTERS

Pre-Gain: The F(1)A(0) and F(17)A(0) CAMAC commands are used to read and write, respectively, the Pre-Gain register. Each bit (1–LSB through 16–MSB) of this register corresponds to a pre-gain selection for each channel (channel 1 through 16) of the module. Specifically, a value of binary "0" on bit "x" produces a pre-gain of unity on channel "x". A value of binary "1" produces a pre-gain of 100.

Attenuation Control: These are the sixteen 16-bit registers–one for each multiplying Digital-to-Analog Converter (DAC)–which hold the Attenuation Multiplier data for the channels. They are written with F(16)A(I) commands where "I" (ranging from 0 through 15) corresponds to channel "I+1". These registers are NOT normally readable except under factory-test conditions (see the 3196 STRAP OPTIONS section above).

INITIALIZATION

Performing a CAMAC "Z" operation will properly initialize all CAMAC functionality on the Model 3196 module to the power-up state. This entails setting all pre-gains to unity gain and setting all DAC output voltages to 0V. (Attenuator Multipliers are set to zero).

SIGNAL CONNECTION

The channel inputs on the front panel "IN" (J1), 36-socket, AMP rectangular connector are received in true differential fashion with no connection to the module's circuit ground. Consequently, any external source connected to these inputs should include a ground reference to ensure that the incoming signals will occupy the valid common-mode range of the receiving devices. Sockets C9 through C12 of the "IN" (and "OUT") front panel connector is internally connected to digital ground. If a separate mid-scale reference does not exist at the input source for connection to these module ground points, the return (–) sides of the input pairs should be connected to these points in some form. Although proper grounding is sometimes considered a "black art", you may find comfort (even bona fide help) in a technical note, TN-107, written by KSC's Robert Cleary entitled "Driving Balanced Analog Inputs From Unbalanced Sources".

Pinout maps for the channel inputs and outputs on the front panel connectors are presented in tables at the end of this document for easy reference.

OPERATION

This module performs two separate and independent gain operations on each of 16 channel inputs. The pre-gain setting (x1 or x100) is intended as a static range control. In conjunction with the multiplying DAC (programmable attenuation) control, pre-gains of x100 allow overall greater-or-less-than-unity gain for low-level input signals (<10 mV).

Programmable attenuation is accomplished by writing Attenuation Multiplier data to the 3196 DACs. This data occupies a 16-bit field in a 2's complement format. Positive full-scale (gain of +1) is represented by $7FFF_{16}$ (+32767) and negative full-scale (gain of –1) is 8000_{16} (–32768). Consequently, the formula for overall gain or attenuation through the a channel of the 3196 in decimal is:

$$\text{Analog Out} = (\text{Analog In}) \cdot (\text{Pre-Gain}) \cdot (\text{Attenuation Multiplier}) / 32768$$

A typical programming sequence involves the following simple steps:

1) F(17)A(0) Write the Pre-Gain settings DATA= 16 bits

This command loads the Pre-Gain register and is formatted such that bits 1(LSB) through 16 (MSB) correspond to the pre-gain settings for channels 1 through 16, respectively. Specifically, bit "x"=1 indicates a pre-gain setting of 100 on channel "x"; bit "x"=0 indicates a pre-gain setting of unity for channel "x". One should determine beforehand which pre-gain level is appropriate for each channel of interest, construct the 16-bit data pattern, and then write it to the Model 3196 with the F(17)A(0) command. Since the Pre-Gain register is cleared on power-up or under a Crate "Z" command, this step may be omitted if all channels of interest are to have pre-gain settings of unity. However, it is good programming practice to initialize ALL registers which affect important parameters rather than rely on defaults.

NOTE: There is nothing to preclude a user from changing individual pre-gain settings later (during data-taking, for example), but remember that ALL channel pre-gains are rewritten with each F(17)A(0) command. One must either retain a copy of the register contents in a host memory location or, alternatively, read back the Pre-Gain register (with the F(1)A(0) command) to use as a mask in order to avoid disturbing the pre-gain settings of other channels.

2) F(16)A(I) Write the Attenuation Multiplier for channel "I+1"– $I \in \{0,\ldots,15\}$ DATA = 16 bits

This command enters the desired Attenuation Multiplier into the DAC for the selected channel. The selected channel is distinguished by the value of the "A" subaddress in the command. Specifically, subaddress "I" (where "I" ranges from 0 to 15) refers to channel "I+1". Attenuation Multiplier data to the 3196 DACs occupies a 16-bit field in a 2's complement format. Thus, positive full-scale (gain of +1) is represented by $7FFF_{16}$ (+32767) and negative full-scale (gain of –1) is 8000_{16} (–32768). Consequently, the formula for attenuation through the DACs in decimal is:

$$\text{ATTENUATION FACTOR} = (\text{Attenuation Multiplier}) / 32768$$

3) F(27)A(0) loop until "Q" is true

The F(16) command cited above may take longer to complete *(approximately 5 μs)* than the speed at which back-to-back CAMAC operations may be performed. Consequently, it produces an internal time-out, /RDY, which will cause a "No Q" response in subsequent affected commands until the time-out has expired. A "Q-Repeat" CAMAC operation or a software construct of "loop until Q" may be used to guarantee a valid subsequent command. Alternatively, an F(27)A(0) command tests for RDY through its "Q" response and, thus, a loop which simply tests for a true "Q" response to this command may be invoked before any RDY-sensitive command is issued.

4) Repeat Steps 2 and 3 above for any channels in any order until all desired operations are complete.

3196 "IN" (J1) CONNECTOR CONNECTION MAP

SKT #	SIGNAL	SKT #	SIGNAL	SKT #	SIGNAL
A1	CHANNEL 1 +	B1	CHANNEL 7 +	C1	CHANNEL 13 +
A2	CHANNEL 1 -	B2	CHANNEL 7 -	C2	CHANNEL 13 -
A3	CHANNEL 2 +	B3	CHANNEL 8 +	C3	CHANNEL 14 +
A4	CHANNEL 2 -	B4	CHANNEL 8 -	C4	CHANNEL 14 -
A5	CHANNEL 3 +	B5	CHANNEL 9 +	C5	CHANNEL 15 +
A6	CHANNEL 3 -	B6	CHANNEL 9 -	C6	CHANNEL 15 -
A7	CHANNEL 4 +	B7	CHANNEL 10 +	C7	CHANNEL 16 +
A8	CHANNEL 4 -	B8	CHANNEL 10 -	C8	CHANNEL 16 -
A9	CHANNEL 5 +	B9	CHANNEL 11 +	C9	DIG GROUND
A10	CHANNEL 5 -	B10	CHANNEL 11 -	C10	DIG GROUND
A11	CHANNEL 6 +	B11	CHANNEL 12 +	C11	DIG GROUND
A12	CHANNEL 6 -	B12	CHANNEL 12 -	C12	DIG GROUND

Front Panel View

A1	B1	C1
A2	B2	C2
A3	B3	C3
A4	B4	C4
A5	B5	C5
A6	B6	C6
A7	B7	C7
A8	B8	C8
A9	B9	C9
A10	B10	C10
A11	B11	C11
A12	B12	C12

3196 "OUT" (J2) CONNECTOR CONNECTION MAP

SKT #	SIGNAL	SKT #	SIGNAL	SKT #	SIGNAL
A1	CHANNEL 1 +	B1	CHANNEL 7 +	C1	CHANNEL 13 +
A2	CHANNEL 1 -	B2	CHANNEL 7 -	C2	CHANNEL 13 -
A3	CHANNEL 2 +	B3	CHANNEL 8 +	C3	CHANNEL 14 +
A4	CHANNEL 2 -	B4	CHANNEL 8 -	C4	CHANNEL 14 -
A5	CHANNEL 3 +	B5	CHANNEL 9 +	C5	CHANNEL 15 +
A6	CHANNEL 3 -	B6	CHANNEL 9 -	C6	CHANNEL 15 -
A7	CHANNEL 4 +	B7	CHANNEL 10 +	C7	CHANNEL 16 +
A8	CHANNEL 4 -	B8	CHANNEL 10 -	C8	CHANNEL 16 -
A9	CHANNEL 5 +	B9	CHANNEL 11 +	C9	DIG GROUND
A10	CHANNEL 5 -	B10	CHANNEL 11 -	C10	DIG GROUND
A11	CHANNEL 6 +	B11	CHANNEL 12 +	C11	DIG GROUND
A12	CHANNEL 6 -	B12	CHANNEL 12 -	C12	DIG GROUND

Front Panel View

A1	B1	C1
A2	B2	C2
A3	B3	C3
A4	B4	C4
A5	B5	C5
A6	B6	C6
A7	B7	C7
A8	B8	C8
A9	B9	C9
A10	B10	C10
A11	B11	C11
A12	B12	C12