Model 3310

2-channel, ARINC-429 Aircraft
Bus Interface

INSTRUCTION MANUAL

May, 1992

2-channel ARINC-429 Aircraft Bus Interface

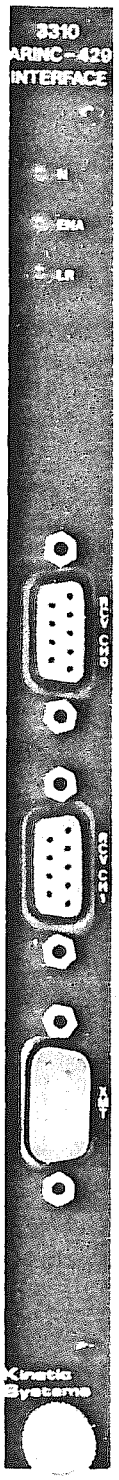
Interfaces with the ARINC-429 commercial aircraft bus **3310**

Features

- **Two ARINC-429 receive channels and one transmit channel**
- **Selection of transmit/receive data rates**
- **A computer-selectable list memory for each receiver channel to read only**
- **Retransmission of FIFO data**

Typical Applications

- **Avionics subsystem development and testing**
- **Aircraft engine testing**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 3310 is a single-width CAMAC module that provides the interface for one transmitter and two receiver channels that are compatible with the ARINC-429 Aircraft Data Bus (Mark 33 Digital Information Transfer System). ARINC-429 is the primary bus standard for modern civil air transports (such as the Boeing 747). A channel of this system, as specified by Aeronautical Radio, Inc., covers the transmission of avionics information in a digital format. Information is sent from a designated output port over a single shielded and twisted pair of wires to all other system elements having need for that information. Bidirectional data flow on a given twisted pair is not permitted. Transmission is made "open loop" (i.e., receiver channels are not required to inform transmitter channels that information has been received).

Detailed Information

Each transmit and receive channel is completely independent. The channel data rate can be set to 12.5 kilobits/second. The transmit channel includes a FIFO, and each receive channel includes a 256 x 32 RAM memory so that data can be efficiently written and read via the CAMAC Dataway. DMA block transfers can be used, if desired.

The transmitter output rate can be selected to be from one millisecond to 2.048 seconds in a binary increment (..., 128 mS, 256 mS, ...). Each ARINC message is generated by two CAMAC 16-bit Write operations. If the transmit FIFO is written at a rate slower than the one selected, a message is transmitted at the first "tic" following the availability of data. If a data Write operation is attempted when the transmit FIFO is full, the data is not written, and a Q = 0 response is given. For test purposes, the data at the "bottom" of the FIFO can be repeated at the selected rate.

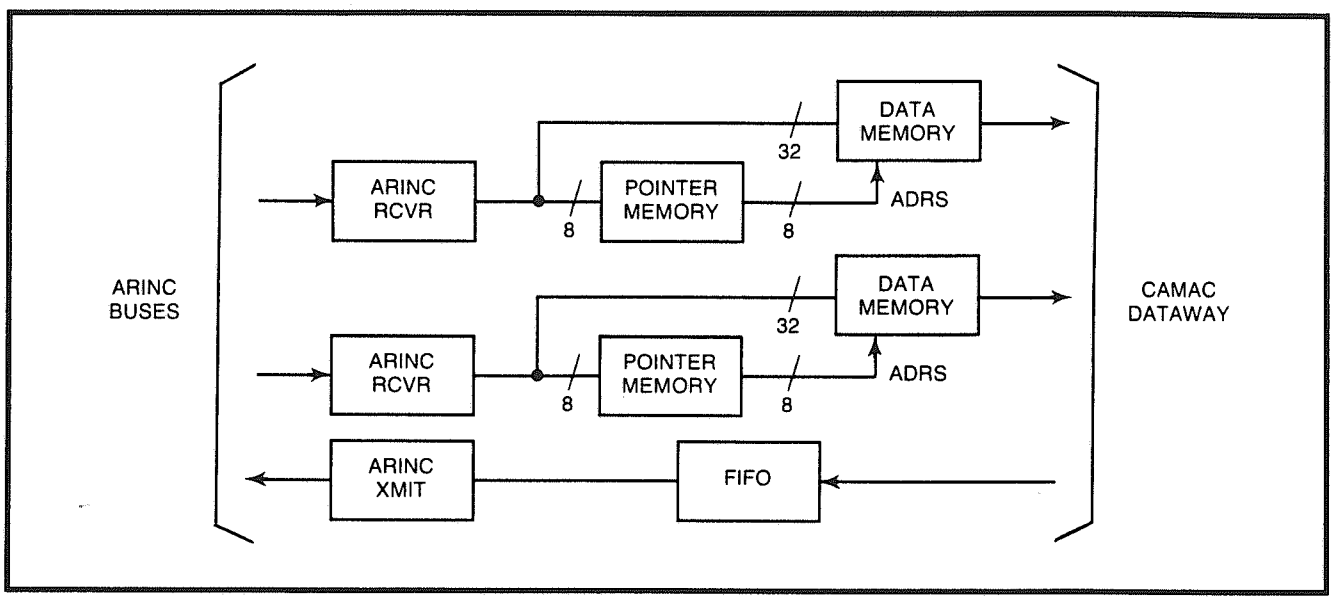
For many applications, reading all messages on a channel will result in the storage of more data than necessary. The 3310 contains a list memory for each channel which selects desired data labels to be read (from the 256 possible combinations). The "list" for each channel is a 256 x 9 memory that can be written from the Dataway. Data associated with a label will be the "last received" ARINC word, even if there has not been another word associated with that label received since the last CAMAC Read operation.

For test purposes, transmit and receive channels can be "looped-back" under computer control. This allows testing of the module regardless of the external environment.

Connections to the ARINC-429 Bus are made through three 9-pin "D" type connectors mounted on the front panel of the module. The receive channels are socket connectors and the transmit channel is a pin connector.

3310 *(continued)*

Simplified Block Diagram



Function Codes

Command		Q	Action
F(0)·A(i)	RD1	1	Reads ARINC-429 half words from Channel i.
F(1)·A(0)	RD2	1	Reads the protocol management control word.
F(1)·A(12)	RD2	1	Reads the LAM Status register.
F(1)·A(13)	RD2	1	Reads the LAM Mask register.
F(1)·A(14)	RD2	1	Reads the LAM Request register.
F(8)·A(15)	TLM	LAM	Tests for a LAM Request.
F(9)·A(0)	CL1	1	Disables the module, clears memories and LAMs.
F(11)·A(i)	CL2	1	Resets the memory pointer for Channel i.
F(16)·A(0)	WT1	FNF	Writes ARINC-429 half words to the XMIT FIFO.
F(16)·A(1)	WT1	IDL	Writes the protocol management control word.
F(17)·A(i)	WT2	1	Writes the Memory Address for Channel i.
F(17)·A(i + 2)	WT2	IDL	Writes the pointer address for Channel i.
F(17)·A(13)	WT2	1	Writes the LAM Mask register.
F(18)·A(i)	SS1	IDL	Writes the memory pointer for Channel i.
F(23)·A(12)	SC2	1	Selectively clears LAM status bits.
F(24)·A(0)	DIS	1	Disables ARINC-429 activity in the module.
F(25)·A(0)	XEQ	1	Retransmits the contents of the XMIT FIFO.
F(26)·A(0)	ENB	1	Enables ARINC-429 activity in the module.
F(27)·A(0)	TST	BSY	Tests the ARINC-429 state of the module.
F(27)·A(1)	TST	CLR	Tests for completion of clear operation.
Z·S2			Initializes the module and clears memory.

Notes:
1. X = 1 for all valid addressed commands.
2. i can range from 0 to 1 (Channels 1 and 2).
3. FNF = Transmit FIFO memory not full.
4. IDL = Module is idle (ARINC-429 ports inactive).
5. BSY = Module is busy (ARINC-429 ports active).
6. CLR = RAM Clear operation complete.
7. The Z and F(9) commands initiate a memory clear sequence that requires 170 microseconds to complete.

Ordering Information

Model 3310-B1A ARINC-429 Aircraft Bus Interface, 2 channels

Power Requirements

+6 volts: 2100 mA

Related Products

Model 5856-Axyz or Bxyz-Series Cable Assemblies

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SCK:rem (WP 3310.man)

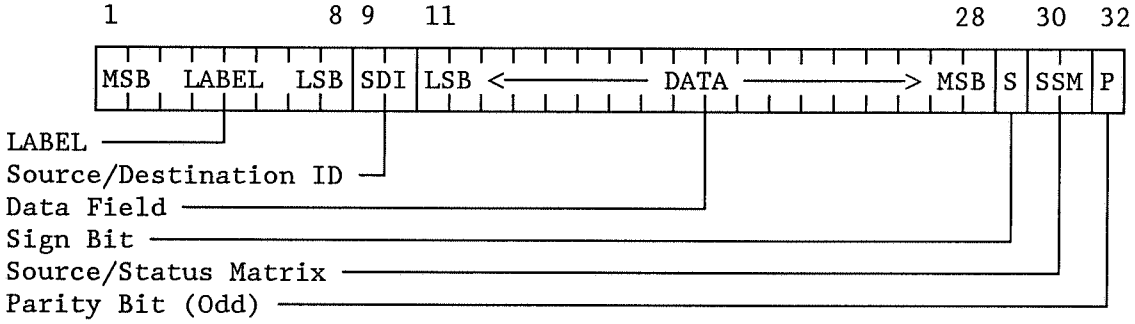
OVERVIEW

The Model 3310 is capable of transmitting and receiving single-word messages (discrete, two's complement BNR, and BCD data per the numerical subset of ISO Alphabet No. 5) over the ARINC-429 bus. Multi-word messages containing AIM data (Acknowledgement, ISO Alphabet No. 5 and Maintenance information encoded in dedicated words) or file transfers are not supported.

The bulk of the ARINC-429 protocol management is performed by a Harris HS-3282 Bus Interface Circuit. This chip will accommodate both the high speed (100 Kbps) and the slow speed (12.5 Kbps) transmission rates, and the long (32-bit) and short (25-bit) message formats specified by the ARINC-429 standard. The 32-bit word formats for both the bit-serial ARINC-429 output and the 16-bit parallel I/O ports are shown below. For the 25-bit word format, the SDI, Sign and Sign/Status Matrix fields are eliminated, and the size of the Data field is reduced to 16 bits; the upper seven bits of Word 1 of the HS-3282 parallel I/O are not used.

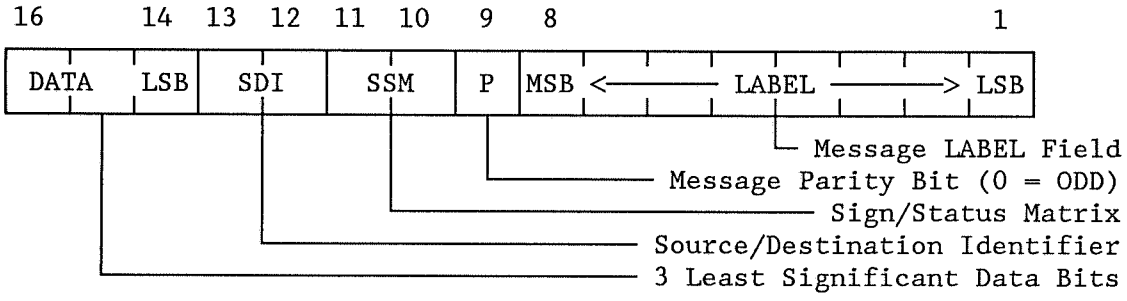
WORD FORMATS

ARINC-429 FORMAT

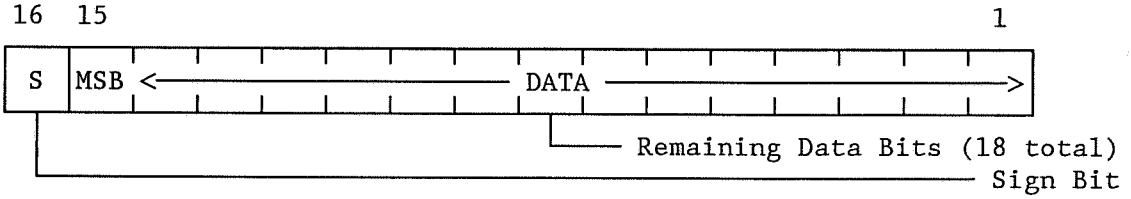


HS-3282 FORMATS

WORD 1



WORD 2



Note that, for the bit serial ARINC-429 word, the most significant bit of the LABEL field (bit 1) is the first bit transmitted or received and the parity bit (bit 32) is the last bit transmitted or received. On the parallel port side, bit position 1 is the LSB, and bit position 16 contains the most significant bit of the word. Single word ARINC messages written to [F(16) A(0)] or read from [F(0) A(0)] the 3310 must be accomplished with two 16-bit CAMAC transfers as shown above, with Word 1 being written or read first, and Word 2 last.

RECEIVER OPERATION

The HS-3282 is capable of receiving ARINC-429 messages from two separate and distinct buses, facilitated by two sets of receiver circuitry within the chip. On the CAMAC side of the chip, duplicate circuitry handles messages from either port. For simplicity sake, only a single port's receiver is described.

Received ARINC-429 messages are stored in a 256-word, 32-bit wide Static RAM array. Since the data bus for this array is used both to load data into RAM and to read messages out to the Dataway, the entire 32-bit wide message is transferred at once. This avoids the situation where a message readout over the Dataway contains half old data and half new data (i.e., the same memory location was in the process of being updated while being read). In response to the assertion of the D/R (Device Ready) flag on the HS-3282, data is gated out (via the EN and SEL lines) to a pair of 16-bit wide registers. Both registers together are then clocked into the storage memory as a 32-bit quantity.

The location in the memory where the messages are stored is determined by the combination of a pointer array and the contents of the message's LABEL field. As the message is transferred to the holding register, the LABEL field is applied to the address lines of a 256 X 9 RAM memory. The lower eight bits of the pointer contents are then used as the address at which the message is stored in the buffer memory. Using this scheme, the user can determine where in the memory array the incoming messages can be stored. Usually, memory allocation would be prioritized such that messages of most interest would be loaded at the front of memory (low order addresses), so that a DMA-type Block Transfer read could most expeditiously retrieve those messages. Optionally, a dedicated location in memory could be designated as a "garbage" location, to collect unwanted messages. The ninth bit of this pointer array (the MSB) can be used to set a LAM source any time a message or messages with a label of interest is received.

The address register for the pointer memory is loaded with an F(17) A(i+2) command, and the memory itself is written with an F(18) A(i) command. The pointer memory address is incremented at S2 time of the F(18) command. The buffer memory containing message data can be read using a Q-Stop type Block Transfer. The 8-bit address register is loaded with an F(17) A(i) command, and the memory itself is read with F(0) A(i) command. Note that two CAMAC read cycles [F(0) A(i) commands] are required to retrieve an entire ARINC-429 message. Word 1 and Word 2 of the message appear on the Dataway as described on by the Word Format section. The memory address is automatically incremented at S2 time of the first F(0) A(i) command, allowing a pre-fetch from memory of the next message word to occur at S2 time of the second F(0) A(i) command. The F(11) A(i) command may be used to reposition the address register so that it

points to location 0. A pre-fetch of the first memory location occurs automatically at S2 time of both the F(17) A(i) and F(11) A(i) commands. Storage memory pre-fetches are also done in response to RAM clear operations. RAM clear operations include power-up, a CAMAC Initialize (Z) cycle, and a F(9) A(0) command. Thus, if a message is received after a RAM clear operation and ARINC activity has been enabled in the 3310, and Storage RAM address location 0 is to contain the message, the first ARINC word readout results in a message containing all zeros. So, if it desired to read all 256 current ARINC messages after a RAM clear operation, the user must execute either an F(11) A(i) or F(17) A(i) command which will do a pre-fetch of the current messages.

TRANSMITTER OPERATION

Messages that are to be transmitted over the ARINC-429 bus are stored in a 512-word deep FIFO. This permits the FIFO to contain up to 256 ARINC messages. Since the transmit FIFO is only 16-bits wide, two successive FIFO load operations are necessary to place each 32-bit (or 25-bit) message into the FIFO. Message halves are loaded into the FIFO with the F(16) A(0) command in the order shown under the Word Format section of this manual; WORD1 and then WORD2. A Q = 1 is generated for this command as long as the FIFO is not full. If the FIFO is full and the write command is executed, a Q = 0 response is obtained and the command is ignored.

Once the 3310 is enabled for ARINC activity, the transmission of messages begins when the transmission rate timer expires. The transmission rate timer controls the rate at which messages are sent out over the ARINC bus. There are 4 bits in the protocol management control word for specifying the transmission rate. These rates range from one millisecond to 1.024 seconds in a binary increment (..,128mS, 256mS,...). Once the timer expires, two 16-bit words are read from the FIFO and stored in the ARINC interface chip. After the two data words are stored, the ARINC interface chip is enabled for message transmission. Subsequent messages are not transmitted until the transmission rate timer expires. This sequence continues as long as the module is enabled for ARINC activity and there is transmit data words in the FIFO. Should only the first half of the message be in the FIFO when the transmission rate timer expires (i.e., the FIFO goes empty after reading the first word), the transmitter is not enabled until the next transmission rate timer expiration, providing that the rest of the message has been loaded into the FIFO.

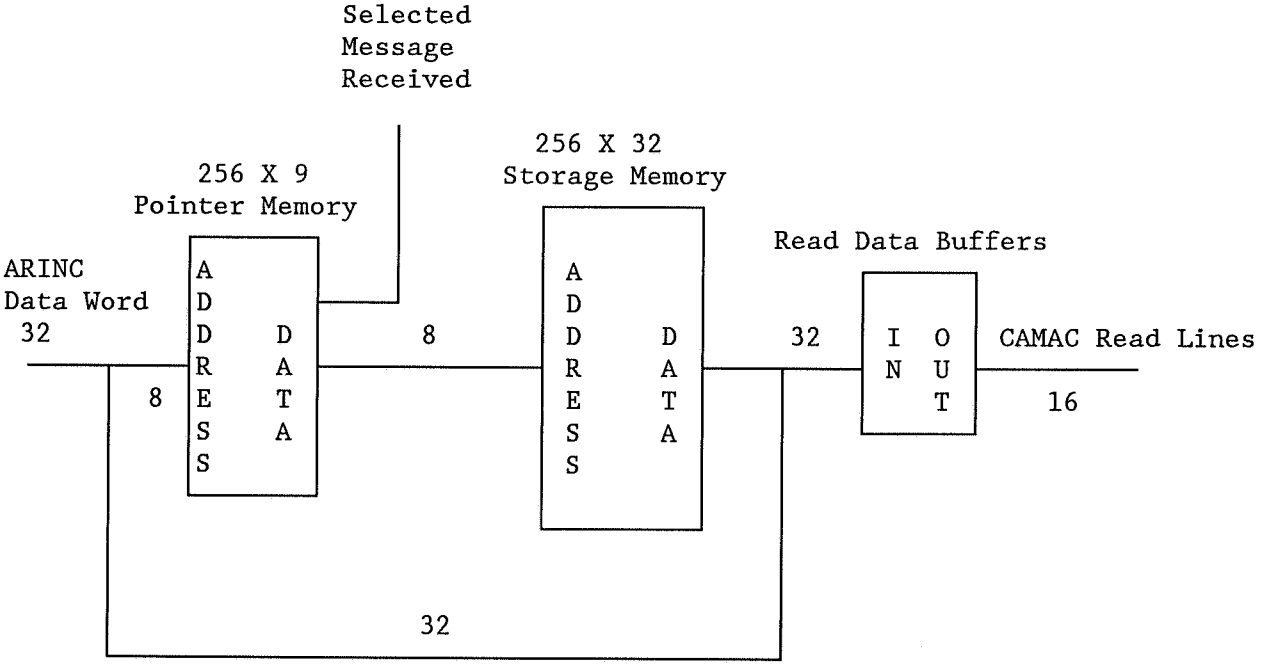
A message re-transmit option is also available for generating repetitive messages. This option may only be used after the initial transmission of the FIFO's contents. After the FIFO has been emptied, the re-transmit command, F(25) A(0), may then be executed. This causes the FIFO's internal read pointer to be reset to the beginning of the data list. Once the pointer has been reset, the transmission proceeds as described above.

ARINC ACTIVITY

The 3310 will not transmit or receive any ARINC messages unless it is enabled to do so. ARINC activity within the 3310 is enabled by a F(26) A(0) command and disabled by a F(24) A(0) command. Optionally, ARINC activity may be enabled by a F(25) A(0) command, which also re-transmits the contents of the transmit data FIFO. Refer to the Transmitter Operation section of this manual for further information regarding the Re-Transmit feature.

MESSAGE POINTER MEMORY

The Pointer Memory is a 256 X 9 static RAM which is used for specifying the message storage address within the 256 X 32 Storage RAM. When an ARINC message is received, the LABEL field of the message is applied to the address inputs of the Pointer Memory. The addressed location of the Pointer Memory is read to determine the address of the Storage RAM where the entire ARINC message is to be stored. The following is a simplified block diagram of the message storage technique.



Along with providing the message mapping protocol, the Pointer Memory also allows for the generation of a LAM source. Each entry in the Pointer Memory contains a bit for enabling the LAM source. When a message is received and the Pointer Memory is read, the ninth bit is checked to see if a LAM source is to be generated. If the bit is set a LAM source is asserted. After the message is stored, the Selected Message Received (SMR) bit is set. The LAM Status Register may then be read to determine which channel generated the source.

The Pointer Memory is written with a F(17) A(i+2) command (i=0 for channel 0 and 1 for channel 1). Once ARINC activity is enabled within the module, these commands are ignored and return a Q=0 response. The format of the Pointer Memory data entries are shown below.

9	8	7	6	5	4	3	2	1
SMR	A7	A6	A5	A4	A3	A2	A1	A0

POINTER MEMORY ADDRESS

The Pointer Memory Address register is used for specifying the address at which subsequent Pointer Memory load operations are to occur. Before loading the Pointer Memory, the address must first be specified. The Pointer Memory Address is written with a F(17) A(i+2) command. The Pointer Memory Address is automatically incremented at S2 time of each F(18) A(i) command. This facilitates loading the Pointer Memory since it is not necessary to reload the address register for each entry. Once ARINC activity is enabled, the Pointer Memory Address load operations are ignored and a Q=0 response is returned. The format of the Pointer Memory Address register is shown below.

8	7	6	5	4	3	2	1
A7	A6	A5	A4	A3	A2	A1	A0

STORAGE MEMORY ADDRESS

The Storage Memory Address register is used for specifying the address at which subsequent F(0) A(i) commands are executed. Two CAMAC commands are available for changing the Storage Memory Address. The F(17) A(i) command loads the Storage Memory Address. The F(11) A(i) command reset the Storage Memory Address to zero. After the execution of either of these commands, a Storage Memory pre-fetch operation is preformed. The format of the Storage Memory Address register is shown below.

8	7	6	5	4	3	2	1
A7	A6	A5	A4	A3	A2	A1	A0

MEMORY CLEAR OPERATIONS

All locations within both the Pointer Memory and Storage Memory can be cleared by several means. Clearing the RAM refers to writing zeros to all locations in the memory. The memories are cleared by the following:

a.) Power-up cycle
b.) CAMAC Initialize (Z) operation
c.) F(9) A(0) command

The clear operation takes approximately 170 microseconds. A test command to the 3310 is used to verify that the clear operation is complete. The test command is a F(27) A(1). If a Q=0 response is returned, the RAM clear operation is still in progress. A Q=1 response confirms the completion of the operation.

After the RAM clear operation has completed, the Pointer Address register and Storage Address register are cleared. Once the addresses are cleared, a pre-fetch of Storage Address location zero is performed. This actually leaves the Storage Address register pointing to Storage RAM location 1, but a read of the Storage RAM [F(0) A(i)] results in the first ARINC message set to all zeros.

PROTOCOL MANAGEMENT CONTROL WORD

Interfacing to the ARINC-429 bus is provided by the Harris HS-3282 interface chip. The clock source for the interface chip is a one Megahertz crystal controlled oscillator. The setting of the Control Word in the module determines the overall operating characteristics of the ARINC interface. The Control Word is written with a F(16) A(1) command and read by a F(1) A(0) command. Once ARINC activity has been enabled in the module, the user is prevented from loading the Control Word. A Q=0 response is received for the F(16) A(1) command if the module is enabled for ARINC activity.

Bits 15 through 5 of the Control Word are contained in the HS-3282 interface chip and control the following characteristics :

a.) ARINC Word Length
b.) Receiver Data Rate
c.) Transmitter Data Rate
d.) Parity
e.) Message Compare Field
f.) Self-Test Mode

Bits 4 through 1 control the rate at which messages are sent out over the ARINC bus. Note that this rate does not control the ARINC data bit-rate, but rather controls the rate at which ARINC messages are loaded into the HS-3282 interface chip before transmission.

All bits in the Control Word are reset to "0" on power-up or a CAMAC Initialize (Z) cycle. The Control Word is clocked into a latch at S1 time of the F(16) A(0) command for the purposes of read-back. Bits 15 through 5 are then clocked into the HS-3282 interface chip at S2 time of the command. Bits 4 through 1 are used for controlling the counter circuitry which derives the various transmitter message rates. The format of the Control Word is shown in the following diagram.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
WLN	RBR	TBR	PIN	Y1	X1	SD1	Y0	X0	SD0	STM	N/U	XR8	XR4	XR2	XR1

Bit	Mnemonic	Function
15	WLN	WORD LENGTH. This bit is used to specify the length of the ARINC message. WLN is reset to a "0" for the 32-bit message format and set to a "1" for the 25-bit message format.

14	RBR	RECEIVER BIT RATE. This bit is used for specifying the low receiver bit data rate. If RBR is reset to "0", then the receiver bit data rate is 100 Kbps (1 Mhz /10) If RBR is set to a "1", then the receiver bit data rate is 12.5 Kbps (1 Mhz / 80).
13	TBR	TRANSMITTER BIT RATE. This bit is used for specifying the either the high or low transmitter bit data rate. If TBR is reset to "0", then the transmitter bit data rate is 100 Kbps (1 Mhz / 10). If TBR is set to a "1", then the transmitter bit data rate is 12.5 Kbps (1 Mhz / 80). Note that the strap option may need to change based on the data bit rate desired. Refer to the Strap Option section of this manual for further information.
12	PIN	PARITY. This bit is used to invert the transmitter parity bit for parity error testing. If PIN is reset to "0", normal odd parity is selected. If PIN is set to a "1", even parity is selected.
11	Y1	This bit is used along with X1 and SD1, bits 10 and 9 of the Control Word, to enable the reception of selected ARINC messages on receiver channel 1. If SD1 = "1", then the Y1 bit is compared with ARINC data bit 10. If X1 also matches (see X1), the word will be accepted by the receiver. If SD1 = "0", then the comparison is ignored.
10	X1	This bit is used along with Y1 and SD1, bits 10 and 9 of the Control Word, to enable the reception of selected ARINC messages on receiver channel 1. If SD1 = "1", then the X1 bit is compared with ARINC data bit 9. If Y1 also matches (see Y1), the word will be accepted by the receiver. If SD1 = "0", the comparison is ignored.
9	SD1	This bit is used to enable or disable the Source/Destination decoder for receiver channel 1. If this bit is set to "1", received ARINC messages are only stored if ARINC data bit 9 matches the X1 bit (see X1) and ARINC data bit 10 matches Y1 (see Y1). If SD1 is reset to "0", the Source Destination decoder is disabled.

8	Y0	This bit is used along with X0 and SD0, bits 10 and 9 of the Control Word, to enable the reception of selected ARINC messages on receiver channel 0. If SD0 = "1", then the Y0 bit is compared with ARINC data bit 10. If X0 also matches (see X0), the word will be accepted by the receiver. If SD0 = "0", the comparison is ignored.
7	X0	This bit is used along with Y0 and SD0, bits 10 and 9 of the Control Word, to enable the reception of selected ARINC messages on receiver channel 0. If SD0 = "1", then the X0 bit is compared with ARINC data bit 9. If Y0 also matches (see Y0), the word will be accepted by the receiver. If SD0 = "0", the comparison is ignored.
6	SD0	This bit is used to enable or disable the Source/Destination decoder for receiver channel 0. If this bit is set to "1", received ARINC messages are only stored if ARINC data bit 9 matches the X0 bit (see X0) and ARINC data bit 10 matches Y0 (see Y0). If SD0 is reset to "0", the source/ Destination decoder is disabled.
5	STM	SELF-TEST MODE. This bit is used to enable or disable the self-test feature of the HS-3282 interface chip. The self-test mode is enabled by writing this bit to a "0", and disabled by a "1" (normal operation). When enabled for the self-test mode, the interface chip connects the self-test signal from the transmitter directly to the receiver shift registers. This connection bypasses the input receivers. This mechanism provides a means for verifying correct operation of the 3310 module without regard for the actual connection to the ARINC bus. NOTE: When receiving data in the self-test mode, Channel 0 returns TRUE data and Channel 1 returns INVERTED data.
4	N/U	NOT USED. This bit is not used and should be written as a "0" when writing to the Control Word. This bit is read back as a "0".

3 : 0 XR8-XR1 TRANSMITTER RATE 8 thru TRANSMITTER RATE 1

These bits are used to specify the rate at which ARINC messages are loaded into the HS-3282 interface chip and sent out onto the ARINC bus. The binary combination of these bits determine the transmit message rate as shown below :

XR8	XR4	XR2	XR1	TRANSMIT MESSAGE INTERVAL
0	0	0	0	1 MILLISECONDS
0	0	0	1	2 MILLISECONDS
0	0	1	0	4 MILLISECONDS
0	0	1	1	8 MILLISECONDS
0	1	0	0	16 MILLISECONDS
0	1	0	1	32 MILLISECONDS
0	1	1	0	64 MILLISECONDS
0	1	1	1	128 MILLISECONDS
1	0	0	0	256 MILLISECONDS
1	0	0	1	512 MILLISECONDS
1	0	1	0	1024 MILLISECONDS
1	0	1	1	
	through			2048 MILLISECONDS
1	1	1	1	

LAM STRUCTURE

A variety of LAM sources are available within the 3310 to alert the user to the fact that the module requires service. The first two LAM sources are generated in response to the transmitter FIFO's status. The second two sources are generated in response to messages received on channel 0 and the third two sources are generated in response to messages received on channel 1.

The following is a list of CAMAC commands that are used to monitor and control LAM's.

F(1) A(12) -- Read LAM Status Register
F(1) A(13) -- Read LAM Mask Register
F(1) A(14) -- Read LAM Request Register

F(8) A(15) -- Test LAM Request

F(17) A(13) -- Write LAM Mask Register
F(23) A(12) -- Selectively Clear LAM Status Bits

LAM STATUS REGISTER

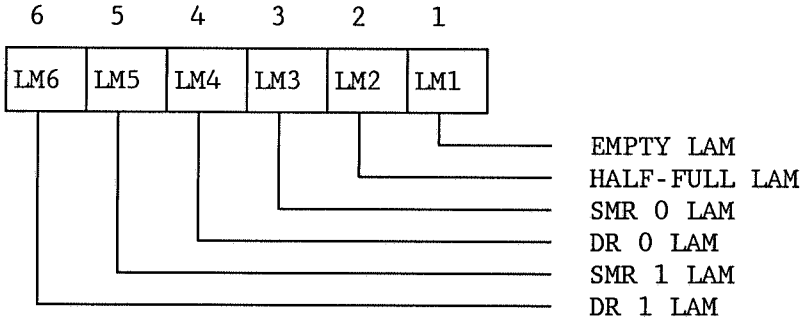
The F(1)A(12) command is used to read the LAM Status bits of the 3310. All bits in the LAM Status Register are cleared on power-up, a CAMAC Initialize (Z) cycle, and a selective-clear operation of the individual bits. The following diagram shows the bit pattern of the LAM Status Register.

6	5	4	3	2	1
DR 1	SMR1	DR 0	SMR0	HFUL	EMTY

Bit	Mnemonic	Function
6	DR 1	DATA RECEIVED 1. This bit is set when any message is received on channel 1.
5	SMR 1	SELECTED MESSAGE RECEIVED 1. This bit is set when a selected message is received on channel 1. To enable the SELECTED MESSAGE RECEIVED status bit, the pointer memory must have been previously written with bit 9 set.
4	DR 0	DATA RECEIVED 0. This bit is set when any message is received on channel 0.
3	SMR 0	SELECTED MESSAGE RECEIVED 0. This bit is set when a selected message is received on channel 0. To enable the SELECTED MESSAGE RECEIVED status bit, the pointer memory must have been previously written with bit 9 set.
2	HFUL	HALF FULL. This bit is set when the FIFO goes less than HALF-FULL. This bit does not represent the static state of the FIFO half-full flag. HALF-FULL is set only when the FIFO makes the transition from more than half-full to less than half-full. The actual transition is made when the FIFO contains 257 words and a word is read out of the FIFO.
1	EMTY	EMPTY. This bit is set when the transmit FIFO goes EMPTY. This bit does not represent the static state of the FIFO's empty flag. EMPTY is set only when the FIFO makes the transition from not-empty to empty (i.e., the last transmit data word has been read from the FIFO).

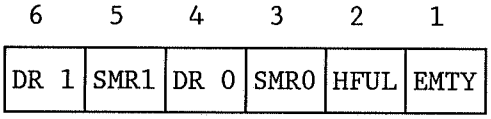
LAM MASK REGISTER

The LAM Mask Register is used for specifying which of the six LAM sources are to generate a LAM Request. If a LAM source is to generate a CAMAC LAM, it must first be masked "on" in the LAM Mask Register. A LAM is masked "on" by writing a "1" into the corresponding bit position that is to generate a LAM. The LAM Mask Register is written by a F(17) A(13) command and is read by a F(1) A(13) command. Each bit position in the LAM Mask Register corresponds to the same LAM status bit in the LAM Status Register. The LAM Mask Register is cleared on power-up and a CAMAC Initialize (Z) cycle. The following diagram shows the bit pattern in the LAM Mask Register.



LAM REQUEST REGISTER

The LAM Request Register is used for determining the source of a CAMAC LAM generated by the 3310. A CAMAC LAM is generated when a LAM Status bit is true AND its associated LAM Mask bit is true. The LAM Request Register is read by a F(1) A(14) command. The LAM Request Register is cleared on power-up, a CAMAC Initialize (Z) cycle, and a Selective-clear operation to individual LAM Status bits. The following diagram shows the bit pattern for the LAM Request Register.



MISCELLANEOUS LAM COMMANDS

Two additional CAMAC commands are available for controlling and monitoring the generation of LAM's by the 3310. The F(8) A(15) command is used for testing for the presence of a CAMAC LAM generated by the 3310. If a CAMAC Q-response of "0" is returned for this command, the 3310 is not asserting a LAM Request. Conversely, a Q-response of "1" indicates that the 3310 is asserting a LAM Request.

A second command is available for selectively clearing any LAM Status bit, which will also clear its corresponding LAM Request bit. The selective clear operation is performed by executing a F(23) A(13) command with the write data set equal to the LAM Status bits to be cleared (i.e., a write data bit set to a "1" clears the corresponding LAM Status bit). More than one LAM Status bit may be cleared with each write operation, depending on the write data used.

STRAP OPTIONS

CAPACITOR SELECTION

The strap option on the 3310 concerns the capacitors used to control the rise and fall times of the signal transmitted onto the ARINC bus. To meet the requirements of the ARINC specification for rise and fall times on the bus, the capacitor values for the high speed of operation must be 68 pf and for low speed 470 pf.

Two straps are used for configuring these rise and fall times. The following chart shows the necessary selections.

Bit rate	Capacitor value	Installation
100 Kbps	68 pf	Straps into the FA1 and FA2 locations
12.5 Kbps	470 pf	Straps into the SL01 and SL02 locations

16/32 BIT SELECTION

The 3310 can be configured so that only 16-bits of information be read for each ARINC message. Each read of a selected channel via the F(0) A(i) command, returns only WORD2 of the 32-bit message. Please refer to the WORD FORMATS section of this manual for the bit definitions in WORD2.

The straps for receive channel 0 are located toward the front of the board, and channel 1 near the rear. To select the 16-bit option, place both of the straps for the desired channel into the "16" position. For selecting the 32-bit option, place both of the straps for the desired channel into the "32" position.

FRONT PANEL

CONNECTORS

Three 9-contact "D" type connectors are used to bring the signals to/from the module and the ARINC-429 bus. A pin type is used for the Transmitter output, and socket type connectors are used for the Receiver inputs (one per channel). All connectors are located on the module's front panel.

Pins 1 and 2 of the 9-pin connectors are used for ARINC bus signal connection. The following chart shows the ARINC bus connections to each 9-pin connector.

Model 3310

CH1 RECEIVE	CH0 RECEIVE	TRANSMIT
Connector J1	Connector J2	Connector J3
Pin 1 - RCV Data high	Pin 1 - RCV Data high	Pin 1 - XMT Data high
Pin 2 - RCV Data low	Pin 2 - RCV Data low	Pin 2 - XMT Data low
Pin 3 - Ground	Pin 3 - Ground	Pin 3 - Ground
Pin 4 - No Connection	Pin 4 - No Connection	Pin 4 - No Connection
Pin 5 - Ground	Pin 5 - Ground	Pin 5 - Ground
Pin 6 thru Pin 9 - No Connection	Pin 6 thru Pin 9 - No Connection	Pin 6 thru Pin 9 - No Connection

DIAGNOSTIC INDICATORS

Light Emitting Diodes (LEDs) on the front panel indicate the state of activity within the module. The following is a description of each LED.

N -- This LED flashes each time the module is addressed.

LR -- This LED is illuminated as long as the module is asserting its CAMAC LAM Request line.

ACTIVE -- This LED is illuminated as long as the module is enabled for ARINC activity.

```
Program ARINC
c
c       This program was written to test the functions of the KSC 3310 ARINC module.
c       The unit was tested using the transmitter section to test the receiver section. This
c       was accomplished using a turn around connector.
c
        implicit none
c
        include 'causer.inc'
c
        integer*4  errstat(StaMax)
        integer*2  chan, crate, counts1, counts2, point(256)
        integer*2  n, xmit(512), rec(512), smr, try, loop, info
        integer*2  inc, lsr, lrr

        crate   = 1
        n       = 8
c
c
c
c       Open a channel to the CAMAC interface. This case using the Serial Highway c Driver.
c
        if ( caopen ( chan, 'KSA0:', errstat ) .ne. 1 ) then
        call camsg ( errstat )
        endif
c
c       Initialize the crate to a powered on state.
c
        call cactrl(chan, crate, init, errstat)
c
        write(6,*)'Wait for Lam Status to equal = '
        read(*,*)lsr
        write(6,*)'Set Lam Request Register equal = '
        read(*,*)lrr
c
c       Dis-Enable Arinc Activity.
c
        if ( cam24 ( chan, crate, n, 0, 24, info, errstat )
     &          .ne. 1 ) then
        call camsg ( errstat )
        endif
c
c       Write LAM Mask Register Enable user selection lrr.
c
        if ( cam24 ( chan, crate, n, 13, 17, lrr, errstat )
     &          .ne. 1 ) then
        call camsg ( errstat )
        endif
c
c       Write Configuration Word
```

```
c
      if ( cam24 ( chan, crate, n, 1, 16, 32, errstat )
     &       .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Init the Selected Message Received pointer.
c
      smr = 1
c
100   continue
c
c     In this section of code we load  the transmit FIFO data buffer. The address portion c
      is loaded with an incrementing pattern 0..255, while the data portion is loaded c
      with a decrementing patter 255..0.
c
      inc = 0
      do 10 loop = 1, 512,+2
            xmit ( loop )    = inc
            xmit ( loop + 1) = 255 - inc
            inc = inc + 1
10    continue
c
c     In this section we do a block transfer write to the transmit FIFO.
c
      if ( cab16E( chan, crate, n, 0, 16, eqign, xmit, 512, errstat )
     &       .ne. 1 ) then
      call camsg (errstat )
      endif
c
c     In this section of code we load the pointer memory. This is the memory which
c     points to the where the received message are to be stored. The MSB determines
c     if the message causes a Selected Message Received LAM to occur.
c
      if ( cam24 ( chan, crate, n, 2, 17, 0, errstat )
     &       .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Fill pointer memory array with a incrementing pattern, 0 .. 255.
c
      inc = 0
      do 15 loop = 1, 256
      point( loop ) = inc
      inc = inc + 1
15    continue
c
c     Select which element gets the SMR bit Set. We increment this pointer each time
c     through the loop.
c
```

```
      point(SMR)= Point(SMR) + 256
c
c     Load the pointer memory with incrementing pattern.
c
      if ( cab16E( chan, crate, n, 0, 18, eqign, point, 256, errstat )
     &      .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Enable ARINC activity in the module.
c
      if ( cam16 ( chan, crate, n, 0, 26, 0, errstat )
     &      .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Before we continue we Poll for LAM status equal to user supplied value lsr. We c
      loop the xmit data back into the module, so we wait for the transmit FIFO to c
      become empty before we proceed.
c
22    call cam24 ( chan, crate, n, 12, 1, info, errstat )
      if (info .LT. lsr ) goto 22
c
c     Reset the receive memory address to zero for memory readout.
c
      if ( cam24 ( chan, crate, n, 0, 17, 0, errstat )
     &      .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Read the information out of the receive FIFO using a block transfer operation.
c
      if ( cab16e( chan, crate, n, 0, 0, eqign, rec, 512, errstat )
     &      .ne. 1 ) then
      call camsg ( errstat )
      endif
c
c     Read the LAM status register so we can clear the status bits.
c
      if ( cam16 ( chan, crate, n, 12, 1, info, errstat )
     &      .ne. 1 ) then
      call camsg ( errstat )
      endif
c
```

```
c       Selectively clear the LAM status bits from the prior read operation.
c
        if ( cam24 ( chan, crate, n, 12, 23, info, errstat )
     &        .ne. 1 ) then
        call camsg ( errstat )
        endif
c
c       Disable ARINC activity.
c
        if ( cam24 ( chan, crate, n, 0, 24, 0, errstat )
     &        .ne. 1 ) then
        call camsg ( errstat )
        endif
c
c       Increment the pointer for the pointer memory word that will contain the SMR bit.
c
        smr = smr + 1
c
c       If the pointer is beyond the pointer memory reset to zero.
c
        if (smr .lt. 257) goto 100
        smr = 1
        if (smr .eq. 1 ) goto 100
c
200     stop
        end
```