Model 3315-Z1A

MIL-STD-1553B Bus Monitor

INSTRUCTION MANUAL

February, 1991

*****Special Option*****

Model 3315-S001

MIL-STD-1553B Bus Monitor

October, 1996

*****Special Option*****

Model 3315-S001

The Model 3315-S001 is the same as Model 3315-B1A except the front-end transformer bias is strapped for +5 volt bias.

March 20, 1996

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FIGURES

SCK:rem(WP/SCK)

MIL-STD-1553B Bus Monitor

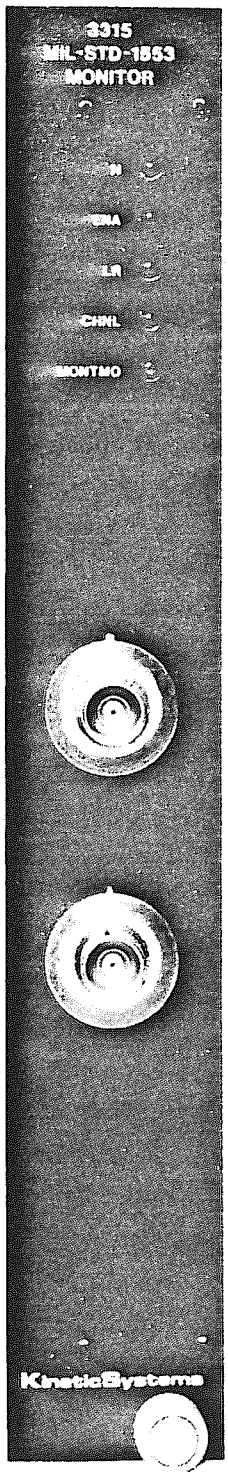
Provides a sophisticated monitor for the MIL-STD-1553 aircraft bus **3315**

Features

- **Monitors BC-to-RT, RT-to-BC, and mode commands**
- **Stores selected data in an 8192-word storage memory for readout**
- **User-programmable configuration memory for storage selection**
- **Error status reported for each stored message**
- **Stale data indicator for each stored message**
- **Dual redundant bus capability**

Typical Applications

- **Avionic subsystem development and testing**
- **Aircraft engine testing**
- **1553B bus diagnostics**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 3315 is a double-width CAMAC module with monitoring and diagnostic capabilities for messages appearing on a single channel of a MIL-STD-1553 Aircraft Internal Time Division Multiplex Data Bus, Revision B. This is the primary communication bus standard for military aircraft. A single bus channel provides the bidirectional command/response protocol over a shielded pair of wires and operates at a rate of one megabit per second. Word size is 20 bits. Each word contains 16 bits of data, a three-bit invalid Manchester pattern for sync, and one bit for parity.

The 3315 monitors bidirectional messages between the bus controller and remote terminals as well as mode commands (both with and without data). Depending on the contents of the user-programmable configuration memory, these messages are stored in an 8K by 16-bit data memory for later system readout. Data memory contains a global error word, an error word for each predetermined message of interest, the 1553 Status words associated with these messages, and preselected data words. The data memory is arranged so that updating the memory does not conflict with a memory Read operation.

The configuration memory appears as a 2K by 58-bit memory which must be loaded prior to activating the module's monitoring capabilities. Each configuration entry contains the data memory address where selected information is to be stored and a 32-bit field designating which of the associated data words to store. This memory is loaded from the Dataway, with each entry requiring three separate CAMAC Write operations.

The 3315 contains a dual redundant bus capability. Bus traffic from either bus port is monitored, with a bit in the global error register indicating which port is currently active. Both bus ports are brought to front-panel triaxial connectors.

Function Codes

Command		Q	Action
F(0)·A(0)	RD1	RDY	Reads the Storage Memory and increments the Address.
F(0)·A(1)	RD1	IDL	Reads the Configuration Memory and increments the Address.
F(0)·A(2)	RD1	RDY	Reads the Global Error Word.
F(1)·A(0)	RD2	1	Reads the Storage Memory Address register.
F(1)·A(1)	RD2	1	Reads the Configuration Memory Address register.
F(1)·A(12)	RD2	1	Reads the LAM Status register.
F(1)·A(13)	RD2	1	Reads the LAM Mask register.
F(1)·A(14)	RD2	1	Reads the LAM Request register.
F(8)·A(15)	TLM	LAM	Tests for the presence of a LAM.
F(9)·A(0)	CL1	1	Disables monitoring, clears all memories and LAM Status bits.
F(11)·A(0)	CL2	1	Resets the Storage Memory Address to zero.
F(11)·A(1)	CL2	1	Sets the Storage Memory Address to one.
F(16)·A(1)	WT1	IDL	Writes the Configuration Memory and increments the Address.
F(17)·A(0)	WT2	1	Writes the Storage Memory Address register.
F(17)·A(1)	WT2	1	Writes the Configuration Memory Address register.
F(17)·A(2)	WT2	IDL	Writes the Monitor Timeout Counter.
F(17)·A(13)	WT2	1	Writes the LAM Mask register.
F(23)·A(12)	SC2	1	Selectively clears the LAM Status bits.
F(24)·A(0)	DIS	1	Disables MIL-STD-1553 monitoring.
F(24)·A(1)	DIS	1	Disables Storage Memory updating.
F(26)·A(0)	ENB	1	Enables MIL-STD-1553 monitoring.
F(26)·A(1)	ENB	1	Enables Storage Memory updating.
F(27)·A(0)	TST	BSY	Tests for MIL-STD-1553 monitoring.
F(27)·A(1)	TST	RDONE	Tests for Memory Clear completion.
F(27)·A(2)	TST	RDY	Tests the Storage Memory Ready.
F(27)·A(3)	TST	CHAN	Tests for active channel.
Z·S2	ZED		Initializes the module, clears all memories and LAM Status bits.

Notes: X = 1 for all valid addressed commands.
RDY = Memory update complete, ready to read.
LAM = Look-At-Me line asserted by 3315.
IDL = Monitoring disabled, ready to configure.
BSY = MIL-STD-1553 monitoring in progress.
RDONE = Memory clear operation complete.
CHAN = Current active channel.

Power Requirements

+6 volts:	2915 mA
+24 volts:	955 mA

Ordering Information

Model 3315-Z1A MIL-1553 Aircraft Bus Interface, 2 channels

Related Products

None

OVERVIEW

The following is an overview of the Mil-STD-1553 message words. Each message word is shown with its bit pattern along with a brief description of the bits.

Mil-STD-1553 MESSAGE WORDS

COMMAND WORD

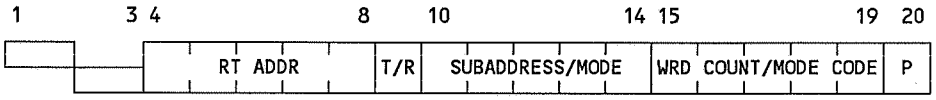


Figure 1.1 Mil-STD-1553B Command Word

Bits	Field	Meaning
1-3	Sync	A three-bit, invalid Manchester code which is at logic "1" for one and one-half bit times and at a logic "0" for the remaining one and one-half bit times.
4-8	Remote Term. Addr.	The unique address of the Remote Terminal (RT) which is receiving this command. A maximum of 31 Remote Terminals may be connected to a single bus. RT Address 31 (11111) is reserved for designating Broadcast Messages (i.e., messages broadcast to all terminals on the bus).
9	T/R Bit	The Transmit/Receive bit determines the action the RT is supposed to take as a result of the incoming message. T/R = "0" if the RT is to receive data from the 1553 bus. T/R = "1" if the RT is to transmit data out onto the 1553 bus.
10-14	Subaddress/Mode	This five-bit field determines which of 30 possible subaddresses (or memory pages?) within the RT that data is to be loaded into or retrieved from. Subaddresses 0 and 31 (00000 and 11111, respectively) indicate that a Mode Command is to be executed. The command is found in the next five-bit field (the Word Count/Mode Code field).
15-19	Data Word Count/ Mode Code	This five-bit field indicates the number of 16-bit data words which are to be transferred to or from the Remote Terminal. A maximum of 32 data words can be transferred with one command. A word count value of 0 (zero) indicates that all 32 words are to be transferred (i.e., no zero-word transfers are allowed).

		If the Subaddress/Mode field contains a 00000 or 11111 value (0 or 31), this field is to be interpreted as the Mode Code to be executed by the RT. (See the discussion on Mode Codes.)
20	Parity	This bit is to be set or cleared such that ODD Parity is maintained for the 17 bits of the message word (bits 4 through 20).

DATA WORD

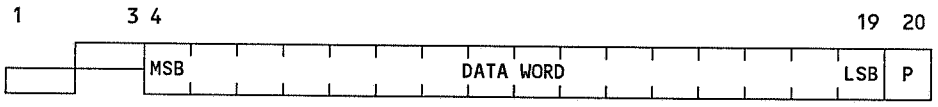


Figure 1.2 Mil-STD-1553B Data Word

Bits	Field	Meaning
1-3	Sync	A three-bit, invalid Manchester code which is at logic "0" for one and one-half bit times and at a logic "1" for the remaining one and one-half bit times.
4-19	Data	The 16-bit Data Word.
20	Parity	This bit is to be set or cleared such that ODD Parity is maintained for the 17 bits of the message word (bits 4 through 20).

STATUS WORD

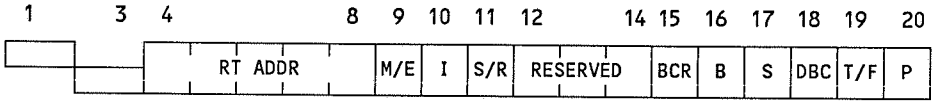


Figure 1.3 Mil-STD-1553B Status Word

Bits	Field	Meaning
1-3	Sync	A three-bit, invalid Manchester code which is at logic "1" for one and one-half bit times and at a logic "0" for the remaining one and one-half bit times.
4-8	Remote Term. Addr.	The unique address of the Remote Terminal (RT) from which the Status Word is being sent.
9	Message Error	This bit is used to indicate that one or more of the data words associated with the preceding Receive Command Word has failed to pass the RT's validity tests (the word begins with a valid Sync

		pattern, the bits are in valid Manchester II form, and word Parity is odd); that the message is discontiguous; that the Command Word has tried to select a function that has not been implemented in the addressed RT; or that a discrepancy exists between the Word Count specified in the Command Word and the number of words transmitted or received by the addressed RT.
10	Instrumentation	This bit in the Status Word is set to distinguish the Status Word from the Command Word. Since the Sync pattern is used to distinguish Command and Status words from Data words, a mechanism for distinguishing Command and Status words is provided by the Instrumentation bit. By setting this bit to a logic "0" for <u>all</u> conditions (as required by the specification) and setting the same bit position in the Command Word to a logic "1", the Command and Status words are identifiable. The use of this scheme is optional; but if used, this approach limits the range of possible subaddresses in the Command Word to 15 (16 through 30) and requires that subaddress 31 (11111) be used to identify Mode Commands. Even if this approach is not used, the Instrumentation bit will be set to a logic "0" for <u>all</u> conditions. The 3315 does not use this bit for differentiating between command and status words.
11	Service Request	The Service Request bit is provided to indicate to the active Bus Controller (BC) that a remote terminal requests service. When this bit in the Status Word is set to a logic "1" the active BC may take a predetermined action or use a Mode Command (i.e., Transmit Vector Word) to identify the specific Service Request.
12-14	Reserved	This three-bit field is reserved for future use and should be set to logic "0". Any bit in this field not set to logic "0" should be disregarded.
15	Broadcast Command Received	This bit is set to a logic "1" when the preceding valid Command Word was a Broadcast Command (address 31). Since Broadcast commands require the receiving RTs to suppress the transmission of their status words, this bit is set to indicate that the command was received properly. This bit will be reset to logic "0" when the next valid command is received by the RT, unless that command is Transmit Status Word or Transmit Last Command, or is another Broadcast command.

16	Busy	This bit is set to a logic "1" to indicate that the RT is unable to move data to or from the RT's subsystem in compliance with the received command. A busy condition can exist within an RT at any time (e.g., while the subsystem memory is being updated) causing it to be unable to send or receive data. This condition can exist for all message formats. Except for the case of Broadcast Messages, the BC will determine the busy condition immediately upon the receipt of the status response. For the Broadcast messages, this information will not be known unless the receiving terminals are polled for their status. If the Status Word has its Broadcast Command Received bit set to a logic "1", the message was received and the terminal was not busy.
17	Subsystem Flag	This bit indicates to the BC that a subsystem fault condition exists and that data being requested from the subsystem may be invalid. This bit may be set in any transmitted status response.
18	Dynamic Bus Control Acceptance	This bit indicates the acceptance by the addressed RT of the active BC's offer to become the next Bus Controller. The offer of bus control occurs when the presently active BC has completed its established message list and issues a Dynamic Bus Control Mode command to the RT that is to be the next potential controller. To accept the offer, the potential bus controller sets the Dynamic Bus Control Acceptance bit in its Status Word and transmits that response. The determination of who the next potential controllers are is an application specific, system level issue.
19	Terminal Flag	Devices (terminals) connected to the 1553 bus can be viewed as having two unique sections: the RT section which interfaces to the bus, and the subsystem section which performs the data manipulation and computational work. Errors within the subsystem can be communicated to the BC via the Subsystem Flag bit in the Status Word. The Terminal Flag bit is used to indicate to the BC that a problem exists in the interface section of the device. This bit is used in conjunction with three Mode Code commands: 1. Inhibit Terminal Flag bit 2. Override Inhibit Terminal Flag bit 3. Transmit Built-in-Test (BIT) Word. The first two Mode Code commands activate and deactivate the functional operation of the bit.

The Transmit BIT Word command is used by the RT to acquire more detailed information about the terminal's failure.

20 Parity — This bit is to be set or cleared such that ODD Parity is maintained for the 17 bits of the message word (bits 4 through 20).

MODE CODES

Mil-STD-1553 Mode Control Commands and Appropriate Responses

MODE CODE	COMMAND	RESPONSE
00000	Dynamic Bus Control	Status Word with DBCA set, assume control or Status Word with DBCA reset, remain idle
00001	Synchronize	Send current Status Word
00010	Transmit Status Word	Send Status from last valid command rcvd; Do not change Status Word contents
00011	Initiate Self-Test	Send current status, Start self-test
00100	Transmitter Shutdown	Send Status Word; disable REDUNDANT Xmtr
00101	Override Xmtr Shutdown	Send Status Word; enable REDUNDANT Xmtr
00110	Inhibit Terminal Flag	Send current status; disable T/F for further status responses
00111	Override Inhibit T/F	Send current status; enable T/F for further status responses
01000	Reset Remote Terminal	Send current status; set terminal to Initial Conditions state
01001 to 01111	Reserved Codes	Responses not currently defined
10000	Transmit Vector Word	Send current status followed by a service request vector word
10001	Synchronize with Data	Send current status
10010	Transmit Last Command	Do not change status; send last status; Send last valid command received
10011	Transmit BIT Word	Send current status word followed by the results of the Initiate Self-test command
10100	Selected Xmtr Shutdown	Send current status; disable transmitter

SELECTED		REDUNDANT
10101	Override S-X-S	Send current status; disable SELECTED REDUNDANT transmitter
10110 to 11111	Reserved Codes	Responses not currently defined

Note:

The following Mode commands are capable of being Broadcast from the Bus Controller to all Remote Terminals. When received as Broadcast commands, no Status Word is to be returned by the terminals.

CODE	COMMAND
00001	Synchronize
00011	Initiate Self-Test
00100	Transmitter Shutdown
00101	Override Transmitter Shutdown
00110	Inhibit Terminal Flag
00111	Override Inhibit Terminal Flag
01000	Reset Remote Terminal
10001	Synchronize with Data
10100	Selected Transmitter Shutdown
10101	Override Selected Transmitter Shutdown

Except where indicated above (i.e., Mode Codes 00010 and 10010), the bit in the status word are reset to logic zero after the reception of a valid command word. If the condition for setting these bits persists after a valid command is received, the bits will be set to logic one and sent over the bus as part of the Status Word response. However, in the case of Mode Codes 00010 and 10010, the status indicators to be returned are those that were generated as a result of the last valid commands received prior to these two mode codes.

THEORY OF OPERATION

The 3315 captures all message activity on the Mil-STD-1553 bus. The 1553 bus is brought into the 3315 via two front-panel mounted connectors. These two connectors are for a dual-redundant 1553 bus. The 3315 monitors both channels to determine which channel is currently active.

Each 1553 bus channel has transformer isolation on the front-end. The output of these transformers is then fed into receiver circuitry for each channel. After each bus channel is received, the encoded message stream is presented to a Manchester decoder. There is a Manchester decoder for each channel. The decoder takes the input message stream and generates the necessary signals for forming a 16-bit message word using shift registers. Additional outputs of the encoder include status bits reflecting the type of message word (command/status

or data) received and the validity of the message word. Word validity depends on such parameters as correct sync and parity.

The 3315 monitors the two Manchester decoders to determine which one is active. This circuitry then switches the outputs of the active Manchester decoder, via a multiplexer, to the input shift registers. The shift registers are used to convert the serial input stream into 16-bit message words. A logic sequencer then controls the loading of a 1024 X 24 bit First-In-First-Out (FIFO) memory device. As message words are received, they are analyzed and written into the FIFO. Each data entry in the FIFO contains the 16-bit message word along with eight status indicators. These indicators include 3 bits for determining the type of message (i.e.; RT to RT, Mode, Controller to RT,..,etc.), 3 bits for determining the word type, either command, status or data, a bit indicating message word validity, and a bit which indicates that a 1553 bus timeout occurred.

Up to this point, all 1553 bus traffic has been received and stored into the FIFO. The next stage in the monitoring process is to determine which messages are to be stored, where they are to be stored, and which data words within the message are to be stored.

A pair of logic sequencers is used to interpret the data stored in the FIFO. After a 1553 Command word is read from the FIFO, it is loaded into a register. The outputs of this register are used to form an address to the Configuration Memory. The Configuration Memory is loaded prior to 1553 message monitoring. This memory is used for specifying message storage criteria for each 1553 message. The address is composed of the Remote Terminal Address, the Transmit/Receive bit, and the Subaddress of the Command word. Once the address is applied to the Configuration Memory, three 16-bit words are read. The first word contains 13 address bits and 3 status bits. The 13 address bits are used for specifying where the message is to be stored in the 8192 X 16 Storage Memory. Two of the other bits are used for generating LAMs and the other for determining whether message storage is required. These 16-bits of information are held in a latch for later use.

The two other 16-bit words read from the Configuration Memory are used to determine which data words in the 1553 are to be stored. Each of the 32 bits represents a corresponding message data word. These bits are set according to the users preference. Each data word can be either stored or ignored. As these two configuration memory words are read out, they are stored in a 32-bit shift register for later use.

After the Configuration Memory is read, the logic sequencers continue to read message words from the FIFO. If a 1553 Status word is read from the FIFO, it is stored in a latch for later use. As message data words are read from the FIFO, they are compared to the bits held in the 32-bit shift register. If the data words are to be stored, they are written into a second FIFO. This FIFO will contain only message data words of interest. All data words that are not to be stored are discarded.

As message data words are written into the FIFO, they are checked for correct parity. If a parity error exists, the Subaddress Error Word is updated to

reflect the error. Please refer to the Subaddress Error Word section of this manual for a more detailed explanation.
After an entire message has been received and analyzed, it is then sent to the Storage Memory. As described earlier, the Configuration Memory determines if the message is to be stored or not, and where it is to be stored. If the message is not to be stored, the message data word FIFO is cleared and processing continues. If the message is to be stored, the logic sequencer reads the holding latches and the data FIFO ,and writes the data to the Storage Memory.

The 3315 can be configured to monitor the following types of 1553 messages :

1. Controller to Remote Terminal transfers
2. Remote Terminal to Controller transfers
3. Mode Commands without data
4. Mode Commands with data (Transmit)
5. Mode Commands with data (Receive)
6. Broadcast Controller to Remote Terminal transfers
7. Broadcast Mode Commands without data
8. Broadcast Mode Commands with data

The 3315 does not support the monitoring of the following types of messages:

1. Remote Terminal to Remote Terminal transfers
2. Broadcast Remote Terminal to Remote Terminal transfers

COMMAND DESCRIPTIONS

F(0)A(0)

The F(0)A(0) command is used to read the Storage Memory. This read command returns the data contained in the Storage Memory at the address specified by the Storage Memory Address register. The Storage Memory Address register is auto-incremented at the end of this command. This eliminates the need for continually re-loading the address register for every read of the memory.

A Q-response of zero is generated for this command if the Storage Memory is in the process of being updated with new message information. Refer to the Storage Memory Readout section of this manual for further details.

F(0)A(1)

The F(0)A(1) command is used to read the Configuration Memory. This read command returns the data contained in the Configuration Memory at the address specified by the Configuration Memory Address register. The Configuration Memory Address register is auto-incremented at the end of the third F(0)A(1) command. Refer to the Configuration Memory section of this manual for further details.

A Q-response of zero is generated in response to this command if the 3315 is enabled for monitoring. This command may only be used while the 3315 is not enabled for monitoring.

F(0)A(2)

The F(0)A(2) command is used to read the Global Error Word. This read command returns the current value of the Global Error Word. At the end of this command, the Global Error Word is reset to zero.

A Q-response of zero is generated for this command if the Storage Memory is in the process of being updated. Refer to the Global Error Word section of this manual for further details.

F(1)A(0)

The F(1)A(0) command is used to read the Storage Memory Address register. This read command returns the current value of the Storage Memory Address register. A Q=1 response is always returned for this command. Refer to the Storage Memory Address section of this manual for further details.

F(1)A(1)

The F(1)A(1) command is used to read the Configuration Memory Address register. This read command returns the current value of the Configuration Memory Address register. A Q=1 response is always generated for this command. Refer to the Configuration Memory Address section of this manual for further details.

F(1)A(12)

The F(1)A(12) command is used to read the LOOK-AT-ME (LAM) Status Register of the 3315. This read command returns the current value of the LAM Status register. A Q=1 response is always generated for this command. Refer to the LAM Status section of this manual for further details.

F(1)A(13)

The F(1)A(13) command is used to read the LAM Mask Register. This read command returns the current value of the LAM Mask Register. A Q=1 response is always generated for this command. Refer to the LAM Mask Register section of this manual for further details.

F(1)A(14)

The F(1)A(14) command is used to read the LAM Request Register. This read command returns the current value of the LAM Request Register. A Q=1 response is always returned for this command. Refer to the LAM Request section of this manual for further details.

F(8)A(15)

The F(8)A(15) command is used to test for the assertion of a LAM Request by the 3315. If the 3315 is asserting a LAM Request, a Q=1 response is generated for this command. Conversely, if the 3315 is not asserting a LAM, a Q=0 response is returned. Refer to the Miscellaneous LAM Command section of this manual for further details.

F(9)A(0)

The F(9)A(0) command is used to reset the 3315. After execution of this command, the LAM registers are cleared, monitoring is disabled, the memory address registers are set to zero, and the memories are reset such that they contain all zeros. A Q=1 is always generated for this control command. A F(27)A(2) command should be executed after this command to verify that the "memory clear" operation is complete. Refer to the Memory Clear Operation section of this manual for further details.

F(11)A(0)

The F(11)A(0) command is used to reset the Storage Memory Address register to zero. This command produces the same results as executing a F(17)A(0) command with the data set to zero. A Q=1 response is always returned for this command. Refer to the Storage Memory Address section of this manual for further details.

F(11)A(1)

The F(11)A(1) command is used to reset the Storage Memory Address register to one. This command produces the same results as executing a F(17)A(0) command with the data set to one. A Q=1 response is always returned for this command. Refer to the Storage Memory Address section of this manual for further details.

F(16)A(1)

The F(16)A(1) command is used for writing data to the Configuration Memory. This command writes data into the Configuration Memory at the address specified by the Configuration Memory Address register. The Configuration Memory Address is auto-incremented at the end of the third F(16)A(1) executed to the 3315. Refer to the Configuration Memory section of this manual for further details.

A Q=0 response is generated for this write command if the 3315 is enabled for 1553 monitoring. This command may only be used when the 3315 is not enabled for 1553 monitoring.

F(17)A(0)

The F(17)A(0) command is used for writing the Storage Memory Address register. A Q=1 response is always generated for this command. Refer to the Storage Memory Address section of this manual for further details.

F(17)A(1)

The F(17)A(1) command is used for writing the Configuration Memory Address register. A Q=1 response is always generated for this command. Refer to the Configuration Address section of this manual for further details.

F(17)A(2)

The F(17)A(2) command is used for writing the value of the Monitor Timeout Counter. A Q=0 response is generated for this command if the 3315 is enabled for 1553 monitoring. This write command may only be used when the 3315 is not

enabled for 1553 monitoring. Refer to the Monitor Timeout Counter section of this manual for further details.

F(17)A(13)

The F(17)A(13) command is used for writing the LAM Mask register. This write operation always returns a Q=1 response. Refer to the LAM Mask Register section of this manual for further details.

F(23)A(12)

The F(23)A(12) command is used for selectively clearing the LAM Status bits. A Q=1 response is always generated for this command. Refer to the Miscellaneous LAM Command section of this manual for further details.

F(24)A(0)

The F(24)A(0) command is used to disable 1553 monitoring. As long as the monitor is disabled, no 1553 messages are received or stored by the 3315. A Q=1 response is always generated for this command.

F(24)A(1)

The F(24)A(1) command is used to disable the 3315 circuitry from updating the Storage Memory. This command is necessary when it is desired to read the Storage Memory in a conservative (non-enhanced) fashion. Disabling the memory update ensures that the data read from the Global Error Word corresponds to the current values in the Storage Memory. If the updates are not disabled, and the memory read, the 3315 may update the memory and Global Error Word in between CAMAC read operations. If this command is executed, and a subsequent F(26)A(1) command is not executed within approximately 20.5 milliseconds, the 1553 input FIFO may be overrun. A FIFO overrun causes 1553 message data to be lost. A Q=1 response is always generated for this command. Refer to the Storage Memory Readout and LAM Status Register sections of this manual for further details.

F(26)A(0)

The F(26)A(0) command is used to enable 1553 monitoring. As long as the monitor is enabled, the 3315 will accept 1553 messages. A Q=1 response is always generated for this command.

F(26)A(1)

The F(26)A(1) command is used to enable the 1553 circuitry to update the Storage Memory. This command is used after the F(24)A(1) command. Normally, the 3315 is enabled for updating the Storage Memory. If the 3315 is read out in an enhanced mode, this command need not be executed. A Q=1 response is always generated for this command. Refer to the Storage Memory Readout section of this manual for further details.

F(27)A(0)

The F(27)A(0) command is used for testing the state of 1553 bus monitoring. If a Q=1 is returned for this command, the 3315 is currently enabled for 1553 monitoring. If the 3315 is not enabled for monitoring, a Q=0 response is generated.

F(27)A(1)

The F(27)A(1) command is used to test for the completion of a memory clear operation. If the memories are in the process of being cleared, a Q=0 response is returned. If the memory clear operation is complete, a Q=1 response is generated. Refer to the Memory Clear Operation section of this manual for further details.

F(27)A(2)

The F(27)A(2) command is used to test for the availability of the Storage Memory. If the Storage Memory is in the process of being updated when this command is executed, a Q=0 response is returned. Conversely, a Q=1 response is generated if the Storage Memory is not being updated. Refer to the Storage Memory Readout section of this manual for further details.

F(27)A(3)

The F(27)A(3) command is used to test for the current active 1553 channel. If channel 0 is currently active when this command is executed, a Q=1 response is returned. Conversely, a Q=0 is returned if channel 1 is active.

MESSAGE STORAGE

A 8192 X 16 static memory is used for holding the monitored 1553 messages. The message storage format in the Storage Memory is determined by the Configuration Memory. The Configuration Memory, which is loaded prior to 1553 bus monitoring, specifies where various messages are stored in the Storage Memory and which message data words are stored. Each message stored contains a Subaddress Error Word. This word is the first entry in the Storage Memory for each message. Following the Subaddress Error Word (SEW), the Storage Memory contains the status word received from the 1553 message. After the 1553 status word, the data words from the message are stored. Please refer to the Subaddress Error Word section of this manual for further details.

The Global Error Word, which is located at address location zero of the Storage Memory, contains information regarding message reception. The location of the Global Error Word (GEW) within the Storage Memory is not programmable. Please refer to the Global Error Word section of this manual for further details.

The following diagram shows the Storage Memory. As shown, the messages are stored in contiguous address locations, but do not necessarily have to be setup that way. The only restriction is that the Configuration Memory cannot be setup to have a message stored at address location zero of the Storage Memory.

GLOBAL ERROR WORD
SUBADDRESS ERROR WORD #1
STATUS
DATA WORD #1
.
DATA WORD n
SUBADDRESS ERROR WORD #2
STATUS
DATA WORD #1
.
DATA WORD n
SUBADDRESS ERROR WORD n
STATUS
DATA WORD #1
DATA WORD #2
.
DATA WORD n

STORAGE MEMORY READOUT

The Storage Memory of the 3315 may be read out in either a conservative or enhanced mode. During conservative readout, each access to the 3315 requires a separate CAMAC Dataway cycle. Most Crate Controllers use the conservative mode of accessing the CAMAC crate. Enhanced readout is provided by several KineticSystems Serial Highway products; including the 2160, 2170, 2185 and 2188. The 3982 Auxiliary Crate Controller can also execute enhanced-type CAMAC operations. These operations maintain control of the CAMAC Dataway for the entire length of a block transfer operation.

During conservative readout, the user must ensure that the 3315 is not going to update the Storage Memory while it is being read. Circuitry on the 3315 actually prevents simultaneous access to the Storage Memory, but this is not sufficient for maintaining the association between the Global Error Word and the data read from the Storage Memory. For instance, the user program may read the Global Error Word from the 3315. By the time a subsequent read operation occurs to the Storage Memory, a Storage Memory update may have occurred. Now, the Global Error Word does not reflect the status of the following storage words that are read. To prevent this, the F(24)A(1) command is used to inhibit the Storage Memory from being updated until the user has read out the required number of data words. After the words are read, a F(26)A(1) command must be

executed to allow further updates of the Storage Memory. The amount of time that the Storage Memory updated can be disabled depends on the amount of 1553 bus activity. The input FIFO, which "holds" the 1553 words from the bus, is 1024 words deep. If the 3315 is receiving a message word every 20 microseconds, the FIFO will overflow after approximately 20.5 milliseconds. (This time does not account for response time or inter-message gaps.)

The following describes the steps necessary for reading the 3315 Storage Memory in a conservative fashion.

1. Execute a F(24)A(1) command to the 3315. This will inhibit further updates of the Storage Memory. If memory update is in progress when this command is executed, the update will continue.

2. Execute F(0)A(0) commands to the 3315 until all the data words of interest are read. The first read of the Storage Memory must be in a Q-Repeat mode which allows the update of the memory to complete. After a Q=1 is returned, the block transfer operation will continue.

3. After all words of interest are read, execute a F(26)A(1) command to the 3315 to allow memory updates to continue.

The other method of reading the 3315 Storage Memory is in a enhanced block transfer operation. This does not require as many programming steps as conservative readout. The updating of the memory does not have to be halted by the execution of the F(26)A(1) command. After the enhanced operation starts, the modules N-line (station number) is held asserted for the entire duration of the enhanced block transfer. This mechanism inhibits the 3315 from updating the Storage Memory since the CAMAC Dataway has "control" of the storage memory for readout. But, initially, Q=0 responses may be returned for the F(0)A(0) command until the CAMAC Dataway read operation obtains "control" of the Storage Memory. As with the conservative mode of readout, the amount of time the 3315 is prevented from updating the Storage Memory should not exceed approximately 20.5 milliseconds. Under normal enhanced readouts, this will not occur since the 8192 memory can be read out in 8.192 milliseconds.

The following describes the steps necessary for reading out the Storage Memory in an enhanced mode.

1. Execute a Q-Repeat enhanced block transfer operation to the 3315. The Q-Repeat operation is necessary since the memory may be in the process of updating when the first read is executed. After the update is complete, a Q=1 is generated for the F(0)A(0) command and the block transfer operation continues. After the initial Q=1 is received, the enhanced read operation has "control" of the Storage Memory which prevents further updates until the transfer is complete.

CONFIGURATION MEMORY ADDRESS

The Configuration Memory Address register is used for specifying the address at which subsequent Configuration Memory write or read operations are to occur. Before writing or reading the Configuration Memory, the address must first be specified. The Configuration Memory Address register is written by a F(17)A(1) command and read by a F(1)A(1). The bit pattern for the Configuration Memory Address register is shown below. The mnemonics under the bit pattern diagram show the actual 1553 command word bits that define each entry. Refer to the Configuration Memory section of this manual for further details.

11	10	09	08	07	06	05	04	03	02	01
CA10	CA09	CA08	CA07	CA06	CA05	CA04	CA03	CA02	CA01	CA00
RT16	RT8	RT4	RT2	RT1	T/R	SA16	SA8	SA4	SA2	SA1

STORAGE MEMORY ADDRESS

The Storage Memory Address register is used for specifying the address at which subsequent Storage Memory read operations are to occur. Before reading the Storage Memory, the address must first be specified. The F(17)A(0) command is executed to the 3315 to load the Storage Memory Address Register. The following diagram shows the bit pattern for the Storage Memory Address register.

13	12	11	10	09	08	07	06	05	04	03	02	01
SA12	SA11	SA10	SA09	SA08	SA07	SA06	SA05	SA04	SA03	SA02	SA01	SA00

The Storage Memory Address is auto-incremented at Strobe S2 time of the F(0)A(0) command. This eliminates the need for continually reloading the address register for subsequent read operations.

CONFIGURATION MEMORY

The Configuration Memory is used for specifying the message storage address within the 8192 X 16 Storage Memory. The Configuration Memory also contains several other parameters concerning message storage.

When a 1553 message is received by the 3315, eleven bits from the 1553 command word are applied to the address inputs of the Configuration Memory. The bits are the Remote Terminal Address bits, the Transmit/Receive bit, and the Subaddress bits. The following block diagram shows the Configuration Memory and its major components.

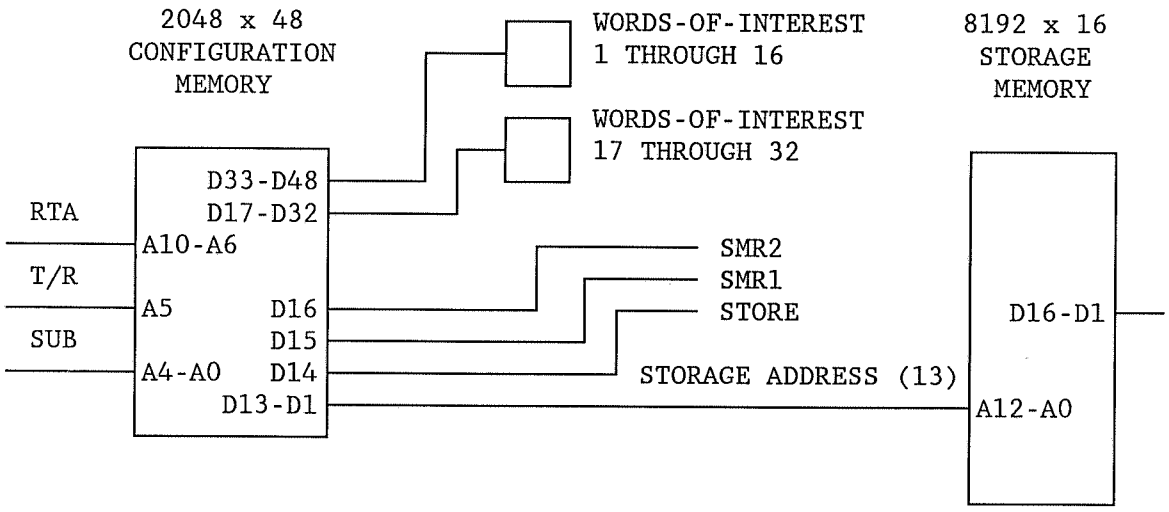


Figure 1.4 Configuration Memory

The Configuration memory is physically composed of a 8K X 16 static RAM. For explanation purposes it will be referred to as a 2048 X 48 memory.

After the address is applied to the Configuration Memory, three 16-bit words (48 bits) are then read from the memory and clocked into a latch. The format of the three words is shown in the following diagram.

CONFIGURATION WORD FORMATS

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
WORD 1	SMR2	SMR1	STOR	MA12	MA11	MA10	MA09	MA08	MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00

	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
WORD 2	WD17	WD18	WD19	WD20	WD21	WD22	WD23	WD24	WD25	WD26	WD27	WD28	WD29	WD30	WD31	WD32

	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33
WORD 3	WD01	WD02	WD03	WD04	WD05	WD06	WD07	WD08	WD09	WD10	WD11	WD12	WD13	WD14	WD15	WD16

In WORD 1, the MA12 through MA0 bits are used for specifying the address of the Storage Memory where the received message is to be stored. The bit STOR, which is the "store" bit, determines whether the received message is to be loaded into the Storage Memory. If this bit is a "1", the message is stored. A "0" for this bit causes the message to be ignored. SMR2 and SMR1 are the Selected-Message-Received bits. After a message is received and stored, these bits are used to generate a LAM source. A LAM source is generated if either of the SMR bits is set to a "1".

In WORD 2 there are 16 bit positions. The bit positions correspond to a received message data word. WORD 2 contains entries for received message data words 17 through 32. Data words that are to be stored from a particular message must have their corresponding bit position set to a "1". If a "0" is entered for a particular position, the associated message data word is ignored and is not loaded into the Storage Memory during updating. For example, if data words 17, 19, 23, and 27 through 32 are to be stored, WORD 2 would contain A23F hex.

In WORD 3 there are 16 bit positions. The bit positions correspond to a received message data word. WORD 3 contains entries for received message data words 1 through 16. Data words that are to be stored from a particular message must have their corresponding bit position set to a "1". If a "0" is entered for a particular position, the associated message data word is ignored and is not loaded into the Storage Memory during updating. For example, if data words 1 through 8, 11, 13, and 15 are to be stored, WORD 3 would contain FF22 hex.

Every binary combination of the 11 bit address field has an entry in the Configuration Memory. As described above, each entry consists of 48 bits, 3 words of 16-bits each. The Configuration Memory is written by a F(16)A(1) command and is read by a F(0)A(1) command. These two commands are ignored and return a Q-response of zero if the module is enabled for monitoring.

Before the Configuration Memory is written or read, the Configuration Memory Address Register must first be loaded with the desired address of access. The Configuration Memory Address Register is written with a F(17)A(1) command and read with a F(1)A(1) command. After the address register is loaded, the Configuration Memory may then be written or read. The following diagram shows the bit pattern for the Configuration Memory Address Register and the corresponding 1553 command word bits that define them.

11	10	09	08	07	06	05	04	03	02	01
CA10	CA09	CA08	CA07	CA06	CA05	CA04	CA03	CA02	CA01	CA00
RT16	RT8	RT4	RT2	RT1	T/R	SA16	SA8	SA4	SA2	SA1

For example, assume it is desired to load the Configuration Memory for a Transmit Command message to Remote Terminal 10 - Subaddress 3. Before accessing the Configuration Memory, the memory address register must first be loaded. For the given message, the address register is loaded with 2A3 hex. The Configuration Memory may then be written to or read from for the given message.

Each access to the memory requires three consecutive 16-bit CAMAC operations to either write or read the memory. The memory address register is automatically incremented after the third write or read operation to the memory. This eliminates the need for constantly reloading the address register for each entry in the Configuration Memory.

The following describes two examples of loading the Configuration memory for two different types of applications. The first example requires two write operations to the memory address register since they are not contiguous entries

in the memory. The second example requires only the initial loading of the memory address register since they are contiguous entries. The auto-increment of the address register will advance to the next entry in the memory.

Example 1.

Assume it is desired to load the Configuration Memory to monitor Transmit Command messages to Remote Terminal 3 - Subaddress 8. Only message data words 1, 2, 5, 15, 25 and 32 are to stored. This message is to be stored starting at address 1 in the Storage Memory. The second message to be monitored is a Receive Command message to Remote Terminal 8 - Subaddress 1. Only data words 5, 7, 10 and 30 are to be stored. This message is to be stored starting at address location 9 in the Storage Memory.

The following is a list of CAMAC commands and the appropriate data necessary to setup the Configuration Memory for this application

CAMAC Command	Operation	Data (hex)
F(17)A(1)	Write address	00E8
F(16)A(1)	Write memory	2001
F(16)A(1)	Write memory	0081
F(16)A(1)	Write memory	C802

At this point, the memory address increments to 00E9, which is the address defined for Transmit Command messages from Remote Terminal 3 - Subaddress 9. Since this is not the next message to be monitored, the address register must be reloaded.

F(17)A(1)	Write address	0201
F(16)A(1)	Write memory	2009
F(16)A(1)	Write memory	0004
F(16)A(1)	Write memory	0A40

After this Configuration Memory has been loaded and the 3315 has received the above messages, the data in the Storage Memory is readout as shown in the following diagram.

Example 2.

Assume it is desired to load the Configuration Memory to monitor Receive Command messages to Remote Terminal 13 - Subaddress 10. Only message data words 1, 9, 18, 27 and 32 are to be stored. This message is to be stored starting at address 1 in the Storage Memory. When this message is received, it should also generate the SMR2 LAM source. The second message to be monitored is a Receive Command message to Remote Terminal 13 - Subaddress 11. Only data words 5, 9, 10, 12, 17, 25 and 30 are to be stored. This message is to be stored starting at address location 8 in the Storage Memory.

The following is a list of CAMAC commands and the appropriate data necessary to setup the Configuration Memory for this application.

CAMAC Command	Operation	Data (hex)
F(17)A(1)	Write address	034A
F(16)A(1)	Write memory	A001
F(16)A(1)	Write memory	4021
F(16)A(1)	Write memory	8080

At this point, the memory address increments to 034B, which is the address defined for Receive Command messages from Remote Terminal 13 - Subaddress 11. Since this is the next message to be monitored, the address register does not need to be reloaded.

F(16)A(1)	Write memory	2008
F(16)A(1)	Write memory	8084
F(16)A(1)	Write memory	08D0

The following chart shows the message storage for each of the above examples:

STORAGE MEMORY ADDRESS	EXAMPLE # 1	EXAMPLE # 2
0	GLOBAL ERROR WORD	GLOBAL ERROR WORD
1	SUBADDRESS ERROR WORD #1	SUBADDRESS ERROR WORD #1
2	STATUS #1	STATUS #1
3	DATA WORD #1	DATA WORD #1
4	DATA WORD #2	DATA WORD #9
5	DATA WORD #5	DATA WORD #18
6	DATA WORD #15	DATA WORD #27
7	DATA WORD #25	DATA WORD #32
8	DATA WORD #32	SUBADDRESS ERROR WORD #2
9	SUBADDRESS ERROR WORD #2	STATUS #2
10	STATUS #2	DATA WORD #5
11	DATA WORD #5	DATA WORD #9
12	DATA WORD #7	DATA WORD #10
13	DATA WORD #10	DATA WORD #12
14	DATA WORD #30	DATA WORD #17
15		DATA WORD #25
16		DATA WORD #30

NOTES:

1. When allocating addresses for messages in the Storage Memory, take care avoid overlapping messages.

2. Since the Word Count/Mode code field is not used for determining unique messages, Mode command messages are all stored at the same defined address in the Storage Memory. Mode command words have the subaddress field set to either 0 or 31. Therefore, all Mode-type messages are stored at the address specified by either the subaddress 0 or subaddress 31 entry in the configuration Memory.

GLOBAL ERROR WORD

The Global Error Word contains status information concerning 1553 monitoring. The Global Error Word (GEW) consists of four status bits and two counters. The following diagram shows the bit pattern for the GEW.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
ACHAN	ISC32	ISC16	ISC8	ISC4	ISC2	ISC1	SC32	SC16	SC8	SC4	SC2	SC1	1553 TMO	MON TMO	ERROR

Bit	Mnemonic	Description
16	ACHAN	ACTIVE CHANNEL. This bit reflects the current active 1553 channel. If this bit is read back as a "0", the current active channel is zero. A "1" indicates that the current active channel is one. This bit does not represent which channel was active at the time the other bits within this word were updated, it is merely a current reflection of the active channel.
15-10	ISC 32-1	INVALID SUBADDRESS COUNTER BITS 32 through 1. These bits are the outputs of a counter which is incremented any time an invalid subaddress is encountered. The counter is incremented on the occurrence of a word count error or if a command word parity error is detected. This counter is reset after the GEW is read via the F(0)A(0) or F(0)A(2) command.
09-04	SC 32-1	SUBADDRESS COUNTER BITS 32 through 1. These bits are the outputs of a counter which is incremented any time a new subaddress is updated. This counter is also incremented at the same time the Invalid Subaddress Counter is incremented. This counter is reset after the GEW is read via the F(0)A(0) or F(0)A(2) command.

03	1553 TMO	1553 TIMEOUT. This bit is set whenever a 1553 bus timeout occurs. A bus timeout is defined by a greater than 14 micro-second delay between a command word transmission and a Remote Terminal response. This bit is reset after the next valid 1553 message received by the 3315.
02	MON TMO	MONITOR TIMEOUT. This bit is set when the Monitor Timeout Counter of the 3315 expires. This indicates that there was no 1553 bus activity for the amount of time specified in the Monitor Timeout Counter. Refer to the Monitor Timeout section of this manual for further details.
01	ERROR	ERROR. This bit is set whenever an error condition exists. The ERROR bit is set by any of the following conditions. 1. Parity error in Subaddress Error Word 2. Word count error in Subaddress Error Word 3. Non-zero Invalid Subaddress Counter in Global Error Word 4. 1553 Timeout in the Global Error Word 5. Monitor Timeout in the Global Error Word

The ERROR bit is reset after the GEW is read via a F(0)A(0) or F(0)A(2) command as long as there is not a Monitor Timeout.

The Global Error Word is located at address location zero of the Storage Memory. To read the GEW, the Storage Memory Address Register must be set to zero, and then a F(0)A(0) command executed. After this read is executed, the GEW is cleared. The GEW may also be read via the F(0)A(2) command. This command always returns the GEW, independent of the memory address.

SUBADDRESS ERROR WORD

The Subaddress Error Word is the first entry in the Storage Memory for any stored message. The address of the entry in the Storage Memory is specified in the Configuration Memory for each message of interest.

The Subaddress Error Word (SEW) contains information regarding the individual messages. The SEW holds parity error information, word count status, and a bit for indicating "Stale Date". The following diagram shows the bit pattern for the SEW.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
PAR ERR	PW32 A	PW16 A	PW8 A	PW4 A	PW2 A	PW1 A	PW32 B	PW16 B	PW8 B	PW4 B	PW2 B	PW1 B	WCT ERR	STALE	ERROR

Bit	Mnemonic	Description
16	PAR ERR	PARITY ERROR. This bit is set if any of the selected (stored) data words associated with the message contain parity errors. This bit is reset after the next valid update of the subaddress.

15-10 PW 32A-1A PARITY WORD 32A through 1A. The binary combination of these bits indicates the first occurrence of a parity error in the data words of a message. This value refers to the position in the storage list, not relative to the position it was received from the 1553 bus. When no parity errors have been found, this field is set to zero.

09-04 PW 32B-1B PARITY WORD 32B through 1B. The binary combination of these bits indicates the second occurrence of a parity error in the data words of a message. This value refers to the position in the storage list, not relative to the position it was received from the 1553 bus. When a second parity error has not occurred, this field is zero.

03 WCT ERR WORD COUNT ERROR. This bit is set whenever a word count conflict occurs. A word count conflict occurs when the word count field of a 1553 command word does not match the actual number of data words transferred. This bit is reset after the next valid update of the subadddress.

02 STALE STALE DATA. This bit is set in response to reading the current subaddress. After a subaddress is read onto the CAMAC Dataway, this bit is rewritten to a "1" in the Subaddress Error Word. When a new subaddress is received, the Storage Memory is written with the Stale Data bit set to zero. A "1" returned for this bit indicates that the subaddress has not been updated since the last read onto the CAMAC Dataway. This bit is also set on the occurrence of a Word Count error. When a Word Count Error occurs, no message data words or status is written into the Storage Memory, but the Stale Data bit will be set.

01 ERROR ERROR. This bit is set if a parity error or word count error for the subaddress has occurred. This bit remains set until there is no parity or word count errors.

The Subaddress Error Word is a programmable location within the Storage Memory. The SEW is the first entry in the Storage Memory for any received message. The SEW for a particular message is read by first loading the Storage Memory Address register with the desired message to be read. As described earlier, this is a combination of the Remote Terminal Address, the Transmit/Receive bit, and the Subaddress messages. After the address register is loaded, the SEW may then be read by an F(0)A(0) command.

LAM STRUCTURE

A variety of LAM sources are generated by the 3315 to alert the user that the module requires service. There is a total of seven LAM sources within the 3315. Two of the sources are for 1553 timeouts, three for various received messages, and two for error conditions.

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The following is a list of the CAMAC commands that are used to monitor and control the LAMs.

F(1) A(12)	--	Read LAM Status Register
F(1) A(13)	--	Read LAM Mask Register
F(1) A(14)	--	Read LAM Request Register
F(8) A(15)	--	Test for LAM Request
F(17)A(13)	--	Write LAM Mask Register
F(23)A(12)	--	Selectively Clear LAM Status Bits

LAM STATUS REGISTER

The F(1)A(12) command is used for reading the LAM Status bits of the 3315. All LAM Status bits are cleared on power-up, a CAMAC Initialize (Z) cycle, and a Selective-Clear operation of the individual bits. The following diagram shows the bit pattern for the LAM Status Register.

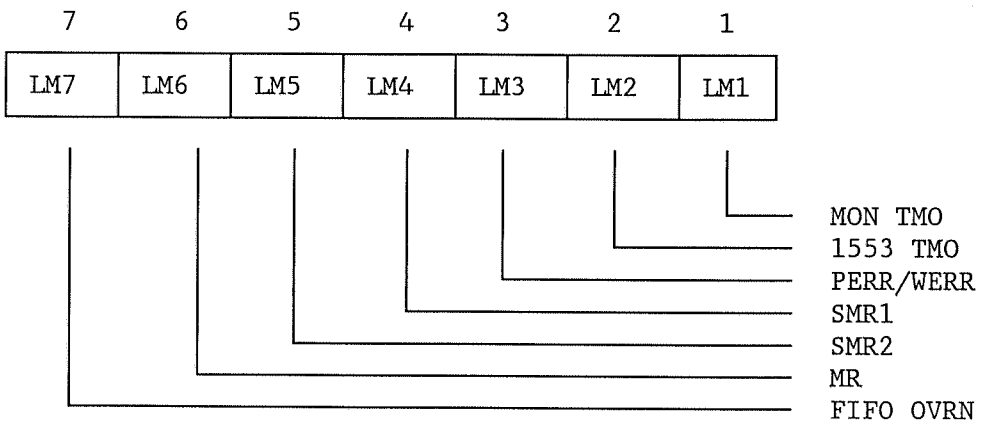
7	6	5	4	3	2	1
FIFO OVRN	MR	SMR2	SMR1	PERR WERR	1553 TMO	MON TMO

Bit	Mnemonic	Function
7	FIFO OVRN	FIFO OVERRUN. This bit is set whenever the input message FIFO overflows. An overflow condition occurs whenever the message processor cannot update the storage memory with processed messages. This may occur when an enhanced block transfer read operation is in progress, which prevents updating. Normally, the enhanced block transfer read operation of the entire 8K of storage RAM takes 8.192 milliseconds. This does not generate a FIFO overrun since only a maximum of 410 message words can be received during that time. The other condition which prevents updating is by executing the F(24)A(1) command. If the F(26)A(1) command is not executed within approximately 20.5 milliseconds after the F(24)A(1), it is possible for an overrun condition to result. This time is calculated for the 1K FIFO receiving message words every 20 microseconds. If a FIFO overrun condition occurs, the user must adjust the time that the storage memory is accessed during the readout.
6	MR	MESSAGE RECEIVED. This bit is set whenever a message is received. The LAM source is actually generated after the entire message is analyzed.

5	SMR2	SELECTED MESSAGE RECEIVED 2. This bit is set when a selected message is received. To enable the SMR2 LAM source, the Configuration Memory must have been previously written with bit 16 of Word 1 set to a "1".
4	SMR1	SELECTED MESSAGE RECEIVED 1. This bit is set when a selected message is received. To enable the SMR1 LAM source, the Configuration Memory must have been previously written with bit 15 of Word 1 set to a "1".
3	PERR/WERR	PARITY ERROR/WORD COUNT ERROR. This bit is set when either a data parity error is detected or a word count error is found. Parity errors are generated for message data words only. A word count error is set when the number of data words specified in the command word of a message does not match the actual number of data words within the message.
2	1553 TMO	1553 TIMEOUT. This bit is set when a Remote Terminal does not respond to a message sent by the Controller within 14 micro-seconds.
1	MON TMO	MONITOR TIMEOUT. This bit is set when the Monitor Timeout Counter expires. The counter times-out when there is no 1553 bus activity for the specified amount of time programmed into the Monitor Timeout Counter. Please refer to the Monitor Timeout section of this manual for further details.

LAM MASK REGISTER

The LAM Mask Register is used for specifying which of the seven LAM sources are to generate a CAMAC LAM Request. If a LAM source is to assert a CAMAC LAM Request, it must first be masked "on" in the LAM Mask Register. A LAM is masked "on" by writing a "1" into the corresponding bit position that is to generate a LAM. The LAM Mask Register is written by a F(17)A(13) command and is read by a F(1)A(13) command. Each bit position in the LAM Mask Register corresponds to the same LAM status bit in the LAM Status Register. The LAM Mask Register is cleared on power-up, a CAMAC Initialize (Z) cycle, and a F(9)A(0) command executed to the 3315. The following diagram shows the bit pattern in the LAM Mask Register.



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LAM REQUEST REGISTER

The LAM Request Register is used for determining the source of a CAMAC LAM generated by the 3315. A CAMAC LAM is asserted when a LAM Status bit is true AND its corresponding LAM Mask bit true (masked "on"). The LAM Request Register is read by a F(1)A(14) command. The LAM Request register is cleared on power-up, a CAMAC Initialize (Z) cycle, a F(9)A(0) command executed to the 3315, and a selective-clear operation to the individual LAM Status bits. The following diagram shows the bit pattern for the LAM Request Register.

7	6	5	4	3	2	1
FIFO OVRN	MR	SMR2	SMR2	PERR WERR	1553 TMO	MON TMO

MISCELLANEOUS LAM COMMANDS

Two additional CAMAC commands are available for controlling and monitoring the generation of CAMAC LAMs by the 3315. The F(8)A(15) command is used for testing for the presence of a CAMAC LAM. If a CAMAC Q-response of "0" is returned for this command, the 3315 is not asserting its LAM Request. Conversely, a Q-Response of "1" indicates that the 3315 is asserting its LAM Request.

The second command is for selectively clearing any LAM Status bit, which also clears the corresponding LAM Request bit. The LAM Mask Register bits are unaffected by this command. The selective-clear operation is performed by executing a F(23)A(13) command with the write data set equal to the LAM Status bit(s) to be cleared (i.e., a write data bit set to a "1" clears the corresponding LAM Status bit). More than one LAM Status bit may be cleared with each write operation, depending on the write data selected.

MEMORY CLEAR OPERATIONS

All locations within both the Storage Memory and Configuration Memory can be cleared. Clearing the memories refers to writing zeros to all locations in the memory. The memories are cleared by the following :

1. Power-up cycle
2. CAMAC Initialize (Z) operation
3. F(9)A(0) command

The clear operation takes approximately 4.1 milliseconds. A test command, F(27)A(0), to the 3315 is used to verify that the memory clear operation is complete. A Q=0 response is returned if the memory clear operation is still in progress. A Q=1 indicates that the operation is complete.

After the clear operation, the Storage Memory Address and Configuration Memory Address are set to zero.

MONITOR TIMEOUT

The Monitor Timeout Counter is used to generate a status indicator which is set when the 1553 bus "dead" time exceeds a predetermined value. "Dead" time refers to no 1553 bus activity on either channel. The Monitor Timeout Counter is a programmable counter. The "dead" time values range from 10 milliseconds to 655.35 seconds in 10 millisecond increments.

The Monitor Timeout Counter is written using the F(17)A(2) command. The data used along with this command is the number of 10-millisecond intervals to be used for determining "dead" time. For example, if it is desired to set the Monitor Timeout Counter to 200 milliseconds, data of 20 decimal is used as the write data.

This command may only be executed when the 3315 is not enabled for monitoring. A Q=1 response is generated for this command if monitoring is disabled. If the monitor is enabled when this command is executed, the command is ignored and a Q=0 response is returned.

Once the monitor is enabled, the timeout counter starts. The counter is reloaded whenever a 1553 message word is received from either channel. If a 1553 message word is not received on either channel for the pre-programmed interval, the Monitor Timeout bit is set. This status bit can be read through the LAM Status register of the 3315. A LAM may be generated, if enabled, in response to the Monitor Timeout.

After a Monitor Timeout occurs, it remains set until the Monitor Timeout Counter is written with a new count value. To write the new value, disable 1553 monitoring and execute the F(17)A(2) command with the new data.