

Model 3320-Z1A

Time Code Interface

INSTRUCTION MANUAL

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Model 3320-Z1A

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KineticSystems Corporation

Standardized Data Acquisition and Control Systems

3320

Time Code Interface

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FEATURES

- Time-of-year information for a CAMAC-based system
- Time resolution of one millisecond
- Interface for the Datum Model 9300A Time Generator
- Internal crystal-controlled counter can be strap-selected
- Sixteen-word scratchpad memory

APPLICATIONS

- Data acquisition
- Jet engine testing
- Rocket engine testing
- Missile system testing

GENERAL DESCRIPTION *(Product specifications and descriptions subject to change without notice.)*

The Model 3320 is a single-width CAMAC module that provides time stamp information for a CAMAC-based data acquisition system. This module can be used alone or in conjunction with a Datum Model 9300A Time Code Generator/Translator. In data acquisition, it is often important to provide time information for each block of data acquired. Reading the 3320 allows the time stamp to be included in the acquired data block.

The Datum Generator/Translator or an internal crystal-controlled counter chain provides timing information to the 3320 with a 44-bit parallel BCD representation for days, hours, seconds, and milliseconds. The time code has a resolution of one millisecond. The Datum unit can use an IRIG-B time code or an internal clock as the original time source. The internal oscillator provides an accuracy of $\pm 0.01\%$.

Time code information is "frozen" in a 3320 register by an F(25)·A(0) execute command or by a front-panel TTL-level pulse. The 44-bit BCD pattern for this stored time is then read by the following commands:

F(0)·A(0), F(16)·A(0)

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
	----- SECONDS -----				----- MILLISECONDS -----											
BCD Code	8	4	2	1	800	400	200	100	80	40	20	10	8	4	2	1

F(0)·A(1), F(16)·A(1)

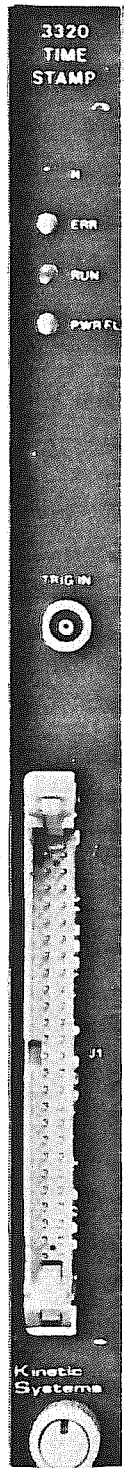
Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
	----- HOURS -----				----- MINUTES -----				----- SECONDS -----							
BCD Code	20	10	8	4	2	1	40	20	10	8	4	2	1	40	20	10

F(0)·A(2), F(16)·A(2)

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
	----- READ AS ZERO -----				----- DAYS -----											
BCD Code					800	400	200	100	80	40	20	10	8	4	2	1

Note: Bits 17 through 24 in all three registers are always read as ZERO.

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GENERAL DESCRIPTION (continued)

During acquisition, the F(25)·A(0) command is normally followed by three (or four) Read commands. Subsequent Read commands will result in the same data until another F(25) command is executed. The module contains special buffering to preclude any metastable effects caused by changing data in the time source during acquisition. A watchdog timer is included to monitor the one-millisecond strobe from the time source. If a subsequent strobe does not occur within 1.5 milliseconds, then the 44-bit word is set to an all-ONEs error state until the proper strobe rate returns. An ERROR LED on the front panel will light (extended by a one-shot) to indicate the error state. The current state of the ERROR watchdog timer can be checked by an F(27) Q-test command. Also, if an F(25) command is executed while in an error state, it will "freeze" this all-ONEs error pattern. Subsequent F(0) Read operations will then result in a 44-bit all-ONEs pattern (until an F(25) command stores good data).

The 3320 also contains a 16-word x 16 scratchpad memory. This general-purpose RAM memory can be written or read, 16 bits at a time, using CAMAC Subaddresses A(0) through A(15). One application for this memory in a data acquisition system is to provide a set of unique (or nearly unique) words to form a sync header. The memory can be written during set-up and the appropriate number of words read as part of each acquisition block.

FUNCTION CODES

Command	Q	Action
F(0)·A(0) RD1	1	Reads the LOW section of the time word (MS1 to S8).
F(0)·A(1) RD1	1	Reads the MIDDLE section of the time word (S10 to H20).
F(0)·A(2) RD1	1	Reads the HIGH section of the time word (D1 to D800).
F(0)·A(3) RD1	1	Reads as all ZEROs. Can be used to provide an even number of 16-bit Read words.
F(1)·A(i) RD2	1	Reads the scratchpad memory element (i). (See Note 2.)
F(9)·A(0) CL1	1	Allows a subsequent front-panel pulse to "freeze" the time data.
F(16)·A(i) WT1	1	Writes the time word. (See Note 3.)
F(17)·A(i) WT2	1	Writes the scratchpad memory element (i). (See Note 2.)
F(25)·A(0) XEQ	1	Updates the 44-bit time code for subsequent reading by F(0) commands.
F(27)·A(0) TST	OK	Tests the state of the Datum pulse watchdog timer (Q = 0 if ERROR, Q = 1 if OK).
Z CZ	1	Sets the 44-bit register to an all-ONEs state; Z does not affect the memory state.

Notes: 1. X = 1 for all valid addressed commands.
 2. Subaddress (i) ranges from 0 to 15.
 3. Subaddress (i) can range from 0 to 2 and follows the same pattern as the F(0) commands. The data should be written with subaddress (0) first (this disables the clock), and subaddress (2) last (this re-enables the clock). These commands are utilized ONLY if the 3320 is used alone.

FRONT PANEL

A 50-contact connector is provided to connect a flat ribbon cable to the Datum Generator/Translator. An 'N' LED flashes whenever the module is addressed. An ERROR LED is ON whenever the one-millisecond strobe from the Datum unit is missing.

POWER REQUIREMENTS

+6 volts — 1650 mA

ORDERING INFORMATION

Weight: .70 kg (1 lb. 8 oz.)

Model 3320-Z1A — Time Code Interface

Accessories — Datum Model 9300-7361 (or equivalent) Time Code Generator/Translator
 Model 5862-Lxyz Interconnection Cable Assembly (Datum to 3320)
 Model 5910-Z1A Mating Connector

Model 3320-Z1A

EXTERNAL UPDATES

Added to the 3320 is the ability to "Freeze" the time code information with an External Update Pulse. This low true pulse is brought in via the front panel on a single pin LEMO.

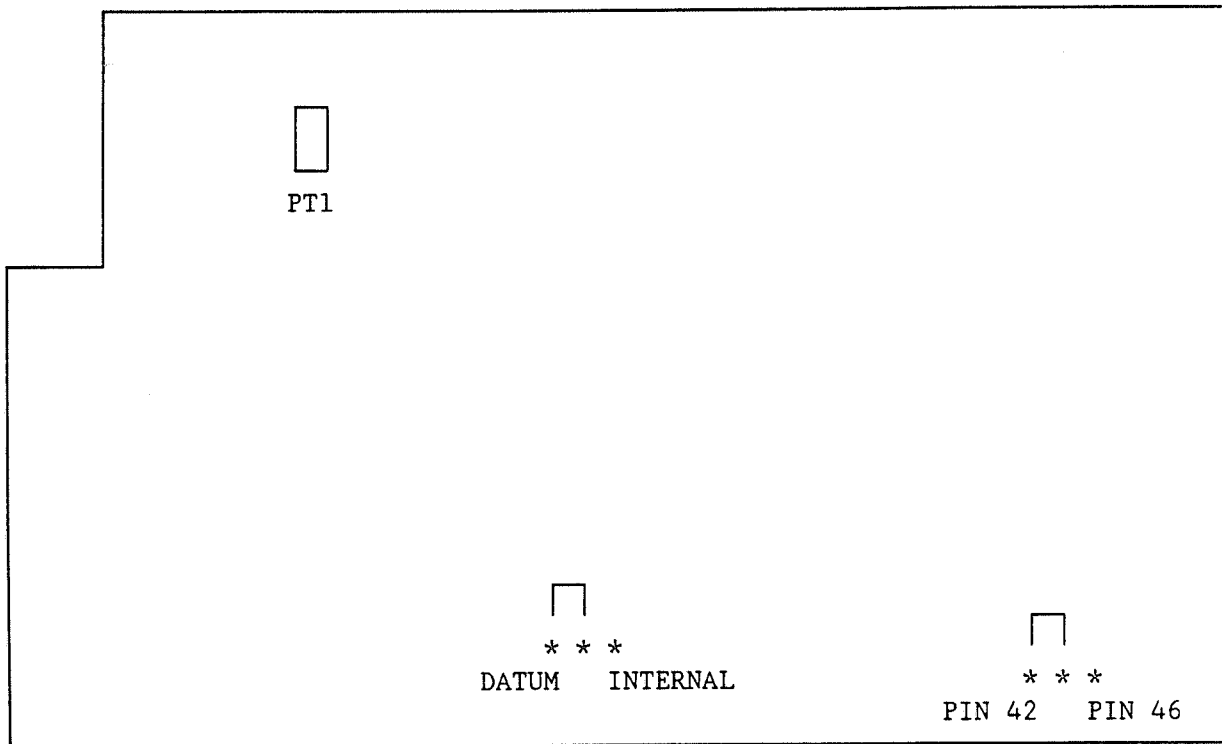
A pull-up is provided to prevent unwanted updates from occurring. Time code information is "Frozen" on a low transition of External Update. The 44-bit BCD pattern can then be read by the appropriate commands. Gating is provided to prevent the time code information from changing while the reads are occurring.

Once an External Update is received and the time code information read out, an F9 A0 command must be executed in order to allow further updates to occur.

REAL TIME CLOCK CIRCUIT

On-board is the counter circuitry for providing the 44 bits of parallel time code information. This on-board counter is loaded by three write commands (F(16).A(0), F(16).A(1), F(16).A(2)) from the dataway. The pattern for data for these writes is the same as for reads and is shown in the register layout. On power-up the counter is inhibited from counting and must be written using F(16).A(0) first and F(16).A(2) last. This sequence is necessary for the counter to start running. A green LED is provided on the front panel which flashes every second to indicate that the counter is running. A strap is provided to select either the datum unit or the internal counter as the time source. When the internal counter is selected the 3320 should not be connected to the datum unit, as both internal counter and datum unit will attempt to drive the data lines. A strap is also provided to allow the sample pulse to enter on pin 46 or pin 42 of the connector to match the datum unit pinout. A LED is also provided which indicates a loss of power since the internal counter was loaded. The state of the power fail error can be checked with an F27 Q-test command when strapped for internal counter.

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3320 STRAP LOCATION

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SOCKET/WIRE LIST
50 SOCKET RIBBON CONN.

SOCKET NO.

50	GROUND
49	M20
48	GROUND
47	M10
46	SAMPLE
45	M8
44	GROUND
43	M4
42	SAMPLE
41	M2
40	NO CONNECTION
39	M1
38	D800
37	S40
36	D400
35	S20
34	D200
33	S10
32	D100
31	S8
30	D80
29	S4
28	D40
27	S2
26	D20

SOCKET NO.

25	S1
24	D10
23	MS800
22	D8
21	MS400
20	D4
19	MS200
18	D2
17	MS100
16	D1
15	MS80
14	H20
13	MS40
12	H10
11	MS20
10	H8
9	MS10
8	H4
7	MS8
6	H2
5	MS4
4	H1
3	MS2
2	M40
1	MS1