Preliminary Model 3321

IRIG-B Time Code Interface

INSTRUCTION MANUAL

May 10, 1999

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IRIG-B Time Code Interface

Provides time code from an internal clock or an IRIG-B source **3321**

Features

- **Provides time-of-year information for a CAMAC-based system**
- **Has a time resolution of one millisecond**
- **Uses an IRIG-B time code input from a GPS receiver or other precision time source**
- **Internal crystal-controlled source is automatically selected when a IRIG-B signal is not present**
- **Internal source exhibits an accuracy of ±5 ppm or better from +10° C to +50° C**
- **16-word scratchpad memory**

Typical Applications

- **Data acquisition**
- **Jet engine testing**
- **Rocket engine testing**
- **Missile system testing**

General Description *(Product specifications and descriptions subject to change without notice.)*

The 3321 is a single-width CAMAC module that provides time stamp information for a CAMAC-based data acquisition system. In data acquisition, it is often important to provide time information for each block of data acquired. The 3321 provides that utility.

This module is designed to receive an industry-standard IRIG-B time source from a GPS (Global Positioning System) receiver or other precision time source. IRIG-B is a 1000 Hz amplitude-modulated signal and contains data for seconds, minutes, hours, days and years. The 1000 Hz carrier adds milliseconds to the stored data. The 3321 presents a high-impedance path to the time code signal so that many devices can be accommodated by a single IRIG-B signal source. If a valid IRIG-B source is not present, the module automatically reverts to an internal crystal-controlled oscillator. The presence of the IRIG-B signal can be tested by software.

Time code information is "frozen" in a 3321 register by an F(25)·A(0) execute command. The 44-bit BCD pattern for this stored time is then read by the following commands:

F(0)·A(0), F(16)·A(0) Lower Time Code Word

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
		SECONDS			MILLISECONDS											
BCD Code	8	4	2	1	800	400	200	100	80	40	20	10	8	4	2	1

F(0)·A(1), F(16)·A(1) Middle Time Code Word

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
			HOURS						MINUTES						SECONDS	
BCD Code	20	10	8	4	2	1	40	20	10	8	4	2	1	40	20	10

F(0)·A(2), F(16)·A(2) Upper Time Code Word

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
	See	Read as "0"			DAYS											
BCD Code	Note				800	400	200	100	80	40	20	10	8	4	2	1

F(0)·A(3) Time Since Active IRIG-B Source (read only)

Read Bits	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
	TIME SINCE IRIG-B ACTIVE (SECONDS)															
Binary Code	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

General Description (continued)

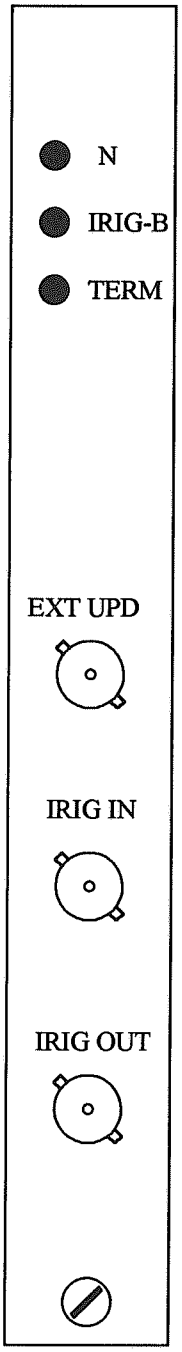
During acquisition, the F(25)·A(0) command is normally followed by three Read commands at F(0)·A(0), A(1) and A(2), respectively. Subsequent Read commands will result in the same data until another F(25) command is executed. This procedure is necessary to assure that all of the read information is from the same time snapshot. An internal oscillator is time-locked to the 1000 Hz carrier of the IRIG signal. If this signal is not present, the crystal-controlled oscillator is used as the time source. As long as the signal is present *and* a new IRIG-B code is stored once each second, the IRIG-B LED on the front panel will be lighted. The current state of the IRIG-B watchdog timer can be checked by an F(27) Q-test command (Q=1 indicates that a valid IRIG-B signal is present). A status word can be read at F(0)·A(3). This 16-bit binary word represents the number of seconds since the last IRIG-B update. If the IRIG-B signal is currently present, this word is read as zero. For internal clock operation the three data words can be written at F(16)·A(0), A(1) and A(20, respectively. If the IRIG-B source is currently active, the data will not be written into the registers and a Q=0 response will be given.

Front Panel

Two BNC connectors are provided, one to receive the IRIG-B signal and the other to pass it on, if desired. An "N" LED flashes whenever the module is addressed. An IRIG-B LED is ON whenever the module is receiving an IRIG-B carrier and valid IRIG-B code information. A TERM LED indicates that the programmable 1000 Ω termination is switched IN. When this termination is active, the IRIG-B signal is not passed on to the IRIG-B OUT connector.

Ordering Information

Model 3321-Z1A IRIG-B Time Code Interface


N
IRIG-B
TERM
EXT UPD
IRIG IN
IRIG OUT

3321 Front Panel LEDs and Connectors

The 3321 front panel contains 3 Light Emitting Diodes (LEDs) and 3 BNC connectors. The LEDs reflect current status of the 3321 and the BNC connectors allow the various signals to be connected to the 3321.

LEDs

The 3321 contains three front panel mounted LEDs, one red LED and two green LEDs. The following describes each LED.

N-LED. The N-LED is a one-shot extended red LED that is illuminated whenever the 3321 is addressed.

IRIG-B. The IRIG-B LED is a one-shot extended green LED that is illuminated as long as the 3321 detects a valid IRIG-B carrier clock.

TERM. The TERM LED is a green LED that is illuminated when the IRIG-B IN connector is terminated. This termination is a 1000 ohm resistor that ties the IRIG-B input signal to +5 volts. On power-up, the termination is not connected to the input signal. The termination is enabled by executing an F(26)A(1) command and disabled by an F(24)A(1) command addressed to the 3321.

Connectors

The 3321 contains three front panel mounted BNC connectors. Two of these connectors are used for the IRIG-B signals and the other is used to update the current time register via an external source.

IRIG-B IN. The IRIG-B IN BNC connector is used to connect the IRIG-B source signal into the 3321. The IRIG-B signal can be terminated at this connector by executing an F(26)A(1) command to the 3321 and the termination can be removed by executing an F(24)A(1) command to the 3321.

IRIG-B OUT. The IRIG-B OUT BNC connector is used to daisy chain the IRIG-B signal from a 3321 to another IRIG-B sink. When the 3321 does not have the termination enabled, the IRIG-B OUT BNC connector is connected to the IRIG-B IN BNC connector. Once termination has been enabled, the IRIG-B IN connector has a 1000 ohm resistor connector to the signal to +5 volts. In this case, the IRIG-B OUT connector is disconnected from the IRIG signal.

EXTERNAL UPDATE. The EXTERNAL UPDATE BNC connector is an input to the 3321 and is used as a mechanism to update the 44-bit IRIG-B time data word. The updating of this 44 bit BCD data word can occur through this external update signal or by CAMAC command (F(25)A(0)).

The External Update signal applied to the 3321 must be a low going pulse that has a minimum pulse duration of 500 nanoseconds. This input to the 3321 is received by a

74LS244 device and is terminated with a 180 ohm resistor to +5 volts and a 390 ohm resistor to ground.

CAMAC Command List

Command	Q	X	Action
F(0)A(0)	1	1	Read Time Word Low
F(0)A(1)	1	1	Read Time Word Middle
F(0)A(2)	1	1	Read Time Word High
F(0)A(3)	1	1	Read IRIG-B Inactive Time
F(1)A(i)	1	1	Read RAM / RAM Address
F(16)A(0)	1	1	Write Time Word Low
F(16)A(1)	1	1	Write Time Word Middle
F(16)A(2)	1	1	Write Time Word High
F(17)A(i)	1	1	Write RAM / RAM Address
F(24)A(0)	1	1	Disable Full RAM Addressing
F(24)A(1)	1	1	Disable IRIG-B Termination
F(25)A(0)	1	1	'Freeze' Time Data
F(26)A(0)	1	1	Enable Full RAM Addressing
F(26)A(1)	1	1	Enable IRIG-B Termination
F(27)A(0)	IRIG_ACTIVE	1	Test for IRIG-B Active

CAMAC Command Description

The following section details each CAMAC command available on the 3321.

F(0)A(0), F(0)A(1), F(0)A(2) – Read Time Word Low, Middle and High

These three CAMAC commands are used to read the 44 bit Binary Coded Decimal (BCD) word from the 3321. This 44-bit word is read out with three CAMAC commands. Before these 3 registers are read, an F(25)A(0) must be executed to the 3321 to 'freeze' the data for static readout. This procedure must be followed in order to update the readout value. Failure to follow this procedure will result in the same data being read out.

The following diagram shows the three read commands and the portion of the BCD time read for each.

F(0)A(0) – Read Time Word Low

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SEC 8	SEC 4	SEC 2	SEC 1	MS 800	MS 400	MS 200	MS 100	MS 80	MS 40	MS 20	MS 10	MS 8	MS 4	MS 2	MS 1

F(0)A(1) – Read Time Word Middle

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
HR 20	HR 10	HR 8	HR 4	HR 2	HR 1	MIN 40	MIN 20	MIN 10	MIN 8	MIN 4	MIN 2	MIN 1	SEC 40	SEC 20	SEC 10

F(0)A(2) – Read Time Word High

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
IRG ACT	0	0	0	DAY 800	DAY 400	DAY 200	DAY 100	DAY 80	DAY 40	DAY 20	DAY 10	DAY 8	DAY 4	DAY 2	DAY 1

The MSx bit locations are the BCD representation of the number of milliseconds recorded.

The SECx bit locations are the BCD representation of the number of seconds recorded.

The MINx bit locations are the BCD representation of the number of minutes recorded.

The HRx bit locations are the BCD representation of the number of hours recorded.

The DAYx bit locations are the number of days recorded.

The IRG ACT bit is a strap selectable bit location that may be used to reflect the status of the IRIG-OK signal. If the 3321 is receiving valid IRIG-B data and the option is enabled, this bit is read back as a one. If the option is enabled and the 3321 is not receiving valid IRIG-B data, this bit is read back as a zero. Please refer to the Strap Selection section of this manual for additional information.

F(0)A(3) – Read IRIG-B Inactive Time

The F(0)A(3) CAMAC command is used to read the IRIG-B Inactive Time Register. This register indicates the duration of time that the IRIG-B signal has been inactive. This value has a resolution of 1 second and has a maximum value of 65535 seconds. This register is incremented every second as long as the IRIG-B signal is absent. If the IRIG-B signal is connected to the 3321, this register is reset to zero until IRIG-B is again removed.

The format of this register is shown in the following diagram.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ACT 16	ACT 15	ACT 14	ACT 13	ACT 12	ACT 11	ACT 10	ACT 9	ACT 8	ACT 7	ACT 6	ACT 5	ACT 4	ACT 3	ACT 2	ACT 1

ACTx are read-only bits that reflect the duration of time that the IRIG-B signal has been inactive to the 3321. The resolution of this register is 1 second.

F(0)A(I) – Read RAM / RAM Address

This command actually performs two functions, depending on the configuration of the RAM. The 3321 contains a 32K x 16 Static RAM (SRAM). This RAM can be

accessed with two modes. In one mode only 16 locations of the SRAM may be accessed. Each individual Subaddress accesses an exclusive location within the SRAM. In the second mode, all 32K of the SRAM can be accessed and the addressing is controlled by an address counter on the 3321. These two modes are selected using the Enable Full RAM Addressing and Disable Full RAM Addressing commands. The 16-location SRAM access is selected on power-up when the Full RAM Addressing is disabled. The Full RAM Addressing may then be enabled by using the Enable Full RAM Addressing command.

When using the 16 location SRAM addressing scheme, each Subaddress accesses an individual memory location. F(1)A(0) accesses the first memory location; F(1)A(1) accesses the second memory location and so on.

When using the full 32K SRAM option, an address counter on the 3321 is incorporated. This address register is written with an F(17)A(1) command and read with an F(1)A(1) command. This address register is 15 bits in length to allow the full 32K addressing. Before an initial attempt is made to write or read from the SRAM in this mode, the RAM Address Register must first be loaded with the RAM address location to be accessed. After this register is loaded, subsequent accesses to the memory automatically increment this register to the next sequential location. After the RAM Address is loaded, the memory may then be read by an F(1)A(0) command.

16 Word Addressing Mode:

F(1)A(i)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM 16	RAM 15	RAM 14	RAM 13	RAM 12	RAM 11	RAM 10	RAM 9	RAM 8	RAM 7	RAM 6	RAM 5	RAM 4	RAM 3	RAM 2	RAM 1

RAMxx are write/read bits used to access the SRAM.

32KWord Addressing Mode:

F(1)A(0)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM 16	RAM 15	RAM 14	RAM 13	RAM 12	RAM 11	RAM 10	RAM 9	RAM 8	RAM 7	RAM 6	RAM 5	RAM 4	RAM 3	RAM 2	RAM 1

RAMxx are write/read bits used to access the SRAM.

F(1)A(1)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	RAD 15	RAD 14	RAD 13	RAD 12	RAD 11	RAD 10	RAD 9	RAD 8	RAD 7	RAD 6	RAD 5	RAD 4	RAD 3	RAD 2	RAD 1

RADxx are write/read bits used to specify the SRAM address at which subsequent read or write operations are to be directed.

F(16)A(0), F(16)A(1), F(16)A(2) – WriteTime Word Low, Middle and High

These three CAMAC commands are used to preload the 44 bit Binary Coded Decimal (BCD) word on the 3321 when using the onboard counter. This 44-bit word is loaded by using three CAMAC commands.

The following diagram shows the three write commands and the portion of the BCD time read for each.

F(16)A(0) – Write Time Word Low

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SEC 8	SEC 4	SEC 2	SEC 1	MS 800	MS 400	MS 200	MS 100	MS 80	MS 40	MS 20	MS 10	MS 8	MS 4	MS 2	MS 1

F(16)A(1) – Write Time Word Middle

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
HR 20	HR 10	HR 8	HR 4	HR 2	HR 1	MIN 40	MIN 20	MIN 10	MIN 8	MIN 4	MIN 2	MIN 1	SEC 40	SEC 20	SEC 10

F(16)A(2) – Write Time Word High

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	0	0	DAY 800	DAY 400	DAY 200	DAY 100	DAY 80	DAY 40	DAY 20	DAY 10	DAY 8	DAY 4	DAY 2	DAY 1

The MSx bit locations are the BCD representation of the number of milliseconds recorded.

The SECx bit locations are the BCD representation of the number of seconds recorded.

The MINx bit locations are the BCD representation of the number of minutes recorded.

The HRx bit locations are the BCD representation of the number of hours recorded.

The DAYx bit locations are the number of days recorded.

F(17)A(I) – write RAM / RAM Address

This command actually performs two functions, depending on the configuration of the RAM. The 3321 contains a 32K x 16 Static RAM (SRAM). This RAM can be accessed with two modes. In one mode only 16 locations of the SRAM may be accessed. Each individual Subaddress accesses an exclusive location within the SRAM. In the second mode, all 32K of the SRAM can be accessed and the addressing is controlled by an address counter on the 3321. These two modes are selected using the Enable Full RAM Addressing and Disable Full RAM Addressing

commands. The 16 location SRAM access is selected on power-up when the Full RAM Addressing is disabled. The Full RAM Addressing may then be enabled by using the Enable Full RAM Addressing command. When using the 16 location SRAM addressing scheme, each Subaddress accesses an individual memory location. F(17)A(0) accesses the first memory location, F(17)A(1) accesses the second memory location and so on.

When using the full 32K SRAM option, an address counter on the 3321 is incorporated. This address register is written with an F(17)A(1) command and read with an F(1)A(1) command. This address register is 15 bits in length to allow the full 32K addressing. Before an initial attempt is made to write or read from the SRAM in this mode, the RAM Address Register must first be loaded with the RAM address location to be accessed. After this register is loaded, subsequent accesses to the memory automatically increment this register to the next sequential location. After the RAM Address is loaded, the memory may then be read by an F(1)A(0) command.

16 Word Addressing Mode:

F(17)A(i)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM 16	RAM 15	RAM 14	RAM 13	RAM 12	RAM 11	RAM 10	RAM 9	RAM 8	RAM 7	RAM 6	RAM 5	RAM 4	RAM 3	RAM 2	RAM 1

RAMxx are write/read bits used to access the SRAM.

32KWord Addressing Mode:

F(17)A(0)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
RAM 16	RAM 15	RAM 14	RAM 13	RAM 12	RAM 11	RAM 10	RAM 9	RAM 8	RAM 7	RAM 6	RAM 5	RAM 4	RAM 3	RAM 2	RAM 1

RAMxx are write/read bits used to access the SRAM.

F(17)A(1)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	RAD 15	RAD 14	RAD 13	RAD 12	RAD 11	RAD 10	RAD 9	RAD 8	RAD 7	RAD 6	RAD 5	RAD 4	RAD 3	RAD 2	RAD 1

RADxx are write/read bits used to specify the SRAM address at which subsequent read or write operations are to be directed.

F(24)A(0) – Disable Full RAM Addressing

The F(24)A(0) command is used to disable the SRAM Full Addressing Mode. The SRAM Full Addressing Mode provides access to the entire 32Kword SRAM by

incorporating an Address Register. This Address Register is written with an F(17)A(1) command and read with an F(1)A(1) command. The SRAM itself is then written with an F(17)A(0) and read with an F(1)A(0).

When the 3321 is power-up, the Full RAM Addressing mode is disabled. In this configuration only 16 locations of the SRAM may be accessed. Each location is written with an F(17)A(I) command and read with an F(1)A(I) command. The Subaddress can range from 0 to 15 which provides access to the 16 locations.

F(24)A(1) – Disable IRIG-B Termination

The F(24)A(1) command is used to disable the IRIG-B 1000 ohm termination resistor from the IRIG-B IN BNC connector and pass the IRIG-B IN signal to the IRIG-B OUT signal. The termination resistor connects the IRIG-B IN signal to the resistor which is in turn connected to +5 volts. When the 3321 is powered-up, the termination is disabled.

F(25)A(0) –'Freeze' Time Data

The F(25)A(0) command is used to 'freeze' the time code data. This command must be used before a read of the time code data registers. This command causes the time code data to be latched into a set of registers for later readout. Failure to execute this command before reading the three time code data registers results in 'old' data being presented.

F(26)A(0) – Enable Full RAM Addressing

The F(24)A(0) command is used to enable the 3321 to access the full address range of the 32K x 16 SRAM. When the 3321is powered up, this mode is disabled and the maximum addressing for the SRAM is 16 locations. If it is required to access more than 16 location in the SRAM, the Full RAM Addressing must be enabled. When using this mode, all 32K of the SRAM may be accessed. When enabled, an internal address counter is used to provide the SRAM address. The SRAM Address Register is loaded with an F(17)A(1) command and read with an F(1)A(1) command. The SRAM data itself is then written with an F(17)A(0) command and read with an F(1)A(0) command. In this mode, each access to the SRAM, be it write or read, increments the SRAM Address Register to the next sequential location. This eliminates the requirement of reloading the address register for each memory access.

The Full RAM Addressing mode is disabled with an F(26)A(0) command.

F(26)A(1) – Enable IRIG-B Termination

The F(26)A(1) command is used to enable IRIG-B termination. The termination is a 1000 ohm resistor connected to +5 volts. When this command is executed, the termination resistor is connected from the IRIG-B IN BNC connector and the

IRIG-B OUT connector is disconnected from the IRIG-B OUT BNC connector. After power is applied to the 3321, the IRIG-B termination is disabled. This CAMAC command must then be executed to the last 3321 in the IRIG chain to terminate the signal.

F(27)A(0) – Test for IRIG-B Active

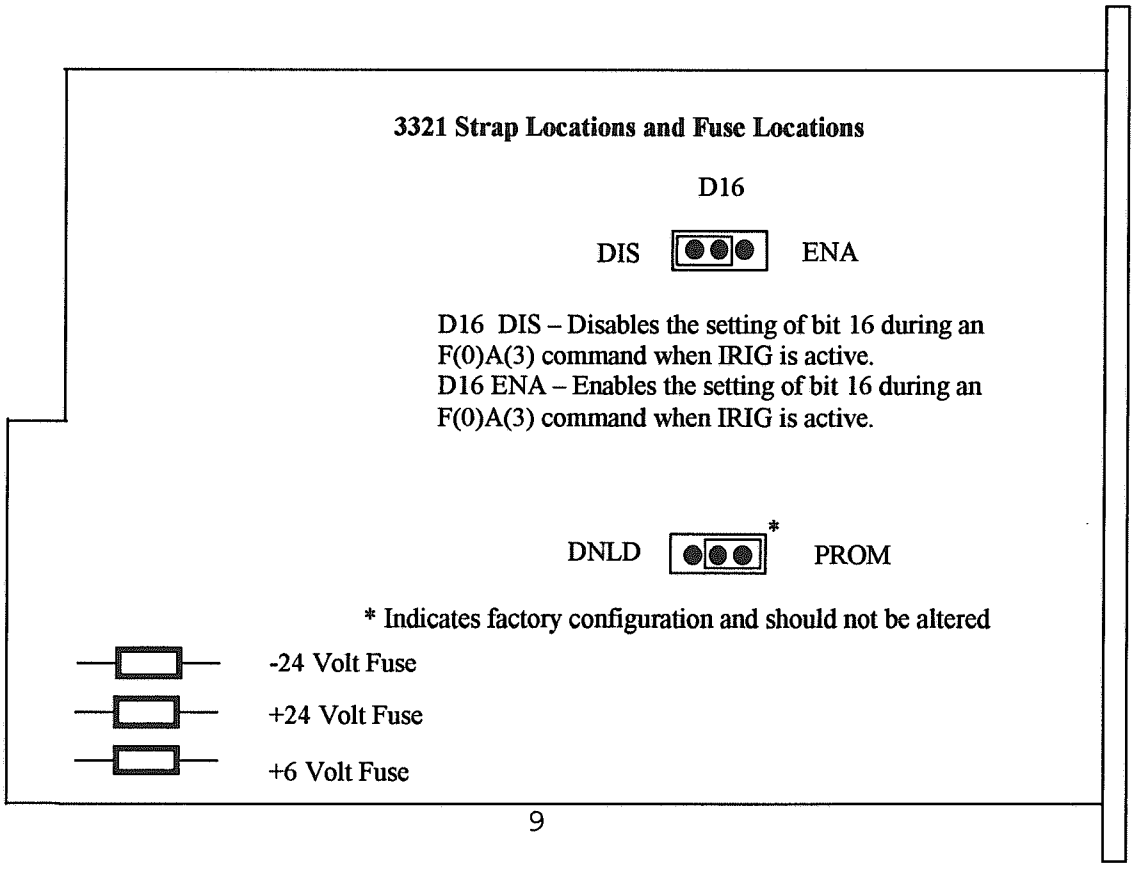
The F(27)A(0) command is used to check for the presence of the IRIG-B signal on the IRIG-B IN BNC connector of the 3321. If the 3321 is receiving a valid carrier clock on this connector, the 3321 is receiving a valid IRIG-B stream. If the F(27) (0) command is executed and the 3321 is receiving a valid IRIG-B signal, this command returns a Q-response of one. If the F(27)A(0) command is executed and the 3321 is not receiving a valid IRIG-B signal, this command returns a Q-response of zero.

The indication of valid IRIG-B data reception by the 3321 can also be detected when reading the time data information from the 3321. Please refer to the F(0)A(2) command for additional information.

Strap Locations

The following section details the various strap selections available on the 3321. Two strap locations are contained on the board. Only one of these straps should be altered by the user. The other strap location is reserved for factory testing of the 3321 and should be left in the position as configured at the factory.

The following diagram shows the strap location and other location information concerning components on the 3321 PC card.



The DNLD/PROM strap is factory configured for the PROM position and should not be altered by the user. This strap is for factory testing.

The D16 DIS/ENA strap is used to enable and disable a status bit found in the third time code data word F(0)A(2) in bit position 16. This bit indicates whether the 3321 is providing time code data words generated from the IRIG-B incoming data stream or from the internal counters on the 3321.

If the D16 DIS/ENA strap is placed in the DISABLE (DIS) position, bit 16 of the third time code word is always read as a zero. If the strap is placed in the ENABLE (ENA) position, bit 16 of the third time code word reflects the status of the incoming IRIG-B data stream. If the IRIG-B stream is providing time code information to the 3321, this bit is read as a one. If for some reason the IRIG-B data stream is not provided to the 3321 and it reverts to using its internal counters to provide the time code information, this bit is read back as a zero.

Using the 3321 To Read IRIG-B Data

This section describes how to setup, read IRIG-B data and interpret data read from the 3321. Before data can be read from the 3321, the following sequence should be performed. This sequence assumes that one is using the 3321 to read IRIG-B data from an IRIG source and not data generated from the internal clock.

1.) Before installing the 3321 into the CAMAC chassis, decide whether to enable or disable the D16 READ IRIG-B ACTIVE signal during readout. For information regarding this strap configurable option, please refer to the Strap Locations section of this manual for additional information.
2.) With the CAMAC chassis powered off, install the 3321 into any unoccupied slot in the chassis.
3.) Connect the IRIG-B source into the 3321 to the IRIG-B BNC connector.
4.) If additional IRIG-B sinks are to be included in the chain, install a BNC cable from the IRIG-B OUT BNC connector to the next IRIG-B sink's IRIG-B IN BNC connector.
5.) If it is desired to update the 44-bit time word from an external source, connect this update source to the EXTERNAL UPDATE BNC connector. Please refer to the ***3321 Front Panel and Connectors*** section of this manual for additional information.
6.) Apply power to the CAMAC chassis.
7.) If the 3321 is the last IRIG-B sink, terminate the IRIG-B signal by executing an F(26)A(1) addressed to the 3321. This CAMAC command causes the 3321 to terminate the IRIG-B input signal to +5 volts through a 1000 ohm resistor. When termination is enabled, the IRIG-B signal does not propagate through the 3321 to the IRIG-B OUT connector.
8.) The 3321 is now configured to read IRIG-B data. If the external update is used, the F(25)A(0) command is not necessary. The 44-bit time data word is updated at the rate supplied by the External Update signal. If the external update is not used, an F(25)A(0) command must be executed to the 3321 to 'freeze' the 44-bit time data word. Failure to execute this command before reading the time data words results in the 'stale data'.
9.) After the time data word is latched, it may then be read out of the 3321. The first read command addressed to the 3321 is the F(0)A(0) command. This command returns the Milliseconds field of the time data word and the units digits of the Seconds field.
10.) Next, execute an F(0)A(1) to the 3321. This read command returns the tens of Seconds field, the Minutes field, and the Hours field.

11.) The Days field can then be read from the 3321 by executing an F(0)A(2) command. If the D16 Read enable strap was enabled, bit 16 of this register contains an IRIG status bit. If the bit is read as a one, the time read is from the IRIG-B data stream. If for some reason the IRIG-B data stream is not provided to the 3321, this bit will be read back as a zero.

WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

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Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

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1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com