3-channel, Digital-to-synchro Converter

INSTRUCTION MANUAL

March, 1992

(C) 1986, 1987, 1992 Copyright by KineticSystems Corporation Lockport, Illinois All rights reserved

CONTENTS

Features and Applications	· · · · · · · · · · · · · · · · · · ·	1
General Description		1
Operation		1
Mode Control Register		1
Function Codes		2
Simplified Block Diagram		2
Specifications		2
Power Requirements & Weight		2
Ordaning Information		ถ
Ordering Information		4
SYSTEM SETUP		3
DATA FORMAT		3
UPDATE CONTROL		4
3395-A2A/E2A Pin Wire List		5
FIGURES		
		_
FIGURE 1 - Bit Weight		3
FIGURE 2 - Mode of Operation		4
Schematic Drawing # 122180-C-5803	See Reply Card Following Warrant	y
•	1,	•
Warranty		
vvairailty		
JRH:JPS:rem		

KineticSystems Corporation

Standardized Data Acquisition and Control Systems

3395

3-channel, Digital-to-synchro Converter

ADVANCE INFORMATION

©1986, 1987 (Rev. Jun. 87)

FEATURES

- Three-channel digital-to-synchro converter module with 16-bit resolution
- Total cumulative output error is less than ± 4 arc-minutes
- Rank 1/Rank 2 registers for simultaneous conversion
- Simultaneous conversions triggered from Dataway P1 line or front-panel input

APPLICATIONS

- · Driving control transformers
- Positioning control systems

GENERAL DESCRIPTION

The Model 3395 Digital-to-synchro Converter (DSC) module provides an interface between the CAMAC Dataway and standard three-wire synchro receivers, allowing the computer to control a device's angular position. It is a double-width module with three DSC channels; each channel contains a separate converter with 16 bits of resolution. The DSC outputs are brought to a 50-pin "D" connector on the front panel.

The 3395 accepts straight binary data, representing the desired angles (0 to 360 degrees) from the CAMAC Dataway. Setting the module's Mode Control register determines whether this data is passed directly to the selected DSC channel or held for subsequent, simultaneous conversion of all channels.

OPERATION

Data is written into the Rank 1 registers for each channel via F(16) commands. External control of the Rank 2 register (and DSC) update is selected by the Mode register. Rank 1 data can be copied directly into the Rank 2 register by the F(16) command for independent conversion; for simultaneous conversion, all three channels of data can be copied into the Rank 2 registers by a one microsecond pulse on the P1 or P2 Dataway lines or by a signal at the front-panel LEMO connector. There are five modes of external Rank 1/Rank 2 update control, determined by the contents of the Mode Control register. This register is written by an F(17)·A(0) command using Dataway bits W1-W3 (W1 = LSB). Rank 1 data can be copied into the Rank 2 register by an F(25)·A(0) command regardless of mode setting.

MODE CONTROL REGISTER

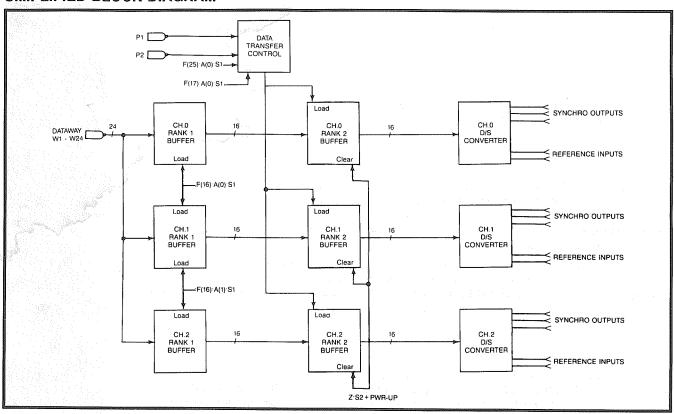
Mode	Control of Rank 1/Rank 2 Transfer	
0	Independent Channel Conversion	
1	Rank 1/Rank 2 Transfer on P1 pulse (See Note)	
2	Rank 1/Rank 2 Transfer on P2 pulse	
3	Rank 1/Rank 2 Transfer on P1 or P2 pulse (See Note)	
4	Rank 1/Rank 2 Transfer on P2 pulse, followed by P1 pulse	



FUNCTION CODES

Comma	nd	Q	Action		
F(16)·A(i)	WT1	1	Writes Channel i to Rank 1 register.		
F(17)·A(0)	WT2	1	Writes External Mode Control register.		
F(25)·A(0)	XEQ	1	Executes a Rank 1/Rank 2 data transfer on all channels.		
Notes: X = 1 for all valid addressed commands. i can range from 0 to 2.					

SIMPLIFIED BLOCK DIAGRAM



SPECIFICATIONS (for each channel, 25 degrees C, except where noted)

Resolution:	16 bits		
Reference signal input:	26 Vrms, 400 hertz		
Output rating:	11.8 Vrms line-to-line at 400 hertz		
Settling:	To within ½ LSB within 50 microseconds with a 179 degree step		
Performance:	Monotonic to 14 bits, 15 to 35 degrees C		
Total cumulative error:	Less than ±4 arc-minutes		
Output drive:	1.3 volt ampere (max)		

POWER REQUIREMENTS

+6 volts — 250 mA

+24 volts — 350 mA

-24 volts - 550 mA

ORDERING INFORMATION

Weight: 1.03 kg. (2 lb. 5 oz.)

Model 3395-A2A — 3-channel, 16-bit Digital-to-synchro Converter, 50-contact Ribbon Connector

Model 3395-E2A - 3-channel, 16-bit Digital-to-synchro Converter, 50-pin "D" Connector

Note: For high-speed applications, a packed data format of this module is available. Consult the factory for details.

Accessories

Model 5950-Z1A Mating Connector

Model 5934-Z1A Mating Connector

Models 1850-A1D or -E1D Rack Termination Panel

SYSTEM SETUP

The DSCs used on the 3395-A2A/E2A are designed for a 400 Hz reference frequency with a 26 volt RMS reference voltage $\pm 10\%$. Outputs are rated for an output of 11.8 volts RMS line-to-line signal voltage with a maximum drive capability of 1.3 volt-ampere.

Output connections to the 3395-A2A/E2A should be kept as short as possible. At distances less than 25 feet, twisted wire is preferred. For distances greater than 25 feet, it is advisable to use individually shielded multicore wire.

DATA FORMAT

The 3395-A2A/E2A accepts straight binary representation of the desired angles (0 to 360°) from the CAMAC Dataway using F16 commands. Figure 1 shows the bit weight for word lengths of 16 bits.

		Angle in		
Bit No.	Angle in Degrees/Decimals	Degrees	Arc. Mins.	Arc. Secs.
B15 MSB	180.00000	180	0	0.0
B14	90.00000	90	0	0.0
B13	45.00000	45	0	0.0
B12	22.40000	22	30	0.0
B11	11.25000	11	15	0.0
B10	5.62500	5	37	30.0
В9	2.81250	2	48	45.0
B8	1.40625	1	24	22.5
В7	0.70313	0	42	11.3
В6	0.35156 0 21		21	5.6
B5	0.17578	0	10	32.8
B4	0.08790	0	5	16.4
В3	0.04395	0	2	38.2
B2	0.02197	0	1	19.1
B1	0.01099		0	39.6
B0 LSB	0.00549	0	0	19.8

FIGURE 1

UPDATE CONTROL

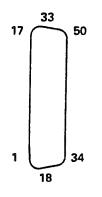
After the F(16) write commands, the data will stay in the Rank 1 registers (see simplified block diagram) until a Rank 2 register update pulse is received. The Rank 1 data is then simultaneously loaded into the Rank 2 register so that all DSCs are updated at the same time.

The updating of the Rank 2 registers is controlled by the Mode Control Register. This register responds to a F(17)A(0) command using Dataway bits W1-W3 (W1-LSB). Rank 1 data is copies to the Rank 2 register by an externally applied one-microsecond pulse to the P1 or P2 free Dataway bus line. Figure 2 shows each mode of operation and the function that causes a Rank 2 update. Rank 1 data may also be copied to the Rank 2 register by an F(25)A(0) command regardless of the mode settings.

Mode	Bits (W3-W1)	External Control of Rank 1/Rank 2 Transfer
0 to 3	(000-011)	Unused modes
4	(100)	P1 or P2 clock pulse
5	(101)	P2 clock pulse
6	(110)	P1 clock pulse
7	(111)	P2 pulse, followed by P1 pulse

NOTE: Upon initialization, the Mode Register is set to mode 7.

FIGURE 2



Pin/Wire List

50 PIN 'D'

FACE VIEW

PIN NO.		9141 A1G
17 DIGITAL GROUND	PIN NO.	PIN NO. DIGITAL GROUND
16	33	49
15		48
14	31	47
13		46
12		45
11 CHANNEL 2 S3		44
10 CHANNEL 2 S2	27	43
9 _ CHANNEL 2 S1		42
8 CHANNEL 2 RL	25	41
7 CHANNEL 2 RH		40
6	23	
5 CHANNEL 1 S3	CHANNEL 3 S3	39
4 CHANNEL 1 S2	21CHANNEL 3 S2	38
	20CHANNEL 3 S1	37
3 CHANNEL 1 S1	19 CHANNEL 3 RL	36
2 CHANNEL 1 RL	18 CHANNEL 3 RH	35
1 CHANNEL 1 RH	10	34