

Model 3474
48-bit Change-of-state Input Register

INSTRUCTION MANUAL

August, 1989

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*****SPECIAL OPTION*****

Model 3474-S001

48-Bit Change-of-state Input Register

May, 1991

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Model 3474-S001

*****SPECIAL OPTION*****

The Model 3474-S001, 48-Bit Change-of-State Input Register, functions the same as the Model 3474-A1A, except for the input circuits which have been modified to handle signals in the +60 to -60 volt range.

JRH:rem(WP)

May 17, 1991

*****SPECIAL OPTION*****

Model 3474-S002

48-Bit Change-of-state Input Register

May, 1991

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Model 3474-S002

*****SPECIAL OPTION*****

The Model 3474-S002, 48-Bit Change-of-state Input Register, functions the same as the Model 3474-A1A, except for the input circuits which have been modified to handle signals in the +100 to -100 volt range.

JRH:rem(WP)

May, 17, 1991

Model 3474

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March, 1988

Kinetic Systems Corporation

Standardized Data Acquisition and Control Systems

3474

48-bit Change-of-state Input Register

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FEATURES

- 48-bit voltage sense
- Change-of-state indication
- Inputs can range from +30 to -30 volts DC
- 100 millisecond input filter

APPLICATIONS

- Event monitoring
- Level detectors
- Alarms

GENERAL DESCRIPTION

The Model 3474 is a single-width CAMAC module providing 48 voltage sense circuits and change-of-state indication. The sense circuits detect changes in the voltage level at the input terminals and are suitable for sensing such remote process signals as limit switches and machine tool relay contacts as well as the transistorized output signals from NC and CNC machines.

In addition to contact-sense inputs, this module accepts signals with a potential as high as ± 30 volts, referenced to module ground. Input current at the switching threshold is 500 microamperes maximum for interfacing with circuits that have a high source impedance. This is accomplished by including a transistor input circuit which is set for a switching threshold of approximately -4.5 volts. A 100 millisecond timing delay on each channel provides noise immunity.

The 3474 contains a 48-bit memory register and a 48-bit comparator. If one or more of the inputs has changed state (1-to-0 or 0-to-1) since the last time the memory register was updated, a common LAM Status is set. This can produce a LAM Request directing the computer program to read the current state of the inputs.

The return path for all input circuits is module ground. If isolated inputs are required, the Model 3473 is recommended.

OPERATION

In the initialized state, the input register and the memory register of the 3474 contain the same data pattern. If any input changes state, a not-compare condition exists and the LAM status is set. This produces a LAM request (if enabled). In response to the LAM request, a program can execute an F(2)·A(0) and an F(2)·A(1) command. Executing these commands reads the new state of the inputs, updates the memory register to equal the input states, and clears the LAM status.

To determine the input states before any recent changes, an F(1)·A(0) and F(1)·A(1) command can be performed to read the state of the memory register. This must be done before executing either of the F(2) Read commands.

Note that the first change-of-state sets the LAM status, and no other indication is given (as other inputs change state) until an F(2)·A(0) or an F(2)·A(1) Read-and-Clear command is performed. The data staticize latch is disabled during the F(0) and F(2) commands to prevent ambiguous results if inputs are changing during that time.

3474
CONTACT
INPUT

N

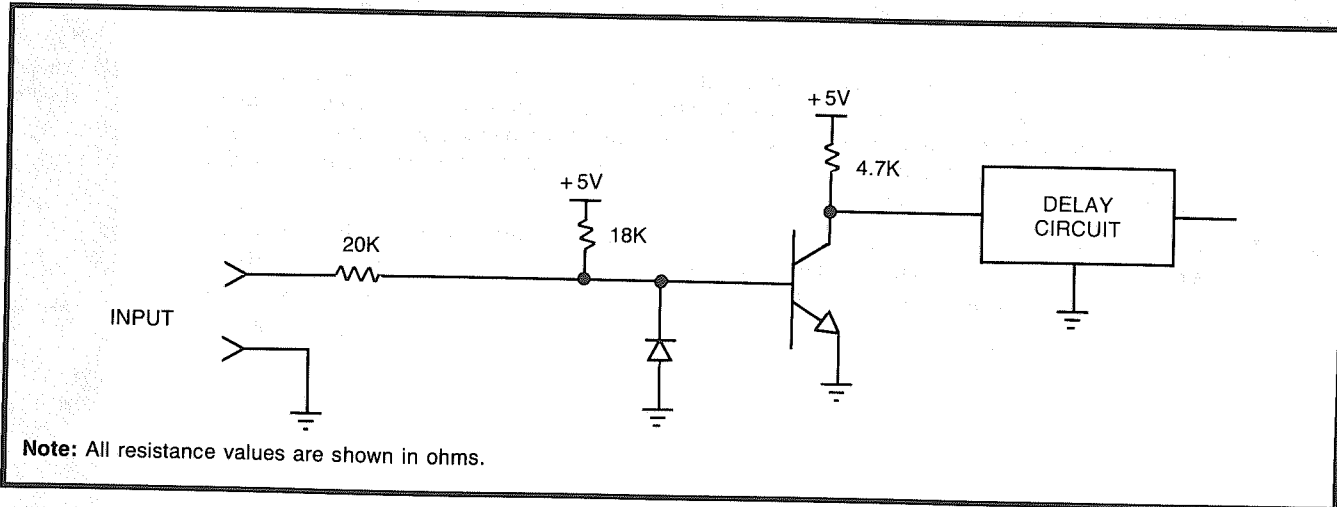
LAM

Kinetic
Systems

FUNCTION CODES

Command		Q	Action
F(0):A(0)	RD1	1	Reads the lower 24 bits of the Input register.
F(0):A(1)	RD1	1	Reads the upper 24 bits of the Input register.
F(1):A(0)	RD2	1	Reads the lower 24 bits of the Memory register.
F(1):A(1)	RD2	1	Reads the upper 24 bits of the Memory register.
F(2):A(0)	RC1	1	Reads the lower 24 bits of the Input register, updates the lower half of the Memory register, and clears the LAM status.
F(2):A(1)	RC1	1	Reads the upper 24 bits of the Input register, updates the upper half of the Memory register, and clears the LAM status.
F(8):A(15)	TLM	LR	Tests for the presence of a LAM request.
F(10):A(0)	CLM	1	Clears the LAM status.
F(24):A(0)	DIS	1	Disables the LAM request.
F(26):A(0)	ENB	1	Enables the LAM request.
F(27):A(0)	TST	I ≠ M	Tests for an equality between the state of the Input register and the Memory register.
Z	CZ		Initializes the Memory register, clears the LAM status, and disables the LAM request.

TYPICAL INPUT CIRCUIT



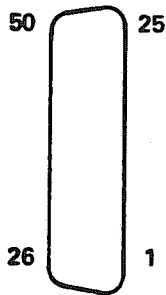
POWER REQUIREMENTS

+6 volts — 1020 mA

ORDERING INFORMATION

- Model 3474-A1A — 48-bit Change-of-state Input Register
- Accessories — Model 5950-Z1A Mating Connector
- Model 1850-A1D Rack Termination Panel

Weight: .46 kg. (1 lb.)



FACE VIEW

Socket/Wire List

50 SOCKET RIBBON CONN.

SOCKET NO.

50	GROUND
49	GROUND
48	INPUT SIGNAL 48
47	INPUT SIGNAL 47
46	INPUT SIGNAL 46
45	INPUT SIGNAL 45
44	INPUT SIGNAL 44
43	INPUT SIGNAL 43
42	INPUT SIGNAL 42
41	INPUT SIGNAL 41
40	INPUT SIGNAL 40
39	INPUT SIGNAL 39
38	INPUT SIGNAL 38
37	INPUT SIGNAL 37
36	INPUT SIGNAL 36
35	INPUT SIGNAL 35
34	INPUT SIGNAL 34
33	INPUT SIGNAL 33
32	INPUT SIGNAL 32
31	INPUT SIGNAL 31
30	INPUT SIGNAL 30
29	INPUT SIGNAL 29
28	INPUT SIGNAL 28
27	INPUT SIGNAL 27
26	INPUT SIGNAL 26

SOCKET NO.

25	INPUT SIGNAL 25
24	INPUT SIGNAL 24
23	INPUT SIGNAL 23
22	INPUT SIGNAL 22
21	INPUT SIGNAL 21
20	INPUT SIGNAL 20
19	INPUT SIGNAL 19
18	INPUT SIGNAL 18
17	INPUT SIGNAL 17
16	INPUT SIGNAL 16
15	INPUT SIGNAL 15
14	INPUT SIGNAL 14
13	INPUT SIGNAL 13
12	INPUT SIGNAL 12
11	INPUT SIGNAL 11
10	INPUT SIGNAL 10
9	INPUT SIGNAL 9
8	INPUT SIGNAL 8
7	INPUT SIGNAL 7
6	INPUT SIGNAL 6
5	INPUT SIGNAL 5
4	INPUT SIGNAL 4
3	INPUT SIGNAL 3
2	INPUT SIGNAL 2
1	INPUT SIGNAL 1