Model 3596-Z1A

24-Bit, 16-Channel Sigma Delta
Analog-to Digital Converter

INSTRUCTION MANUAL

August, 1994

16-channel, 24-bit Sigma-Delta A/D Converter

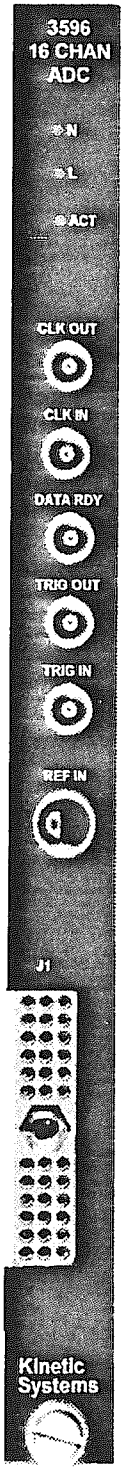
Provides up to 19 bits of single-shot resolution **3596**

Features

- **16-channels, 24-bit data fields (up to 19 bits single-shot resolution---more with sample averaging)**
- **Automatic tracking filtering (-3dB at 0.262 sample rate)**
- **Channel-by-channel programmable pre-gain (1 or 100)**
- **Channel-by-channel programmable post-gain (1 through 128)**
- **Continuous scan mode at 9.76 Hz to 1.028 kHz sampling rates (per channel)**
- **Single-Scan mode through synchronizing front-panel trigger (in and out) or CAMAC command (F25A0 or CAMAC "C" Clear operation)**
- **Two calibration modes internal zero/full-scale references or external (front-panel LEMO) full-scale reference**

Typical Applications

- **Magnetic modeling**
- **Low-level signal monitoring**
- **Applications with a high level of background noise**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 3596 CAMAC module functions as either a single-scan or continuously active 16-channel Sigma-Delta ADC. Sigma-Delta conversion is a technique which attains its very high accuracy by digitally decimating/filtering the output of a fast, single-bit converter. This eliminates the need of expensive tracking filter, sample/hold, and gain functions allowing a simple ADC-per-channel structure. This further eliminates the need of multiplexing inputs to a common ADC and thereby reduces crosstalk effects to negligible levels. Another important consequence of the digital filtering is that filter notches are produced which can be made to coincide with 60 Hz (or 50 Hz) power line frequencies and their harmonics. Thus, even in environments with severe signal corruption due to power line noise, very good results are possible.

The 3596 module provides for independently selectable gains of 1 to 128 on differentially-received inputs which accept up to ±10 volts full-scale. A common sampling rate should be chosen for all channels and may range from 9.76 Hz to 1.028 kHz. These frequencies also define the first notch in the built-in lowpass tracking filters. The -3dB bandwidth is consequently always 0.262 times the selected sampling rate. The effective resolution of each channel is derated by increased gain and sampling rate, and ranges from 19 bits at a gain of one and a 10 Hz rate to 8 bits at a gain of 128 and a 1 kHz rate. For all gains at rates of 100 Hz and below, resolution is at least 15 bits. In addition, a channel-by-channel programmable pre-gain of 100 may be selected with only minimal reduction of effective resolution. The effect on resolution under various sampling rate conditions is described in the table below.

When a Single-Scan operation is triggered, a single conversion cycle takes place and one sample point for each channel is recorded. The channels are first synchronized so that these samples correspond to the same point in time. This synchronization process causes the data to remain invalid for four sample periods of the sample rate selected. When all 16 channel samples have been recorded after this interval, a LAM Request signal, if enabled, is issued to indicate that the channels are ready for read-out. Alternatively, the LAM Status condition may be polled by waiting for a valid "Q" response to an F(27)·A(0) CAMAC command to indicate that data is available. In addition to LAM, a TTL "DATA RDY" trigger output is provided on the front-panel which may be used to trigger a CAMAC list-processing device such as the KineticSystems 3982 module.

If Active-Scanning is initiated, the channels are first synchronized causing the first valid sample of each channel to be inaccessible for a period of four sample intervals. Thereafter, new valid samples appear in the space of each sample period. Once again, when all 16 channels have deposited valid data for a given sample period, a LAM signal, if enabled, will be issued (or LAM status may be polled) to indicate that read-out may commence. The front-panel DATA RDY trigger is also activated.

The 3596 module provides for two mechanisms of offset and gain calibration. A self-calibration mode uses a mid-scale (0 volts) and positive full-scale reference internal to each channel's Sigma-Delta converter to calculate offset and gain for that converter. Alternatively, a system calibration mode may be selected which connects mid- and full-scale voltages through the entire front-end circuitry of each channel for greater absolute accuracy. This method uses the module's analog ground as the mid-scale voltage and an external full-scale reference through the REF IN front-panel two-conductor LEMO connector.

The LAM and Overwrite Status commands may be used to avoid rereading "stale" data and to indicate if samples were missed (overwritten before being read). A full complement of clock and trigger inputs and outputs are available to allow synchronous data-taking over many 3596 modules.

Item	Specification
Number of inputs	16
Type of input	Differential
Input impedance	10^{10} Ω ll 35 pF
Full-scale range	±10 V @ unity gain
Conversion data rate	10...25...30...50...60...100...1028
Resolution	19 bits minimum (10 Hz data rate, Gain = 1) 18 bits minimum (30 Hz data rate, Gain = 1) 17 bits minimum (60 Hz data rate, Gain = 1)
Missing codes	None below 60 Hz data rate
Crosstalk	-130 dB (measured at unity gain with full-scale change applied to adjacent channels)
Programmable gain: Pre gain Post gain	 1 or 100 +0.025%, uncalibrated 1, 2, 4, 8, 16, 32, 64, 128
Pre-gain settling time	140 µsec to 0.01%
Offset drift error	+0.4% + 3/G µV/°C, typical
50 Hz normal-mode attenuation	100 dB minimum (@ 50, 25, ...50/n data rates)
60 Hz normal-mode attenuation	100 dB minimum (@ 60, 30, ...60/n data rates)
Common-mode rejection ratio	80 dB (DC to 60 Hz at all data rates)
Effective bandwidth (-3 dB)	0.262 x converter data rate (e.g., 2.62 Hz @ l0 Hz rate)

Power Requirements

+6 volts: 1700 mA –6 volts: 24 mA +24 volts: 110 mA –24 volts: 80 mA

Ordering Information

Model 3596-Z1A Sigma-Delta A/D Converter, 16 channels, 24 bits

Related Products

Model 5911-Z1A 2-contact LEMO mating connector
Model 5944-Z1A 36P AMP Rectangular mating connector
Model 5857-Hxyz 1-contact LEMO to BNC shielded cable
Model 5857-Gxyz 2-contact LEMO to BNC shielded cable
Model 1992-Z1A Rack-Mount Isothermal Panel
Model 5855-Bxyz 50S Amphenol Ribbon to 36P Rectangular AMP Connector Cable

3596 STRAP OPTIONS

There are five sets of straps on the Model 3596. Figure 1 shows their locations on the board.

TRIG IN: The position of this strap determines whether an external Single-Scan/ resynchronizing trigger will be received through the front panel (FP—factory default—strap position) or through the CAMAC backplane P1 bus line (P1 strap position). In either case, the signal is expected to be a falling-edge-active TTL signal of at least 100 nsec in width. NOTE: In order to receive a trigger through the P1 line, the **P1** strap must also be set to the IN position.

P1: This strap has three valid positions over the four posts. The OUT position causes a pulled-up, open-collector TTL signal (active low; ≈1600 nsec width) to be asserted onto the CAMAC backplane P1 bus line whenever a resynchronizing action takes place on the 3596. This can occur as a result of CAMAC F(25)A(0) or F(26)A(1) commands, a CAMAC crate "CLEAR" operation, or an external trigger through the front panel TRIG IN LEMO connector if the module is strapped for this.

The middle NO (factory default) strap position disconnects the CAMAC backplane P1 bus line from any and all signal paths on the 3596 module.

The IN position of this strap when used in conjunction with the **TRIG IN** strap described above, allows an external signal present on the CAMAC backplane P1 bus line to perform the resynchronization or Single-Scan function on the 3596 module. A typical configuration would include a "master" 3596 module which outputs a trigger signal onto P1, with "slave" 3596 modules receiving this trigger signal by having this strap placed in the IN position and the **TRIG IN** strap in the P1 position.

/TST: This strap is only to be removed for in-factory testing and should ALWAYS remain in place during normal module use.

CLK: In the EXT position, an external TTL module clock (typically 10 MHz) must be provided at the CLK IN front panel LEMO connector. In the INT (factory default) position, an on-board clock provides this function. NOTE: For proper operation, the 3596 must always have a clock source consistent with the position of this strap.

A-H, SPR: This group of straps controls the use of channel 1. When strapped as A-B, C-D, E-F, G-H, channel 1 is configured to receive an isothermal reference current (e.g., from the KSC Model 1992-Z1A Rack-Mount Isothermal Panel). The current passes through a precision 1000 ohm resistor in this configuration to produce a reference voltage proportional to the temperature at the isothermal panel. This information, read through channel 1, may then be used to calibrate thermocouple information input through the other 3596 channels.

To use channel 1 as a normal input (the default factory setting), strap B-F and C-G only. The extra straps may be placed across the **SPR** spare locations.

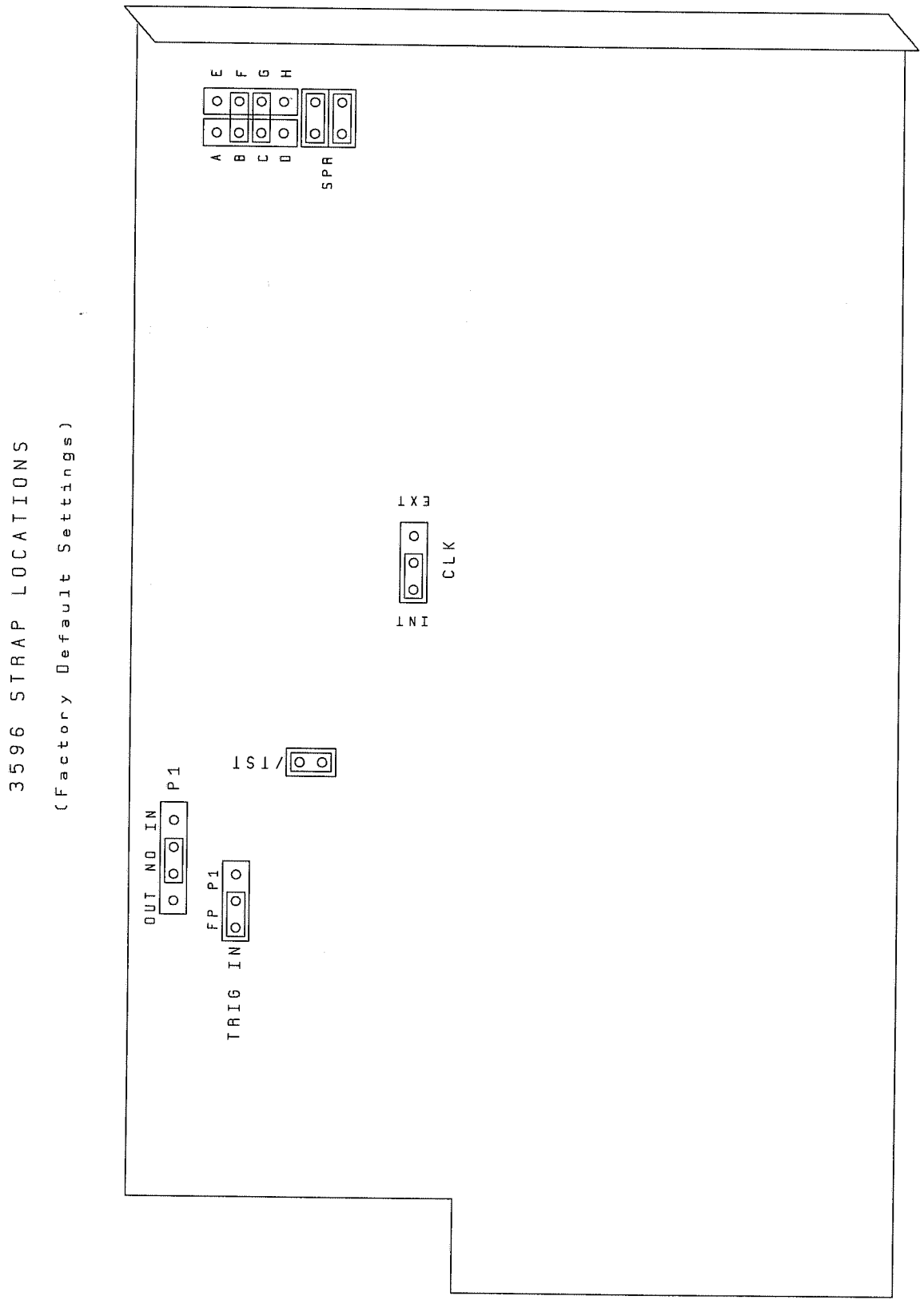

3596 STRAP LOCATIONS
(Factory Default Settings)
E F G H
A B C D
SPR
EXT
CLK
INT
1ST/
P1
OUT NO IN
P1
FP
TRIG IN

Figure 1.

REGISTERS

Pre-Gain: The F(1)A(0) and F(17)A(0) CAMAC commands are used to read and write, respectively, the Pre-Gain register. Each bit (1–LSB through 16–MSB) of this register corresponds to a pre-gain selection for each channel (channel 1 through 16) of the module. Specifically, a value of binary "0" on bit "x" produces a pre-gain of unity on channel "x". A value of binary "1" produces a pre-gain of 100.

Control Word: Each channel has an associated 24-bit Control Register which is simply the internal control register of each Sigma-Delta converter chip. The meanings of each bit within this control word are described in detail in a section of the Analog Devices AD7712 data sheet which is reprinted as an appendix to this document. However, the three fields of interest for use in this module are the Mode, (post-)Gain, and Filter Selection/Output Rate fields. The settings for accomplishing calibration and data scanning/retrieving are described in the appropriate sections below.

Each Control Register may be written individually using the F(16)A(i) CAMAC command group. Specifically, F(16)A(i), where $i \in \{0,...,15\}$, writes the Control Register for channel i+1. If the control words are to be set identically for all channels, a single F(18)A(0) command may instead be issued to write all channel Control Registers at once.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

With Active-Scanning mode disabled, the Control Registers may be read by first issuing an F(25)A(1) Control Register Scan command. This command places the internal control words from the AD7712 converters into a dual-port memory which is accessible to CAMAC. Once the module returns to the ready (RDY) state, the control words for any and all channels may then be read through CAMAC in the same manner that sampled data is normally read (i.e., with F(0)A(i) CAMAC commands). The control word data will remain in the dual-port memory and will not be overwritten with sampled data until either an F(25)A(0) Single Data Scan or F(26)A(1) Enable Active-Scan command is issued or a valid external trigger is received.

INITIALIZATION

Performing a CAMAC "Z" operation will properly initialize all CAMAC functionality on the Model 3596 module including disabling Active-Scan mode, clearing LAMs and LAM Enable, setting all pre-gains to unity gain, etc. However, NO new control words are written to the Sigma-Delta devices. They will retain whatever control information was last written to them. Therefore, it is advisable to write all control words (using the F18A0 or F16A(i) commands) subsequent to any power-up or initialization sequence.

SIGNAL CONNECTION

Both the REF IN and channel inputs are received in true differential fashion with no connection to the module's circuit ground. Consequently, any external source connected to these inputs should include a ground reference to ensure that the incoming signals will occupy the valid common-mode range of the receiving devices. Sockets C9 through C12 of the 36-socket AMP connector are internally connected to digital ground as is the shell of the REF IN LEMO connector. If a separate mid-scale reference does not exist at the input source for connection to these module ground points, the return (–) sides of the input pairs should be connected to these points in some form. Although proper grounding is sometimes considered a "black art", you may find comfort (even bona fide help) in a technical note, TN-107, written by KSC's Robert Cleary entitled "Driving Balanced Analog Inputs From Unbalanced Sources".

CALIBRATION

There are two basic modes of calibration supported by the 3596 module.

Self-Calibration

The first (and simplest to implement) is the Self-Cal mode. This method corrects ONLY the offset and gain errors attributable to the Sigma-Delta chips themselves. It has the disadvantage of not accounting for offsets and gain errors in the front-end amplifier/filter circuitry nor any errors in the system external to the module. (Obviously, this Self-Cal mode will NOT take into consideration any pre-gain setting.) An internal mid-scale and positive full-scale reference within each channel's Sigma-Delta device is used to calibrate out the internal offset/gain errors within each device. The following command structure will implement the Self-Cal mode from an initialized state:

1) F(18)A(0) DATA= 001 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(i) " "

For each channel to be calibrated, select a Sigma-Delta gain (post-gain) and filter cutoff (output rate) which will be used for data accumulation after calibration. It is important to calibrate the devices for the same gain/rate conditions under which data will be measured.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Having selected these parameters, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip. Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since Self-Cal is to be the operation (Mode = 001_2), the Control Word in binary is:

001 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(i) command where i+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same and all channels are to be calibrated, a single F(18)A(0) command transmitting a common control word will suffice to setup all channels.

2) F(27)A(1) loop until "Q" is true

Certain operations (especially group operations like F(18)A(0) cited above) may take longer to complete than the speed at which back-to-back CAMAC operations may be performed. Such operations produce an internal time-out, /RDY, which will cause a "No Q" response in subsequent affected commands until the time-out has expired. A "Q-Repeat" CAMAC operation or a software construct of "loop until Q" may be used to guarantee a valid subsequent command. Alternatively, an F(27)A(1) command tests for RDY through its "Q" response and, thus, a loop which simply tests for a true "Q" response to this command may be invoked before any RDY-sensitive command is issued.

3) LOOP: F(25)A(1)
F(27)A(1) loop until "Q" is true
F(0)A(i) read Control Word for channel "i+1"
UNTIL: Mode<23:21> of Control Word returns to 000_2

Information is transferred—via the F(25) commands—from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. Similarly, F(25)A(1) transfers the **control word** of each Sigma-Delta device to the dual-port. Since the Sigma-Delta devices automatically return Mode to the normal data-taking value (Mode = 000_2) when calibration is complete, the above loop will not exit until each channel that is checked has successfully completed Self-Cal.

System Calibration

Although involving more steps, this calibration mode includes the entire front-end circuitry and can eliminate gain errors introduced by the pre-gain amplifier/filter on each channel. The following command structure will implement Sys-Cal from an initialized state:

1) F(26)A(2) enables External Calibration mode

Input to the front-end is received either independently for each channel through the 36-socket AMP connector or through a common reference path. This reference path is selected when External Calibration mode is enabled by an F(26)A(2) command.

2) F(27)A(1) loop until "Q" is true

Certain operations (like the F(26)A(2) command above) may take longer to complete (several microseconds in this case) than the speed at which back-to-back CAMAC operations may be

performed. Such operations produce an internal time-out, /RDY, which will cause a "No Q" response in subsequent affected commands until the time-out has expired. A "Q-Repeat" CAMAC operation or a software construct of "loop until Q" may be used to guarantee a valid subsequent command. Alternatively, an F(27)A(1) command tests for RDY through its "Q" response and, thus, a loop which simply tests for a true "Q" response to this command may be invoked before any RDY-sensitive command is issued.

3) F(17)A(0) DATA = 16 bits

Since the pre-gain amplifiers are "in the loop" of system calibration, setting pre-gain for all channels must occur BEFORE the actual calibration takes place. The data for the F(17)A(0) command is such that bit "x" (<MSB:LSB> = <16:1>) determines the pre-gain for channel "x". Specifically, a binary "1" on bit "x" will program a gain of 100 for channel "x"; a binary "0" yields a pre-gain of unity.

A sufficient analog settling time should be allowed before proceeding to the next step. Especially, when switching from gains of one to gains of 100, several milliseconds should be allotted.

4) F(18)A(0) DATA= 010 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(i) " "

For each channel to be calibrated, select a Sigma-Delta gain (post-gain) and filter cutoff (output rate) which will be used for data accumulation after calibration. It is important to calibrate the devices for the same gain/rate conditions under which data will be measured.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Having selected these parameters, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip. Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Sys-Cal is divided into two operations. Step 1 (Mode = 010_2) uses a reference mid-scale point (analog ground) to remove any offsets in the data readings. This zero reference is automatically switched onto the reference path INTERNALLY to the 3596 when this Mode is entered into a Control Word either by the F(18)A(0) command or any F(16)A(i) command. Since Sys-Cal Step 1 (Mode = 010_2) is the desired operation, the Control Word in binary is:

010 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(i) command where i+1 refers to channel 1 through 16. If, however, all channel pre- AND post-gains are to be the same and all channels are to be calibrated, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels.

5) F(27)A(1) loop until "Q" is true

This ensures that the module will be ready for subsequent commands.

6) LOOP: F(25)A(1)
F(27)A(1) loop until "Q" is true
F(0)A(i) read Control Word for channel "i+1"
UNTIL: Mode<23:21> of Control Word returns to 000_2

Information is transferred—via the F(25) commands—from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. Similarly, F(25)A(1) transfers the **control word** of each Sigma-Delta device to the dual-port. Since the Sigma-Delta devices automatically return Mode to the normal data-taking value (Mode = 000_2) when Step 1 calibration is complete, the above loop will not exit until each channel that is checked has successfully completed Step 1 of Sys-Cal.

7) F(18)A(0) DATA= 011 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(i) " "

NOTE: THE EXTERNAL REFERENCE SOURCE MUST BE PRESENT AND STABLE BEFORE EXECUTING THIS COMMAND.

Using the same gain/filter parameters selected for each channel during Step 1 calibration, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip. Step 2 (Mode = 011_2) uses an external full-scale reference point (through the front-panel REF IN 2-contact LEMO connector) to calibrate the gain of each selected channel. This external reference is automatically switched onto the internal 3596 reference path when this Mode is entered into a Control Word either by the F(18)A(0) command or any F(16)A(i) command. Since Sys-Cal Step 2 (Mode = 011_2) is the desired operation, the Control Word in binary is:

011 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(i) command where i+1 refers to channel 1 through 16. If, however, all channel pre- AND post-gains are to be the same and all channels are to be calibrated, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels.

8) F(27)A(1) loop until "Q" is true

This ensures that the module will be ready for subsequent commands.

9) LOOP: F(25)A(1)
F(27)A(1) loop until "Q" is true

F(0)A(i) read Control Word for channel "i+1"
UNTIL: Mode<23:21> of Control Word returns to 000_2

Information is transferred–via the F(25) commands–from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. Similarly, F(25)A(1) transfers the **control word** of each Sigma-Delta device to the dual-port. Since the Sigma-Delta devices automatically return Mode to the normal data-taking value (Mode = 000_2) when Step 2 calibration is complete, the above loop will not exit until each channel that is checked has successfully completed Step 2 of Sys-Cal.

10) F(24)A(2) disables External Calibration mode

Disabling external calibration switches the input path for each channel from the common reference path (internal ground or external reference input) to the independent data paths from the 36-socket AMP connector.

11) F(27)A(1) loop until "Q" is true

This ensures that the module will be ready for subsequent commands.

Steps 1) and 10) above should be omitted if external multiplexing presents the mid- and full-scale reference voltages directly over the independent data paths on the 36-socket AMP connector.

DATA RETRIEVAL

Data from the 3596 occupies a 24-bit field in a 2's complement format. Thus, positive full-scale is represented by $7FFFFF_{16}$ (+8388607) and negative full-scale is 800000_{16} (–8388608). There are two independent but not necessarily mutually exclusive modes for retrieving digitized data from the 3596 channels.

Single-Scan

The more straightforward method involves nothing more than triggering the 3596 to take data, waiting for data to become valid, and reading this data through CAMAC. The advantage of this method is that it allows the user to time the initiation of each data-taking operation to, for example, synchronize readings with external events. The primary disadvantage is that this requires the Sigma-Delta Converters to be resynchronized which elongates the sampling period to four times the programmed period (one-fourth the programmed rate). The following command structure will implement this Single-Scan mode from an initialized state:

1) F(18)A(0) DATA= 000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(i) " "

Using the same gain/filter parameters selected for each channel during calibration, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since normal data-taking (Mode = 000_2) is the desired operation, the Control Word in binary is:

000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(i) command where i+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels. It is good programming practice to set the Control Words of all channels even if prior operations (such as calibration) should leave the Sigma-Delta Converters in the desired state.

NOTE: FOR PROPER OPERATION, ALL 16 CHANNELS SHOULD ALWAYS BE WRITTEN WITH CONTROL WORDS REGARDLESS OF HOW MANY CHANNELS ARE TO BE READ

2) F(25)A(0) (or external TRIG IN, active low)

Information is transferred–via the F(25) commands–from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. (The F(25)A(1) transfers the control word of each Sigma-Delta device to the dual-port). When **not** in Active-Scan mode, an external trigger pulse on the TRIG IN LEMO (or over the P1 line if strapped) will also initiate a data transfer identically to the F(25)A(0) command.

3)	F(27)A(0)	loop until "Q" is true
or	F(26)A(0)	enable LAM Request and branch to interrupt routine

The 3596, like most CAMAC modules, has an internal LAM assertion state (LAM Status) as well as a maskable LAM interrupt line to the Crate Controller (LAM Request). The LAM Status becomes true whenever new data for all sixteen channels is ready to be read from the dual-port memory onboard. This status will remain true until a) an F(10)A(0) Clear LAM command is issued, b) a re-trigger by CAMAC command–F(25)A(0) or F(26)A(1)–is issued, or c) the crate is reinitialized with a CAMAC "Z" operation.

Thus, one method of determining when data is available is to set up a software loop which repeatedly checks for LAM Status by the "Q" response to F(27)A(0). Alternatively, an interrupt routine can perform the following read-out steps based on the reception of an actual LAM

Request over the backplane. The LAM interrupt line will follow exactly the LAM Status state when LAM is enabled. This Enable LAM function is accomplished through the F(26)A(0) command.

4) F(10)A(0) clears LAM Status

In order to avoid either rereading "stale" data or missing valid data, LAM Status should be cleared immediately after a true LAM Status (or LAM Request) has been detected.

5) F(0)A(i) read digitized data from channels– i ϵ {0,...,15}

Random access to channel data from any or all channels as a result of the last trigger is possible. F(0)A(i) reads data from channel i+1. Channels may be read in any order, once, many times, or not at all, with no ill effects.

Active-Scan

A second method of data retrieval employs the Active-Scan mode of the 3596. This method has the advantage of automatically updating the dual-port memory with fresh data for all channels at the full output rate programmed for the Sigma-Delta Converters. The following command structure will implement the Active-Scan mode of data retrieval from an initialized state:

1) F(18)A(0) DATA= 000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(i) " "

Using the same gain/filter parameters selected for each channel during calibration, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since normal data-taking (Mode = 000_2) is the desired operation, the Control Word in binary is:

000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(i) command where i+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels. It is good programming practice to set the Control Words of all channels even if prior operations (such as calibration) should leave the Sigma-Delta Converters in the desired state.

NOTE: FOR PROPER OPERATION, ALL 16 CHANNELS SHOULD ALWAYS BE WRITTEN WITH CONTROL WORDS REGARDLESS OF HOW MANY CHANNELS ARE TO BE READ

2) F(26)A(1) enables Active(continuous)-Scan mode

This operation resynchronizes all of the Sigma-Delta Converters and automatically updates the dual-port memory with converter data as it becomes available (i.e., when ALL channels have completed a sampling period). Note that once this mode is entered, certain operations (notably External Calibration mode changes and Control Word reading/writing) are rejected (i.e., no "Q") until Active-Scan mode is again disabled.

NOTE: SINCE A "SYNC" IS ISSUED TO THE CONVERTERS WHEN THIS COMMAND IS GIVEN, AN INITIAL DELAY OF **FOUR** SAMPLING PERIODS WILL BE INCURRED BEFORE THE FIRST SET OF DATA BECOMES AVAILABLE. LAM STATUS WILL STILL PROPERLY REFLECT THIS–BECOMING TRUE ONLY WHEN VALID DATA IS AVAILABLE TO THE CAMAC INTERFACE FROM THE DUAL-PORT MEMORY.

3) F(27)A(0) loop until "Q" is true
or F(26)A(0) enable LAM Request and branch to interrupt routine

The 3596, like most CAMAC modules has an internal LAM assertion state (LAM Status) as well as a maskable LAM interrupt line to the Crate Controller (LAM Request). The LAM Status becomes true whenever new data for all sixteen channels is ready to be read from the dual-port memory onboard. This status will remain true until a) an F(10)A(0) Clear LAM command is issued, b) a re-trigger by CAMAC command–F(25)A(0) or F(26)A(1)–is issued, or c) the crate is reinitialized with a CAMAC "Z" operation.

Thus, one method of determining when data is available is to set up a software loop which repeatedly checks for LAM Status by the "Q" response to F(27)A(0). Alternatively, an interrupt routine can perform the following read-out steps based on the reception of an actual LAM Request over the backplane. The LAM interrupt line will follow exactly the LAM Status state when LAM is enabled. This Enable LAM function is accomplished through the F(26)A(0) command.

4) F(10)A(0) clears LAM Status

In order to avoid either rereading "stale" data or missing valid data, LAM Status should be cleared immediately after a true LAM Status (or LAM Request) has been detected.

5) F(0)A(i) read digitized data from channels– $i \in \{0,...,15\}$

Random access to channel data from any or all channels as a result of the last trigger is possible. F(0)A(i) reads data from channel i+1. Channels may be read in any order, once, many times, or not at all, with no ill effects. To minimize CAMAC readback time, a Q-Scan operation may be performed for F(0) over many adjacent 3596 modules.

6) F(27)A(2) check for "Q" is true–no data overwritten

This command tests (through a "Q" is true response) that no channel information has been written into the dual-port memory for ANY channel since the last clear of LAM Status was invoked by any method described in step 3) above. Thus, by waiting for the appearance of LAM, immediately clearing LAM, reading data (possibly many channels over many 3596 modules), and receiving a true "Q" response from this command, one is GUARANTEED that each element of data from each channel is read exactly once, and that no data was overwritten with the next sample for a channel before it was read through CAMAC. Conversely, if a No "Q" response is received in this step, it indicates that at least one channel has been overwritten with new data since the last LAM Status Clear and that some data from the previous conversion cycle MAY HAVE been missed.

7) F(24)A(1) disables Active(continuous)-Scan mode

This returns the module to the non-active state. The dual-port memory will cease to be updated with data and access for calibration and rewriting Control Words is once again possible.

It is possible in the Active-Scan mode to resync the Sigma-Delta Converters to each other and, if desired, to some external event without exiting and reentering this mode. Once Active-Scan has begun, reissuing the F(26)A(1) Enable Active-Scan command, or issuing the F(25)A(0) Single-Scan command, will immediately resync the channels and clear LAM Status without initiating ANY other action. Similarly, an external low-going edge (as strapped either from the P1 bus line or from the front panel TRIG IN LEMO), or a CAMAC "C" (CLEAR) operation will, likewise, perform the resync function. (These latter two operations DO NOT clear LAM Status!)

Note that, as always, this resynchronization process will interrupt the appearance of valid data for FOUR sample periods (as programmed into the control word Output Rate fields). However, the LAM Status (or LAM Request) will still properly indicate only when VALID data is available.

3596 CONNECTOR J1 CONNECTION MAP

SKT #	SIGNAL	SKT #	SIGNAL	SKT #	SIGNAL
A1	CHANNEL 1 +	B1	CHANNEL 7 +	C1	CHANNEL 13 +
A2	CHANNEL 1 -	B2	CHANNEL 7 -	C2	CHANNEL 13 -
A3	CHANNEL 2 +	B3	CHANNEL 8 +	C3	CHANNEL 14 +
A4	CHANNEL 2 -	B4	CHANNEL 8 -	C4	CHANNEL 14 -
A5	CHANNEL 3 +	B5	CHANNEL 9 +	C5	CHANNEL 15 +
A6	CHANNEL 3 -	B6	CHANNEL 9 -	C6	CHANNEL 15 -
A7	CHANNEL 4 +	B7	CHANNEL 10 +	C7	CHANNEL 16 +
A8	CHANNEL 4 -	B8	CHANNEL 10 -	C8	CHANNEL 16 -
A9	CHANNEL 5 +	B9	CHANNEL 11 +	C9	DIG GROUND
A10	CHANNEL 5 -	B10	CHANNEL 11 -	C10	DIG GROUND
A11	CHANNEL 6 +	B11	CHANNEL 12 +	C11	DIG GROUND
A12	CHANNEL 6 -	B12	CHANNEL 12 -	C12	DIG GROUND

Front Panel View

A1	B1	C1
A2	B2	C2
A3	B3	C3
A4	B4	C4
A5	B5	C5
A6	B6	C6
A7	B7	C7
A8	B8	C8
A9	B9	C9
A10	B10	C10
A11	B11	C11
A12	B12	C12

CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12-bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	X	BO	B/U

FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

LSB

X = Don't Care.

Operating Mode			
MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete the part returns to Normal Mode (with MD2, MD1, MD0 of the control registers returning to 0,0,0). The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System-Offset Calibration. This activates system-offset calibration on the channel selected by CH. This is a one-step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7712 provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits regardless, of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.

PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the Internal Power-On Reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel		
0	AIN1	Low Level Input	(Default Condition After the Internal Power-On Reset)
1	AIN2	High Level Input	

Power-Down

PD		
0	Normal Operation	(Default Condition After the Internal Power-On Reset)
1	Power-Down	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After Internal Power-On Reset)
1	24-Bit	

Burn-Out Current

BO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After Internal Power-On Reset)
1	Unipolar	

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7712, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7712. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). This settling time is to 100% of the final value. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be 3 × 1/(output data rate). If a change of channel takes place, the settling time is 3×1/(output data rate) regardless of the $\overline{SYNC}$ input.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.