Model 3596-Z1B
24-Bit, 16-Channel Sigma Delta
Analog-to Digital Converter
w/Sensor Group Power
INSTRUCTION MANUAL

October, 1996

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CAMAC

3596-Z1B 24-Bit, 16-channel Sigma-Delta ADC

FEATURES

16-channels, 24-bit data fields (up to 19 bits single-shot resolution--more with sample averaging)

Separate front-panel connectors for each 8-channel input group

Controls end-to-end calibration circuit for magnetic sensors

Automatic tracking filtering (-3 dB at 0.262 sample rate)

Channel-by-channel programmable pre-gain (1 or 100)

Channel-by-channel programmable post-gain (1 through 128)

Continuous scan mode at 9.76 Hz to 1.028 kHz sampling rates (per channel)

Single-Scan mode through synchronizing dataway P1 line trigger (in and out), CAMAC command (F(25)A(0) or CAMAC "C" Clear operation)

GENERAL DESCRIPTION

The Model 3596-Z1B CAMAC module functions as either a single-scan or continuously active 16-channel Sigma-Delta ADC. Sigma-Delta conversion is a technique which attains its very high accuracy by digitally decimating and filtering the output of a fast, single-bit converter. This eliminates the need for expensive tracking filter, sample/hold, and gain functions, allowing a simple ADC-per-channel structure. This further eliminates the need to multiplex inputs to a common ADC and thereby reduces crosstalk effects to negligible levels. Another important consequence of the digital filtering is that filter notches are produced which can be made to coincide with 60 Hz (or 50 Hz) power line frequencies and their harmonics. Thus, even in environments with severe signal corruption due to power line noise, very good results are possible.

The 3596-Z1B module provides for independently selectable post-gains of 1 to 128 on differentially-received inputs which accept up to ±10 V full-scale. A common sampling rate should be chosen for all channels and may range from 9.76 Hz to 1.028 kHz. These frequencies also define the first notch in the built-in, lowpass tracking filters. The -3 dB bandwidth is consequently always 0.262 times the selected sampling rate. The effective resolution of each channel is derated by increased gain and sampling rate, and ranges from 19 bits at a gain of one and a 10 Hz rate to 8 bits at a gain of 128 and a 1 kHz rate. For all gains at rates of 100 Hz and below, resolution is at least 15 bits. In addition, a channel-by-channel programmable pre-gain of 100 may be selected with only minimal reduction of effective resolution. The effect on resolution under various sampling rate conditions is described in the specifications.

When a Single-Scan operation is triggered, a single conversion cycle takes place and one sample point for each channel is recorded. The channels are first synchronized so that these samples correspond to the same point in time. This synchronization process causes the data to remain invalid for four sample intervals of the selected sample rate. When all 16 channel samples have been recorded after this interval, a LAM Request signal, if enabled, is issued to indicate that the channels are ready for read-out. Alternatively, the LAM Status condition may be polled by waiting for a valid "Q" response to an F(27)A(0) CAMAC command to indicate that data is available

The 3596-Z1B module provides for two mechanisms of offset and gain calibration. A self-calibration mode uses a mid-scale (0 volts) and positive full-scale reference internal to each

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channel's Sigma-Delta converter to calculate offset and gain for that converter. Also, circuitry is provided for switchable positive and negative current supplied to the remote sensor assemblies.

The LAM and Overwrite Status commands may be used to avoid rereading "stale" data and to indicate if samples were missed (overwritten before being read). A strappable P1 CAMAC Dataway connection is available to allow synchronous data-taking over multiple 3596-Z1B modules.

SIGNALS/ CONNECTORS

SG1 Sensor Group 1; eight differential analog channel inputs, ± calibration
Up to ±10 volt signal range (depending on setting of channel gain)
Includes ± 15 volt power with a 300 mA trip point for the load from this sensor group. A short circuit on this sensor group will not adversely affect analog power to the module or to the other sensor group.
Connector type: 26-socket D-subminiature connector

SG2 Sensor Group 2; eight differential analog channel inputs, ± calibration
Up to ±10 volt signal range (depending on setting of channel gain)
Includes ±15 volt power with a 300 mA trip point for the load from this sensor group. A short circuit on this sensor group will not adversely affect analog power to the module or to the other sensor group
Connector type: 26-socket D-subminiature connector

MONITOR Analyzer; monitors all 16 input channels, contains control signals for the end-to-end +/- calibration. Connector type: 26-socket D-subminiature connector

INDICATORS

"N" LED Module addressed

"ACT" LED Active-Scan mode initiated or flash on when a Single-Scan is initiated. LED will blink off during Active-Scan mode if a resyncing action occurs.

"OC1+, OC2+" LEDs Lighted when the +15 volt power source to Sensor Group SG1 *or* SG2 is overloaded. respectively.

"OC1-, OC2-" LEDs Lighted when the -15 volt power source to Sensor Group SG1 *or* SG2 is overloaded. respectively.

The following four LEDs are bicolor:

"CS1" LED Lighted red when a +cal is selected by software for Sensor Group 1.
Lighted green when a -cal is selected by software for Sensor Group 1.

"CR1" LED Lighted red when a +voltage is found on a calibration signal line for Sensor Group 1
Lighted green when a -voltage is found on a calibration signal line for Sensor Group 1

"CS2" LED Lighted red when +cal is selected by software for Sensor Group 2.
Lighted green when -cal is selected by software for Sensor Group 2.

"CR2" LED Lighted red when a +voltage is found on a calibration signal line for Sensor Group 2
Lighted green when a -voltage is found on a calibration signal line for Sensor Group 2

FUNCTION CODES

Command		Q	Action
F(0)A(i)[1]	RD1	1	Reads the Converted Data Memory for channel i+1.[1]
F(1)A(0)	RD2	1	Reads a 16-bit Pre-Gain Register for all channels. Bit "x"=1 indicates a gain of 100 on channel "x".
F(8)A(0)	TLM	LR	Tests if a LAM Request is set.
F(9)A(0)[3]	DIS	/ACTV·RDY	Clears the Calibration Register for Sensor Groups SG1 and SG2
F(10)A(0)	CLM	1	Clears the LAM Status bit.
F(16)A(i)[1, 3]	WT1	/ACTV·RDY	Writes the Control Word for channel i+1.[1]
F(17)A(0)	WT2	1	Writes a 16-bit Pre-Gain Register for all channels. Bit "x"=1 indicates a gain of 100 on channel "x".
F(18)A(0)[3]	SS1	/ACTV·RDY	Writes a common Control Word to all 16 channels.
F(18)A(1)[3]	ENB	/ACTV·RDY	Writes the Calibration Register for Sensor Groups SG1 and SG2.
F(24)A(0)	DIS	1	Disables the LAM Request.
F(24)A(1)	DIS	1	Disables Active(continuous)-Scan mode.
F(25)A(0)[2, 3]	XEQ	RDY	Initiates a Single-Scan operation, resynchronizes the converters, clears the LAM Status bit, asserts TRIG OUT at Dataway P1 connector.
F(25)A(1)[3]	XEQ	/ACTV·RDY	Initiates a single scan of the Control Words (accessible via F(0) commands), asserts TRIG OUT at Dataway P1 connector.
F(26)A(0)	ENB	1	Enables the LAM Request
F(26)A(1)[2]	ENB	RDY	Enables Active(continuous)-Scan mode, resynchronizes the converters, clears the LAM Status bit, asserts TRIG OUT at P1 connector.
F(27)A(0)	TST	LS	Tests if the LAM Status bit is set. "Q" response indicates data is available.
F(27)A(1)	TST	RDY	Tests (through the "Q" response) if module is ready for further commands.
F(27)A(2)	TST	/OVRWT	Tests (through the "Q" response) if channel data has NOT been overwritten since the last F(10)A(0) Clear LAM command (or F(25)A(0), F(26)A(1), CAMAC "Z" commands).
Z·S2[3]	CZ	0	Disables Active-Scan mode, clears LAM Status, disables LAM Request, clears the Calibration Register, clears the Pre-Gain Register.
C·S2	CZ	0	Resynchronizes channel scanning.

Notes:

1. Channel numbers 1 to 16 correspond to i=0 to 15.
2. Issuing these commands while Active-Scan mode is enabled resynchronizes the converters, clears the LAM Status bit, and asserts "TRIG OUT" at the Dataway P1 connector without otherwise affecting Active-Scanning.
3. These commands require more than 1 μsec to perform their functions and consequently produce a NOT READY (/RDY) condition until they are completed.

Item	Specification
Number of Inputs	16
Type of input	Differential
Input Impedance	$10^{10}\Omega$ || 35 pF
Full-scale Range	±10 V @ unity gain
Conversion Data Rate	10...25...30...50...60...100...1028 Hz
Resolution	19 bits minimum (10 Hz data rate, Gain = 1) 18 bits minimum (30 Hz data rate, Gain = 1) 17 bits minimum (60 Hz data rate, Gain = 1)
Missing Codes	None below 60 Hz data rate
Cross-talk	-130 dB (measured at unity gain)
Programmable Gain	Pre: 1 or 100, ±0.025% uncalibrated Post: 1, 2, 4, 8, 16, 32, 64, 128
Pre-gain settling time	140 μsec to 0.01%
Offset Drift Error	± 0.4% + 3/G μV/°C, typical
50 Hz normal-mode attenuation	-100 dB minimum (@ 50, 25, ..., 50/N data rates)
60 Hz normal-mode attenuation	-100 dB minimum (@ 60, 30, ...,60/N data rates)
Common-mode rejection ratio	-80 dB (DC to 60 Hz at all data rates)
Effective Bandwidth (-3 dB)	0.262 x converter data rate (e.g., 2.62 Hz @ 10 Hz rate)

POWER REQUIREMENTS

+6 volts	1700 mA
-6 volts	24 mA
+24 volts	100 mA (1)
-24 volts	100 mA (2)

WEIGHT

0.7 kg. (1 lb., 9 oz.)

Notes:

1. This is the current drain for the module only. With two sensor groups connected with loads of 150 mA each, the total +24 V current is 400 mA. With short circuits on both sensor groups and a nominal current limiting of 300 mA each, the total +24 V current is 700 mA.

2. This is the current drain for the module only. With two sensor groups connected with loads of 150 mA each, the total -24 V current is 400 mA. With short circuits on both sensor groups and a nominal current limiting of 300 mA each, the total -24 V current is 700 mA.

ORDERING INFORMATION

Model 3596-Z1B	24-bit, 16-channel Sigma-Delta ADC Module w/ Sensor Group Power

3596 STRAP OPTIONS

There are two sets of straps on the Model 3596. Figure 1 shows their locations on the board.

P1: This strap has three valid positions over the four posts. The OUT position causes a pulled-up, open-collector TTL signal (active low; ≈1600 nsec width) to be asserted onto the CAMAC backplane P1 bus line whenever a resynchronizing action takes place on the 3596. This can occur as a result of CAMAC F(25)A(0) or F(26)A(1) commands or a CAMAC crate "CLEAR" operation.

The middle NO (factory default) strap position disconnects the CAMAC backplane P1 bus line from any and all signal paths on the 3596 module.

The IN position of this strap allows an external signal present on the CAMAC backplane P1 bus line to perform the resynchronization or Single-Scan function on the 3596 module. A typical configuration would include a "master" 3596 module which outputs a trigger signal onto P1, with "slave" 3596 modules receiving this trigger signal by having this strap placed in the IN position.

/TST: This strap is only to be removed for in-factory testing and should ALWAYS remain in place during normal module use.

REGISTERS

Pre-Gain: The F(1)A(0) and F(17)A(0) CAMAC commands are used to read and write, respectively, the Pre-Gain register. Each bit (1–LSB through 16–MSB) of this register corresponds to a pre-gain selection for each channel (channel 1 through 16) of the module. Specifically, a value of binary "0" on bit "x" produces a pre-gain of unity on channel "x". A value of binary "1" produces a pre-gain of 100.

Control Word: Each channel has an associated 24-bit Control Register which is simply the internal control register of each Sigma-Delta converter chip. The meanings of each bit within this control word are described in detail in a section of the Analog Devices AD7712 data sheet which is reprinted as an appendix to this document. However, the three fields of interest for use in this module are the Mode, (post-)Gain, and Filter Selection/Output Rate fields. The settings for accomplishing calibration and data scanning/retrieving are described in the appropriate sections on the following pages.

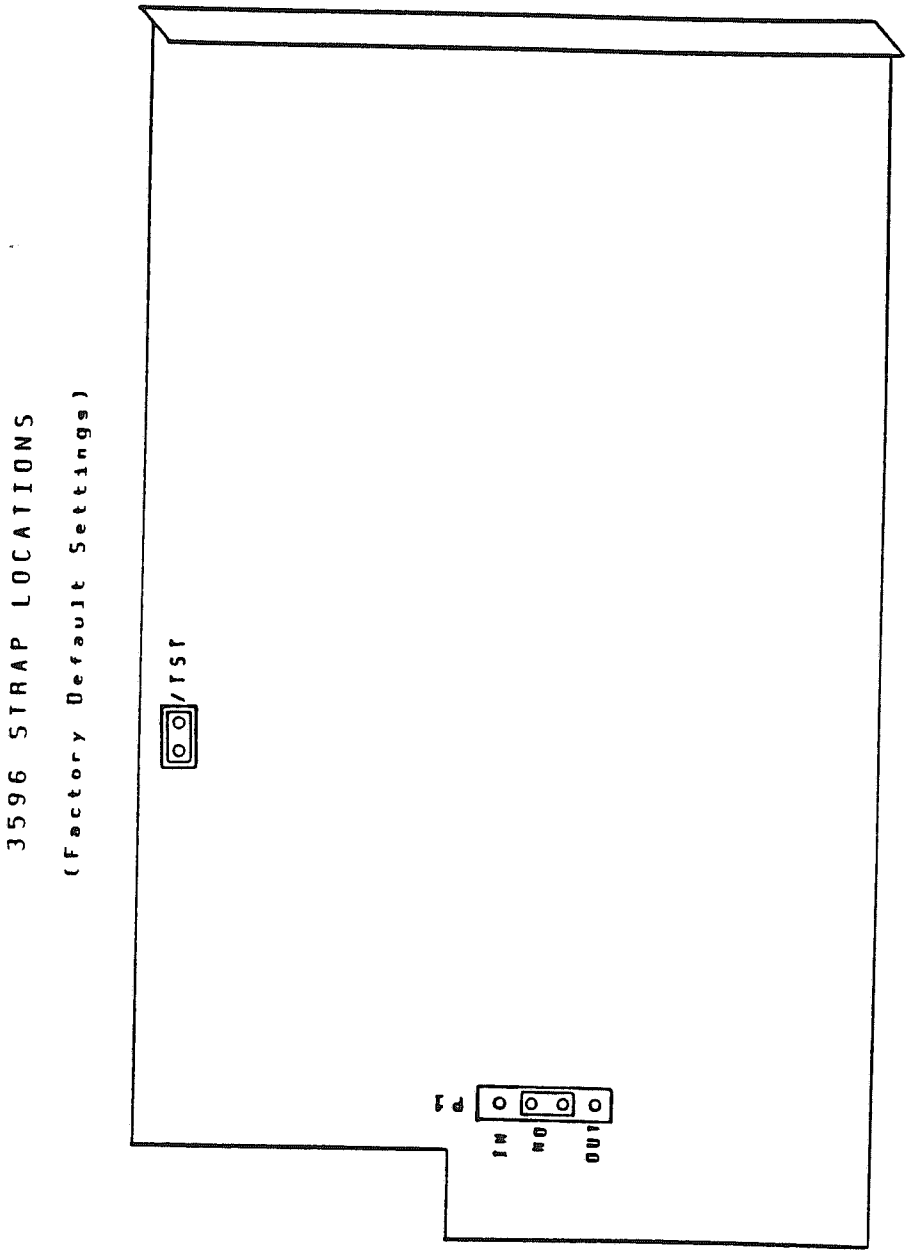


Figure 1: 3596 Strap Location

Each Control Register may be written individually using the F(16)A(I) CAMAC command group. Specifically, F(16)A(I), where I ϵ {0,...,15}, writes the Control Register for channel I+1. If the control words are to be set identically for all channels, a single F(18)A(0) command may instead be issued to write all channel Control Registers at once.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

With Active-Scanning mode disabled, the Control Registers may be read by first issuing an F(25)A(1) Control Register Scan command. This command places the internal control words from the AD7712 converters into a dual-port memory which is accessible to CAMAC. Once the module returns to the ready (RDY) state, the control words for any and all channels may then be read through CAMAC in the same manner that sampled data is normally read (i.e., with F(0)A(I) CAMAC commands). The control word data will remain in the dual-port memory and will not be overwritten with sampled data until either an F(25)A(0) Single Data Scan or F(26)A(1) Enable Active-Scan command is issued or a valid P1 trigger is received.

INITIALIZATION

Performing a CAMAC "Z" operation will properly initialize all CAMAC functionality on the Model 3596 module including disabling Active-Scan mode, clearing LAMs and LAM Enable, setting all pre-gains to unity gain, etc. However, NO new control words are written to the Sigma-Delta devices. They will retain whatever control information was last written to them. Therefore, it is advisable to write all control words (using the F18A0 or F16A(I) commands) subsequent to any power-up or initialization sequence.

SIGNAL CONNECTION

The 3596-Z1B channel inputs are received in true differential fashion with no connection to the module's circuit ground. Consequently, any external source connected to these inputs should include a ground reference to ensure that the incoming signals will occupy the valid common-mode range of the receiving devices. Sockets 18 and 21 of the 26-socket front panel connectors SG1 and SG2 are internally connected to digital ground If a separate mid-scale reference does not exist at the input source for connection to these module ground points, the return (-) sides of the input pairs should be connected to these points in some form. Although proper grounding is sometimes considered a "black art", you may find comfort (even bona fide help) in a technical note, TN-107, written by KSC's Robert Cleary entitled "Driving Balanced Analog Inputs From Unbalanced Sources".

SIGMA-DELTA ADC SELF-CALIBRATION

Self-Calibration corrects ONLY the offset and gain errors attributable to the Sigma-Delta chips themselves. It does not account for offsets and gain errors in the front-end amplifier/filter circuitry nor any errors in the system external to the module. (Obviously, this Self-Cal mode will NOT take into consideration any pre-gain setting.) An internal mid-scale and positive full-scale reference within each channel's Sigma-Delta device is used to calibrate out the internal offset/gain errors within each device. The following command structure will implement the Self-Cal mode from an initialized state:

1)	F(18)A(0)	DATA= 001 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or	F(16)A(I)	" "

For each channel to be calibrated, select a Sigma-Delta gain (post-gain) and filter cutoff (output rate) which will be used for data accumulation after calibration. It is important to calibrate the devices for the same gain/rate conditions under which data will be measured.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Having selected these parameters, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip. Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since Self-Cal is to be the operation (Mode = 001_2), the Control Word in binary is:

001 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(I) command where I+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same and all channels are to be calibrated, a single F(18)A(0) command transmitting a common control word will suffice to setup all channels.

2) F(27)A(1) loop until "Q" is true

Certain operations (especially group operations like F(18)A(0) cited above) may take longer to complete than the speed at which back-to-back CAMAC operations may be performed. Such operations produce an internal time-out, /RDY, which will cause a "No Q" response in subsequent affected commands until the time-out has expired. A "Q-Repeat" CAMAC operation or a software construct of "loop until Q" may be used to guarantee a valid subsequent command. Alternatively, an F(27)A(1) command tests for RDY through its "Q" response and, thus, a loop which simply tests for a true "Q" response to this command may be invoked before any RDY-sensitive command is issued.

3) LOOP: F(25)A(1)
F(27)A(1) loop until "Q" is true
F(0)A(I) read Control Word for channel "I+1"
UNTIL: Mode<23:21> of Control Word returns to 000_2

Information is transferred–via the F(25) commands–from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. Similarly, F(25)A(1) transfers the **control word** of each Sigma-Delta device to the dual-port. Since the Sigma-Delta devices automatically return Mode to the normal data-taking value (Mode = 000_2) when calibration is complete, the above loop will not exit until each channel that is checked has successfully completed Self-Cal.

SENSOR POWER AND CALIBRATION

Sensor Group Power

The 3596-Z1B provides ±15 volt power with a 300mA trip point for the load from each sensor group. These voltages are available at front-panel connectors SG1 and SG2 (See Connector PinOut information). A short circuit on either sensor group will not adversely affect analog power to the module or to the other sensor group. Front-panel over-current LED indicators are provided for each sensor group. Front-panel LEDs OC1+ or OC2+ are lighted when the +15 volt power source to sensor group SG1 or SG2 is overloaded, respectively. Front-panel LEDs OC1- or OC2- are lighted when the -15 volt power source to sensor group SG1 or SG2 is overloaded, respectively.

Sensor Calibration

Sensor calibration for Sensor Group 1 (SG1) and Sensor Group 2 (SG2) is controlled via the "cal" pins at front-panel connectors SG1 and SG2. A +15v "+cal" or -15v "-cal" signal may be sent to these pins by either a CAMAC software command or by external hardware control through the Set SG1/SG2 Cal pins at the front-panel Monitor connector. Software calibration is achieved by writing to a four-bit calibration register using an F(18)A(1) command. A bit map of this register is shown below:

BIT 4	BIT 3	BIT 2	BIT 1
- CAL SG2	+ CAL SG2	- CAL SG1	+ CAL SG1

If both the "+cal" and "-cal" bits are inadvertently set at the same time for a given sensor group, the voltage at the "cal" pin will be approximately zero volts (no cal). Also, to prevent confusion if a software "-cal" was set at the same time a hardware "+cal" was, or vice-versa, the following chart will hold true:

		SOFTWARE		
		+CAL	-CAL	NO CAL
HARDWARE	+CAL	+CAL	NO CAL	+CAL
	-CAL	NO CAL	-CAL	-CAL
	NO CAL	+CAL	-CAL	NO CAL

Front-panel Cal-Send and Cal-Receive bi-color LEDs provide visual verification of the voltage levels on the "cal" lines. The Cal-Send LEDs ("CS1" for Sensor Group 1 and "CS2" for Sensor Group 2) are lighted red when a "+cal" is selected by software and lighted green when a "-cal" is selected by software for the corresponding Sensor Group. The Cal-Receive LEDs ("CR1" for Sensor Group 1 and "CR2" for Sensor Group 2) are lighted red when a + voltage is found on a calibration signal line and lighted green when a - voltage is found on a calibration signal line. The voltage on the calibration signal line may have been produced by a software cal generated by an F(18)A(1) command or by a hardware cal generated through the front-panel Monitor connector Set Cal pins.

DATA RETRIEVAL

Data from the 3596 occupies a 24-bit field in a 2's complement format. Thus, positive full-scale is represented by $7FFFFF_{16}$ (+8388607) and negative full-scale is 800000_{16} (–8388608). There are two independent but not necessarily mutually exclusive modes for retrieving digitized data from the 3596 channels.

Single-Scan

The more straightforward method involves nothing more than triggering the 3596 to take data, waiting for data to become valid, and reading this data through CAMAC. The advantage of this method is that it allows the user to time the initiation of each data-taking operation to, for example, synchronize readings with external events. The primary disadvantage is that this requires the Sigma-Delta Converters to be resynchronized which elongates the sampling period to four times the programmed period (one-fourth the programmed rate). The following command structure will implement this Single-Scan mode from an initialized state:

1) F(18)A(0) DATA= 000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(I) " "

Using the same gain/filter parameters selected for each channel during calibration, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since normal data-taking (Mode = 000_2) is the desired operation, the Control Word in binary is:

000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(I) command where I+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels. It is good programming practice to set the Control Words of all channels even if prior operations (such as calibration) should leave the Sigma-Delta Converters in the desired state.

NOTE: FOR PROPER OPERATION, **ALL** 16 CHANNELS SHOULD ALWAYS BE WRITTEN WITH CONTROL WORDS REGARDLESS OF HOW MANY CHANNELS ARE TO BE READ

2) F(25)A(0) (or P1 trigger, active low)

Information is transferred–via the F(25) commands–from the Sigma-Delta devices to a dual-port memory accessible by CAMAC. Specifically, F(25)A(0) (as well as Active-Scanning) causes the digitized values of each input channel to be transferred. (The F(25)A(1) transfers the control word of each Sigma-Delta device to the dual-port). When **not** in Active-Scan mode, a trigger pulse on the P1 line (if strapped for P1 IN) will also initiate a data transfer identically to the F(25)A(0) command.

3) F(27)A(0) loop until "Q" is true
or F(26)A(0) enable LAM Request and branch to interrupt routine

The 3596, like most CAMAC modules, has an internal LAM assertion state (LAM Status) as well as a maskable LAM interrupt line to the Crate Controller (LAM Request). The LAM Status becomes true whenever new data for all sixteen channels is ready to be read from the dual-port memory onboard. This status will remain true until a) an F(10)A(0) Clear LAM command is issued, b) a re-trigger by CAMAC command–F(25)A(0) or F(26)A(1)–is issued, or c) the crate is reinitialized with a CAMAC "Z" operation.

Thus, one method of determining when data is available is to set up a software loop which repeatedly checks for LAM Status by the "Q" response to F(27)A(0). Alternatively, an interrupt routine can perform the following read-out steps based on the reception of an actual LAM Request over the backplane. The LAM interrupt line will follow exactly the LAM Status state when LAM is enabled. This Enable LAM function is accomplished through the F(26)A(0) command.

4) F(10)A(0) clears LAM Status

In order to avoid either rereading "stale" data or missing valid data, LAM Status should be cleared immediately after a true LAM Status (or LAM Request) has been detected.

5) F(0)A(I) read digitized data from channels– I ϵ {0,...,15}

Random access to channel data from any or all channels as a result of the last trigger is possible. F(0)A(I) reads data from channel I+1. Channels may be read in any order, once, many times, or not at all, with no ill effects.

Active-Scan

A second method of data retrieval employs the Active-Scan mode of the 3596. This method has the advantage of automatically updating the dual-port memory with fresh data for all channels at the full output rate programmed for the Sigma-Delta Converters. The following command structure will implement the Active-Scan mode of data retrieval from an initialized state:

1) F(18)A(0) DATA= 000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$
or F(16)A(I) " "

Using the same gain/filter parameters selected for each channel during calibration, 24-bit Control Words may be built which follow exactly the format given for the AD7712 Sigma-Delta chip.

THIS MODULE SHOULD ALWAYS BE OPERATED SUCH THAT ALL 16 CHANNELS ARE PROGRAMMED FOR IDENTICAL FILTER CUTOFFS (OUTPUT RATES).

Since this module uses the ±10 volt AIN2 input of the AD7712, 101000_2 will always occupy bits <17:12> out of <23:0>. Since normal data-taking (Mode = 000_2) is the desired operation, the Control Word in binary is:

000 "Gain<20:18>" 101000 "Filter<11:0>"$_2$

where the meanings of the Gain and Filter groups are described in the AD7712 data sheet (reprinted as an appendix to this document). Each control word (for each channel) may be written individually with an F(16)A(I) command where I+1 refers to channel 1 through 16. If, however, all channel post-gains are to be the same, a single F(18)A(0) command transmitting the common control word will suffice to setup all channels. It is good programming practice to set the Control Words of all channels even if prior operations (such as calibration) should leave the Sigma-Delta Converters in the desired state.

NOTE: FOR PROPER OPERATION, **ALL** 16 CHANNELS SHOULD ALWAYS BE WRITTEN WITH CONTROL WORDS REGARDLESS OF HOW MANY CHANNELS ARE TO BE READ

2) F(26)A(1) enables Active(continuous)-Scan mode

This operation resynchronizes all of the Sigma-Delta Converters and automatically updates the dual-port memory with converter data as it becomes available (i.e., when ALL channels have completed a sampling period). Note that once this mode is entered, certain operations (notably Control Word reading/writing) are rejected (i.e., no "Q") until Active-Scan mode is again disabled.

NOTE: SINCE A "SYNC" IS ISSUED TO THE CONVERTERS WHEN THIS COMMAND IS GIVEN, AN INITIAL DELAY OF **FOUR** SAMPLING PERIODS WILL BE INCURRED BEFORE THE FIRST SET OF DATA BECOMES AVAILABLE. LAM STATUS WILL STILL PROPERLY REFLECT THIS–BECOMING TRUE ONLY WHEN VALID DATA IS AVAILABLE TO THE CAMAC INTERFACE FROM THE DUAL-PORT MEMORY.

3) F(27)A(0) loop until "Q" is true
or F(26)A(0) enable LAM Request and branch to interrupt routine

The 3596, like most CAMAC modules has an internal LAM assertion state (LAM Status) as well as a maskable LAM interrupt line to the Crate Controller (LAM Request). The LAM Status becomes true whenever new data for all sixteen channels is ready to be read from the dual-port memory onboard. This status will remain true until a) an F(10)A(0) Clear LAM command is issued, b) a re-trigger by CAMAC command–F(25)A(0) or F(26)A(1)–is issued, or c) the crate is reinitialized with a CAMAC "Z" operation.

Thus, one method of determining when data is available is to set up a software loop which repeatedly checks for LAM Status by the "Q" response to F(27)A(0). Alternatively, an interrupt routine can perform the following read-out steps based on the reception of an actual LAM Request over the backplane. The LAM interrupt line will follow exactly the LAM Status state when LAM is enabled. This Enable LAM function is accomplished through the F(26)A(0) command.

4) F(10)A(0) clears LAM Status

In order to avoid either rereading "stale" data or missing valid data, LAM Status should be cleared immediately after a true LAM Status (or LAM Request) has been detected.

5) F(0)A(I) read digitized data from channels– $I \in \{0,...,15\}$

Random access to channel data from any or all channels as a result of the last trigger is possible. F(0)A(I) reads data from channel I+1. Channels may be read in any order, once, many times, or not at all, with no ill effects. To minimize CAMAC readback time, a Q-Scan operation may be performed for F(0) over many adjacent 3596 modules.

6) F(27)A(2) check for "Q" is true–no data overwritten

This command tests (through a "Q" is true response) that no channel information has been written into the dual-port memory for ANY channel since the last clear of LAM Status was invoked by any method described in step 3) above. Thus, by waiting for the appearance of LAM, immediately clearing LAM, reading data (possibly many channels over many 3596 modules), and receiving a true "Q" response from this command, one is GUARANTEED that each element of data from each channel is read exactly once, and that no data was overwritten with the next sample for a channel before it was read through CAMAC. Conversely, if a No "Q" response is received in this step, it indicates that at least one channel has been overwritten with new data since the last LAM Status Clear and that some data from the previous conversion cycle MAY HAVE been missed.

7) F(24)A(1) disables Active(continuous)-Scan mode

This returns the module to the non-active state. The dual-port memory will cease to be updated with data and access for calibration and rewriting Control Words is once again possible.

It is possible in the Active-Scan mode to resync the Sigma-Delta Converters to each other and, if desired, to some external event without exiting and reentering this mode. Once Active-Scan has begun, reissuing the F(26)A(1) Enable Active-Scan command, or issuing the F(25)A(0) Single-Scan command, will immediately resync the channels and clear LAM Status without initiating ANY other action. Similarly, an external low-going edge (from the P1 bus line), or a CAMAC "C" (CLEAR) operation will, likewise, perform the resync function. (These latter two operations DO NOT clear LAM Status!)

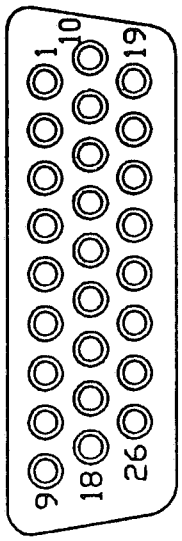
Note that, as always, this resynchronization process will interrupt the appearance of valid data for FOUR sample periods (as programmed into the control word Output Rate fields). However, the LAM Status (or LAM Request) will still properly indicate only when VALID data is available.

3596-Z1B CONNECTOR PINOUT

	J2	J3	J1
Contact	Connector SG1	Connector SG2	Connector Monitor
1	Chan 1+	Chan 9+	Chan 1+
2	Chan 1-	Chan 9-	Chan 2+
3	Chan 2+	Chan 10+	Chan 3+
4	Chan 2-	Chan 10-	Chan 4+
5	Chan 3+	Chan 11+	Chan 5+
6	Chan 3-	Chan 11-	Chan 6+
7	Chan 4+	Chan 12+	Chan 7+
8	Chan 4-	Chan 12-	Chan 8+
9	Chan 5+	Chan 13+	Chan 9+
10	Chan 5-	Chan 13-	Chan 10+
11	Chan 6+	Chan 14+	Chan 11+
12	Chan 6-	Chan 14-	Chan 12+
13	Chan 7+	Chan 15+	Chan 13+
14	Chan 7-	Chan 15-	Chan 14+
15	Chan 8+	Chan 16+	Chan 15+
16	Chan 8-	Chan 16-	Chan 16+
17	No Connection	No Connection	Sig Gnd SG1 (1)
18	Digital Gnd	Digital Gnd	Sig Gnd SG2 (2)
19	Cal Sig (SG1)	Cal Sig (SG2)	Set SG1 Cal
20	No Connection	No Connection	Set SG2 Cal
21	Digital Gnd	Digital Gnd	Digital Gnd
22	Ground (Pwr Ret)	Ground (Pwr Ret)	Ground (Pwr Ret)
23	+15V Power	+15V Power	No Connection (3)
24	-15V Power	-15V Power	No Connection (3)
25	No Connection	No Connection	No Connection
26	No Connection	No Connection	No Connection

NOTE: (1) This is the Chan 1 -signal.
(2) This is the Chan 9 -signal.
(3) No connections are made to these contacts to prevent damage in case the monitor connector accidently is plugged into one of the Sensor Group connectors.

3596-Z1B FRONT PANEL VIEW



CONTROL REGISTER (24 BITS)

A write to the device with the A0 input low writes data to the control register. A read to the device with the A0 input low accesses the contents of the control register. The control register is 24-bits wide and when writing to the register 24 bits of data must be written otherwise the data will not be loaded to the control register. In other words, it is not possible to write just the first 12-bits of data into the control register. If more than 24 clock pulses are provided before $\overline{TFS}$ returns high, then all clock pulses after the 24th clock pulse are ignored. Similarly, a read operation from the control register should access 24 bits of data.

MSB

MD2	MD1	MD0	G2	G1	G0	CH	PD	WL	X	BO	B/U

FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0

LSB

X = Don't Care.

Operating Mode			
MD2	MD1	MD0	Operating Mode
0	0	0	Normal Mode. This is the normal mode of operation of the device whereby a read to the device accesses data from the data register. This is the default condition of these bits after the internal power-on reset.
0	0	1	Activate Self-Calibration. This activates self-calibration on the channel selected by CH. This is a one-step calibration sequence, and when complete the part returns to Normal Mode (with MD2, MD1, MD0 of the control registers returning to 0,0,0). The $\overline{DRDY}$ output indicates when this self-calibration is complete. For this calibration type, the zero scale calibration is done internally on shorted (zeroed) inputs and the full-scale calibration is done on V_{REF}.
0	1	0	Activate System Calibration. This activates system calibration on the channel selected by CH. This is a two-step calibration sequence, with the zero scale calibration done first on the selected input channel and $\overline{DRDY}$ indicating when this zero scale calibration is complete. The part returns to Normal Mode at the end of this first step in the two-step sequence.
0	1	1	Activate System Calibration. This is the second step of the system calibration sequence with full-scale calibration being performed on the selected input channel. Once again, $\overline{DRDY}$ indicates when this full-scale calibration is complete. When this calibration is complete, the part returns to Normal Mode.
1	0	0	Activate System-Offset Calibration. This activates system-offset calibration on the channel selected by CH. This is a one-step calibration sequence and when complete the part returns to Normal Mode with $\overline{DRDY}$ indicating when this system offset calibration is complete. For this calibration type, the zero scale calibration is done on the selected input channel and the full-scale calibration is done internally on V_{REF}.
1	0	1	Activate Background Calibration. This activates background calibration on the channel selected by CH. If the background calibration mode is on, then the AD7712 provides continuous self-calibration of the reference and shorted (zeroed) inputs. This calibration takes place as part of the conversion sequence, extending the conversion time and reducing the word rate by a factor of six. Its major advantage is that the user does not have to worry about recalibrating the device when there is a change in the ambient temperature. In this mode, shorted (zeroed) inputs and V_{REF}, as well as the analog input voltage, are continuously monitored and the calibration registers of the device are automatically updated.
1	1	0	Read/Write Zero-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the zero scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the zero scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits regardless, of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.
1	1	1	Read/Write Full-Scale Calibration Coefficients. A read to the device with A0 high accesses the contents of the full-scale calibration coefficients of the channel selected by CH. A write to the device with A0 high writes data to the full-scale calibration coefficients of the channel selected by CH. The word length for reading and writing these coefficients is 24 bits, regardless of the status of the WL bit of the control register. Therefore, when writing to the calibration register, 24 bits of data must be written, otherwise the new data will not be transferred to the calibration register.

PGA Gain

G2	G1	G0	Gain	
0	0	0	1	(Default Condition After the Internal Power-On Reset)
0	0	1	2	
0	1	0	4	
0	1	1	8	
1	0	0	16	
1	0	1	32	
1	1	0	64	
1	1	1	128	

Channel Selection

CH	Channel		
0	AIN1	Low Level Input	(Default Condition After the Internal Power-On Reset)
1	AIN2	High Level Input	

Power-Down

PD		
0	Normal Operation	(Default Condition After the Internal Power-On Reset)
1	Power-Down	

Word Length

WL	Output Word Length	
0	16-Bit	(Default Condition After Internal Power-On Reset)
1	24-Bit	

Burn-Out Current

BO		
0	Off	(Default Condition After Internal Power-On Reset)
1	On	

Bipolar/Unipolar Selection (Both Inputs)

B/U		
0	Bipolar	(Default Condition After Internal Power-On Reset)
1	Unipolar	

Filter Selection (FS11–FS0)

The on-chip digital filter provides a $Sinc^3$ (or $(Sinx/x)^3$) filter response. The 12 bits of data programmed into these bits determine the filter cutoff frequency, the position of the first notch of the filter and the data rate for the part. In association with the gain selection, it also determines the output noise (and hence the effective resolution) of the device.

The first notch of the filter occurs at a frequency determined by the relationship: filter first notch frequency = $(f_{CLK\ IN}/512)/code$ where *code* is the decimal equivalent of the code in bits FS0 to FS11 and is in the range 19 to 2,000. With the nominal $f_{CLK\ IN}$ of 10 MHz, this results in a first notch frequency range from 9.76 Hz to 1.028 kHz. To ensure correct operation of the AD7712, the value of the code loaded to these bits must be within this range. Failure to do this will result in unspecified operation of the device.

Changing the filter notch frequency, as well as the selected gain, impacts resolution. Tables I and II and Figure 2 show the effect of the filter notch frequency and gain on the effective resolution of the AD7712. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, then a new word is available at a 50 Hz rate or every 20 ms. If the first notch is at 1 kHz, a new word is available every 1 ms.

The settling time of the filter to a full-scale step input change is worst case 4 × 1/(output data rate). This settling time is to 100% of the final value. For example, with the first filter notch at 50 Hz, the settling time of the filter to a full-scale step input change is 80 ms max. If the first notch is at 1 kHz, the settling time of the filter to a full-scale input step is 4 ms max. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with $\overline{SYNC}$ low, the settling time will be 3 × 1/(output data rate). If a change of channel takes place, the settling time is 3×1/(output data rate) regardless of the $\overline{SYNC}$ input.

The −3 dB frequency is determined by the programmed first notch frequency according to the relationship: filter −3 dB frequency = 0.262 × first notch frequency.