Model 3623-L1A

6-channel, Opto-isolated Counter

INSTRUCTION MANUAL

July, 1988

*** NOTICE OF PRODUCT SPECIFICATION CHANGE ***

May, 1995

MODEL 3623-L1A
6-channel, Opto-isolated Counter

The minimum input signal pulse width for this module has been increased from 50 nanoseconds to 200 nanoseconds. If the change in specification causes a problem for your application, please contact the factory.

SPECIAL OPTION

Model 3623-S002

6-channel, Opto-isolated Counter

October, 1990

SPECIAL OPTION

The Model 3623-S002 is the same as a Model 3623-L1A that has been modified to handle a single-ended 24 volt input signal.

October, 1990
DFD:bh

Model 3623
Operating Manual
(Rev. 7/88)

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KineticSystems Corporation

Standardized Data Acquisition and Control Systems **3623**

6-channel, Opto-isolated Counter

FEATURES

- **Six counters**
- **Maximum count, each counter, 24 bits (16,777,215)**
- **Optically isolated inputs**
- **External latch signal to update output registers**
- **Counter inhibit input**
- **LAM on overflow or external latch signal**
- **dc to 10 megahertz**

APPLICATIONS

- **Event counting**
- **Totalizing**
- **Process monitoring**
- **Timed-division counting**

GENERAL DESCRIPTION

The Model 3623 is a single-width CAMAC module containing six 24-bit, optically isolated counters. Each counter channel receives its input pulse through a front-panel-mounted, two-contact LEMO connector. Before a pulse can reach the counters, it must proceed through the inhibit control circuit. Each counter's value must be loaded into its output register before it can be read onto the Dataway. Two ways are provided for the output registers to be updated. One is to constantly update them at the beginning of every command to the module. In this way, the value that is read is the current value of the counters. The user's second option is to use the external latch signal. Upon the receipt of this signal at the front-panel LEMO connector, all six output registers will be updated with the present value of the counters. The output registers will not change until the next recognized external latch signal is received. However, the counters will continue to count independently.

A strap provided for each channel allows the counters to be cleared after the output register is updated. This latch and clear mode will allow the user to read the number of pulses between latch signals.

The 3623 counter's LAM status register is strap-selectable for both an overflow or external latch mode. In overflow mode, when any of the counters reach 2^{24} (or 2^{16} selected by a jumper), that counter will set its overflow LAM status bit. The six LAM status bits are 'OR'ed and, when enabled, produce a LAM request. The pattern of the six LAM status bits can be read to locate the specific counter that overflowed. The LAM status bits are cleared by Dataway commands. In the External Latch Mode, the LAM status bit is set when the external latch signal is received, and if enabled, a LAM Request is produced. This LAM status bit is cleared either by an F(10)·A(6) or a Read of the last counter, F(0)·A(5).

All six counter inputs and the external latch input are optically isolated from the module. A signal of 2.4 to 5.0 volts across the two contacts of the input connector will turn on the optical isolator, when received from an 8830 type line-driver supplying at least five milliamperes. All counter inputs accept this signal as a logical "one" and clock the counter on the zero-to-one transition. The polarity of the external latch signal is user-strap-selectable. Each of the above-mentioned inputs has room for the insertion of a termination resistor by the user. All the inputs accept a signal with a minimum pulse width of 50 nanoseconds. The six counter inputs and the external latch input can be strapped to accept a TTL open-collector output signal.

The counters can be inhibited by the Dataway Inhibit or by a low-true TTL signal on the front-panel-mounted single-contact LEMO connector. When precise timing of sequenced events is desired, the Model 3655 Timing module can provide a time base for the 3623 by asserting the Dataway Inhibit line for a programmable time interval.

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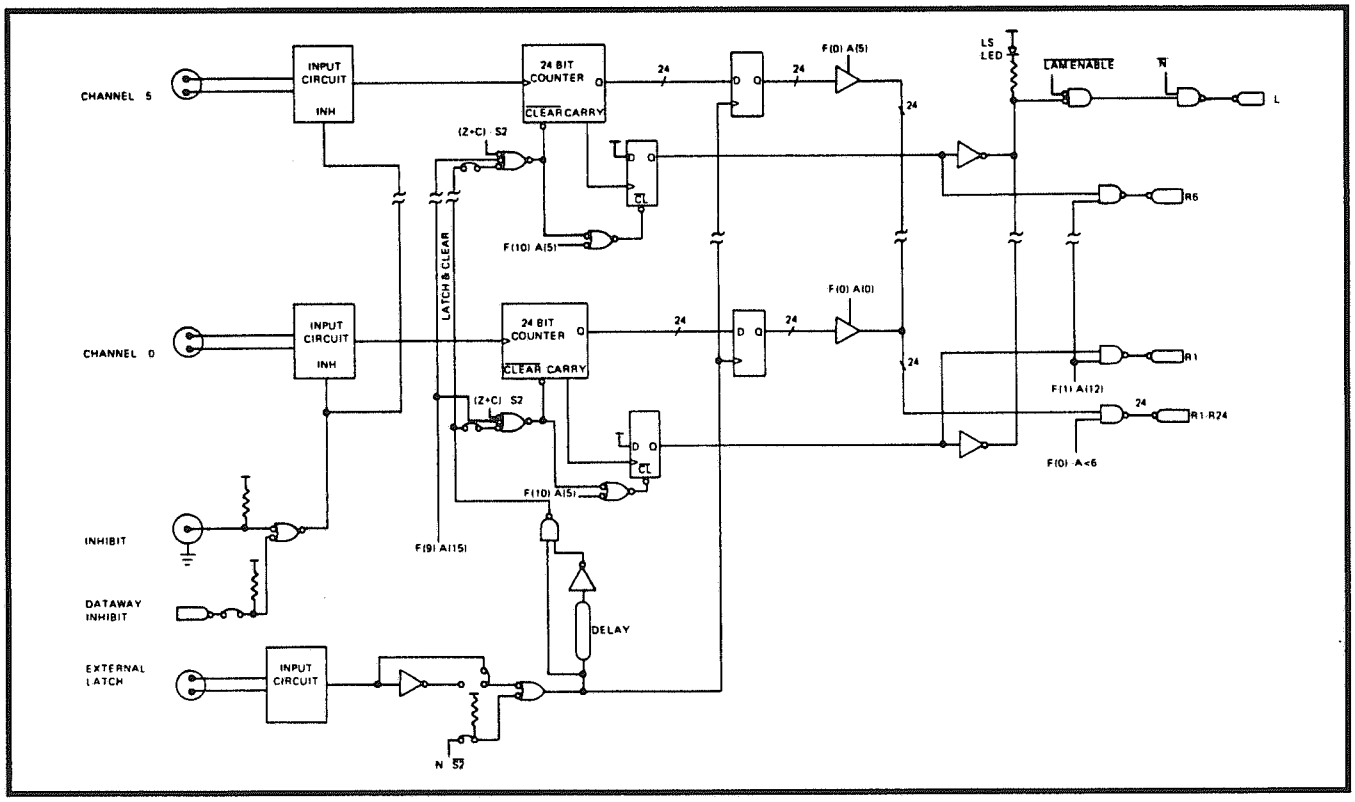
FUNCTION CODES

Command		Q	Action
F(0)·A(i)	RD1	1	Reads the Counter i. (See Note 6)
F(1)·A(12)	RD2	1	Reads the LAM Status register.
F(8)·A(0)	TLM	OVR LR ·	Tests Overflow LAM request.
F(8)·A(1)	TLM	LATCH LR	Tests Latch LAM request.
F(9)·A(15)	CL1	1	Clears LAM Status register and all counters.
F(10)·A(i)	CLM	1	Clears Overflow LAM Status i.
F(10)·A(6)	CLM	1	Clears external Latch LAM status.
F(24)·A(0)	DIS	1	Disables Overflow LAM request.
F(24)·A(1)	DIS	1	Disables external Latch LAM request.
F(25)·A(0)	XEQ	1	Increments all counters.
F(26)·A(0)	ENB	1	Enables Overflow LAM request.
F(26)·A(1)	ENB	1	Enables external Latch LAM request.
C	CZ	0	Clears all counters and the LAM Status register.
Z	CZ	0	Clears all counters and the LAM Status register, disables both LAM requests.

Notes: 1. i can range from 0 to 5.
2. Dataway Inhibit prevents counting.
3. X = 1 for all valid addressed commands.
4. OVR LR = 1 if Overflow LAM request is set.
5. LATCH LR = 1 if external Latch LAM request is set.
6. F)0)·A(5) will clear Latch LAM status bit.

SIMPLIFIED BLOCK DIAGRAM



POWER REQUIREMENTS

+6 volts — 1400 mA

ORDERING INFORMATION

Weight: .58 kg. (1 lb. 4 oz.)

Model 3623-L1A — 6-channel, Opto-isolated Counter

Accessories — For Counter and Latch Inputs: Model 5911-Z1A Mating Connector
Model 5857-Cxyz Cable Assembly
Model 5857-Dxyz Cable Assembly

For Inhibit Input: Model 5910-Z1A Mating Connector
Model 5857-Axyz Cable Assembly
Model 5857-Bxyz Cable Assembly

FUNCTION CODES:

F(0)A(i) Reads 24 bit value stored in output register of channel i (i=0 to 5). The output register holds the value of the counter at the time the latch signal was received, F(0)A(5) also clears the Latch LAM status bit.

F(1)A(12) Reads the LAM Status Register. This register will show which of the channels has overflowed and whether a latch signal has been received.

A LAM Request is generated to the Crate Controller when a LAM status bit is set and a LAM Request is enabled (F26·A0 and/or F26·A1).

NOTE: When channels are strap for Latch and Clear Mode and with the receipt of the Latch Signal, those channels LAM status bit will be cleared.

Bit 7						Bit 1
LATCH	CHAN 5 OVRFLW	CHAN 4 OVRFLW	CHAN 3 OVRFLW	CHAN 2 OVRFLW	CHAN 1 OVRFLW	CHAN 0 OVRFLW

LAM STATUS REGISTER

F(8)A(0) This command indicates if a LAM Request is present on the module by returning Q=1. This LAM Request is the result of the LAM Request being enabled by the F(26)A(0) command and that at least one of the six channels has overflowed.

F(8)A(1) Like the F(8)A(1), Q=1 is returned when a LAM Request is present. This LAM Request is the result of the F(26)A(1) command enabling the LAM Request and the LATCH LAM status bit being set.

F(9)A(15) Clears LAM Status Register and all counters. Does not disable LAM Requests.

F(10)A(i) Clears the LAM Status overflow bit of channel i. Does not clear the counters.

F(10)A(6) Clears the LAM Status bit that is set by the external latch signal.

F(24)A(0) Disables the overflow LAM Request. The module powers up with the LAM Request disabled so it is only necessary to do this command after the LAM Request has been enabled.

F(24)A(1) Disables the External Latch LAM Request. Module powers up with LAM Request disabled.

F(25)A(0) This is self-test command which will clock all the counters once every time it is performed. The opto-isolators should be turned off when this command is being used. If the inputs to the module are left in a true state they will prevent the F(25)A(0) command from clocking the counters.

F(26)A(0) Enables the overflow LAM Request. With the LAM Request enabled and at least one of the channels have overflowed the LAM signal will be put onto the Dataway for the crate controller to detect.

F(26)A(1) Enables the External LATCH LAM Request. Allows a LAM to be generated when the LATCH signal is received.

Front-Panel Description

LED's:

N - Pulses whenever the 3623 is addressed

LE - Lit whenever the 3623 has one of the LAM Requests enabled allowing the appropriate LAM status bit to generate a LAM Request to the Crate Controller.

LS - Lit when any of the LAM Status bits are set. This is readable by an F(1)·A(12) command.

CONNECTORS:

The front-panel of the Model 3623 has seven 2-contact LEMO's and one single-pin LEMO, six of the 2-contact LEMO's are for clock inputs while the seventh one accepts the External Latch signal. The female contact of the connector is the positive side (pin 1) and the male contact is the negative (pin 2). The single-pin LEMO accepts a low-true signal to Inhibit the modules counting.

KineticSystems cable assemblies Model 5857-Axyz through 5857-Dxyz mate with the front-panel LEMO connectors.

INPUT SELECTION:

Each input can be strapped separately to accept either a TTL open-collector signal or a differential line-driver (8830 type) signal. If it is necessary to have the line-driver signal terminated solder pad locations are provided for the user to insert a ¼ watt resistor. All input signals should have a minimum pulse width of 50 nanoseconds.

LINE-DRIVER INPUT:

With Strap Bi loaded the input will accept the output of a differential line-driver with the output characteristics like National's 8830. A voltage signal of approximately 2.4 volts will turn on the optical-isolator. This voltage is considered a logical "one" for all the counter inputs, and the Latch Input when the "NOR" strap is loaded. The female contact facing the front, toward the left-hand side of connector, should be the more positive contact for the optical-isolator to turn-on. The counters are incremented on the transition from a logical "zero" to a logical "one" of the input pulse. The optical-isolators provide an isolation voltage of 3000 Volts DC in this configuration.

If the Latch Input is not used, strap the Latch Input to Driver and place the NOR/INV strap to the NOR position. The N·S2 must also be loaded if the Latch Input is not used.

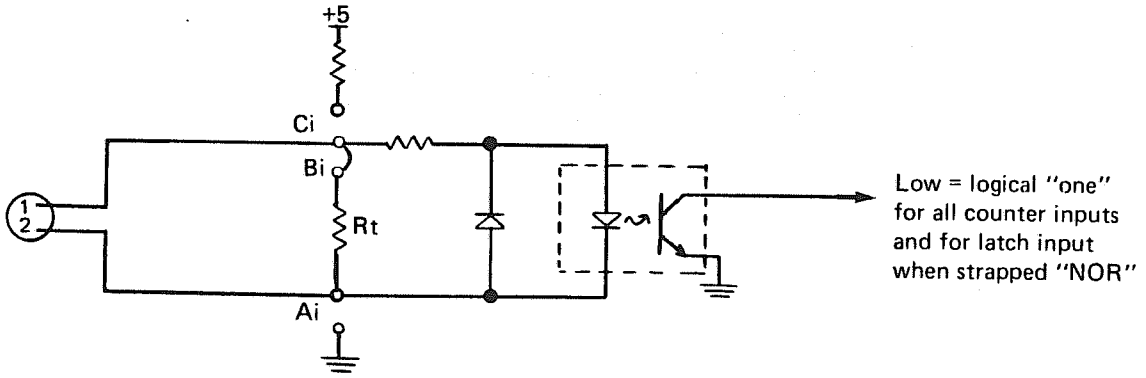


FIGURE 1: Straps Loaded in Ai and Ci Open-Collector Input.
Strap loaded in Bi line driver input.

TTL OPEN-COLLECTOR INPUT:

A TTL Open-Collector output gate can drive each input two different ways. When both Ai and Ci are loaded the open-collector output is connected to the positive input. A logical "zero" is the result of the output sinking at least 10 milliamps, and a logical "one" occurs when the output gate is turned off.

The output gate is connected to the negative input when strap Ai is removed and Ci is loaded. The logic convention for inputting a clock signal is the inverse of the previous paragraph.

Due to the addition of the pull-up resistor to the input circuit the module's circuitry will not be isolated from the device supplying the signal to the 3623.

If the Latch Input is not used, then strap the Latch Input to Driver and place the NOR/INV strap to NOR position. The N·S2 must also be loaded if the Latch Input is not used.

INHIBIT:

Either Dataway Inhibit or an external inhibit signal can prevent the counters from accepting clock pulses. Toggling of the Inhibit lines will not cause any false counts. The Dataway Inhibit line is user strap-selectable.

A low-level TTL signal on the external Inhibit line will prevent the counting process on the module. This output signal can be either a relay contact closure or an open-collector TTL device. A pull-up resistor is provided on the Inhibit input for these outputs. It is not necessary to terminate the external Inhibit signal when it is not used.

On crate power-up, the Crate Controller sets the inhibit line true. This will inhibit any counting to occur, if the 3623 has INH strapped. The user should clear the Crate Controllers inhibit before counting.

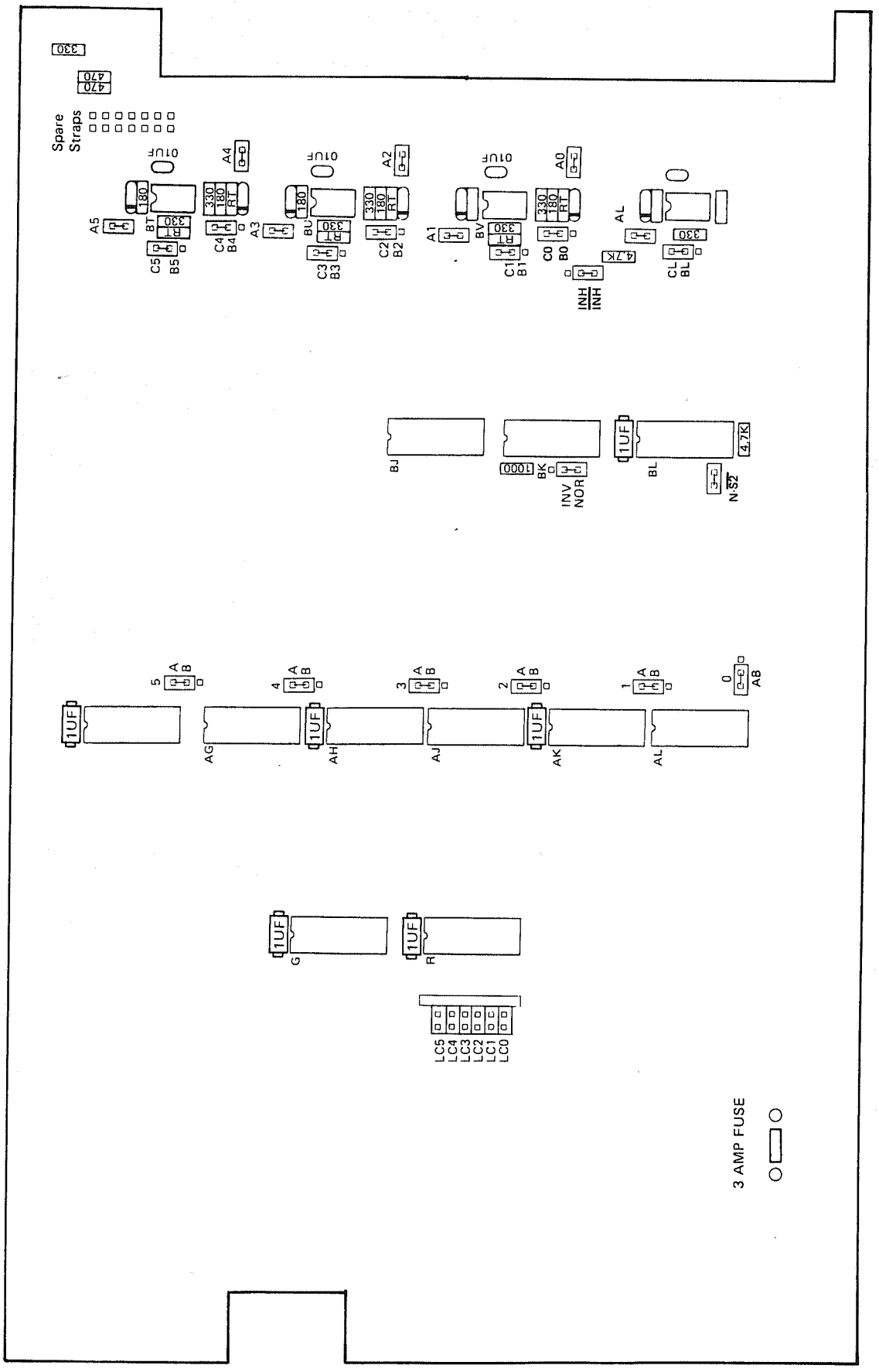
LATCH AND CLEAR MODE:

After every external Latch signal is received a clear pulse is generated. This clear pulse can be gated to each channel by loading the appropriate LCi strap (i=0 to 5). So, after the latch signal has stored the counters value into the output register the clear pulse is sent to the selected channels to clear the counter and LAM status bit. This latch & clear mode works only for the External Latch signal.

STRAPS:

LC0-LC5	When loaded this strap will clear the appropriate channel after the latch signal has clocked the counter's value into the shift register. One strap is provided per channel.
A,B	With Strap A loaded that channel will set the LAM status after the counters overflow the 24th bit. Loading the strap into location B the LAM status bit is set on 16 bit overflow. Each channel has its own strap. These straps are located in a column starting by chip AL. Each channel will continue to count after it has overflowed.
Ai,Bi,Ci*	Selects if either a Line Driver or TTL open-collector signal will be accepted by the input. Load Ai & Ci for TTL open-collector input. Load Bi for Line Driver input.
AL,BL,CL	Latch Input
A0,B0,C0	Channel 0 Input
A1,B1,C1	Channel 1 Input
A2,B2,C2	Channel 2 Input
A3,B3,C3	Channel 3 Input
A4,B4,C4	Channel 4 Input
A5,B5,C5	Channel 5 Input
INH	Dataway Inhibit Enabled to Inhibit counting
$\overline{\text{INH}}$	Dataway Inhibit Disabled
N.S2*	With this strap loaded the counters output register will be updated before and after every command to the 3623. The latch strap should be set to "NOR".
NOR*	This strap loaded when a high true latch signal is used.
INV*	For use with a low true latch signal

*NOTE: Refer to TTL open-collector or Driver Input section for proper operation.



STRAP LOCATION DIAGRAM

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KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

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Products will not be accepted for credit or exchange without the prior written approval of KineticSystems. If it is necessary to return a product for repair, replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center prior to shipping the product to KineticSystems. The following steps should be taken before returning any product:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com