Model 3655-L1A

8-channel Timing Pulse Generator

User's Manual

March 12, 1987

*** Special Option ***

Model 3655-S002

October 1985

****Special Option******

Model 3655-S002

The 3655-S002 is a 3655-L1A which has been modified such that the assertion of the Dataway Inhibit line has the same effect as the execution of a CAMAC Z cycle (i.e., the counters are disabled and the LAM status bits are cleared).

In this Special 3655-S002, drawing #02250-D-1559 replaces #02250-D-291

October 1985

**** SPECIAL OPTION ****

Model 3655-S003

Eight-Channel Timing Pulse Generator

November, 1986

**** SPECIAL OPTION ****

Model 3655-S003

Eight-Channel Timing Pulse Generator

The Model 3655-S003 is the same as the Model 3655-L1A except that it has been modified to assert P1 on the dataway instead of the Inhibit line. This will be used as an external trigger for the 3595. This special takes away the Inhibit line feature of the 3655. The intended application requires that one channel be programmed to SET the P1 line, and the next channel be programmed to CLEAR the P1 line. This change has been made to meet SPERRY specifications.

November, 1986

*** SPECIAL OPTION ***

Model 3655-S004

Eight-Channel Timing Pulse Generator

September, 1988

*** SPECIAL OPTION ***

Model 3655-S004

Eight-Channel Timing Pulse Generator

The Model 3655-S004 is the same as the Model 3655-L1A except that it has been modified to extend the output pulse width to 10 Microseconds.

September, 1988
MLH:rem(3000 13)

*** SPECIAL OPTION ***

Model 3655-S005

8-channel Timing Pulse Generator

May, 1989

*** SPECIAL OPTION ***
Model 3655-S005
8-channel Timing Pulse Generator

The Model 3655-S005 is the same as a 3655-L1A, except that it has been modified
to reset (clear) the Dataway Inhibit Signal (I) when an External Start Signal
is applied to the module's front panel. In all other instances, the module
performs as described in this manual.

May, 1989
MLH:rem (WP\MLH)

*** SPECIAL OPTION ***

Model 3655-S008

8-channel Timing Pulse Generator

February, 1991

*** **SPECIAL OPTION** ***

Model 3655-S008
8-channel Timing Pulse Generator

The Model 3655-S008 is the same as a 3655-L1A, except that it has been modified to provide an accurate time reference signal to be used for calibrating the 3664. The crystal accuracy is .0025%.

JRH:rem(WP)
February 8, 1991

SPECIAL OPTION

Model 3655-S009

8-channel Timing Pulse Generator

November, 1991

SPECIAL OPTION

3655-S009

The Model 3655-S009 is the same as the 3655-L1A except it has been modified to bring an internal clock disable signal in through the front panel on the EXT. CLOCK LEMO. A +5 signal on EXT. CLOCK will disable the internal clock until it is again enabled by EXT START, F(25)A(0) or F(9)A(2).

JRH:rem

(Rev. November 13, 1991)

Model 3655-S2002

The Model 3655-S2002 is an Eight-Channel Timing Pulse Generator.
One channel is enabled at a time. The channel selection is made
by Bits 4 through 6 of the Cycle Control register. This register
is accessed using the $F(17) \cdot A(0)$ command. Bits 4 through 6 set
to 0 selects Channel 1. Bits 4 through 6 set to 1 selects Chan-
nel 8.

23 January 1979

*** SPECIAL MODULE ***

This 3655 has been modified so that OUTPUTS 1 - 4 are high true and OUTPUTS 5 - 8 are low true.

The output IC's are as follows:

      IC BY   7406   (outputs 1 - 4)

      IC BX   7407   (outputs 5 - 8)

28 Nov. 78

8-channel Timing Pulse Generator

Features

- Eight independent outputs
- Self-contained crystal clock
- Provision for external clock
- Option for high-true or low-true output pulses
- LAM status bit associated with each output channel
- 8-bit LAM mask register
- Clock variations from one hertz to one megahertz in decade steps
- Clock rate under software control
- Ability to cycle through any number of channels from one to eight
- Ability to control Dataway Inhibit
- Ability to cycle once and stop or to continue cycling
- Ability to start cycle by external signal or by internal command

Typical Applications

- Counting-system time base
- Programmable clock
- Programmable timed interrupt
- Timing mark generator
- Accelerator clock

General Description *(Product specifications and descriptions subject to change without notice.)*

The 3655 is a single-width CAMAC module containing a 16-bit counter and eight 16-bit set-point registers that are compared with the counter. The comparisons produce output pulses, and any of them can be used to either stop or clear the counter. The comparisons also produce LAM status bits, which can be individually enabled to produce LAM requests.

A flag bit determines whether the counter stops with the last output pulse or whether it is cleared to produce repeating sequences of timing pulses. In the former mode of operation, additional pulse sequences are initiated either by programmed command or by external signal or contact closure.

The 3655 provides its own crystal clock, and the input frequency to the counter is software-controlled for any decade from one hertz to one megahertz. Input to the counter can also come from an external source. Two of the comparisons can set and clear the Dataway Inhibit.

Numbers in the eight registers (or fewer, if less than eight pulse sources are required) must be stored in increasing numerical order for proper timing of output pulses.

Two control registers provide programmable control of the clock frequency (one hertz to one megahertz), the number of channels that generate a pulse (one to eight), the assertion of Dataway Inhibit, and whether to stop or recycle after the last pulse. The bit assignments in the registers are shown on the following page.

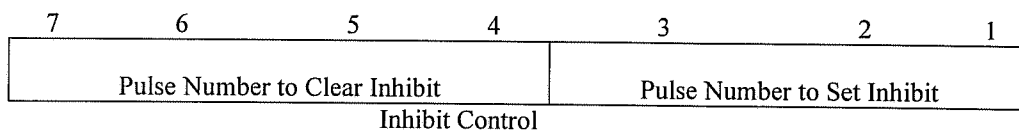| 7	6	5	4	3	2	1
Stop/ Recycle	Number of Output Pulses			Clock Frequency		

Cycle Control
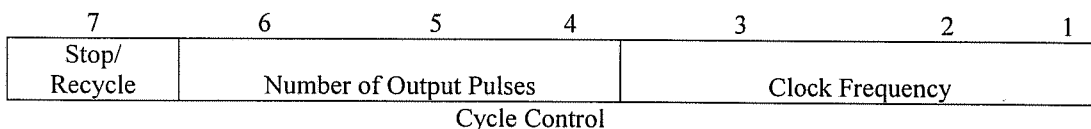
Bits 1, 2, 3 = N, where clock frequency = 10^NHz (N = 7 selects the external input).
Bits 4, 5, 6 = P, where P + 1 = number of channels that generate a pulse.
Bits 7 = 1 to continuously cycle, 0 to cycle once and stop.

7	6	5	4	3	2	1
	Pulse Number to Clear Inhibit			Pulse Number to Set Inhibit		

Inhibit Control

All inputs and outputs appear on front-panel LEMO connectors as well as on the 36-pin P.C. connector at the rear of the module

Function Codes

Command		Q	Action
F(0) A(i)	RD1	1	Reads Set Point
F(1) A(12)	RD2	1	Reads the LAM status bits
F(1) A(15)	RD2	1	Reads the module identifying number (3655 = 7107_8)
F(8) A(15)	TLM	LR	Tests whether a LAM request is present
F(9) A(8)	CL1	1	Clears and enables the counter and clears the LAM status bits
F(11) A(12)	CL2	1	Clears the LAM status bits
F(16) A(i)	WT1	1	Writes Set Point i
F(17) A(0)	WT2	1	Writes the Cycle Control register
F(17) A(9)	WT2	1	Writes the Inhibit Control register
F(17) A(13)	WT2	1	Writes the LAM Mask register
F(24) A(9)	DIS	1	Disables the ability of the module to assert Inhibit
F(25) A(0)	XEQ	1	Executes start of counting cycle (clears and enables counter)
F(26) A(9)	ENB	1	Enables the ability of the module to assert Inhibit
C	CC	0	Clears the LAM status bits
Z	CZ	0	Disables the counter and clears the LAM status bits

Notes:
1. i can range from 0 to 7
2. X = 1 for all valid addressed commands.

Power Requirements

Weight: .60 kg. (1 lb. 5 oz.)

+6 volts 1400 mA

Ordering Information

Model 3655-L1A   8-channel Timing Pulse Generator, Low-true Outputs

The Model 3655 is shipped with ICs for low-true outputs loaded in sockets. ICs for high-true output pulses are included, and the conversion from low to high-true outputs may be made by the user.

Accessories

Model 5910-Z1A, 5960-Z1A or 5960-Z1B Mating Connector

FRONT PANEL

LEDs

N	Flashes whenever this module is addressed
L	Indicates the LAM source is set
IS	Indicates that this module is asserting Dataway Inhibit
1-8	Indicates that this channel is "armed" to pulse next

I/O CONNECTORS (All are TTL level)

1 – 8 Eight single pin LEMOs, one for each channel's output

Recycle One single pin LEMO for an external start signal. A low true clock pulse should be used. The high-to-low transition clears the counters, and the low-to-high transition then starts the count.

Clock One single pin LEMO for an external clock signal. This clock is selected by setting bits one, two and three of the cycle control register. A high-to-low transition constitutes one tick of the clock.

OUTPUT SIGNALS

The output pulses are TTL level and 200 μSec in duration. Model 3655-L1A has low true outputs, provided by 7407 ICs in locations BX and BY. Model 3644-L1B has high true outputs, provided by 7406 ICs in locations BX and BY. The ICs in BX and BY are mounted in sockets for convenient conversion.

BLOCK DIAGRAM

The following sections describe the operation of the 3655 in detail. It will be useful to refer to the enclosed block diagram #02150-C-1351, while reading these sections.

CYCLE CONTROL REGISTER, F(17) A (0)

Timing Source

The timing source can be the internal crystal clock (0.025% accuracy) or an external clock input. The basic clock source is selected by the three bits in an F(17) A (0) command. If these three bits are represented by a decimal number, N, the time-base clock frequency (derived from the internal crystal clock), is 10 NHz for N = 1 to 6, (1 Hz to 1 Megahertz in decade steps). When N = 7, the external clock input is selected. The external TTL clock can be any frequency from DC to 1 Megahertz.

Number of Channels

Bits four to six in the Cycle Control register select the number of channels that generate a pulse. If these three bits represent a decimal number, P, then P = 1 = number of pulsed channels, starting with Channel 1. For example, if P = 7, all eight channels will pulse, starting with Channel 1 and ending with Channel 8. If P = 0, only Channel 1 will pulse.

Single Cycle/Recycle

Single cycles (Bit seven in cycle control register = 0)
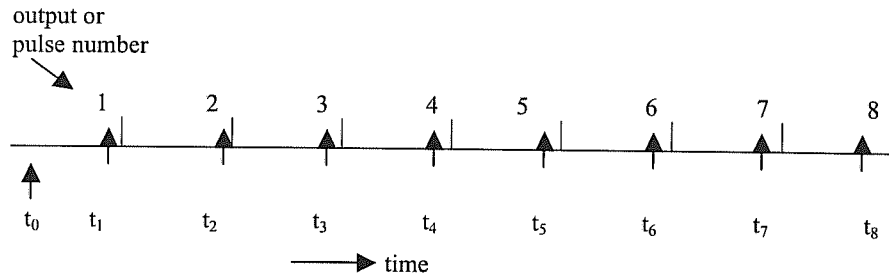
1. The cycle is started at t_0 by an F (25) A (0) command, and F (9) A (8) command or external start pulse.

2. The cycle is terminated at t_8 when the last pulse is generated (in the example above). If bits four to six are set, for example, to select only seven channels, the cycle is terminated at t_7.

3. If any of the start signals described in (1) are asserted during the pulse sequence, the sequence will terminate at that point and be restarted at t_0.

4. Power-up or crate initialization causes the module to be in the "single cycle" mode.

Recycle (Bit seven in cycle control register = 1.)

NOTE:
Numbers shown indicate when that channel is pulsed
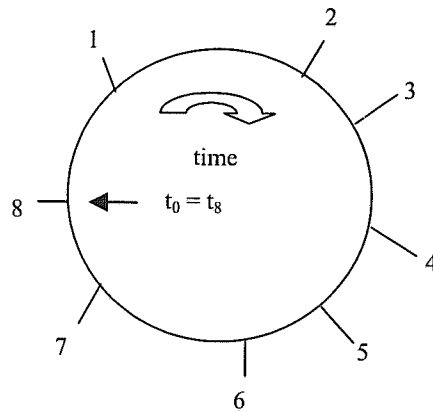
1. If counting cycle is stopped and recycle operation is desired, the recycle bit should be set to one; then the cycle can be started at t_0 by an F (25) A (0) command, and F (9) A (8) command or external start pulse. NOTE: Pulse output 8 will not be produced initially; the first pulse will be Pulse Output 1. In this example all eight pulse outputs were selected by bits four through six. If seven channels were selected $t_7 = t_0$.

2. If bit seven in the cycle is changed to zero during counting, the cycle will terminate at the next t_8.

WRITE SET POINT, F (16) A (I)

The timing delay for channels 1 to 8 is written at subaddress A0 through A7, respectively. All timing references are made to time t_0 on the previous charts. A pulse is produced from a channel output when the number of counts of the time base (referenced to t_0) equals 16-bit set point number for that channel.

For example, if the Cycle Control register is set for 100 kilohertz (one pulse per 10 microseconds), and the set point for Channel 1 is 50 (decimal), the Channel 1 pulse will occur 500 microseconds after t_0. If the channel 2 set point is 80, its pulse will occur 800 microseconds after t_0 and 300 microseconds after t_1.

Since the set point registers are 16 bits each, any number from 1 to 65,536 (decimal) can be written, (zero is not a valid setting). The shortest time is one microsecond (1 MHz and set point = 1), while the longest time (with internal clock) is 65,536 seconds (1 Hz and set point = 65,536). This is slightly longer than 18.2 hours.

Since the internal counter in the 3655 is compared with the set point memory in sequence (channels 1 through 8, THE NUMBERS STORED IN THE EIGHT REGISTERS (or fewer if less than eight pulse sources are selected) MUST BE IN INCREASING NUMERICAL ORDER. Failure to do this will cause the counter to "go all the way around" when that set point is compared.

LAM ACTION

As set by the MAL mask, the module will assert a LAM when a particular channel is pulsed. The LAM status register can be read by an F (1) A (8) command to determine the source of the LAM. The LAM status register is then cleared by an F (11) A (12) command or F (9) A (8) command. If the F (9) A (8) command is used, an internal start pulse is also generated (time becomes t_0).

The versatile LAM structure can be used for Real Time Clock applications. The assertion of the LAM can be the result of the delay from an internal of external event, or it can be a repetitive clock (50 to 60 Hz rate, for example).

INHIBIT CONTROL REGISTER, F (17) A (9)

It is often useful to determine the number of external events that occur in a fixed period (one seconds, for example). The3655 can be set to assert the Dataway Inhibit line coincident with any output pulse and release that line coincident with another output pulse. This can be used as a timing "window" for counting modules, such as the 3610, 3615 or 3640.

The lower three bits select the channel to set Inhibit (0 = channel 1, etc.), and the next three bits select the channel to release Inhibit. The Inhibit line is actually set only if the enable command, F (26) A (9) has been previously sent. If the enable command is sent after power up or initialized, the Inhibit line will be set. The front panel LED indicates that the 3655 is setting the Inhibit line.

The Inhibit control by the 3655 is a very powerful tool. Sequence is being presented to external devices and counting by a 3610, etc., is to be done only during one phase of this external sequence. The Inhibit line would be released only during that time.

```
1R  ▯  1



18R ▯  18
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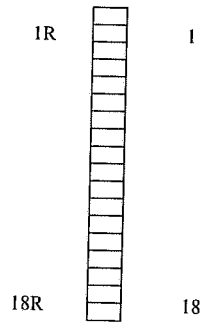
FACE VIEW

Pin/Wire List
18/36 POSITION P.C. EDGE

PIN #		PIN #	
1R	GND	1	GND
2R	SP 1	2	GND
3R	SP 2	3	GND
4R	SP 3	4	GND
5R	SP 4	5	GND
6R	SP 5	6	GND
7R	SP 6	7	GND
8R	SP 7	8	GND
9R	SP 8	9	GND
10R	RECYCLE	10	GND
11R	EXTERNAL CLOCK	11	GND
12R		12	
13R		13	
14R		14	
15R		15	
16R		16	
17R		17	
18R		18	

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1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com