Model 3660-Z1A\Z1B

Programmable Clock Generator

INSTRUCTION MANUAL

March, 1993

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Schematic Drawing #222245-C-6416

See Reply Card Following Warranty

Warranty
MJS:rem(WP)

Programmable Clock Generator

Creates custom clock rate profiles for digitizing signals **3660**

Features

- **Programmable frequency sequence of up to 256 steps**
- **Programmable frequency range from 0.5961 Hz to 10.00 MHz**
- **Strobe and gate outputs to delineate groups of output clocks (steps) programmable by number of clocks per group, number of external input triggers, or CAMAC command**
- **Optional LAM generation at end of each program step**

Typical Applications

- **Programmable transient recorder clock**
- **Programmable clock for data acquisition**
- **Synchronized data acquisition e.g. from shaft encoder**

General Description *(Product specifications and descriptions subject to change without notice.)*

The 3660 is a single-width CAMAC module that provides a very flexible programmable multi-step clock generator for clocking ADCs and other front-end data acquisition modules. It provides a programmable sequence of clock rates for applications requiring different sampling rates during different phases of data collection, the ability to synchronize data sampling with an external trigger, as well as the ability to divide down an external clock source.

The 3660 provides storage for sequences as long as 256 steps where the frequency and duration of each step can be programmed. The module derives the output clock from one of three sources: a 10 MHz crystal clock, a 10.24 MHz crystal clock, or an external clock. Each step is defined by a division factor by which the base clock is divided. The duration of each step is determined by an associated count or external trigger. In the case of external trigger, the next step is initiated synchronously with the 2nd tick of the base clock. An optional LAM can be generated at the end of any step to signal the host processor that a new step has been initiated. The current frequency division, current step, sample count, previous step sample count, and program step address are located in directly accessible registers.

The frequency steps are loaded by software into the program RAM. Each step includes a base frequency divisor, a step termination selection based on a specified count, external trigger, or software command only, and a flag word that selects various options on a step by step basis. The frequency divisor is a 16-bit modulo-N value by which the base frequency is divided. This provides a frequency range from 152.59 Hz to 10 MHz range for the 10 MHz base clock. For low frequency applications, the base clock divided by 256 may be selected providing frequency ranges of 0.5961 Hz to 39.062 KHz (10 MHz base clock) or 0.6104 Hz to 40.0 KHz (10.24 MHz base clock). The count field is a 24-bit count that permits from 1 to 16 Msamples per step. When external trigger is selected, these bits are used to select a trigger divisor. A value of 4 would, for example, terminate the step on the 4th trigger.

The module is also capable of generating the following signals at the completion of a step:

- Generate a LAM.
- Generate a 50-nanosecond, high-true TTL output pulse on one or two front panel connectors.
- Generate a 50-nanosecond, high-true TTL output pulse on completion of the *last* program step.

General Description (continued)

The module can selectively set or clear a TTL level signal at the start of each step. This signal is available on the Gate-Out LEMO connector on the front panel and can be selected to drive the CAMAC Inhibit line.

The following control options are associated with each program step:

- Select external trigger, output pulse count, or software step termination,
- Disable clock output pulse for step duration (used to generate a delay).

The base clock frequency is selected by bits in the CSR register.

A previous pulse count register is provided that is loaded with the current sample count at the end of each step and is accessible by CAMAC command. This register can be read following a step to determine the number of samples from the previous step. Thus, the actual number of samples acquired during a step which was terminated by an external trigger or CAMAC command can be determined.

Function Codes

Command		Q	Action
F(0)·A(i)	RD1	1	Reads the Control Status Register (CSR).
F(0)·A(1)	RD1	1	Reads the Previous Pulse Count bits 0-23 (PPC).
F(0)·A(2)	RD1	1	Reads the Current Count bits 0-23 (CPC).
F(1)·A(0)	RD2	1	Reads the RAM Address Register (RAP).
F(1)·A(1)	RD2	INACTIVE	Reads the RAM at Selected Address and Increment Address (FSD).
F(8)·A(0)	TLM	LR	Tests the LAM Request.
F(10)·A(0)	CLM	1	Clears the LAM Status.
F(16)·A(0)	WT1	1	Writes the Control Status Register (CSR).
F(17)·A(0)	WT2	INACTIVE	Writes the program RAM Address Register (RAP).
F(17)·A(1)	WT2	INACTIVE	Writes the RAM at Selected Address and Increment Address (FSD).
F(24)·A(0)	DIS	1	Disables the LAM.
F(25)·A(0)	XEQ	INACTIVE	Resets the Program Counter.
F(25)·A(1)	XEQ	ACTIVE	Steps the Program Counter (sync with 2nd base clock tick).
F(25)·A(2)	XEQ	1	Places the module in Inactive state, clears the LAM Status, LAM Request, Inhibit, and CSR Register.
F(26)·A(0)	ENB	1	Enables the LAM.
F(27)·A(0)	TST	LS	Tests the LAM Status.
Z·S2			Places the module in Inactive state, clears the LAM Status, LAM Request, Inhibit, and CSR Register.

Notes: 1. X = 1 for all valid addressed commands.
2. Inactive Q = 1 when the 3660 is inactive, else Q = 0.
3. These commands should only be issued when the 3660 is in the Inactive state.

Power Requirements

+6 volts: 2.1 A

Ordering Information

Model 3660-Z1A Programmable Clock Generator

Related Products

Model 5910-Z1A Single-pin LEMO Connector
Model 5857-Bxyz 1-pin LEMO/RG174/1-pin LEMO Cable Assembly

OPERATION

The Model 3660 Programmable Clock Generator provides precise control over generated clock frequency. Moreover, the conditions under which the Output Clock may be altered or disabled are programmable and quite flexible.

The operation is conceptually quite simple. With the 3660 in the inactive state, the program RAM address is initialized to zero with either an F(25)A(0) command or an F(17)A(0) command with data equal to zero. A predetermined sequence of output frequency and control information governing the response of the Output Clock, LAM, CAMAC Inhibit, and other outputs is written into the on-board RAM memory. One set of frequency and control information constitutes a Step in the sequence. A Step then, consists of four consecutive 16-bit words in the RAM: a frequency divisor, a flag word, and two words containing a 24-bit termination count whose meaning is determined by Flag bits.

Once an entire sequence (up to 256 Steps) of Step information is loaded, the RAM pointer can be set to a starting Step address (usually zero). Through the CSR register, the user chooses a clock source (Base Clock) upon which the Output Clock is derived — either one of two internal crystal oscillators (10 MHz or 10.24 MHz) or an external clock provided through a front-panel single-pin LEMO connector. The user may also choose to predivide the Base Clock by 256 if the Output Clock is to be in a frequency range that is much smaller than the Base Clock. When the FPA (Frequency Program Active) bit in the CSR is set along with this Base Clock and other initializing information, the module will begin to exercise the program list.

The 3660-Z1B option provides a divide by 10 range of possible frequencies from the 3660-Z1A option. Moreover, all strobe pulse widths are longer on the Z1B option (200 nanoseconds versus 35 nanoseconds) for compatibility with modules which require longer trigger input pulses.

Control information within each Step describes the internal and external conditions required for the termination of that Step. If and when these conditions are reached, the next Step is executed with its own set of frequency and control information. Step termination can be programmed to occur after a) a predetermined number of external triggers are received (from either one of two sources), b) a predetermined number of output clocks are produced, or, at any time, upon receipt of a CAMAC F(25)A(1) command. Step executions will continue until the completion of a Step containing an EOL (End-of-List) flag bit. This will cause the next accessed Step to be the "first" step (i.e., the Step located at RAM address zero). At this point, the program will either seamlessly continue execution with this step or deactivate completely. The decision is based on the state of the RCM (Recycle Mode) bit in the CSR when the EOL Step is completed.

3660 STRAP OPTIONS

SYNChronous/ASYNChronous (2 groups)

Normally, with either the internal clocks or a free-running external clock selected as the Base Clock, the timing relationship between the transitions of the selected clock and the setting of the FPA bit through the CAMAC F(16)A(0) command is arbitrary. Since an asynchronous activation of the module program through the FPA bit could result in ambiguous counting, these straps, when in the SYNC position, synchronize the internal program activation to a safe phase of the Base Clock. This will occur (and will be displayed on the front panel "ACTIVE" LED) on the second negative-going edge of the base clock following the F(16)A(0) command. Clock frequency division and counting will begin on the succeeding, rising edge of the Base Clock.

If an external clock is used and it is externally gated off until after the F(16)A(0) command (which sets FPA) is complete, the straps may be set to the ASYNC position. This is only necessary if it is important to begin program execution and counting at the first incoming clock transitions. Otherwise, the straps may remain in the SYNC position. **AT NO TIME** should these straps be in the opposite position from one another.

Program RAM Layout

The program RAM is a 1K x 16 Static RAM. Program steps are configured as follows in the RAM:

Modulo-N bits 0-15 (N_p)	
0	Flag bits 0-7
Count bits 0-15 (Np)	
0	Count bits 16-23 (Np)

The FLAG field would be as follows:

EOL	DFLG	SGTO	LAMF	STC2	STC1	TS

Where:

EOL	End of List (This flags the last item in list.)
DFLG	Delay Flag = 1 disables CLK-OUT for step duration
SGTO	Set Gate Out (Inhibit)
LAMF	Set LAM at end of step
STC2	Generate Step Complete strobe STC-2 at end of step
STC1	Generate Step Complete strobe STC-1 at end of step
TS	Trigger Select 0-software only 1-Output Pulse Count reached 2-External Step Trigger-1 3-External Step Trigger-2

Previous Pulse Count Register (PPC)

This register is READ ONLY and contains the number of Clock output pulses generated by the previous step. Since by design the Programmable Clock can generate an indeterminate number of clocks on a given step, in some applications it may be necessary to be able to determine the number of clocks generated. This is the only means to do this. The read command is F(0)A(1). This is a 24-bit register.

PPC:	Previous Count 0-24

Control Status Register (CSR)

This is the Control/Status Register. The CSR can be read F(0)A(0) or written F(16)A(0). The format or the register is shown below:

FPA	RCM	EINH	SGO	CGO	D256	CSEL

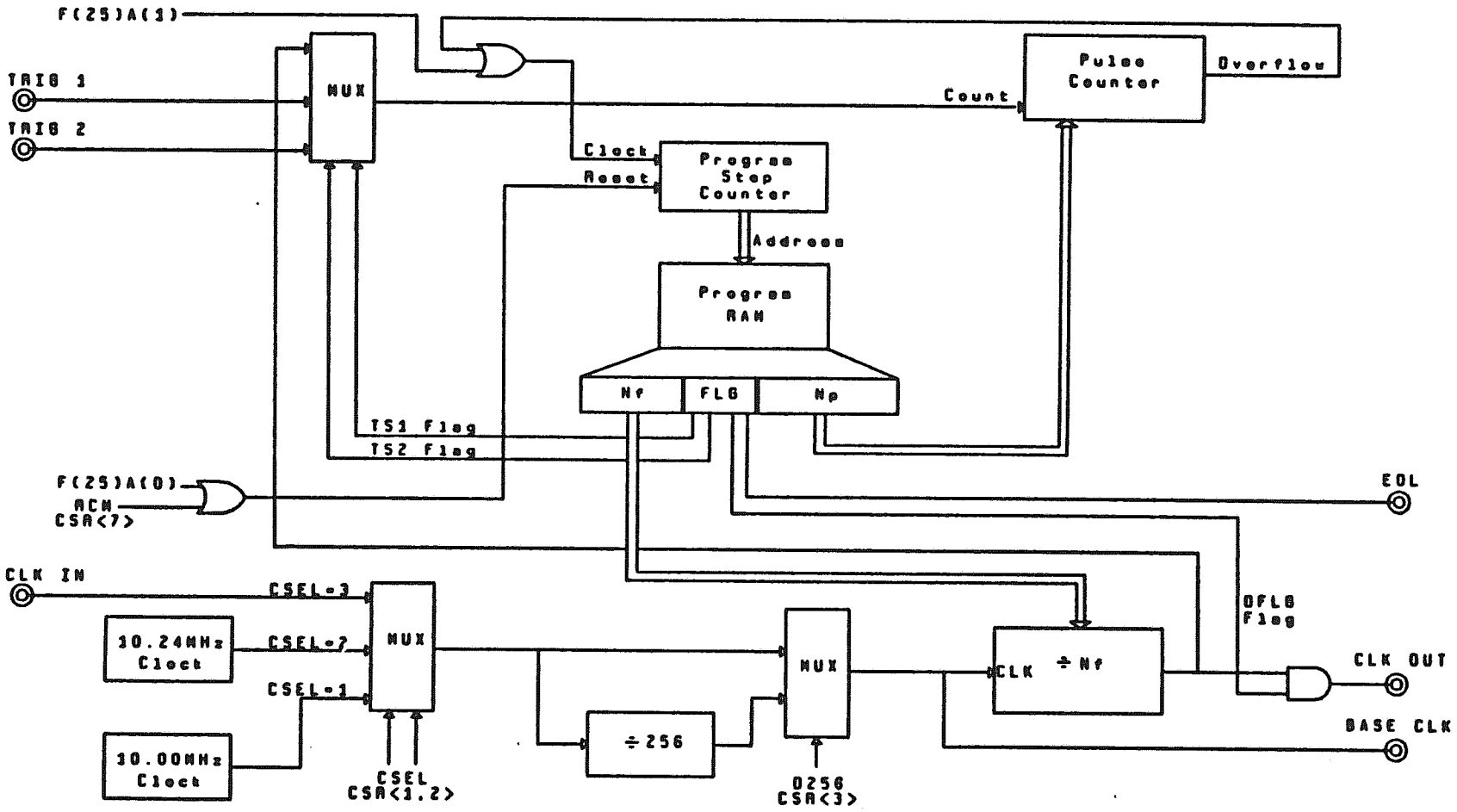
Where:

FPA	Frequency Program Active: This flag is set whenever the frequency step program is active (read). To start 3660 set FPA=1 (write), and FPA=0 to stop.
RCM	=1 Set Recycle Mode (read/write bit)
EINH	=1 Enable Inhibit when Gate-Out is true
SGO	=1 Set Gate-Out true (initialize Gate-Out)
CGO	=1 Clear Gate-Out
D256	=1 Divide Base Clock selected by CSEL bits by 256
CSEL	=0 (10.00 MHz internal clock/1.0 MHz for Z1B) =1 (10.24 MHz internal clock/1.024 MHz for Z1B) =2 (external clock)

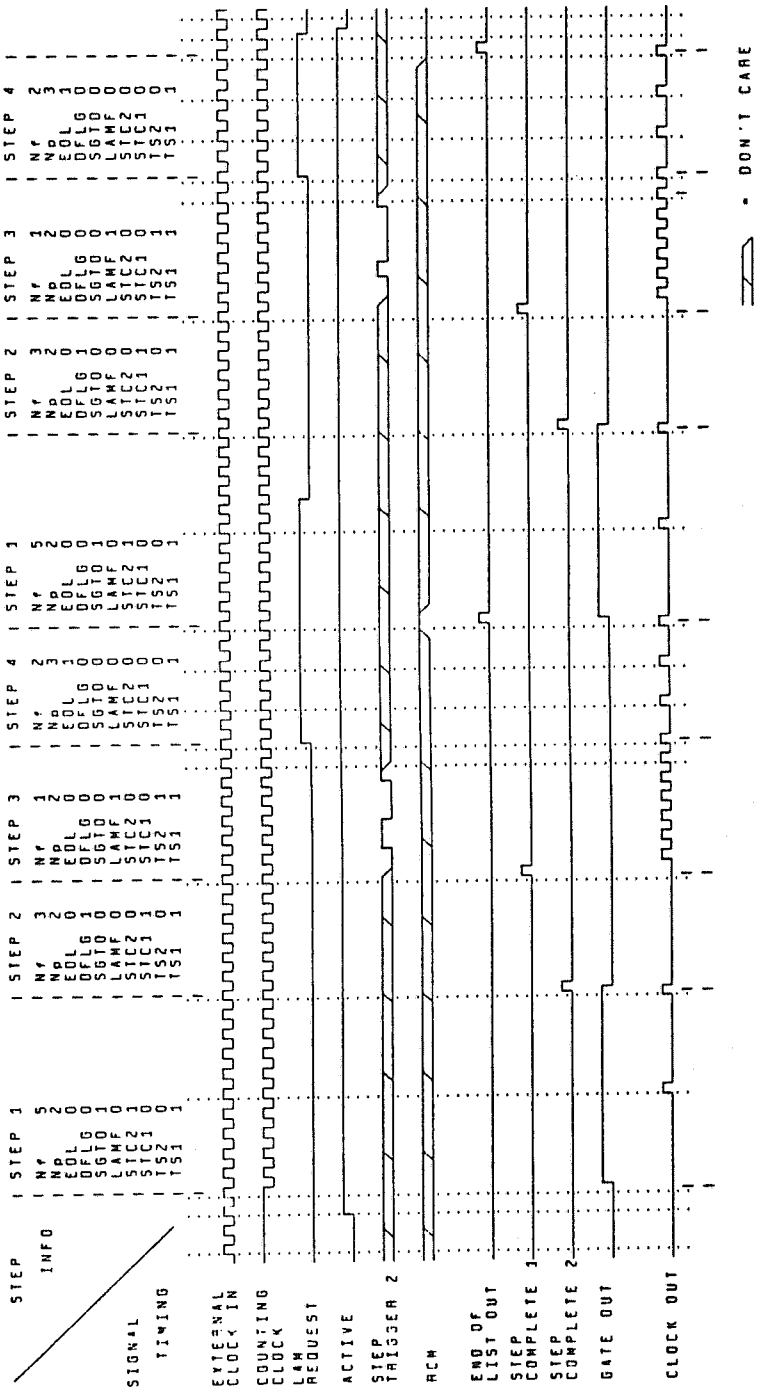
Inputs and Outputs

Inputs (Lemo)	
TRIG 1	External trigger to proceed to next step in program. The trigger is counted down by a predetermined count for each step. The step takes effect at the 2nd "tick" of the base frequency clock following the selected number of step triggers.
TRIG 2	An alternate trigger which functions identically to TRIG 1 when selected
CLK IN	Input Base Frequency from external TTL frequency source (10 MHz maximum) (1MHz maximum for the 3660-Z1B option)
Outputs (Lemo)	
BASE CLK	This output is provided to drive other Programmable Clocks from a common frequency source.
EOL	This output is pulsed at the end of the last step (step with EOL bit set). The purpose of this output is to permit external counting of the number of times the list is reset (program cycles). This count could be used to signal shutdown of the 3660 after a fixed number of cycles.
STEP CMPL 1	This output is generated at the end of selected program steps when the STC1 flag is set in the Program Step Flag byte.
STEP CMPL 2	This output is generated at the end of selected program steps when the STC2 flag is set in the Program Step Flag byte.
GATE-OUT	Latched output set or cleared at the start of each program step based on the SGTO-bit in the Program Step Flag byte.
CLK OUT	This is the generated output clock. The clock pulse is derived from the base clock in such a way as to minimize jitter in the clock output.

3660 Block Diagram



3660 Timing Example



Clock Program RAM

The programmable clock includes a 1K RAM to hold a sequence of program steps that control the frequency and duration of each step. Step duration is selected on a step-by-step basis from one of three conditions:

1. A programmed number of output clock pulses (COUNT).
2. Front Panel LEMO "step" pulses (TRIG 1 or TRIG 2 rising edge TTL triggers) or Normally Closed (to ground) contact closures.
3. Software only F(25)A(1).

Note: A step can always be terminated by F(25)A(1) CAMAC command.

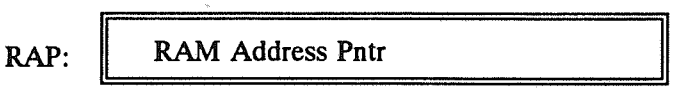
Registers

The following registers are accessible from CAMAC.

RAM Address Pointer (RAP)

In the *inactive* state, this register serves as an address register for loading a *frequency step program* into RAM. It is associated with the FSD register and is incremented following a read or write to the FSD. This register can be read F(1)A(0) any time and written F(17)A(0) only when the 3660 is in the *inactive* state. This register is used for reading or writing a program sequence into the 3660 RAM. It may also be used to define an arbitrary starting point in a list.

In the *active* state, this register provides the address of the *next* program step. Note: Each frequency step starts on a quad-word boundary (0, 4, 8, 12, ...).



Frequency Step Data (FSD)

This register provides access to the RAM at the address pointed to by the RAP register. To load a frequency step sequence, the RAP is written with an appropriate starting address (typically 0), followed by sequential 16-bit writes to the FSD with a program sequence in the order of Modulo-N bits 0-15, Flag bits 0-7, Count bits 0-15, and Count bits 16-23 using F(17)A(1) commands. The RAM can be read with a F(1)A(1) command. Both commands auto increment the RAP register. The FSD can only be accessed when the 3660 is in the *inactive* state.

FSD: | Frequency Step Data |

Current Pulse Count Register (CPC)

This register is READ ONLY and contains a count of the number of Clock output pulses generated so far by the current step. When CPC = Np and termination on number of pulses is selected, the program step occurs. This register is required so that software can determine the current state. This register is read with a F(0)A(2) command. This is a 24-bit register.

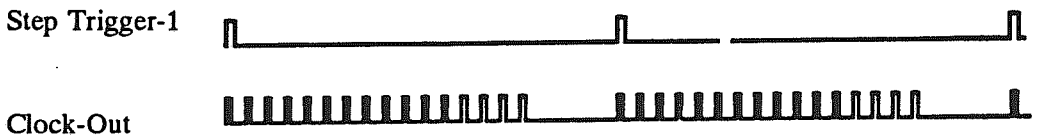
CPC: | Current Pulse Count 0-23 |

3660 PROGRAMMABLE PULSE GENERATOR APPLICATIONS

The following text illustrates several examples of use of the 3660 and how to program it. All relevant frequency parameters should be divided by 10 for the 3660-Z1B option.

Example 1

As a first example, the 3660 will be programmed to generate 500 clock pulses at 5 KHz each time an external trigger is received. The clock will be based on the internal 10 MHz base clock.



The 3660 program required is as follows:

1. Wait for trigger on "Step Trigger-1". This is accomplished by a program step with the "flag" word associated with the step set with DFLG=1 to disable clock output and TS=2 to select External Step Trigger-1. The number of triggers required to terminate the step is set to 1 (Np). The value of Nf does not matter.

2. Generate 500 output pulses at 5 KHz from 10 MHz base clock and recycle. The program step parameters are set as follows:

   a. To generate a 5 KHz clock from the 10 MHz base clock, set Nf = (10MHz)/(5KHz) = 2000

   b. To terminate the step on Np, set TS = 1 in the *flag word.*

   c. To designate that this is the last step in the program list, set EOL = 1 in the *flag word.*

d. To generate 500 pulses, set Np = 500.

Finally, to start the clock you must write a control word to the Control Status Register (CSR). The 3660 always powers up in the *inactive* state. The following status bits must be written:

1. *FPA = 1* must be set to place the 3660 in the *active* mode.

2. *RCM = 1* must be set so the 3660 will "recycle" to the start of the program when the End-of-List (EOL) step completes.

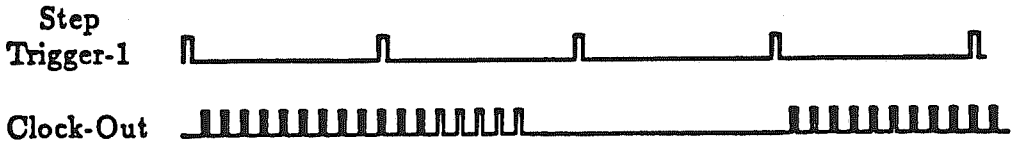
3. *CSEL = 0* must be set to select the 10 MHz internal base clock.

The following FORTRAN program segment illustrates how this application might be set up. It uses the KineticSystems' standard CAMAC library calls and assumes that the program has properly opened the CAMAC device. The parameters C3660 and N3660 refer respectively to the crate and slot numbers where the 3660 is located. Also, in a real application, the user will likely want to check status return (stat) to be sure that each CAMAC I/O operation has been successfully performed.

```
C       The following program segment sets the 3660 up to
C       generate 500 pulses at 5 KHz each time it is triggered.
C
C       Force 3660 into inactive state
        call cam16(chan, C3660, N3660, 0, 16, 0, stat)
C
C       Set the 3660 RAM Address Pointer (RAP) to zero
        call cam16(chan, C3660, N3660, 0, 17, 0, stat)
C
C       Write the 3660 program to RAM
C       Program Step 1
        call cam16(chan, C3660, N3660, 1, 17, 1000, stat)
        call cam16(chan, C3660, N3660, 1, 17, '42'X, stat)
        call cam16(chan, C3660, N3660, 1, 17, 1, stat)
        call cam16(chan, C3660, N3660, 1, 17, 0, stat)
C       Program Step 2
        call cam16(chan, C3660, N3660, 1, 17, 2000, stat)
        call cam16(chan, C3660, N3660, 1, 17, '81'X, stat)
        call cam16(chan, C3660, N3660, 1, 17, 500, stat)
        call cam16(chan, C3660, N3660, 1, 17, 0, stat)
        :
        :
C       Start up the 3660
C
C       Initialize the RAM Address Pointer (RAP) to first step.
        call cam16(chan, C3660, N3660, 0, 17, 0, stat)
C       Place 3660 in Active state FPA = 1, RCM = 1, CSEL = 0
        call cam16(chan, C3660, N3660, 0, 16, 'C0'X, stat)
```

Example 2

In this example we shall assume the parameters are identical to above except that rather than generating a group of clock-out pulses for each trigger input we shall generate a group of clock-out pulses on every 3rd trigger. We shall also increase the sample length to 1000 samples such that we sample for a period that is longer than the trigger interval (see timing diagram below). In this example we shall assume that an external clock source is used and that it is at the desired sampling frequency. In particular the required 3660 frequency division factor Nf = 1.



In this case the program is almost identical to the first case except that Np = 2 in the first step and Np = 1000 in the second step. Note that Np in the first step is the count of triggers received during that step before going to the next step. Also, since we are using an external frequency source of the desired frequency Nf = 1 in the second step and CSEL in the CSR must be set to 2 to select the external clock source.

Below is the program segment to set up and start the 3660:

```
C       The following program segment sets the 3660 up to
C       generate 1000 pulses at the external clock frequency.
C       A clock burst is initiated on the 2nd external trigger
C       following the previous clock burst.
C
C       Force 3660 into inactive state
        call cam16(chan, C3660, N3660, 0, 16, 0, stat)
C
C       Set the 3660 into inactive state
        call cam16(chan, C3660, N3660, 0, 17, 0, stat)
C
C       Write the 3660 program to RAM
```

```
C       Program Step 1
        call cam16(chan, C3660, N3660, 1, 17, 1, stat)
        call cam16(chan, C3660, N3660, 1, 17, '42'X, stat)
        call cam16(chan, C3660, N3660, 1, 17, 2, stat)
        call cam16(chan, C3660, N3660, 1, 17, 0, stat)
C       Program Step 2
        call cam16(chan, C3660, N3660, 1, 17, 1, stat)
        call cam16(chan, C3660, N3660, 1, 17, '81'X, stat)
        call cam16(chan, C3660, N3660, 1, 17, 1000, stat)
        call cam16(chan, C3660, N3660, 1, 17, 0, stat)
        :
        :
C       Start up the 3660
C
C       Initialize the RAM Address Pointer (RAP) to first step.
        call cam16(chan, C3660, N3660, 0, 17, 0, stat)
C       Place 3660 in Active state FPA=1, RCM=1, CSEL=2
        call cam16(chan, C3660, N3660, 0, 16, 'C2'X, stat)
```

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2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com