

Model 3843

1K to 16K-word FIFO Buffer

INSTRUCTION MANUAL

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WARRANTY

SCHEMATIC DRAWING # 12223-C-5788 See Reply Card Following Warranty

JPS(WP)

1K to 16K-word FIFO Buffer

ADVANCE INFORMATION

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(Rev. Apr. 90)

FEATURES

- Asynchronous buffer for up to 16K words
- 24 bits wide
- Write/Read in enhanced mode
- 4-bit LAM and LAM Mask registers
- TTL-level front-panel input and output ports

APPLICATIONS

- Peripheral buffering
- Data-rate smoothing
- Asynchronous/synchronous buffering
- Long-term data retention
- Data buffering

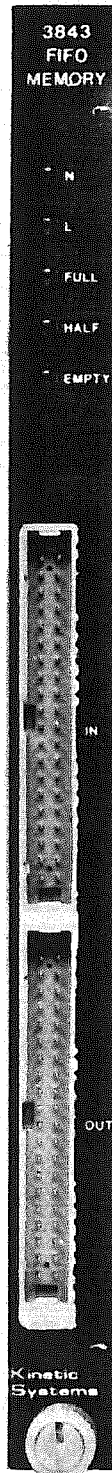
GENERAL DESCRIPTION

The Model 3843 is a single-width module containing a First-In-First-Out memory stack organized as 1K, 2K, 4K, 8K, or 16K 24-bit words. The memory has two ports for both input and output. It may be read and written from the Dataway or under control of external signals. External connections are made by way of two 40-pin, front-panel connectors. All external signals are single-ended TTL, except for strobes (Write, Read, and Clear).

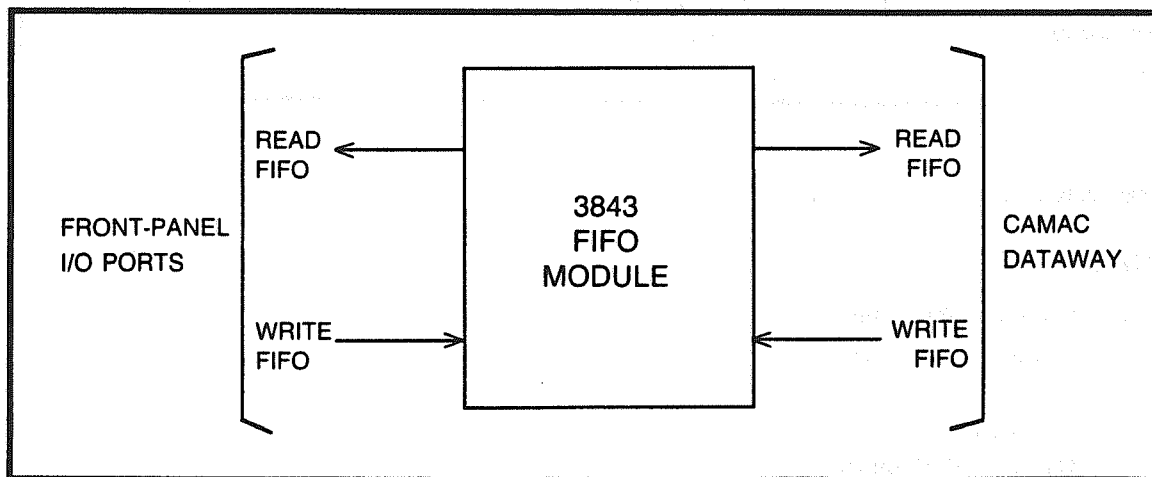
Reading and writing operations are independent. This module is useful in applications where input or output data operations require a different clock rate from the data transfer rate in the CAMAC system. For example, it is possible to load the memory externally and read it from the Dataway or, alternatively, to load the memory from the Dataway and dump it externally. An input which sets a LAM source and a signal indicating the state of the LAM are provided on the external connectors allowing communication of "ready" and "done" status information.

A 4-bit LAM register is provided, which for Dataway operations occupies Bits 13-16. Memory-full and Memory-empty signals set Bits 15 and 13, respectively. A LAM source is provided which sets Bit 14 when the memory is half full. Bit 16 is the external LAM. The LAM register can be cleared and selectively cleared, and Bit 16 can be selectively set.

In addition to the 4-bit LAM status register, a LAM mask register is provided which can be selectively set and selectively cleared as well as written and cleared. A 5-bit status register provides information on the current stack size in the memory.



READ/WRITE DATA PATHS

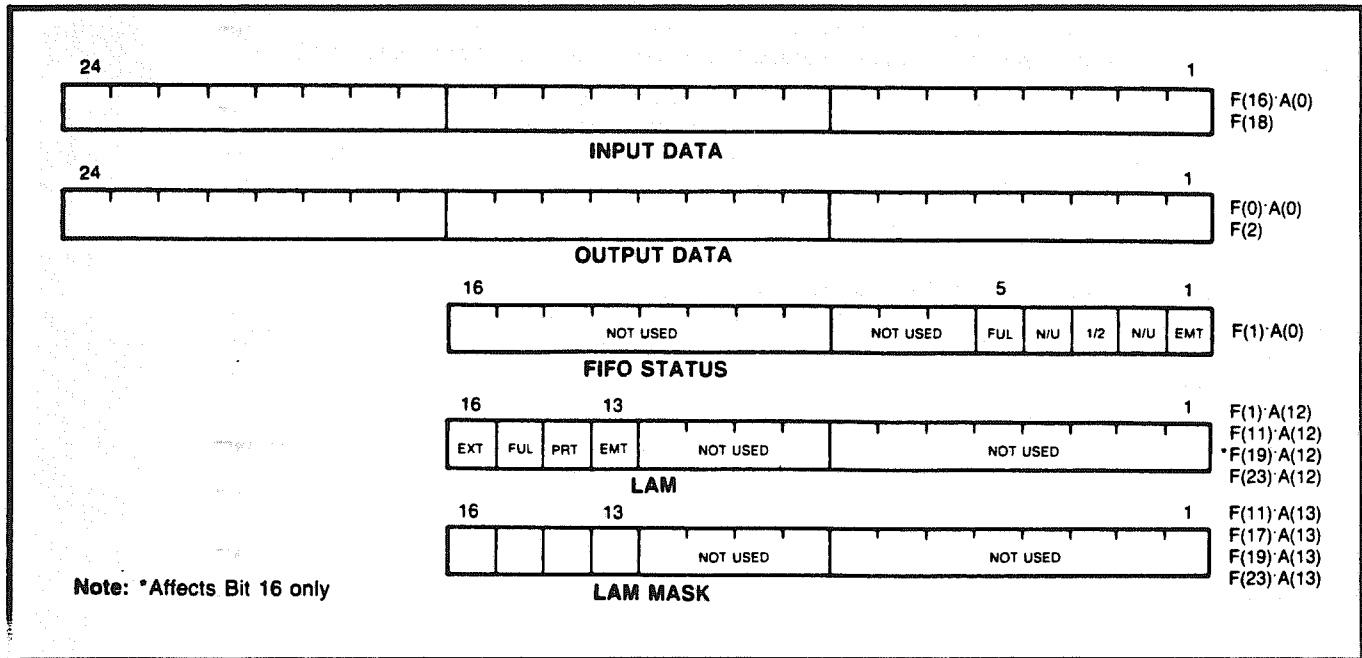


FUNCTION CODES

Command	Q	Action	
F(0)·A(0)	RD1	EMPTY	Reads FIFO memory output word.
F(1)·A(0)	RD2	1	Reads FIFO Status register.
F(1)·A(12)	RD2	1	Reads LAM status.
F(2)·A(i)	RC1	EMPTY	Reads FIFO memory output word.
F(8)·A(15)	TLM	LR	Tests whether a LAM request is present.
F(9)·A(0)	CL1	0	Clears FIFO memory.
F(11)·A(12)	CL2	0	Clears LAM Status register.
F(11)·A(13)	CL2	0	Clears LAM Mask register.
F(16)·A(0)	WT1	FULL	Writes FIFO memory.
F(17)·A(13)	WT2	1	Writes LAM Mask register.
F(18)·A(i)	SS1	FULL	Writes FIFO memory.
F(19)·A(12)	SS2	1	Selectively sets LAM Status register (operates on Bit 16 only).
F(19)·A(13)	SS2	1	Selectively sets LAM Mask register.
F(23)·A(12)	SC2	1	Selectively clears LAM Status register.
F(23)·A(13)	SC2	1	Selectively clears LAM Mask register.
Z	CZ	0	Clears LAM Status and LAM Mask registers and FIFO memory.

Note: X = 1 for all valid addressed commands.

REGISTERS



POWER REQUIREMENTS:

+ 6 volts — 800 mA

ORDERING INFORMATION

Weight: .70 kg. (1 lb. 8 oz.)

Model 3843-J1A	—	1K-word FIFO Buffer
Model 3843-J2A	—	2K-word FIFO Buffer
Model 3843-J3A	—	4K-word FIFO Buffer
Model 3843-J4A	—	8K-word FIFO Buffer
Model 3843-J5A	—	16K-word FIFO Buffer
Accessories	—	None

LOADING AND DUMPING THE MEMORY

The FIFO memory can be written or read from the Dataway or externally via two front panel connectors, (one for writes and one for reads). The front panel connectors have single ended high true data and low true status signals, and low true differential control strobes.

LAM MASK REGISTER

The 3843 contains a four (4) bit internal register used for masking CAMAC LAMs. This register is write only.

Bit Description

EXT	FULL	HALF	EMP
-----	------	------	-----

<u>Bit</u>	<u>Label</u>	<u>Description</u>
16	EXTERNAL	When set, strap selection allows either an external source or not empty to generate a LAM request.
15	FULL	When set, allows the FIFO full condition to generate a LAM request.
14	HALF-FULL	When set, allows the 3843 to set a LAM request when the FIFO is at least half-full. Note that this bit does not apply for the 3843-J5A, 16-K Kword FIFO buffer option.
13	EMPTY	When set, allows the FIFO empty condition to generate a LAM request.

LAM STATUS REGISTER

The LAM request register is a four (4) bit read only register (with the exception of bit sixteen (16) which shows LAMs set in the 3843.

Bit Description

EXT	FULL	HALF	EMP
-----	------	------	-----

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<u>Bit</u>	<u>Label</u>	<u>Description</u>
16	EXTERNAL	Strap selectable to be set when the 3843 receives an external pulse or the FIFO is not empty.
15	FULL	Set when the FIFO is full.
14	HALF	Set when the FIFO is at least half-full. Note that this bit does not apply for the 3843-J5A, 16-K Kword FIFO buffer option.
13	EMP	Set when the FIFO is empty.

STATUS REGISTER

The 3843 contains a three (3) bit read only register which shows the FIFO status.

Bit Description

FULL	N/U	HALF	N/U	EMP
------	-----	------	-----	-----

<u>Bit</u>	<u>Label</u>	<u>Description</u>
5	FULL	Indicates the FIFO is full.
4	NOT USED	
3	HALF-FULL	Indicates the FIFO is at least half-full. Note that this bit does not apply for the 3843-J5A, 16-K Kword FIFO buffer option.
2	NOT USED	
1	EMPTY	Indicates there is not data in the FIFO.

FRONT PANEL

LED INDICATORS

N	Indicates that the module is being addressed.
L	Indicates that a LAM is present.
FULL	Indicates that the FIFO is full.

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HALF	Indicates that the FIFO is at least half-full. Note that this bit does not apply for the 3843-J5A, 16-K Kword FIFO buffer option.
EMPTY	Indicates that the FIFO is empty.

INPUT/OUTPUT CONNECTORS

Input (40-position right angle header)

<u>SIGNAL</u>	<u>PIN</u>
DATA BIT 1	1
DATA BIT 2	2
" "	
" "	
" "	
" "	
DATA BIT 24	24
FIFO FULL	26
FIFO ½ FULL	27
SET LAM	32
LAM OUT	33
NOT USED	37, 38
GROUND	25, 28, 31, 34, 39, 40
WRITE	29+, 30- DIFFERENTIAL
CLEAR FIFO	35+, 36- DIFFERENTIAL

Output (40-position right angle header)

<u>SIGNAL</u>	<u>PIN</u>
DATA BIT 1	1
DATA BIT 2	2
" "	
" "	
" "	
" "	
DATA BIT 24	24
FIFO ½ FULL	26
FIFO EMPTY	27
SET LAM	32
LAM OUT	33
LAM SOURCE	34
NOT USED	37, 38
GROUND	25, 28, 31, 35, 36, 39, 40
READ	29+, 30- DIFFERENTIAL

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NOTES:

1. Data signals are high true - all other signals are low true.
2. All signals are single ended except Write, Read and Clear.
3. Read and Write pulses are 300nS minimum.
4. Clear is 100nS minimum.
5. For FIFO Writes, data must be valid during Write pulse.
6. For FIFO Reads, Data is valid during Read pulse.
7. Cable length up to 25 feet.

WARRANTY

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1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com