Model 3924-F1A

LAM Encoder for Serial System

INSTRUCTION MANUAL

May, 1987

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KineticSystems Corporation

Standardized Data Acquisition and Control Systems **3924**

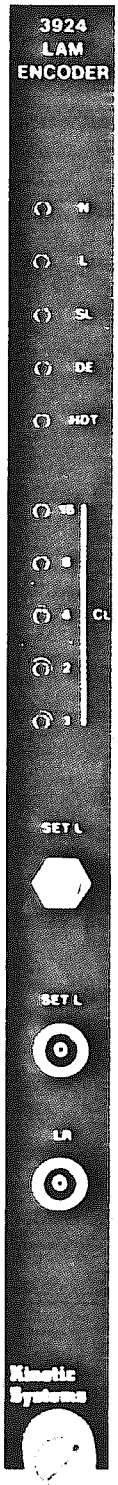
LAM Encoder for Serial System

FEATURES

- **LAM mask can be selectively set or cleared**
- **Highest priority LAM encoded into 5-bit number**
- **Provision for the orderly handling of overlapping LAMs**
- **Internal LAM request set by external signal, switch or command**
- **Based upon ESONE serial driver subgroup recommendations**

APPLICATIONS

- **LAM handling in a serial system with Type L-2 SCCs**
- **Systems where "simple patching" of LAMs is not sufficient**
- **Systems with auxiliary crate controllers where masking off LAMs is important**



GENERAL DESCRIPTION

The Model 3924 is a single-width CAMAC module providing the means to encode the 24 Look-At-Me (LAM) signals into a 5-bit number suitable for use by a Type L-2 serial crate controller (SCC), such as KSC Model 3952 in generating a Demand message. This module has a rear-panel connector which connects via a jumper cable to the Serial Graded LAM (SGL) connector on the SCC. The LAMs are staticized and then masked to give a set of selected LAMs. The selected LAMs are then priority-encoded to give the 5-bit SGL number which is passed to the SCC and incorporated into the Demand message. The 3924 includes the logic for synchronizing its operation with the demand generation sequence in the SCC.

USE WITH AUXILIARY CRATE CONTROLLER

Auxiliary crate controllers (ACC) such as the Model 3920-Series, 3988, or 3989 can operate in the same crate as the 3924. These controllers will normally address one or more modules in the crate. If this interaction makes use of LAMs in these modules, it is important that they do not generate Demand messages through the SCC. This can be accomplished by masking these LAMs off in the 3924 LAM Encoder module.

INTERNAL LAM REQUEST

The 3924 has provisions for an internal LAM request. The LAM request is set by a front-panel switch, a signal applied to a front-panel connector, or by command. The front-panel connector receives TTL signal levels. The LAM request is set on either the positive or negative-going edge depending on an internal strap. The receiver has hysteresis and, therefore, will not produce multiple triggers on signals with slow rise times. A 50 ohm termination can be selected by an internal strap.

HUNG DEMAND TIMER FLAG

If a Demand message is sent and the associated LAM is not serviced within a predetermined time (selectable from one millisecond to one second in the 3924), a Hung Demand message is sent with all one's in the SGL field, or 31 (base 10). This causes the HDT flag to be set in the 3924. The further generation of Demand messages (except for additional Hung Demand messages, if not serviced) is prevented until the HDT flag is cleared. This flag is cleared by an F(22)·A(11) command with data equal to 31 (base 10) or by F(25)·A(1).

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FUNCTION CODES

Command		Q	Action
F(1)·A(0)	RD2	1	Reads the selected LAM (5-bit binary number, highest priority present).
F(1)·A(12)	RD2	1	Reads the staticized LAM pattern (24 bits).
F(1)·A(13)	RD2	1	Reads the LAM Mask register (24 bits).
F(1)·A(14)	RD2	1	Reads the selected LAM pattern (24 bits).
F(8)·A(0)	TLM	LR	Tests whether the internal LAM request is present.
F(10)·A(0)	CLM	1	Clears the internal LAM status.
F(11)·A(13)	CL2	1	Clears the LAM Mask register.
F(14)·A(0)	F14	1	Sets the internal LAM status.
F(20)·A(13)	F20	1	Selectively sets the LAM Mask register (uses 5-bit binary number).
F(22)·A(11)	F22	1	Selectively clears LAM Mask register (uses 5-bit binary number). For data less than 31: Selectively clears mask and causes another Demand to be sent if an unmasked LAM is present AND the HDT flag is not set. For data equal to 31: Clears HDT flag; Demand initiated if unmasked LAM is present.
F(22)·A(13)	F22	1	Selectively clears LAM Mask register (uses 5-bit binary number). For data less than 31: Selectively clears mask and disables LAM generation.
F(24)·A(1)	DIS	1	Disables Demand generation.
F(25)·A(1)	XEQ	1	Clears HDT flag; Demand initiated if unmasked LAM is present.
F(26)·A(1)	ENB	1	Enables Demand generation.
Z	CZ	0	Clears LAM Mask register, HDT flag, and internal LAM status, disables Demand generation.

Notes: All commands contain N. To provide for future allocation by the CAMAC specifications, N = N (this slot) + N(28) + N(30).
X = 1 for all valid addressed commands.

POWER REQUIREMENTS

+6 volts — 1000 mA

ORDERING INFORMATION

Weight: .70 kg. (1 lb. 8 oz.)

Model 3924-F1A — LAM Encoder for Serial System

Accessories — Models 5910-Z1A, 5942-Z1A Mating Connectors
Model 5860-B000 SGL Cable for 3952 with 3296
Model 5860-R000 SGL Cable for 3952

MASK REGISTER

The staticized L's are gated by a 24-bit wide LAM Mask Register to produce selected L's. A unique feature of the LAM Mask Register is that it is selectively set and selectively cleared, one bit at a time, by a five-bit binary number on the Dataway (W5-W1). For example, Bit 3 in the register is set by the selective set command with write lines W2 and W1 true. Since LAM numbers in binary form are sent to the serial driver as part of the demand message, the use of the same binary numbers for selectively setting and clearing the mask results in a simplified software handler.

Two selective clear commands are provided. The operations of each command are described here:

1) F(22).A(11) with data less than 31 (base 10): The appropriate mask bit is cleared by the five-bit binary number on the Write lines. Also, another demand message is initiated if an unmasked LAM is present AND the HDT Flag is not set (see description of the Hung Demand Timer Flag). This has the advantage of quick response with one CAMAC command from the SD and the disadvantage that interrupt service routine nesting could occur for one crate.

2) F(22).A(13) with data less than 31: The appropriate mask bit is cleared by the five-bit binary number and further demands are disabled. After the demand handler software has serviced the LAM, an F(26).A(1) command causes demands to be again enabled. If an unmasked LAM is present, a demand message will be initiated. This has the advantage that interrupt service routine nesting cannot occur for one crate and the disadvantage that two CAMAC commands are required.

3) F(22).A(11) with data equal to 31 or F(25).A(1): The HDT flag is cleared and a demand message is initiated if there is an unmasked LAM pending. For additional details, see Hung Demand Timer Flag.

Only bits W5-W1 are used in this register; all others are ignored. The mask register can be read (24 bits) and the entire register cleared by command. The selected LAM's can also be read by command.

STATICIZE REGISTER

Since many modules with L signals pending remove the assertion of these L's when addressed (and older modules during Dataway BUSY), it is necessary to staticize the L signals. The 3924 has a 24-bit wide staticize register which latches the state of the L signals from the leading edge of the Dataway BUSY signal until approximately 200ns after the trailing edge. The trailing edge delay provides protection during the propagation delay of L signals through the module and the serial crate controller. The staticized L's can be read via Dataway command.

LAM ENCODER

The selected LAM's are priority encoded to produce a five-bit number. This number represents the highest priority LAM pending and corresponds to the slot number for the L1-L23. A binary number ZERO corresponds to L24. The priority is arranged with L24 having the highest priority, followed by L1-L23 in that order.

The five-bit number is staticized during Demand Busy so that it cannot change while a demand message is being sent. Note that in order to send a demand message demands must be enabled in the 3924 and the SCC.

HUNG DEMAND TIMER

A hung demand timer is included in the Model 3924. This timer can be strapped for timing periods from 1 millisecond to 10 seconds (five timeout settings), or it can be disabled (no hung demands sent). With the provision of this "external" timer, the hung demand timer in the Type L SCC is not operable. Also the Demand Enable bit in the SCC status register has no effect. Demands are now enabled in the 3924.

FRONT PANEL

LED Indicators

N	Flashes when the module is addressed.
L	On when the 3924's internal LAM request is true.
SL	On when a selected L (unmasked and enabled) is present.
DE	On when demands are enabled.
HDT	On when the Hung Demand Timer flag is set.
CL	Indicates the current highest priority selected binary-coded L (CL16, 8, 4, 2, 1)

Switches

SET L	Sets the internal LAM request (Momentary pushbutton).

Connectors

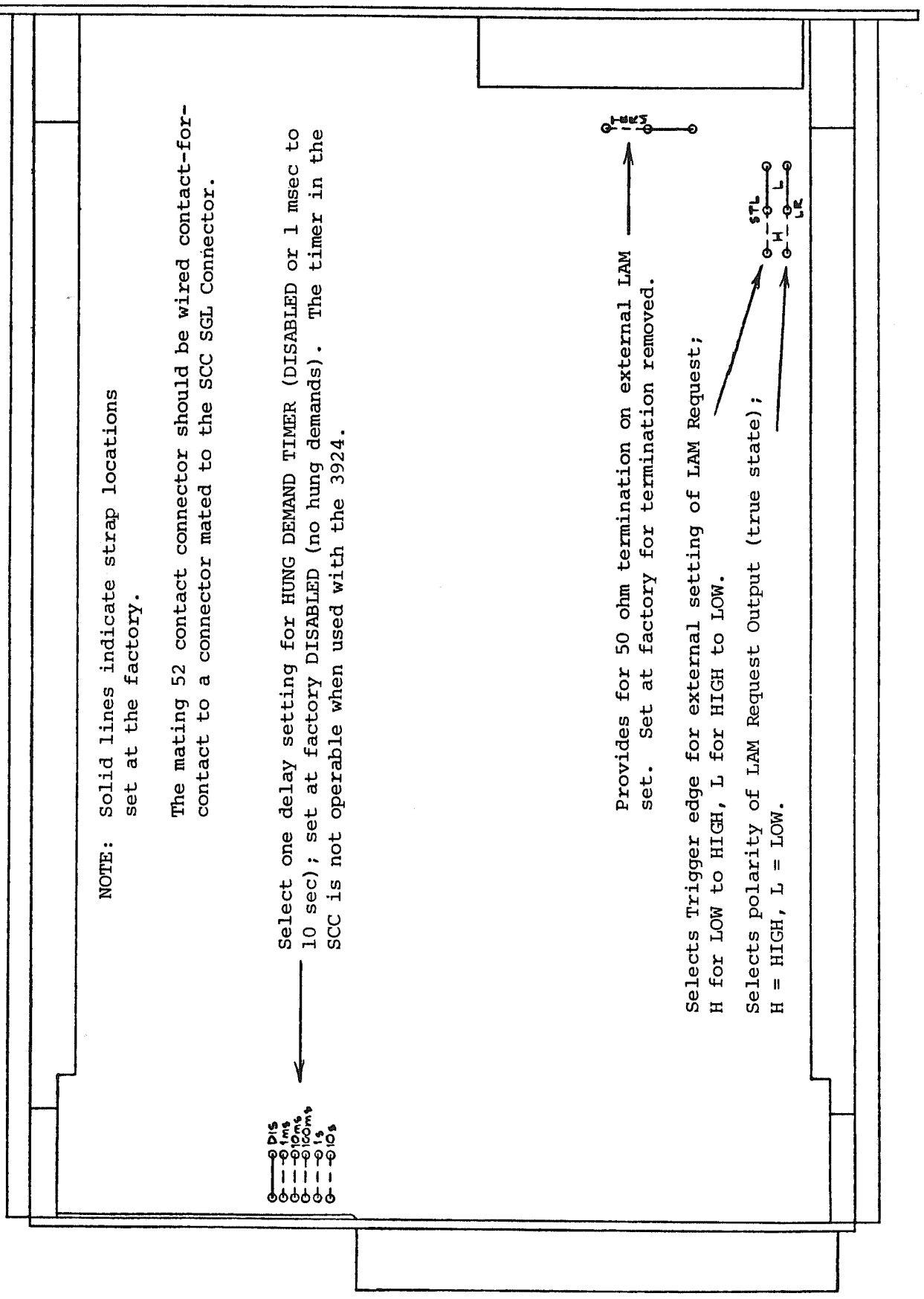
SET L	Sets the internal LAM request (LEMO, mating connector F00250).
LR	Monitors the internal LAM request (LEMO, mating connector F00250).

REAR PANEL

SGL	Connects to the SGL connector of the serial crate controller. It is a Cannon 2DB52P (mating connector 2DB52S).

SGL–ENCODER CONNECTOR

Contact	Signal	Contact	Signal
1	Demand Busy	2	L1
3	SGLE1	4	L2
5	SGLE2	6	L3
7	SGLE3	8	L4
9	SGLE4	10	L5
11	SGLE5	12	L6
13	External Repeat	14	L7
15	———	16	L8
17	———	18	L9
19		20	L10
21	Demand Message Initiate	22	L11
23		24	L12
25	Selected L's present	26	L13
27	———	28	L14
29		30	L15
31		32	L16
33	———	34	L17
35	———	36	L18
37	———	38	L19
39	———	40	L20
41		42	L21
43		44	L22
45		46	L23
47		48	L24
49		50	
51		52	Gnd



Model 3924 Strap Options