Model 3927-Z1A

Parallel I/O Crate Controller

INSTRUCTION MANUAL

September, 1988

KineticSystems Corporation

Standardized Data Acquisition and Control Systems **3927**

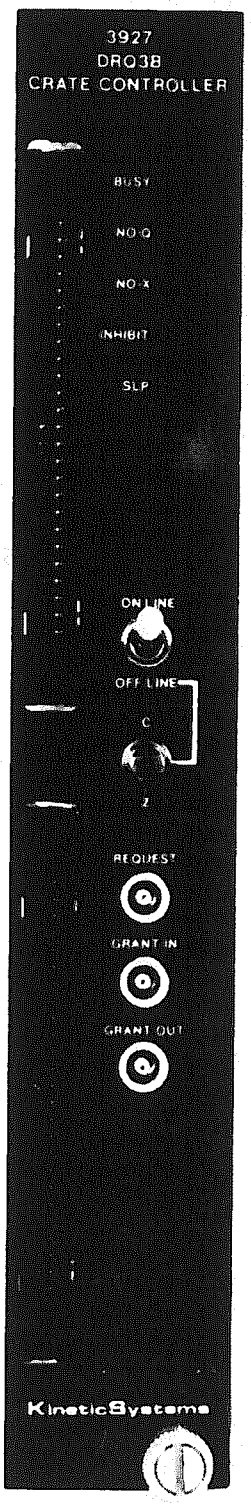
Parallel I/O Crate Controller

FEATURES

- **Forms a dedicated Q-bus® interface with a DIGITAL DRQ3B module**
- **Supports CAMAC block data transfer rates to two megabytes per second**
- **Includes a 24-bit LAM mask**
- **Field-selectable as a main or auxiliary crate controller**

APPLICATIONS

- **General-purpose acquisition and control**
- **Laboratory automation**
- **Industrial process control**
- **Distributed acquisition and control**



GENERAL DESCRIPTION

The Model 3927 is a double-width crate controller which, when connected to Digital Equipment Corporation's DRQ3B parallel I/O module, forms an interface between the Q-bus and the CAMAC Dataway. Data and control information are passed between the DRQ3B and the 3927's internal registers via the two-wire handshake signals on the DRQ3B's input and output ports. Register selection within the 3927 is accomplished via the six Function Out lines set through the DRQ3B's Function Register Zero. CAMAC Read and Write data is double-buffered on the 3927 to improve Dataway cycle execution rates, while taking advantage of the DRQ3B's one megahertz transfer capabilities. Thus, data transfer rates to two megabytes per second are supported for 16-bit transfers.

The 3927 contains a 1024 by 16-bit, FIFO-type memory for storing control information and CAMAC NAF parameters. This control structure permits implementation of block data transfers based on the CAMAC Q response. Q-Scan, Q-Stop, and Q-Repeat transfer types are supported. Once initiated, data transfers occur as directed by information stored in the FIFO, until either the end-of-command bit is encountered or an exception occurs within the CAMAC crate (ie., X = 0, N 23, etc.). Status is returned in a four-word data block sent to the DRQ3B at the conclusion of all operational sequences.

A 24-bit LAM mask simplifies the host software. A "Selected LAM Present" condition is reported to the host through the DRQ3B's External Interrupt input. Reading the LAM register determines the source of the LAM request.

This module is configured at the factory as a main crate controller. It can be changed in the field to function as an auxiliary crate controller. A 40-contact, rear-panel connector provides interconnection to the Auxiliary Controller Bus.

INTERNAL FUNCTION CODES (N = 30)

Command		Q	Action
F(1)·A(0)	RD1	1	Reads the Status register.
F(1)·A(12)	RD1	1	Reads the LAM pattern.
F(1)·A(13)	RD1	1	Reads the LAM mask.
F(17)·A(0)	WT2	1	Writes the Status register.
F(17)·A(13)	WT2	1	Writes the LAM mask.
Note: X = 1 for all valid addressed commands.			

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OPERATION

The flow of data and command information between the DRQ3B and the 3927 is controlled by manipulating the six general-purpose function bits in the DRQ3B's Function Register Zero. Since there are no strobe signals associated with these bits, the MSB (Bit 5) of this field is used for that purpose. The remaining five-bit field has the following meaning:

Bit Position 4 3 2 1 0	Description
0 0 0 0 0	LOAD COMMAND FIFO. Data from the DRQ3B's Output port are loaded into the 3927's command FIFO memory.
0 0 0 0 1	EXECUTE LIST. Initiates execution of commands previously loaded into the 3927's command FIFO. Data for CAMAC operations is taken from or sent to the DRQ3B's Output or Input ports based on the CAMAC function code to be performed. List execution begins from the beginning of the FIFO.
0 0 0 1 0	CONTINUE FROM HALT. Reinitiates list execution from current location in the command FIFO. This function can be useful when debugging the list of commands to be executed.
0 0 0 1 1 through 1 1 1 1 0	RESERVED FOR FUTURE USE. Not implemented at this time. An attempt to use one of these combinations will result in an operational error in the 3927 and will cause an End-of-Process interrupt to be sent to the DRQ3B.
1 1 1 1 1	RESET DEVICE. Executing this function causes the 3927 to stop executing the current command list. It clears the command FIFO and causes an End-of-Process interrupt to be sent to the DRQ3B.

Proper use of these command bits requires that the five-bit pattern be established in the DRQ3B's Function Register Zero, and then that the MSB (Bit 5) be toggled ON and then OFF. It is the assertion of this bit that strobes the other five function bits into the 3927.

ORDERING INFORMATION

Model 3927-Z1A — Parallel I/O Crate Controller

Accessories — Model 5700-180 DRQ3B-M I/O module
Model 5700-181 DRQ3B-SF I/O Module
Model 5700-182 CK-DRQ3B-KA Cabinet Kit for BA23 System Box
Model 5700-183 CK-DRQ3B-KB Cabinet Kit for BA123 System Box
Model 5700-184 CK-DRQ3B-KF Cabinet Kit for H9642 Cabinet
Model 5849-Axyz Series Cable Assembly (two required)