Model 3982

List Sequencing Crate Controller

INSTRUCTION MANUAL

January, 1990

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List Sequencing Crate Controller

Adds I/O list capability to the Model 3952 L-2 SCC

3982

Features

- **Autonomous auxiliary crate controller**
- **8192 word (16-bit) NAF memory**
- **1K, 2K or 4K 24-bit CAMAC data memories**
- **External event, LAM-synchronized or timer-initiated execution of NAF list**
- **Programmable execution rate**
- **Front-bus for FIFO readout of Read data**
- **External clock rate input**

Typical Applications

- **High-speed data acquisition**
- **Event-triggered data acquisition**
- **Mixed NAF block transfers**
- **Distributed control in remote crates**

General Description *(Product specifications and descriptions subject to change without notice.)*

The 3982 is a single-width CAMAC module that functions as an autonomous auxiliary controller within a CAMAC crate. Connection to the crate's N (Station Number) and L (Look-at-Me) lines is made through the Auxiliary Controller Bus (ACB) via a main crate controller such as the 3952, 3968, 3988, or 3989. Up to 8192 unique commands may be executed from a preloaded NAF list. This list is loaded in a Random Access Memory (RAM) from the host computer prior to execution. Commands to be executed may also be optionally drawn from a preprogrammed Programmable Read Only Memory (PROM) mounted in place of the RAM components.

Data associated with commands in the NAF list is stored in one of two 24-bit FIFO memories. Module options determine whether this memory is 1024, 2048, or 4096 words deep. For CAMAC Write commands, data is preloaded into one of the FIFOs before list execution begins. Data from CAMAC Read commands is stored in the other FIFO for subsequent readout by the host computer. The CAMAC Read data may also be read out over the Front-bus. The Front-bus is a 50-position front-panel connector that allows the CAMAC Read data FIFO to be read by an external device. RS-485 balanced signaling is used to maintain signal integrity. Optionally, only one FIFO may be used for data storage. In this mode, data received during CAMAC Read commands is used as Write data for subsequent CAMAC Write commands. This option allows the 3982 to read data from one CAMAC module and write that data to another. For CAMAC Control commands no storage space is required in either FIFO.

Once the List Sequencing mode is enabled, list execution can be triggered by CAMAC command, by the receipt of a front-panel TTL level logic signal (200 nanosecond minimum pulse width), or by the assertion of a prestrapped LAM signal on the CAMAC Dataway. A register on the module allows the user to program the rate at which Dataway cycles occur. This register provides for nominal execution rates ranging from five kilohertz (a Dataway cycle every 200 microseconds) to nearly one megahertz (a Dataway cycle every 1.1 microseconds) in 1-2-5-10 progression. Optionally, the list execution rate may also be controlled by an external clock input. A bit in the command field provides for the immediate reissuance of a command if that command results in a NO-Q condition. In this mode of operation, no data is strobed into or out of the data FIFOs for the NO-Q cycle. Execution of commands in the list continues in this manner until the "End-of-List" indicator is encountered in the RAM.

List execution begins again...from the beginning of the NAF list...on receipt of a new trigger signal or on the expiration of a Sequence Repeat timer, if enabled. This Dataway-programmable timer allows the entire NAF sequence to be repeated at rates ranging from two hertz to 500 hertz. Two straps on the module establish the data storage format for repeated operations. One strap is used to enable/disable the "retransmission" of CAMAC Write data stored in the Write data FIFO to accomplish a repetitive output data pattern. A second strap is used to enable/disable the clearing of the Read data FIFO so that a list of only "currently available data" can be maintained.

Certain events cause a cessation of list execution. These include receiving a NO-X response to a Dataway cycle, attempting a CAMAC Write operation while the Write data FIFO is empty, attempting a Read operation while the Read data FIFO is full, and the expiration of the Sequence Repeat timer while the module is still in the list execution process. Such "Exception" reporting is available through the module's LAM structure, as is the status of the FIFO Full/Empty and Half-full/Half-empty flags, a List Completion indicator, and an External LAM Source indicator.

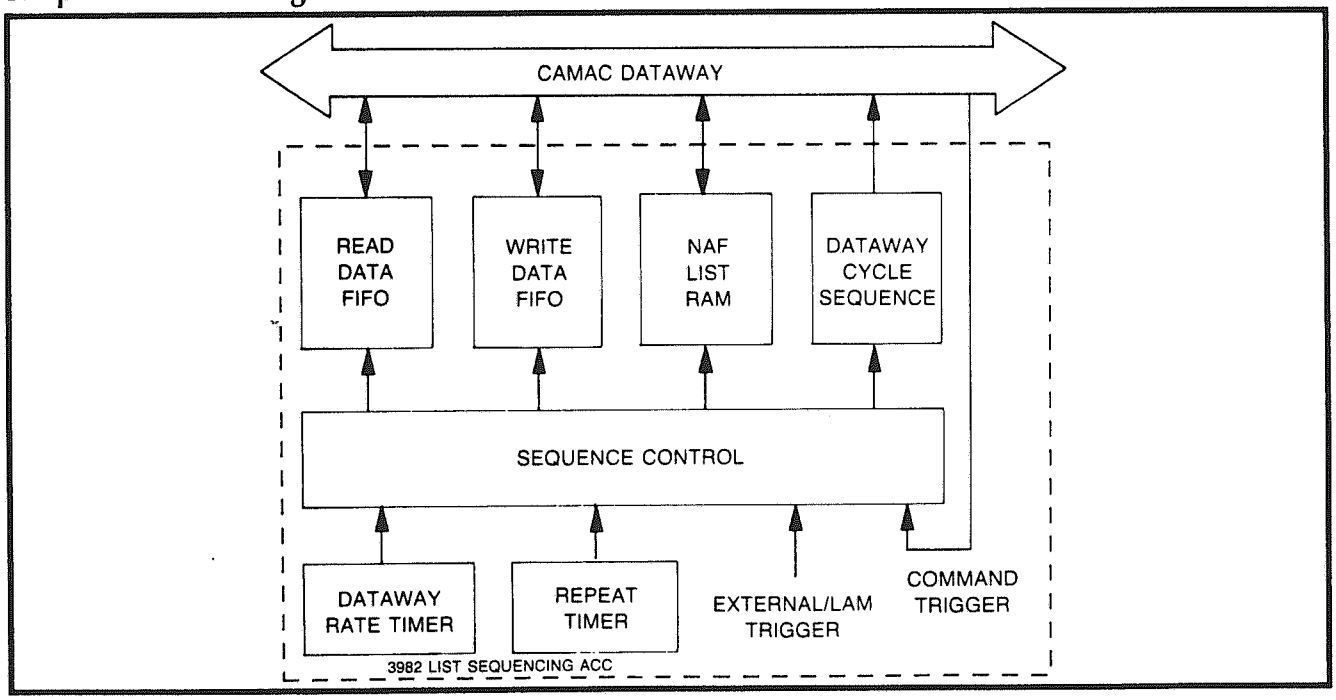
3982 *(continued)*

Function Codes

Command		Q	Action
F(0)·A(0)	RD1	$\overline{\text{EMPTY}}$	Reads the Data FIFO memory.
F(0)·A(1)	RD1	$\overline{\text{XEQ}}$	Reads the NAF storage memory, increments the Memory Address at S2.
F(0)·A(2)	RD1	$\overline{\text{XEQ}}$	Reads the NAF Memory Address register.
F(1)·A(0)	RD2	1	Reads the Status register.
F(1)·A(12)	RD2	1	Reads the LAM Status register.
F(1)·A(14)	RD2	1	Reads the LAM Request register.
F(8)·A(15)	TLM	LR	Tests for the presence of a LAM Request.
F(9)·A(0)	CL1	$\overline{\text{XEQ}}$	Initializes the Data FIFO pointers.
F(10)·A(0)	CLM	1	Clears LAM Trigger LAM source.
F(16)·A(0)	WT1	$\overline{\text{FULL}}$	Writes the Data FIFO memory.
F(16)·A(1)	WT1	$\overline{\text{XEQ}}$	Writes the NAF storage memory, increments the Memory Address at S2.
F(16)·A(2)	WT1	$\overline{\text{XEQ}}$	Writes the NAF Memory Address register.
F(17)·A(0)	WT2	$\overline{\text{XEQ}}$	Writes the Timing Control register.
F(17)·A(13)	WT2	$\overline{\text{XEQ}}$	Writes the LAM Mask register.
F(23)·A(12)	SC2	1	Selectively clears the LAM Status signals.
F(24)·A(0)	DIS	1	Disables execution of the NAF list, aborts the operation of a currently executing NAF list.
F(25)·A(0)	XEQ	XEQ	If enabled, initiates execution of the NAF list from the beginning of the list.
F(26)·A(0)	ENB	$\overline{\text{XEQ}}$	Enables execution of the NAF list.

Notes: 1. X = 1 for all valid addressed commands.
2. $\overline{\text{EMPTY}}$ = Data FIFO not empty; $\overline{\text{XEQ}}$ = Module is not enabled for list execution; LR = LAM Request; $\overline{\text{FULL}}$ = Data FIFO not full; XEQ = Module enabled for list execution.

Simplified Block Diagram



Ordering Information

Model 3982-Z1B Auxiliary Crate Controller, autonomous list sequencing, FP Parallel Bus and 1K R/W buffer
Model 3982-Z2B As above but 2K R/W buffer
Model 3982-Z3B As above but 4K R/W buffer
Model 3982-Z4B As above but 8K R/W buffer
Model 3982-Z5B As above but 16K R/W buffer

Model 3982-001 3982 Upgrade Kit - 1K to 2K R/W buffers
Model 3982-002 3982 Upgrade Kit - 1K/2K to 4K R/W buffers

Related Products

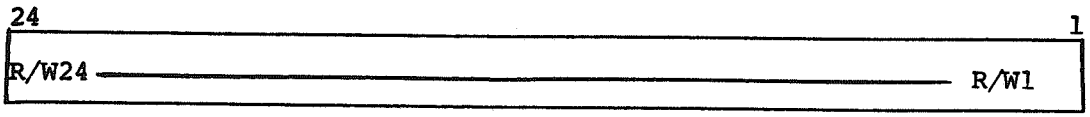
Model 5843-Series Auxiliary Controller Bus Cable Assembly
Model 5857-Axyz/Bxyz LEMO Cable Assembly
Model 5820-Series Front-bus Cable Assembly

Power Requirements

+6 volts: 2800 mA

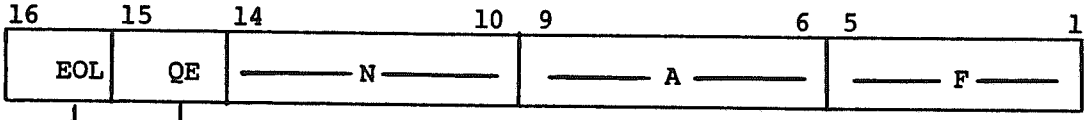
DATA FORMATS

CAMAC READ/WRITE DATA



F(0)·A(0)
F(16)·A(0)

CAMAC COMMAND DATA

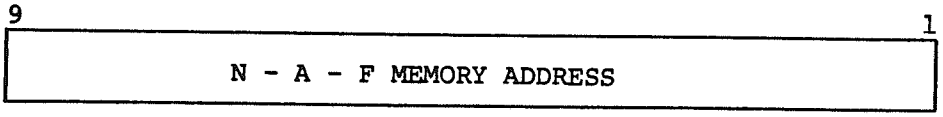


F(0)·A(1)
F(16)·A(1)

Q-Expected: 0 = Ignore Q response for this command
1 = Enable Q-Repeat for this N-A-F combination; i.e., command is repeated until Q = 1 is returned

End-of-List: 0 = This is not the last N-A-F combination in the list; more commands follow
1 = This is the last command in the list; sequencing stops following the successful execution of this N-A-F until a new sequence trigger is received

N-A-F MEMORY ADDRESS



F(0)·A(2)
F(16)·A(2)

STATUS REGISTER

F(1)·A(0)

Sequence Status: 0 = List idle or disabled
1 = List being executed

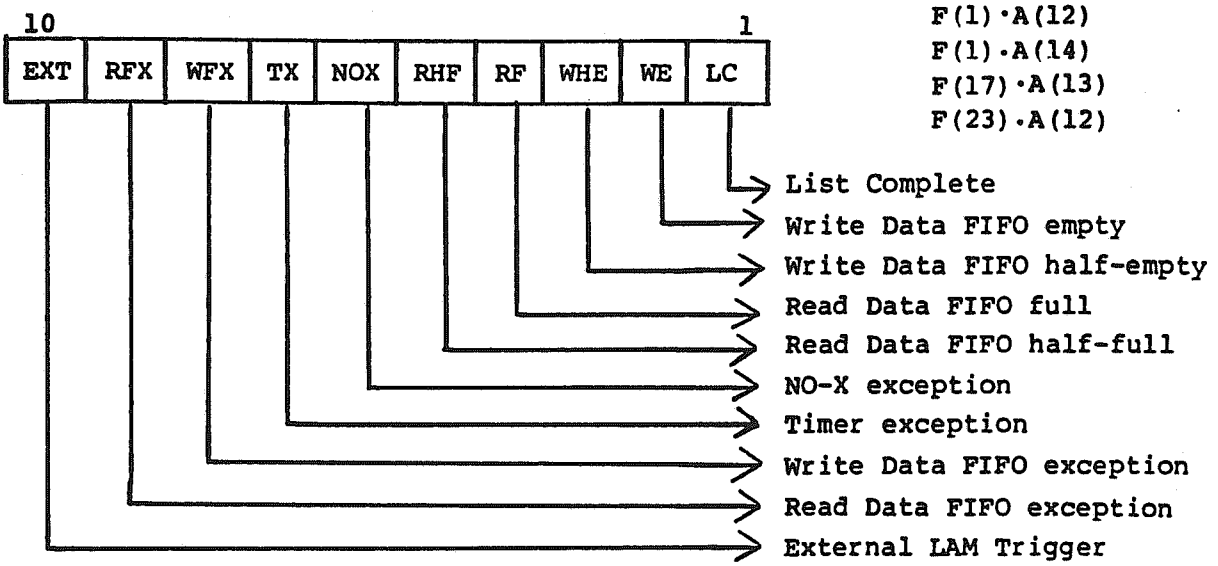
Write Data FIFO empty

Write Data FIFO half-empty

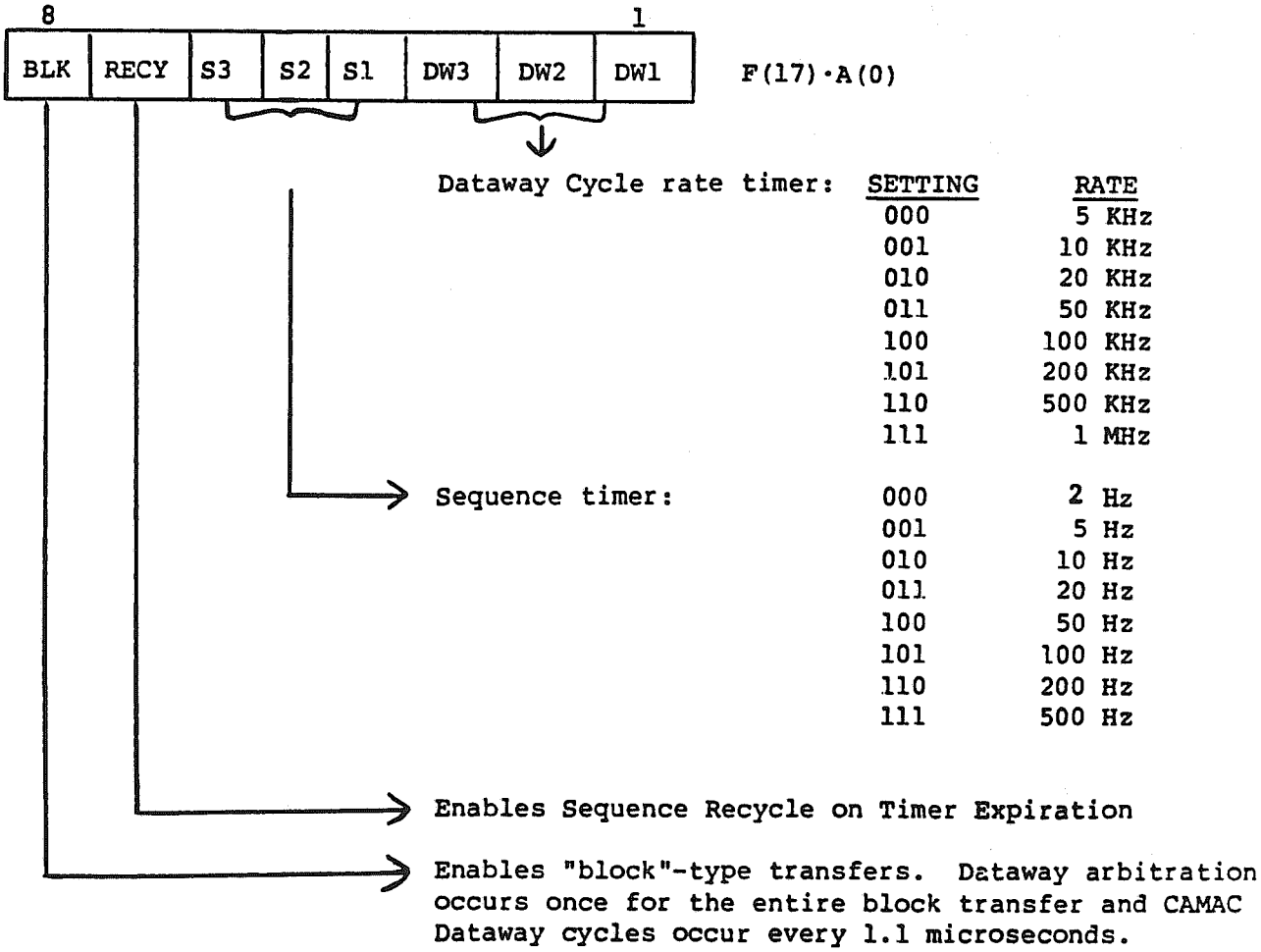
Read Data FIFO full

Read Data FIFO half-full

LAM REGISTERS

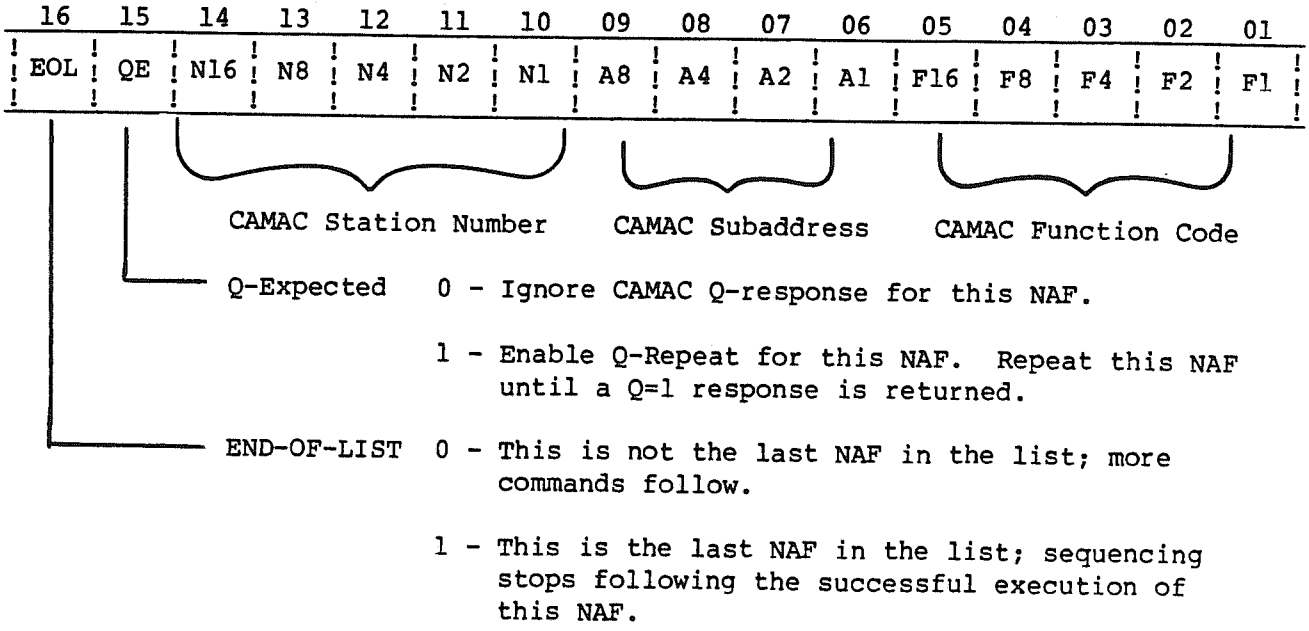


TIMER CONTROL REGISTER



LIST SEQUENCING

The 3982 List Sequencing Auxiliary Crate Controller performs a list of pre-programmed CAMAC commands in a sequential manner. Once list execution begins, CAMAC commands are drawn from a memory device, either RAM or PROM, and executed. In each command word instruction is a CAMAC station number (N), Function Code (F) and Subaddress (A). Along with the CAMAC NAF to be executed are two bits: one for specifying that 'this is the LAST command' and the other for enabling a 'repeat-till-Q = 1'. The format of the instruction is shown below.



Each CAMAC NAF to be executed is loaded into the memory device starting at address location 0. Subsequent NAF's are loaded into the next available memory locations. If the list is to be executed from a PROM, refer to the section entitled 'LIST STORAGE' for further information. To load the RAM with the list, first zero the memory address by executing an F(16)·A(2) with data of zero to the 3982. Next, write the list of command words to the RAM by executing F(16)·A(1) commands to the 3982. The memory address is incremented at strobe S2 time so that it is not necessary to update the address after every F(16)·A(1) command. For data verification, the RAM may be read by an F(0)·A(1) command. As with the F(16)·A(1) command, the F(0)·A(1) command increments the memory address at strobe S2 time.

If CAMAC write commands are loaded into the list, the Write Data FIFO must be loaded with the appropriate CAMAC Write Data. Data is loaded by executing F(16)·A(0) commands to the 3982. Data can be written to the 3982 while a list execution is in progress. CAMAC control commands are dataless operations and do not require 'space' in the Data FIFO's for these operations.

The 3982 is capable of execution DATALESS NAF (Control) commands addressed to itself. (e.g., F(a)A(0) which clears the FIFO pointers).

Once the list has been loaded, the Timer Control Register must be loaded. This register controls the various list sequencing rates. The Dataway Cycle Rate Timer controls the rate at which each CAMAC command within the list is executed. The rates range from 5 KHz to approximately 1 MHz. If the 5 KHz rate was selected, the 3982 executes one CAMAC command every 200 microseconds. The Sequence Repeat Timer controls the rate at which the entire list of commands is repeated. The rates range from 2 Hz to 500 Hz. If the 20 Hz rate was selected, the entire list of commands is executed every 50 milliseconds. To enable the 3982 to repeat the list on the timer expiration, the 'RECYCLE ENABLE' bit, bit 7, of the Timer Control Register must be set. This feature is disabled if this bit is set to zero. If the Sequence Repeat Rate Timer expires while the 3982 is in the process of executing a command from the list, list execution ceases and the 'TRIGGER EXCEPTION' bit in the LAM status register is set. The Trigger Exception is also generated when the 3982 is strapped for an External Trigger, and the trigger occurs while the 3982 is in the process of executing a command from the list. This 'timeout' feature is always enabled, independent of the 'RECYCLE ENABLE' bit. Refer to the section entitled 'TIMER CONTROL REGISTER' for further details.

After the memory device and Timer Control Register have been loaded, the 3982 must be enabled for execution. To enable execution, execute an F(26)·A(0) to the 3982. This command enables list execution but does not initiate it. To disable list execution or to terminate a list being executed, execute an F(24)·A(0) command to the 3982.

Once enabled, the 3982 is ready to receive an initiate command. List execution can be initiated in any of the following ways:

1.) An F(25)·A(0) command executed to the 3982.
2.) If enabled, a trigger signal on the 3982 front panel.
3.) If enabled, a selected LAM.
4.) If enabled, by expiration of the Sequence Repeat Timer.
NOTE: Before the Sequence Repeat Timer may initiate sequencing, a trigger source of either 1, 2, or 3 of the above must occur.

When the list sequence operation is initiated, the NAF memory address is reset to zero. The 3982 reads the first command from the NAF memory, increments the NAF memory pointer, and executes the command. If the command executed returns valid status and data, the 3982 waits for the next expiration of the Dataway Cycle Timer. If, due to a trigger exception condition, the list sequencing ceases, the 3982 will clear the EXECUTE (XEQ) status signal. This XEQ signal is used for conditional Q-responses. To determine the NAF command which causes the exception condition, decrement the memory address by 1 and then read the command.

Model 3982

For this application:

4-channel multiplexer

1.) Channel Selection: F(16)·A(0) with data for desired channel

Analog-to-Digital Converter

1.) Initiate conversion: F(25)·A(0)
2.) Read converted data: F(0) ·A(0) Q=1 when conversion is complete

To setup the 3982:

1.) Execute F(9) ·A(0) command to clear the data FIFO's
2.) Execute F(16)·A(2) command with data equal 0 to reset the RAM address.
3.) Execute F(16)·A(1) commands to load the NAF instruction memory. The following list contains the necessary values to be loaded. All numbers are in octal.

1020		N(1)·F(16)·A(0)	First Conversion
2031		N(2)·F(25)·A(0)	
42000	Q-repeat	N(2)·F(0) ·A(0)	
1020		N(1)·F(16)·A(0)	Second Conversion
2031		N(2)·F(25)·A(0)	
42000	Q-repeat	N(2)·F(0) ·A(0)	
1020		N(1)·F(16)·A(0)	Third Conversion
2031		N(2)·F(25)·A(0)	
42000	Q-repeat	N(2)·F(0) ·A(0)	
1020		N(1)·F(16)·A(0)	Fourth Conversion
2031		N(2)·F(25)·A(0)	
142000	EOL & Q-repeat	N(2)·F(0) ·A(0)	

4.) Load the CAMAC write data FIFO with the data for the multiplexer selection.

0	Channel 0
1	Channel 1
2	Channel 2
3	Channel 3

Assume the 3982 is in the Re-Transmit mode so that this data only has to be loaded once.

5.) Load the Timer Control Register with the appropriate rates. Execute F(17)·A(0) command with octal data of 135.

6.) Execute F(26)·A(0) command to enable execution.

7.) Execute F(25)·A(0) command to start list sequencing.

The 3982 will execute the sequence according to the given application. It is up to the host computer to read the Read Data FIFO, via F(0) A(0) commands before subsequent "re-cycle" operations occur since the Read Data FIFO is reset on the timer expiration.

NOTE: The 3982-Z1A, -Z2A and -Z3A options cannot be readout in the enhanced mode. A special 3982 is available which incorporates the enhanced readout feature. Contact the factory for additional details.

LIST STORAGE

Up to 512 commands may be executed from the pre-loaded NAF list. The list is loaded in a Random Access Memory (RAM) from the host computer prior to execution. Optionally, commands to be executed may be drawn from a pre-programmed Programmable Read Only Memory (PROM) mounted in place of the RAM components.

To load the NAF RAM, first execute an F(16) A(2) to the 3982 to setup the RAM address for instruction loading. (Note that list sequencing always begins at address location 0 when a "start list sequence" command is received.) Then, execute F(16) A(1) commands to the 3982 with the data to be placed in RAM. The memory address is incremented at Strobe S2 time by the 3982. Thus, it is not necessary to load the address register for every write command executed.

The NAF RAM can also b e red by executing an F(0) A(1) command to the 3982. As in the case of writes, the memory address is incremented at Strobe S2 time of the read command. If a PROM is installed in place of the RAM, it may also be read by the same F(0) A(1) command.

PROM INSTALLATION

Two 74S472 512 x 8 PROM's may be used in place of the RAM storage devices. After programming the PROMs with the desired list data, follow the procedure below for installation.

1. Remove the two 2016-1 RAM chips. These chips are mounted in sockets and located at chip locations U42 and U48.

2. Install the 74S472 PROM which is programmed with the low-byte data into chip location U45.

3. Install the 74S472 PROM which is programmed with the high-byte data into chip location U46.

NOTE: Never leave both the PROM and RAM chips installed at the same time.

LIST INSTRUCTION FORMAT

A list instruction consists of one 16-bit word. Within this word is the CAMAC station number (N), function code (F), subaddress (A), a Q-repeat bit and an End-of-List bit. The bit assignments for the instruction word are shown below.

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
EOL	QE	N16	N8	N4	N2	N1	A8	A4	A2	A1	F16	F8	F4	F2	F1

EOL — End-of-List. This bit is set to indicate that this is the last N-A-F combination in the list. If this bit is cleared, it indicates that this is not the last command in the list and more commands are to follow.

QE — Q-Expected. This bit is set to allow the 3982 to repeat this command until a Q-response of 1 is obtained. The list sequencer will not advance to the next instruction until a Q=1 is received. If this bit is cleared the Q-response for this command is ignored.

N16-N1 — Station number 16 through 1. These bits are used to specify the CAMAC Station Number for the Dataway cycle.

A8-A1 — Subaddress 8 through 1. These bits are used to specify the CAMAC subaddress for the Dataway cycle.

F16-F1 — Function Code 16 through 1. These bits are used to specify the CAMAC Function code for the Dataway cycle. The bits F16 and F8 determine what type of CAMAC command to execute.

F16	F8	COMMAND OPERATION
0	0	READ
0	1	CONTROL
1	0	WRITE
1	1	CONTROL

LAM REGISTERS

The 3982 contains the following three LAM registers: LAM Status, LAM Request, and LAM Mask. The LAM Status register is a read-only register which contains information regarding FIFO status and exception conditions. The LAM Request register is a read-only register used to identify the source of a 3982 LAM Request. A LAM Request is issued whenever a LAM Status bit is true, and its corresponding LAM Mask bit is true. Therefore, if all of the LAM Mask bits are false, the 3982 is disabled from asserting a LAM Request.

A selective-clear operation is available for selectively clearing a LAM Source. The selective-clear operation is executed with the write data equal to the LAM Source bit to be cleared.

The following CAMAC commands are used to access the various LAM registers:

F(1) ·A(12) : Read the LAM Status Register
F(1) ·A(14) : Read the LAM Request Register
F(17)·A(13) : Write the LAM Mask Register
F(23)·A(12) : Selectively Clear the LAM Status bits

LAM STATUS REGISTER

10	09	08	07	06	05	04	03	02	01
EXT	RFX	WFX	TX	NOX	RHF	RF	WHE	WE	LC

All bits in the LAM status register are latched. They are cleared by either a CAMAC Initialize (Z) cycle or by the selective clear operation.

EXT — External LAM Trigger. This bit is set when the 3982 receives a 'trigger' pulse via a selected LAM trigger connection.

RFX — Read Data FIFO Exception. This bit is set when the 3982 is instructed to execute a CAMAC read command and the Read Data FIFO is full.

WFX — Write Data FIFO Exception. This bit is set when the 3982 is instructed to execute a CAMAC write operation and the Write Data FIFO is empty.

TX — Trigger Exception. This bit is set when either one of two conditions occur.

1.) When the Sequence Repeat Timer expires while the 3982 is currently executing a list.

2.) When a 'Start List Execution' command is received while the 3982 is currently executing a list.

NOX — NO-X Exception. This bit is set when a CAMAC operation initiated by the 3982 resulted in a CAMAC X-response of zero.

NOTE: On the occurrence of an exception condition (RFX, WFS, TX or NOX) execution of the command list is halted; and the Sequence Status bit in the Status Register is cleared.

RHF — Read Data FIFO Half-Full. This bit is set when the Read Data FIFO becomes half-full due to storage of read data.

RF — Read Data FIFO Full. This bit is set when the Read Data FIFO becomes full due to storage of read data.

WHE — Write Data FIFO Half-Empty. This bit is set when the Write Data FIFO is more than half-full and, due to the 3982 executing a CAMAC write operation, the FIFO becomes half-empty.

WE — Write Data FIFO Empty. This bit is set when the Write Data FIFO becomes empty due to the 3982 executing a CAMAC write operation.

LC — List Complete. This bit is set when the 3982 ceases list execution. This can be due to an error (exception) condition or the 3982 executing the last valid CAMAC operation in the list.

STATUS REGISTER

The Status Register is a read-only register used to obtain information regarding the Write and Read Data FIFO flags, and the Sequence Status. These bits, when read, represent the current status of the indicated signals. These bits are not latched. The Status Register is read by executing a F(1)·A(0) to the 3982.

Status Register

05	04	03	02	01
RHF	RF	WHE	WE	SS

RHF — Read Data FIFO Half-Full. This bit is set when the Read Data FIFO contains at least 513 valid CAMAC read data words. This bit is cleared if the Read Data FIFO contains less than 513 valid CAMAC read data words.

RF — Read Data FIFO Full. This bit is set when the Read Data FIFO is full. The FIFO is full when it contains 1024 valid CAMAC read data words. If the 3982 is instructed to execute a CAMAC read command and the Read Data FIFO is full, a Read Data FIFO exception condition will occur.

WHE — Write Data FIFO Half-Empty. This bit is set when the Write Data FIFO contains less than 513 CAMAC write data words. This bit is cleared if the Write Data FIFO contains at least 513 CAMAC write data words.

WE — Write Data FIFO Empty. This bit is set when the Write Data FIFO is empty. If the 3982 is instructed to execute a CAMAC write command and the Write Data FIFO is empty, a Write Data FIFO exception condition will occur.

SS — Sequence Status. This bit is set while the 3982 is in the process of executing a list sequence operation. This bit is cleared while the list execution is disabled or idle.

After a CAMAC Initialize (Z) operation, the following bit pattern is found in the Status Register.

05	04	03	02	01
0	0	1	1	0

TIMER CONTROL REGISTER

The Timer Control Register is a write-only register which is used to select the Dataway Cycle Timer Rate, and the Sequence Repeat Timer Rate. This register also contains a bit for enabling or disabling the recycle feature, and a bit for selecting the 'block' mode of operation. The Timer Control Register is accessed by executing an F(17)·A(0) command. The bit assignments for the register are shown below. After a CAMAC initialize (Z) operation, all bits in the Timer Control Register are cleared.

Timer Control Register

08	07	06	05	04	03	02	01
BLK ENA	RCY ENA	S3	S2	S1	DW3	DW2	DW1

DATAWAY CYCLE RATE TIMER				SEQUENCE REPEAT RATE TIMER			
DW3	DW2	DW1	RATE	S3	S2	S1	RATE
0	0	0	5 Khz	0	0	0	2 hz
0	0	1	10 Khz	0	0	1	5 hz
0	1	0	20 Khz	0	1	0	10 hz
0	1	1	50 Khz	0	1	1	20 hz
1	0	0	100 Khz	1	0	0	50 hz
1	0	1	200 Khz	1	0	1	100 hz
1	1	0	500 Khz	1	1	0	200 hz
1	1	1	1 Mhz	1	1	1	500 hz

BLK ENA

Block Enable. This bit is set to enable the 'block' mode of operation or cleared to disable 'block' mode. To enable this mode the Dataway Cycle Rate Timer must be set to its fastest cycle rate, 1MHz. With the 'BLK ENA' bit set and the Dataway Cycle Rate Timer set to 1MHz, the 3982 executes Dataway cycles back-to-back. Dataway cycles occur every 1.1 microseconds with the Dataway Busy signal held asserted until list execution ceases. The 3982 requests control of the Dataway for the first CAMAC command it is instructed to execute. After obtaining control of the Dataway, through the Request/Grant protocol, the 3982 maintains the 'Request Inhibit' signal on the Auxiliary Controller Bus (ACB) until it has sequenced through all of its list. The 3982 relinquishes control of the Dataway when it receives the A.C.B. signal 'Auxiliary-Controller-Lockout' (A.C.L.). Crate Controllers using the 'normal' Request/Grant protocol are locked-out until the 3982 releases control of the Dataway.

If the 'BLK ENA' bit is cleared and the Dataway Cycle Rate Timer is set to 1MHz, Dataway cycles occur approximately every 1.5 microseconds. (This is a nominal time and measured with only one 3982 as an Auxiliary Controller.) With 'BLK ENA' cleared, the 3982 requests the Dataway for each CAMAC command executed.

RCY ENA

Recycle Enable. This bit is set to enable the Sequence Recycle feature and cleared to disable it. If enabled, the 3982 will re-execute the list of commands at a rate determined by the Sequence Repeat Rate Timer. When the Sequence Repeat Rate Timer expires, the list address is reset to zero and list execution begins. If the Sequence Repeat Rate Timer expires while the 3982 is in the process of executing a list, list execution ceases and the 'Trigger Exception' bit in the LAM Status Register is set.

When the 'Recycle Enable' bit is cleared, the list recycle feature is disabled. Even though the expiration of the Sequence Repeat Rate Timer does not re-execute the list, it will still generate a 'Trigger Exception' if a list is currently being executed. This provides a 'timeout' for list execution in cases where the 3982 is taking an inordinate amount of time to complete its list of commands.

S3,S2,S1 Sequence Repeat Rate Timer Select. These bits are used to select the Sequence Repeat Rate. The binary combination of these bits select one of eight rates: 2Hz, 5Hz, 10Hz, 20Hz, 50Hz, 100Hz, 200Hz, or 500Hz. This timer is used to repeat a list of commands at a predetermined rate. When the timer expires, the 3982, if enabled, resets the list address to zero and initiates list execution. The entire list of commands is repeated on every expiration of the timer as long as there are no exception conditions.

The Sequence Repeat Rate Timer generates a 'Trigger Exception' condition if the timer expires and the 3982 is currently executing a list. This feature provides a 'timeout' in cases where list execution is taking an inordinate amount of time to complete. The re-execution of a list is enabled or disabled via the 'RCY ENA' bit of the Timer Control Register.

NOTE: The 'RCY ENA' bit controls only the enabling and disabling of list re-cycling, but does not affect the 'timeout' feature.

DW3,DW2,DW1 Dataway Cycle Rate Timer Select bits. These bits are used to select the Dataway Cycle Rate. The binary combination of these bits selects one of eight rates: 5KHz, 10KHz, 20KHz, 50KHz, 100KHz, 200KHz, 500KHz or 1MHz. This timer is used to select the rate at which each command in the list is to be executed. For example, if the 50KHz rate is selected, the 3982 executes a Dataway cycle every 20 microseconds (50KHz). When the timer expires, the 3982 gains control of the Dataway, via the Request/Grant protocol, and then executes the CAMAC command.

The 1MHz cycle rate is not actually obtainable. If the 1MHz cycle rate is selected, and the 'BLK ENA' bit in the Timer Control Register is cleared, the 3982 executes CAMAC cycles as quick as it can while arbitrating for the Dataway for every CAMAC command. If the 'BLK ENA' is set, the 3982 gains control of the Dataway and maintains control until the list of commands has been executed or the A.C.B. signal Auxiliary-Controller-lockout is asserted. In 1MHz 'block' mode, a CAMAC Dataway cycle is executed every 1.1 microseconds (909.1KHz). In 1MHz 'non-block' mode, a CAMAC Dataway is executed every 1.5 microseconds (666.6KHz).

During list execution, the Dataway Cycle Rate Timer is disabled from counting during certain instances to avoid setting the 'Trigger Exception' bit and ceasing list execution. The timer is disabled on the following:

1.) During a Q-Repeat mode transfer while obtaining Q-responses of zero.

2.) The 3982 is requesting the Dataway and some other controller has control of the Dataway.

3.) The 3982 is requesting the Dataway and Auxiliary-Controller-Lockout is asserted.

4.) The 3982 is requesting the Dataway and 'P2' Hold is asserted. (If enabled via P2 Hold enable/disable strap).

The Sequence Repeat Timer is not disabled in the above conditions so that the 'timeout' feature is still active.

STRAP OPTIONS

P2 Hold Option

The CAMAC Dataway connector includes two free bused signals, P1 and P2, at each normal station. The 3982 responds to the signal P2 as follows. If a module asserts P2 before the 3982 asserts the CAMAC signal Strobe S1, the completion of the CAMAC cycle is delayed. The 3982 retains control of the Dataway with the CAMAC signal BUSY asserted. Once P2 is negated, the 3982 completes the delayed CAMAC cycle. The P2 Hold option can be either enabled or disabled by a strap. The location of the strap is shown on the '3982 Strap Location' diagram.

Retransmit Option

The retransmit option provides two modes for CAMAC data storage. In one mode, data is stored into/drawn from consecutive FIFO locations. In the other mode, data for CAMAC write operations will be "re-transmitted" from the FIFO to provide a repetitive output data pattern, and the Read Data FIFO pointer will be initialized to the beginning of memory.

When the re-transmit option is disabled, CAMAC read data is stored in consecutive FIFO locations and CAMAC write data is fetched from the FIFO at the current FIFO pointer location. When list execution begins, the FIFO pointers remain unchanged. In this mode, CAMAC read data is stored into the next available location in the FIFO. Therefore, if previous read data is contained in the FIFO when list execution begins, subsequent words of read data are stored into the FIFO 'behind' the previous data. This allows read data from multiple list sequence operations to be stored in the FIFO without loss of data.

If the re-transmit option is enabled, data for CAMAC write operations is re-transmitted from the FIFO and the CAMAC read data FIFO pointer is initialized to the beginning of memory so that a list of only "currently available data" can be maintained. When list sequence execution begins, the Read Data FIFO is cleared and the Write Data FIFO is "re-transmitted".

The following is an example to illustrate the differences between the two modes.

1.) Execute an F(9)·A(0) command to clear all FIFO's.
2.) Load the following instructions into RAM.

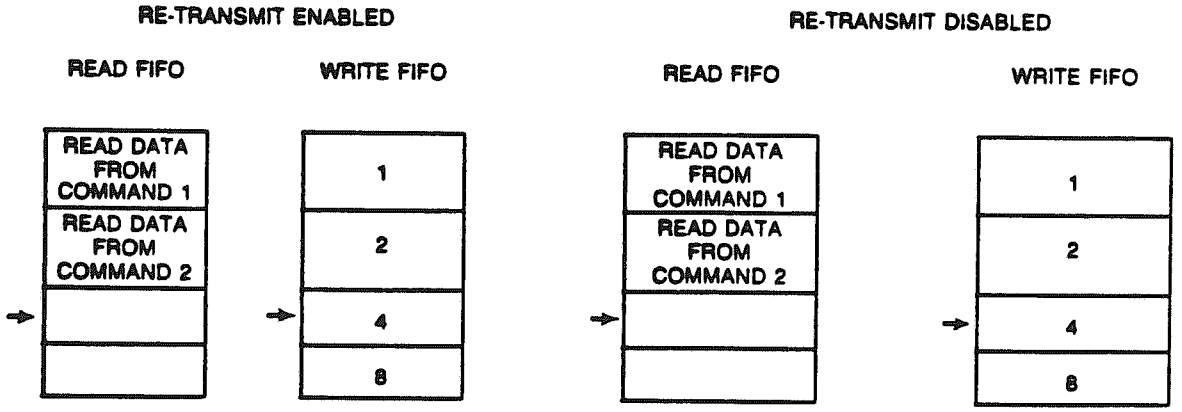
N(1)·F(0) ·A(0)	Command 1
N(1)·F(0) ·A(0)	Command 2
N(1)·F(16)·A(0)	Command 3
Last Command +N(1)·F(16)·A(0)	Command 4

3.) Load the CAMAC Write Data FIFO 'with':

Word 1 = 1
Word 2 = 2
Word 3 = 4
Word 4 = 8

4.) Execute an F(26)·A(0) to enable execution.
5.) Execute an F(25)·A(0) to initiate the list sequence.

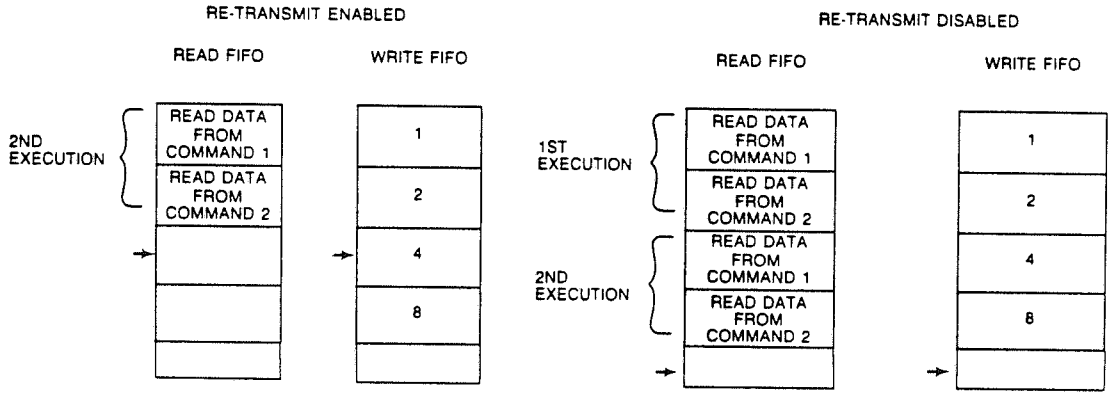
After this sequence is complete, the CAMAC Read and Write Data FIFO pointers and contents are as follows:



The commands executed were:

N(1)·F(0)·A(0)	N(1)·F(0)·A(0)
N(1)·F(0)·A(0)	N(1)·F(0)·A(0)
N(1)·F(16)·A(0) with Data = 1	N(1)·F(16)·A(0) with Data = 1
N(1)·F(16)·A(0) with Data = 2	N(1)·F(16)·A(0) with Data = 2

6.) Execute a second F(25)·A(0) to initiate the list sequence. After this sequence is complete, the CAMAC Read and Write Data FIFO pointers and contents are as follows:



The commands executed were:

1st Execution	N(1)·F(0)·A(0)	N(1)·F(0)·A(0)
	N(1)·F(0)·A(0)	N(1)·F(0)·A(0)
2nd Execution	N(1)·F(16)·A(0)w/data = 1	N(1)·F(16)·A(0)w/data = 4
	N(1)·F(16)·A(0)w/data = 2	N(1)·F(16)·A(0)w/data = 8

One/Two Buffer Option

The 3982 provides a strap option to allow use of separate CAMAC Write Data and CAMAC Read Data FIFO's or to use one FIFO to contain both the CAMAC Write and Read data.

If both FIFO's are to be used, select the option 'BUFFER-2'. In this mode, CAMAC Write Data is fetched from the Write Data FIFO and CAMAC Read Data is stored in the Read Data FIFO. This method requires that the host computer supply the 3982 with the CAMAC Write Data to be used during the list sequence and that the host also read the Read Data FIFO.

If only one FIFO is to be used, select the option 'BUFFER-1'. In this mode, both CAMAC Write and Read Data are stored in the same FIFO. Thus, data obtained from executing CAMAC read commands is used as write data for CAMAC write commands. CAMAC Read data is stored in both FIFO's so that the read data may be read from the Read Data FIFO. This allows data to be transferred from one module to another.

Note that the READ DATA is stored into both of the FIFO's; consequently, if repetitive executions of the NAF list is required, a READ FIFO overflow exception will occur if no action is taken to prevent it. There are two possible approaches to handling this situation.

1. Include an F(9)A(0) addressed to the 3982 (itself) as the last CAMAC command in the 3982's list, which will initialize the FIFO pointers each time the list is executed.

2. Utilize another Crate Controller to read the data from the Read Data FIFO before the exception occurs.

EXTERNAL TRIGGER

List execution can be initiated by a TTL level signal pulse on the 3982 front panel 'TRIGGER' connector. This pulse must be at least 200 nanoseconds long. This signal will initiate the list sequence operation, as long as the 3982 is enabled for execution.

If this mode of list initiation is desired, place the trigger enable/disable strap in the 'TRIG ENA' position. To disable this option, place the strap in the 'TRIG DIS' position.

The 3982 provides for selection of either low-true or high-true edge triggering for the 'TRIGGER' input. To initiate list sequencing on a low-going-edge, place the TRIG HI/LO strap in the 'TRIG LO' position. If high-going-edges are required, place the strap in the 'TRIG HI' position.

> NOTE: Enabling the External Trigger and the Sequence Repeat Timer function simultaneously may lead to execpected Trigger Exception indications if care is not taken to synchronize the external trigger and internal timer.

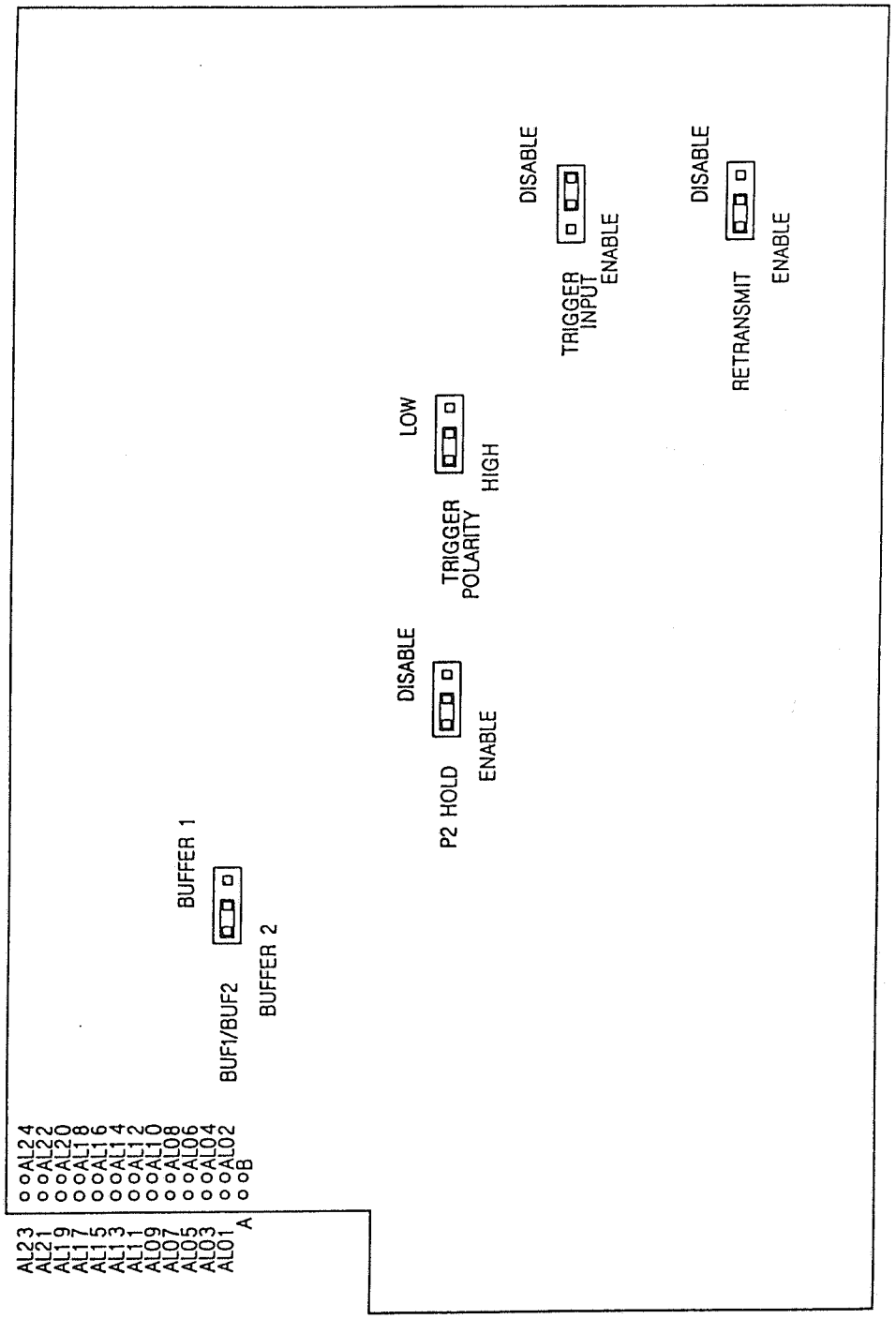
LAM TRIGGER

A list sequence operation may be initiated by the assertion of one of the 24 CAMAC LAM Signals. The selection of a LAM bit which initiates a sequence is made via wire-wrap selection. The wire-wrap posts are located near the Auxiliary Controller Bus 40-pin connector. Only one LAM signal is to be connected at any time. The wire-wrap post signal allocation is as follows:

AL 23 •	• AL 24
AL 21 •	• AL 22
AL 19 •	• AL 20
AL 17 •	• AL 18
AL 15 •	• AL 16
AL 13 •	• AL 14
AL 11 •	• AL 12
AL 9 •	• AL 10
AL 7 •	• AL 8
AL 5 •	• AL 6
AL 3 •	• AL 4
AL 1 •	• AL 2
PULL UP •	• LAM TRIGGER

To disable the initiation of a list sequence operation by a LAM, wire-wrap pins 'Pull UP' to 'LAM TRIGGER'. To enable LAM triggering, wire the appropriate 'ALn' LAM signal pin to the 'LAM Trigger' pin.

When a selected LAM is asserted, it sets the 'EXT' bit, bit 10, of the LAM Status Register.



MODEL 3982 STRAP LOCATIONS