Model 3992

Serial Highway Driver

INSTRUCTION MANUAL

May, 1987

**** SPECIAL OPTION ****

MODEL 3992-S001

SEPTEMBER 1983

Model 3992-S001

****** SPECIAL OPTION ******

3992-S001

The Model 3992-S001 Serial Highway Driver allows redundant host computers to communicate on the serial highway using standard Model 3936 and 3933 U-ports.

The following modifications were made to the standard Model 3992 to make it a special option.

1. Lengthen the "N" one slot to approximately 6 seconds.

2. Gate the serial highway clock driver with the output of the "N" one slot.

Special programming instructions:

1. When switching host computers, wait 6 seconds or more to allow the 3992-S001 to time out.

2. Do several non-highway type commands (e.g., Read Status Register) to the 3992-S001 which will be used for the next highway transfer. This allows the highway to gain sync.

3. To maintain sync, successive commands must now be issued in less than 6 seconds.

Special Option

Model 3992-S002

Serial Highway Driver

October, 1987

*** Special Option ***

Model 3992-S002

The Model 3992-S002 is a Model 3992-Z1A which has been modified such that the Repeat Command mode of operation will operate for both Read and Write operations to the remote CAMAC crate. The Repeat Command mode for Read operations is described on pages 18 and 19 of the Model 3992 Manual. For Write operations, the C-N-A-F parameters loaded into the Model 3992's Command Register are executed each time a new data word is loaded into the Write Data Register with an F(16)·A(1) function.

This modification will allow both the Q-Stop and Word Count types of block transfers to be performed, as described on page 19 of the 3992 Manual. As with Block Read operations, the user must check the status of operation when the Serial Highway transaction has been completed.

October, 1987
MLH:rem(3000 Ser. 12)

TABLE OF CONTENTS

TABLE OF CONTENTS

(Continued)

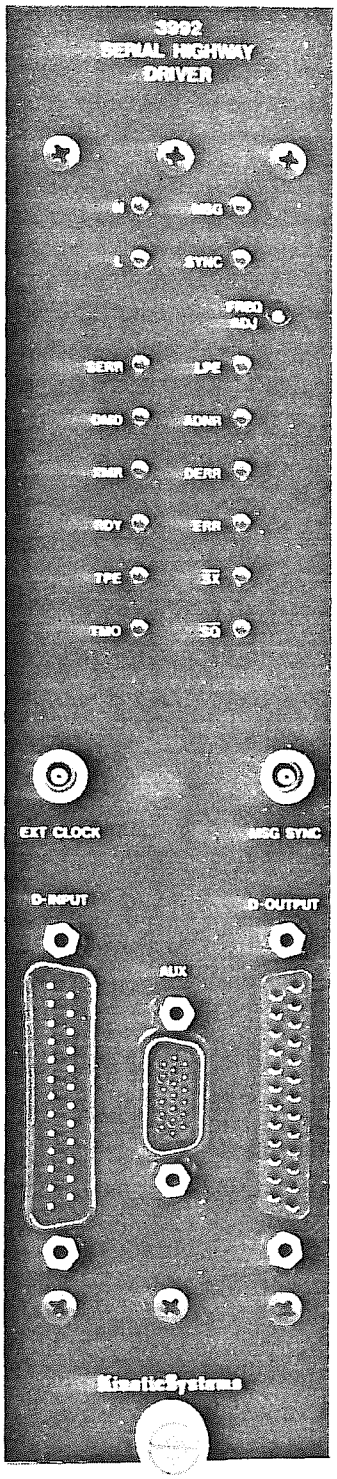
Serial Highway Driver

Operates as a CAMAC module and a Serial Highway driver **3992**

Features

- **Operates as a module in a CAMAC system**
- **Complies with CAMAC specifications IEEE-583 and IEEE-595**
- **Bit-serial and byte-serial modes to five megahertz**
- **Crystal-controlled and variable-frequency clock sources**
- **Flexible means for selecting clock frequency**
- **Separate buffers for incoming demand and reply messages**
- **Lost-sync indication**
- **12-bit LAM register with mask and front-panel LED display**
- **Seven internal registers**
- **Four internal status signals**
- **Q-scan mode**
- **Reply timeout**

(Product specifications and descriptions subject to change without notice.)



General Description

The Model 3992 is a three-wide CAMAC module which transmits and receives signals on the CAMAC Serial Highway. It fully complies with CAMAC specifications IEEE-583 and IEEE-595. Bit-serial and byte-serial ports for data and clock are provided for transmitting command messages and for receiving Reply and Demand messages.

All functions of the module are controlled by the Dataway. Serial messages are initiated by Dataway operations involving Command and Data registers. Transverse-parity and longitudinal-parity are checked on incoming messages.

The output clock can be controlled by a crystal or variable-frequency oscillator or from an external source. Means for selecting frequencies from one kilohertz to five megahertz are provided for both the crystal-controlled and variable-frequency oscillators. The external source can range from arbitrarily slow to five megahertz.

Twelve-bit LAM and LAM Mask register provide flexible interrupt capability. The LAM register can be cleared and selectively cleared, and the LAM Mask register can be written, cleared, selectively set, and selectively cleared.

The module is set to a predefined state upon power-up.

Operational Features

Six registers provide communication between the Dataway and the Serial Highway. Message transmission is initiated by:

1. Writing the Command register with a serial Read or command function, or

2. Writing the Write Data register while the Command register contains a serial Write function.

Loading the Command register with a serial Write command does not initiate transmission.

Serial Read data is retrieved by F(0)·A(0) command after the Reply message has been received. The serial Q and X signals (SQ and SX) are transmitted on the Dataway Q and X lines to the crate controller along with the Read data.

Operational Features (continued)

SQ and SX for serial non-Read operations are retrieved by reading the Status register. A new transfer cannot be initiated while the serial transmitter is in the process of sending out a message. Attempts to write the Data and Command register while the transmitter is busy are inhibited, and Q = 0 will be returned. Programmed utilization of the Serial Highway requires transmitting a serial command message and waiting until a reply is received before transmitting a new message. Since systems may contain from one to 62 crates, each of which may or may not have a three-byte delay switched in, the timing of the receipt of Reply messages may range from coincidental with the issuance of serial command space-bytes to as many as 186-bytes following completion of the Serial Command. Condition flags are provided which can be tested by software to determine when message transmission is complete or when a reply has been received.

Function Codes

Command		Q	Action
F(0)·A(0)	RD1	SQ	Reads the Read Data register.
F(1)·A(0)	RD2	$\overline{\text{CMD}}$·SHR	Reads the Status register.
F(1)·A(8)	RD2	1	Reads the Demand register.
F(1)·A(12)	RD2	$\overline{\text{CMD}}$·SHR	Reads the LAM Status register.
F(8)·A(15)	TLM	LR	Tests whether a LAM request is present.
F(11)·A(12)	CL2	0	Clears the LAM Status register.
F(11)·A(13)	CL2	0	Clears the LAM Mask register.
F(16)·A(0)	WT1	$\overline{\text{CMD}}$	Writes the Command register.
F(16)·A(1)	WT1	$\overline{\text{CMD}}$	Writes the Write Data register.
F(16)·A(2)	WT1	$\overline{\text{CMD}}$	Writes the lower 16 bits of Command register.
F(17)·A(13)	WT2	1	Writes the LAM Mask register.
F(19)·A(13)	SS2	1	Selectively sets the LAM Mask register.
F(23)·A(12)	SC2	1	Selectively clears the LAM Status register.
F(23)·A(13)	SC2	1	Selectively clears the LAM Mask register.
F(27)·A(0)	TST	$\overline{\text{CMD}}$	Returns Q = 1 if transmission of output messsage has been completed.
F(27)·A(1)	TST	$\overline{\text{CMD}}$·SHR	Returns Q = 1 if $\overline{\text{CMD}}$ is true and if a reply has been received or a timeout has occurred since initiation of previous output message.
F(27)·A(2)	TST	SYNC	Returns Q = 1 if the receiver sync signal SYNC is true.
F(27)·A(4)	TST	DMD	Returns Q = 1 if the Demand LAM is set.
Z	CZ	0	Clears the LAM Status and LAM Mask registers.
Note: X = 1 is returned for all valid commands except F(0)·A(0); for that command, X = SX.			

Power Requirements

+6 volts: 2800 mA
–6 volts: 50 mA

Ordering Information

Model 3992-Z1A Serial Highway Driver

Related Products

Model 5800-Axyz Bit-serial Highway Cable
Model 5800-Bxyz Bit-serial Highway Cable
Model 5801-Axyz Byte-serial Highway Cable
Model 3936-Z1B U-Port Adapter
Model 3939-Z1C U-Port Adapter
Model 3939-Z2A U-Port Adapter

Q-MODE

If the MR-bit is true in the Command register, an F(0).A(0) command to the 3992 initiates another serial transmission. The serial Command message is the same as the previous message if the MQ-bit = 0. If MQ = 1, the new serial message has SA incremented if the previous SQ was true or SA reset and SN incremented if the previous SQ was false. If the N-counter advances beyond N = 32 in this mode, the crate address is cleared. A subsequent transmission with CRATE = 0 will cause the ADNR (address not recognized) bit in the LAM register to be set upon receipt of the reply message.

TIMEOUT

If 350 msec elapses between the start of a message transmission and receipt of a reply message (or unrecognized command message) the TIMEOUT signal is asserted, which sets the TMO LAM source. SHR also becomes true (SHR = RPL + TIMEOUT) and the RDY LAM source is set if/when CMD is true. Reply messages received after TIMEOUT is asserted are ignored.

SPACE BYTE REQUIREMENT

BYTE RATE (megabytes/sec)	MINIMUM NUMBER OF SPACE BYTES	
	write/test	read
to .67*	3	7
.67 to 1.33	4	8
1.33 to 2.0	5	9
2.0 to 2.67	6	10
2.67 to 3.33	7	11
3.33 to 4.0	8	12
4.0 to 4.67	9	13
4.67 to 5.33**	10	14

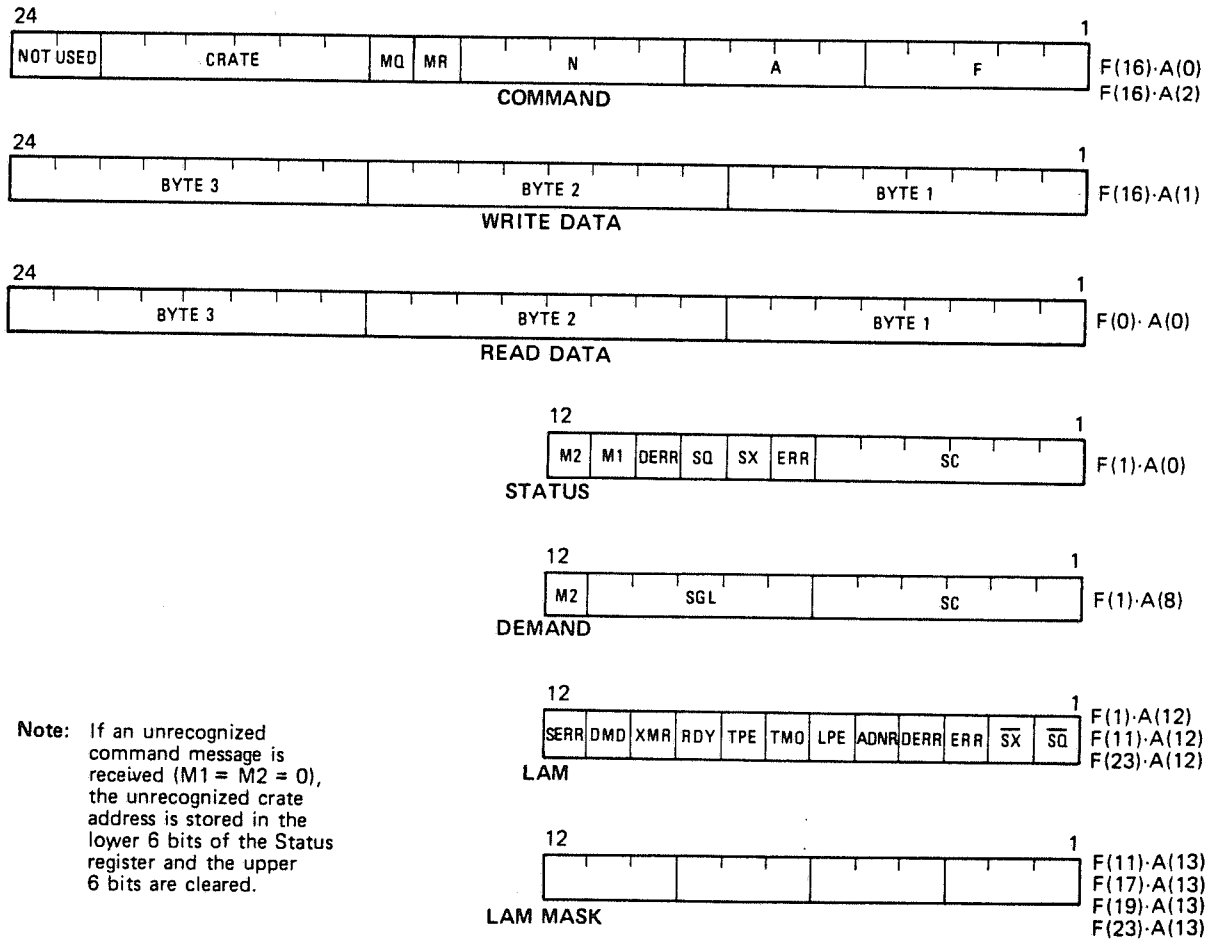
Notes: *All bit-serial operation is in this range.

**Proper SCC operation is not guaranteed above 5 MHz

CONDITION FLAGS

Binary Flag	Condition	Test Command
CMD	Indicates that a serial command message is in the process of being transmitted.	F(27)·A(0) Q = $\overline{CMD}$
SHR	SHR = RPL + TIMEOUT, where: RPL indicates that a message other than a demand message has been received since the last serial transmission. TIMEOUT indicates that 350 msec has elapsed since the last serial transmission without receipt of a reply or unrecognized command message.	F(27)·A(1) Q = SHR·$\overline{CMD}$
SYNC	Indicates that the receiver is receiving bytes and has acquired byte sync (if in bit serial mode). If more than four bytes are transmitted (including wait bytes) without receipt of a byte, SYNC becomes false.	F(27)·A(2) Q = SYNC
DMD	Indicates that a demand message has been received and that the demand LAM source bit is set.	F(27)·A(4) Q = DMD

REGISTERS



Note: If an unrecognized command message is received (M1 = M2 = 0), the unrecognized crate address is stored in the lower 6 bits of the Status register and the upper 6 bits are cleared.

LAM REGISTER

Bit	Label	Type*	Description
12	SERR	A	Indicates that either bytes are not being received or that the receiver has lost byte sync. Set by the assertion of $\overline{SYNC}$.
11	DMD	A	Indicates that a demand message was received
10	XMR	A	Indicates that the serial transmitter is ready. It is set by the assertion of $\overline{CMD}$.
9	RDY	A	Indicates that a serial command has been transmitted and that either the reply message has been received (or command message if the crate address was unrecognized) or that the timeout period has elapsed. It is set by the assertion of $\overline{CMD}$·SHR
8	TPE	A	Indicates that a transverse parity error was detected in a reply message. It is not set if a transverse parity error occurs on a wait byte.
7	TMO	A	Indicates that 350 msec has elapsed from the start of a serial message transmission without receipt of a reply. It is set on assertion of TIMEOUT.
6	LPE	S	Indicates that a longitudinal parity error was detected in the reply message.
5	ADNR	S	Indicates that the crate address was not recognized by any crate on the serial highway. This condition is recognized by M1 and M2 both being false in the reply message ($\overline{M1}$·$\overline{M2}$ = TRUE).
4	DERR	S	Indicates that an error was detected by the addressed SCC in the previous message addressed to it.
3	ERR	S	Indicates that an error was detected in the command message by the addressed SCC. $\overline{SQ}$ and $\overline{SX}$ will normally be set along with ERR since a detected error inhibits the Dataway cycle.
2	$\overline{SX}$	S	Indicates X = 0 response to the serial message. This bit also is not set if $\overline{M1}$·$\overline{M2}$ is true in the reply.
1	$\overline{SQ}$	S	Indicates Q = 0 response to the serial message. The bit is not set if $\overline{M1}$·$\overline{M2}$ is true in the reply.

*The 12 LAM bits may be classed as synchronous (S) and asynchronous (A). The synchronous bits are set or not set depending upon the status of signals at the receipt of a reply message. Asynchronous bits are set as events occur. The bits are cleared by F(11)A(12) or F(23)A(12) commands.

FRONT PANEL

LED Indicators

N	Flashes when the module is addressed.
L	On when L signal is true
MSG	Flashes when a serial message is initiated.
SYNC	On when the receiver is synchronized to incoming bytes.
LAM REG (12)	Each LED is on when its respective bit in the LAM register is true.

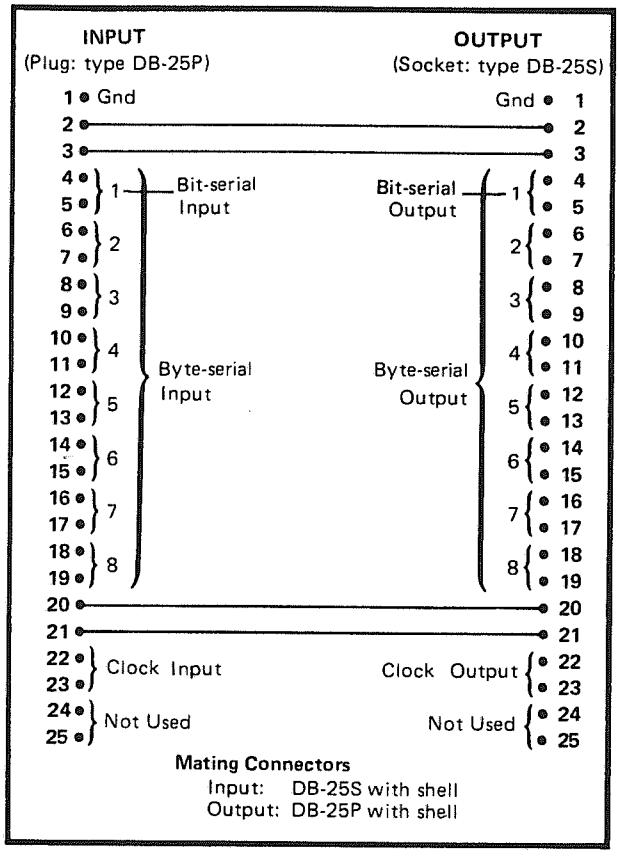
I/O Connectors

D-OUTPUT	D — Port output connector, 25-way Cannon Type DBC-25S or equivalent.
D-INPUT	D — Port input connector, 25-way Cannon Type DBC-25P or equivalent.
EXT CLOCK	(LEMO) Provides input for optional external clock, TTL level.
MSG SYNC	(LEMO) Provides scope sync signal that goes low when message is being sent out.

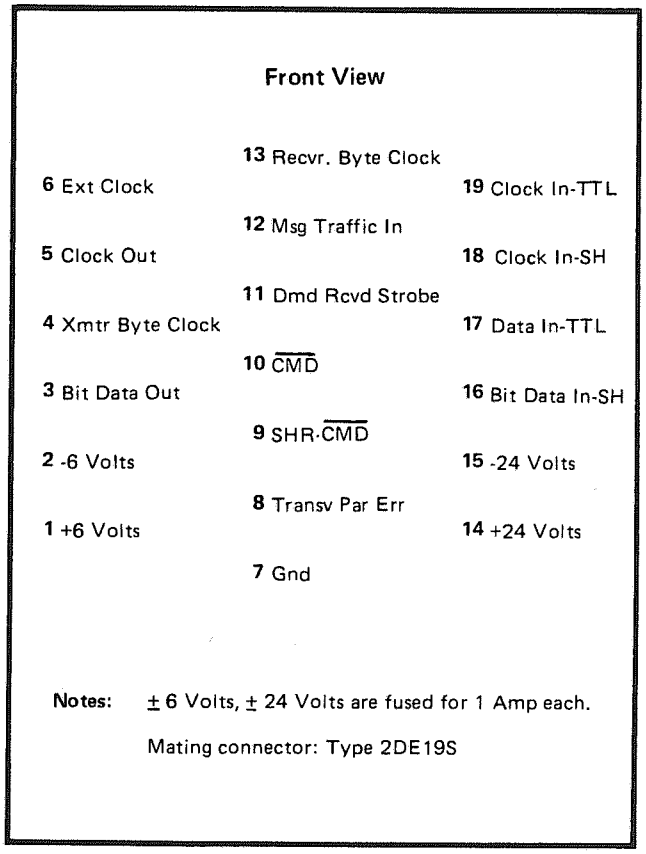
Test Points

19-way type 2D miniature connector provides fused ±6 Volts, ±24 Volts, power common and access points for observing and using fourteen internal logic-level signals.

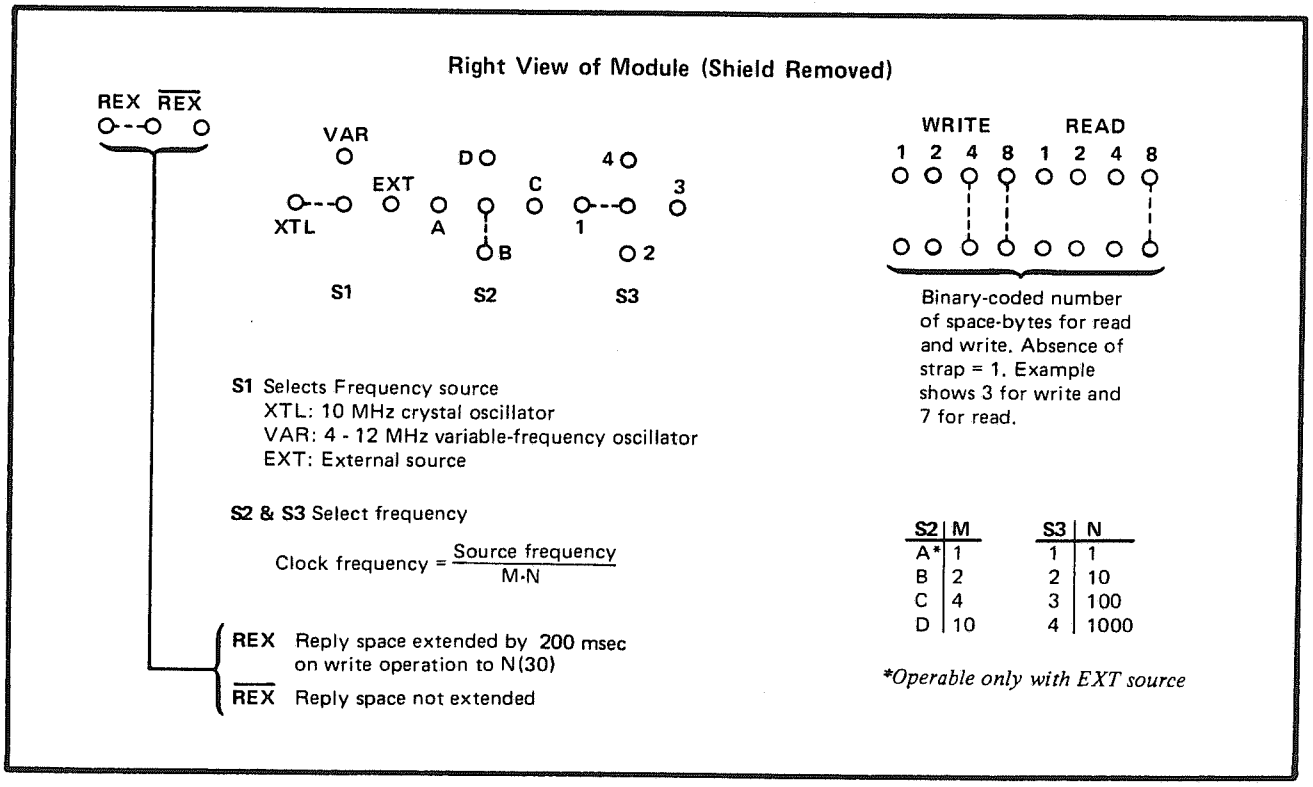
SERIAL HIGHWAY CONNECTORS



AUXILIARY CONNECTOR



STRAP OPTIONS



HIGHWAY DATA RATE STRAP SELECTION

Selection of frequency and source is shown below:

Frequency Strap	Crystal Controlled	Variable	External
	Strap XTL	Strap VAR	Strap EXT
A1	---	---	EXT
B1	5 MHz	2.5 - 5 MHz	EXT/2
C1	2.5 MHz	1 - 2.5 MHz	EXT/4
D1	1 MHz	0.5 - 1 MHz	EXT/10
B2	500 KHz	250-500 KHz	EXT/20
C2	250 KHz	100-250 KHz	EXT/40
D2	100 KHz	50 - 100 KHz	EXT/100
B3	50 KHz	25 - 50 KHz	EXT/200
C3	25 KHz	10 - 25 KHz	EXT/400
D3	10 KHz	5 - 10 KHz	EXT/1000
B4	5 KHz	2.5 - 5 KHz	EXT/2000
C4	2.5 KHz	1 - 2.5 KHz	EXT/4000
D4	1 KHz	0.5 - 1 KHz	EXT/10,000

Notes:

1) Remove ground plane from right side of module to access "push-on" straps.

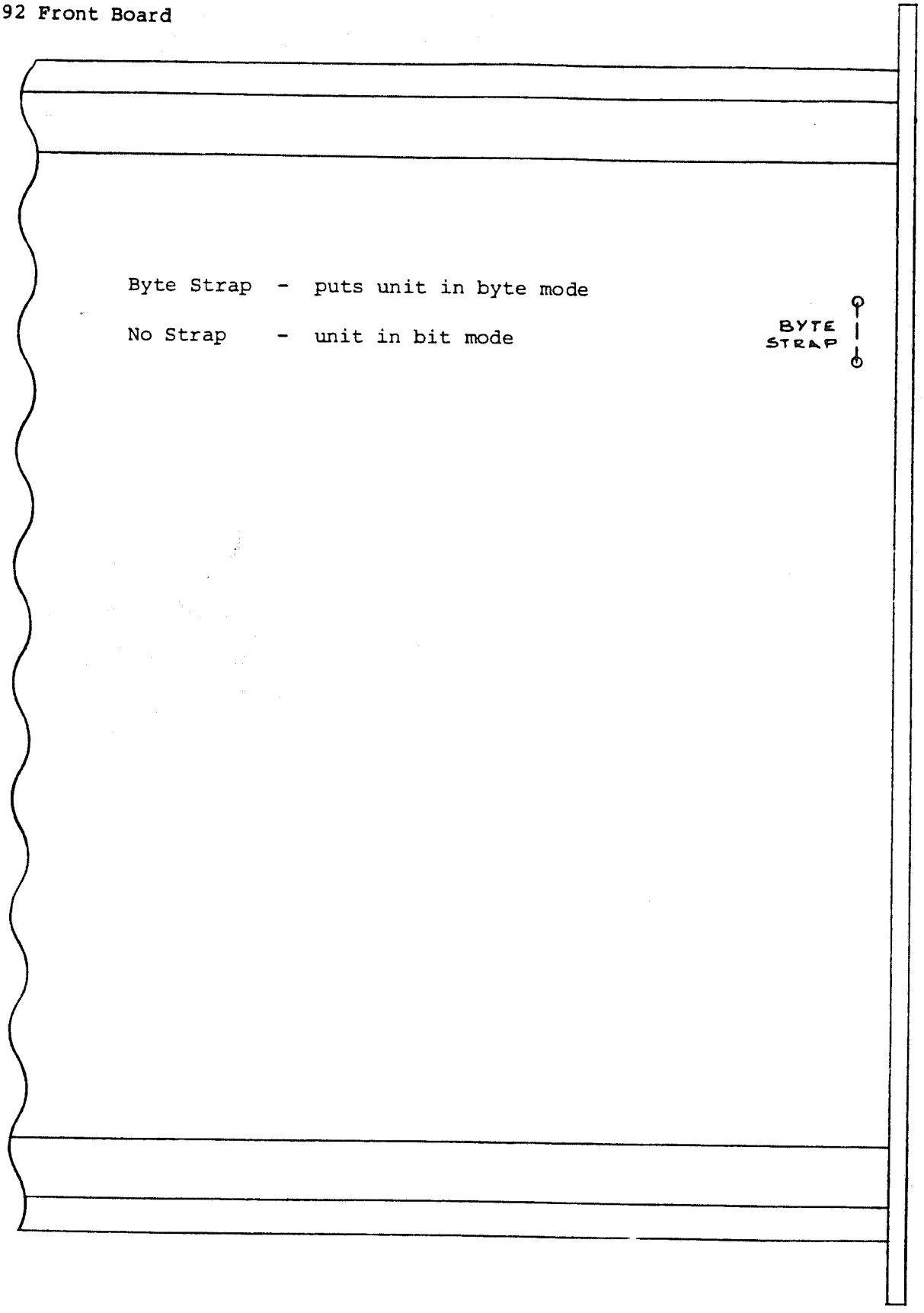
2) Some overlap is provided on variable frequency range. Variable adjustment is made from front of module.

MODEL 3992-Z1B OPTION

The Model 3992-Z1B Serial Highway Driver can be converted for use without the Model 3993 Block Transfer Controller by removing the ground shield from the rear of the 3992 "C" board (far right P.C. board) and inserting the 3992 strap located to the right of the space byte straps.

BIT/BYTE STRAP SELECTION

3992 Front Board



DEFINED SERIAL HIGHWAY

The 3992 front panel contains a 25-contact D-socket connector (D-OUTPUT) for driving the serial highway and a 25-contact D-plug connector (D-INPUT) for receiving Reply and Demand messages from the serial highway. These connectors are called "D-ports" because they are defined in the CAMAC serial highway system specifications (IEEE 595-1976). Figure 1 shows the simple "loop" connections between a 3992 and 3952 Type L-2 Serial Crate Controllers (L-2 SCCs).

DATA RATE CONSIDERATIONS AND STRAP OPTIONS

The serial highway may be operated in bit-serial mode (one pair for clock and one pair for data), or in byte-serial mode (one pair for clock and eight pair for data). With all other conditions the same, byte-serial operation results in a transmission rate an order of magnitude faster than bit-serial. The serial driver/L-2 SCC combination can operate at any data rate to five megabits/second.

The length of time required to send one message depends upon the selection of a bit or byte mode and the clock rate chosen. Figure 2 shows the typical message length versus clock rate. Various factors affect the actual message length, and these will be described later in this document; however, the information shown here can be used as a general operating guide.

Note that the actual length of time required to send one message is not the only factor in system operating rate. Any software overhead must be considered in determining the overall rate.

The maximum clock rate is controlled by the transmission medium (cable size, etc.) used and the length of the serial highway. It is often desirable to add U-port adapters to a serial highway system. The term "U-port" is used because the serial highway is connected to Undefined ports (specified by the module designer, not defined by IEEE 595-1976). These U-port adapters can provide transformer or optical isolation of the serial highway, crate bypass and loop collapse, as well as other features. Figure 3 shows how U-ports are connected in the D-port patch.

Prior to inserting the 3992 into the crate, the following parameters must be considered:

1) Bit-serial or byte-serial operation
2) Internal variable clock, internal crystal clock, or external clock
3) System operating speed

The 3992 strap options should be selected as follows:

Bit/byte Serial

If the serial system is to be operated in byte serial, the Byte Strap should be inserted; for bit-serial operation, the Byte Strap should be removed.

Internal/External Clock

For most applications, the 3992 serial driver should be operated with its internal crystal clock. The variable clock can be used for special applications; however,

most of our U-port adapters require an accurate clock source. The external clock connection is used with applications such as the 3934 modem adapter.

Clock Rate

As discussed earlier, the maximum system operating speed is determined by transmission considerations. Note that, when used with most U-port adapters, the 3992 clock rate MUST equal the clock rate selected on the U-port adapters.

During the initial set-up of a new system, it is generally a good idea to use a clock rate lower than the maximum so that the system can be made operational without any transmission problems interfering with software debugging, etc. For most systems, a 500 kilobit or 1 megabit selection can be made for initial set-up.

Space Bytes

A typical Command/Reply sequence for byte-serial operation is shown in Figure 4. The Command from the serial driver (SD) to the SCC and the Reply from the SCC to the SD is shown. Note that space bytes are sent from the SD to allow time for the Dataway cycle in the SCC and the reply.

The minimum number of space bytes required is controlled by the operating speed and whether bit-serial or byte-serial mode is being used. The space byte selection on the 3992 is shown in Figure 5. Note that too many space bytes will cause no harm except a longer message time; however, too few space bytes will cause aborted reply messages.

3992 OPERATION WITH 16-BIT CRATE CONTROLLERS

The 3992 Serial Highway Driver operates as a module in any CAMAC crate capable of 24-bit read/write operations. A limited number of crate controllers provide only 16-bit Dataway operations. In such a case, our 3940 Crate Controller Expander can be used to provide the 24-bit transfers to the 3992.

TYPE L-2 CRATE CONTROLLER SETUP

A serial highway can include one serial highway driver and up to 62 serial crate controllers (SCCs). Throughout this document, we shall describe the SCCs as "Type L-2" and indicate the location of strap options on our Type 3952 L-2 SCC. As the serial specification was being developed, various versions of Type L-1 SCCs were produced by several manufacturers (as changes were made to the proposed specification). These L-1 SCCs will generally operate in the same system as L-2s; however, minor differences exist, such as lockout signals for autonomous controllers and the meaning of the error bits in the Reply message.

Bit/Byte Serial

Our 3952 L-2 SCC contains a strap for selection of bit serial or byte serial operation. This strap must be in the same mode as that selected on the serial driver.

Demand Message Generation

L-2 SCCs are arranged to send Demand messages back to the serial driver in response to L-signals in the crate. The SCC contains an SGL (Serial graded L) connector on its rear panel. This 52-contact "D" plug connector contains various signals for Demand generation as well as signals that can be used for auxiliary crate controllers (such as our 3909, 3981 and the auxiliary versions of our 3912). Figure 10 shows the signal layout on the SGL connector.

Demand generation can be implemented with simple patch connections on a mating connector to the SGL connector or in conjunction with a LAM grader. These optional connections, as well as operation with auxiliary crate controllers, is shown in Appendix B.

The 3952 contains a Demand repeat timer. This is used to send "repeat" Demand messages, in the event that the original Demand message was not acted upon after a predetermined time. This could be caused by computer overhead or a transmission error in the original demand message. This will continue to "repeat" at the time interval set until Demand Message Initiate is cleared.

Note that the serial system will operate without any connections to the SGL connector or any selection of repeat time. However, Demand messages will not be generated.

Crate Address Selection

The 3952 SCC can be set to any decimal crate address from 1 to 62. Once an SCC is set to a crate address by the front panel thumbwheel switches, it will respond to that address from the serial driver. The switches will allow the address to be set from 0 to 69; however, any out-of-range selection (67, for example), will result in no action. Note that more than one SCC must not be set to the same address. If this is inadvertently done, the downstream SCC will "garble" the reply message from the upstream SCC.

On-Line/Off-Line Switch

For normal operation, this switch should be set to the "On-Line" position. When in the "Off-Line" position, the SCC can be addressed, but Dataway operations are disabled. As will be discussed later, the "On-Line" position is really "On-Line Enable". This switch state is ANDed with an internal bit in the status register and set from the serial driver to produce an on-line state.

CONNECTING THE SD AND SCC TO THE HIGHWAY

As described earlier, the serial highway can be configured with D-port connections or U-port adapters. Appendix A shows detailed connections for various of these configurations as well as guidelines for application and operating speed.

Remember that, while the L-2 SCC does not require any rate adjustment, most U-port adapters include a data rate selection, and all such adapters in a system MUST be set to the same operating speed as the serial driver. The Model 2958 Byte Serial Adapter is an exception to this--a separate clock signal is sent and no data rate selection is required.

INITIAL STATE AFTER POWER-UP

Serial Driver (3992)

If all connections are properly made to the D-port connectors (and to the U-port adapters, if used), and the operating speed has been selected properly, the 3992 should be receiving Wait bytes and, therefore, the receiver should be in sync. This is indicated by the 3992 Sync LED being ON.

For systems operating in bit serial, this means that the Wait bytes and appropriate Start and Stop bits are being received. This indicates that the transmission of a serial message will likely succeed.

For systems operating in byte serial, Sync ON means that the clock is being received back at the serial driver; in byte serial, a stream of Wait bytes results in some data pair being static in the TRUE state and some being static in the FALSE state. Therefore, a data pair could be broken or transposed on the serial highway and Sync would still be present.

L-2 SCC (3952)

The 3952 contains a 16-bit status register. These bits are set to a defined state on power-up. This is shown in Figure 12. Note that the Dataway off-line control bit is set to one, and the Bypass control bit is set to one on power-up. Therefore, the Bypass LED is ON and the On-line LED is OFF (regardless of On-line switch setting), immediately after power-up. The SCC also initiates a crate Z as part of the power-up sequence.

If the No sync LED is ON (in bit serial mode), this indicates that the Wait byte pattern is not being received properly. This could be generally caused by improper serial highway connections, too much transmission loss at the data rate chosen, serial driver and all U-port adapters not set to the same data rate, or equipment problems.

If the No sync LED "flickers", the signal being received is marginal. This could possibly be caused by extensive interference and/or excessive transmission loss. This can generally be eliminated by reducing system speed.

Since there is no byte sync requirement in byte serial (each bit in the byte is transmitted over a different pair), the No sync LED remains OFF in byte serial mode regardless of the signal received from the serial highway.

COMMAND SEQUENCE EXAMPLES

In order to better understand the operation of the serial highway system, simple command sequence examples are shown here. They do not represent the complete software for an "operating" system (software error detection and recovery is not provided, etc.). However, they should be useful in order to become familiar with the serial system or to debug the hardware set-up.

Setting an SCC to On-Line and Unbypassed State

(All commands are middle slot - 3992, data is shown in binary (BN), octal (OC), and hexadecimal (HX). The least significant bit (or digit), is on the right.)

1. F(11).A(12) Without data
   This clears the LAM status register. Since the LEDs monitor LAM status bits, they remain ON until cleared. This clearing allows the LEDs to give an indication of the results of the serial message to follow. All 12 LAM status LEDs should now be OFF. If a momentary loss of sync were to occur, SERR would go ON.

2. F(16).A(0) Data: BN 10011110000010111, OC 236027, HEX 13C17
   This loads the command register with the following serial information: crate one, N(30), A(0), F(23). It "prepares" for a selective clear operation to serial crate address one.

3. F(16).A(1) Data: BN 1100000000000, OC 14000, HEX 1800
   This causes the serial message to be sent. The data associated with the serial selective clear command should set bits 12 and 13 in the SCC status register to zero, placing it in the unbypassed and on-line state.

   During the serial message transmission, the MSG LED in the 3992 and the ADD REC (address received) LED in the 3952 should flash. Of the 12 LAM status LEDs, only the XMR and RDY LEDs should be ON, indicating that the message has been transmitted (XMR), and a reply has been received (RDY). If other LAM satus LEDs are set, refer to Figure 13 for their meaning.

   If Bypass is implemented in a U-port adapter associated with the SCC, the SERR LED may go ON as the result of an unbypass operation because the serial highway is momentarily "broken" when the highway is transferred at the SCC.

   At the 3952 SCC, the Bypass LED should now be OFF and the On-Line LED should be ON (if the On-Line switch is ON).

The above procedure can be repeated from Step 1, or Step 3 can be repeated to retransmit the serial message. The F(11).A(12) command should be repeated if it is desired to clear the LAM status bits (and LEDs).

Note that in this example it is assumed that the commands are performed single-step so that the time between commands is greater than the time for a serial message transfer. Therefore, the F(27).A(1) Q-test is not performed.

USING THE MODEL 3992 SERIAL HIGHWAY DRIVER

REGISTERS

Command Register

The Command Register is used to specify the Serial Crate Address, Station Number, Subaddress and Function Code.

Bits 1 through 5 specify the CAMAC Function code, F(0) through F(31), and can be written by F(16).A(0) or F(16).A(2).

Bits 6 through 9 specify the CAMAC Subaddress, A(0) through A(15), and can be written by F(16).A(0) or F(16).A(2).

Bits 10 through 14 specify the CAMAC Station Number, N(1) through N(31), and can be written by F(16).A(0) or F(16).A(2).

Bits 15 and 16, MR and MQ, specify the mode of operation the SH Driver will run in. These bits can be written by F(16).A(0) or F(16).A(2).

Mode Number	MR	MQ	Description
1	0	0	single command
2	1	0	repeat command
3	1	1	Q Scan

The repeat modes, two and three, can be used with serial read commands. A new serial transaction is initiated when the serial Read data is read with the F(0).A(0) command. For further information, refer to the Operating Modes section of this manual.

Bits 17 through 22 specify the Serial Crate Address, SC(1) through SC(62), and can be written by F(16).A(0) only. When executing several commands in the same serial crate, the F(16).A(2) command can be used to load the NAF in the command register without altering the crate address.

Write Data

The Write Data Register specifies the write data for Serial Write commands. It can be written with the F(16).A(1) command.

Read Data

The Read Data Register contains the data from the last Serial Read command. It can be read with the F(0).A(0) command. The 3992 places the Serial Q and X responses on the Q Bus and X Bus of the local crate during the F(0).A(0) command.

Status

The Status Register contains status information regarding the last command executed by the SH Driver. This register can be read with the F(1).A(0) command.

Bits 1 through 6 specify the address of the crate from which the last Reply Message was received, or, in the case of no crate accepting a command message, the crate address to which the command was sent.

Bits 7 through 10 specify the status information included in the Reply Message by the addressed Serial Crate Controller.

Bit 7, ERR, is set to Logic 1 if the addressed SCC detects a longitudinal or transverse parity error in the command message it receives. If the ERR bit is set, the command was not executed by the SCC.

Bit 8, SX, corresponds to the X Command Accepted response to the Dataway command executed by the SCC.

Bit 9, SQ, corresponds to the Q Response to the Dataway command executed by the SCC.

If the SCC does not execute the Dataway command, that is, ERR = 1, SX and SQ are set to Logic 0.

Bit 10, DERR, indicates whether the previous command to the SCC was executed successfully. The DERR bit is set to Logic 1 if the previous command message to the SCC contained a parity error or the X Command Accepted response to the last command executed by the SCC was zero.

Bits 11 and 12, M1 and M2, correspond to the message identifier field of the message received by the SHD. If M1 and M2 equal zero, the crate address stored in bits 1 through 6 refers to the crate address the command message was directed to. If M1 is one and M2 is zero, bits 1 through 6 refer to the address of the crate which sent the reply message.

Further information regarding the use of the information provided in the status register will be found in the Operating Procedures and Error Recovery sections of this manual.

Demand

The Demand Register contains the Serial Crate Address and Serial Graded LAM information received in the last serial Demand Message. The serial Demand provides the SCC with a method of asynchronously notifying the serial driver that a LAM is pending in its crate.

Bits 1 through 6 indicate the address of the crate which sent the demand.

Bits 7 through 11 correspond to the Serial Graded LAM pattern in the serial crate.

Bit 12 corresponds to the state of the message identifier bit in the demand message.

LAM Status

The LAM Status Register provides a latched source of status information regarding serial highway operation. Once a LAM Status bit is set, it remains true until cleared by Dataway command.

The states of LAM Status bits 1 through 6 are updated upon receipt of the last byte of a Reply message.

Bit one, $\overline{SQ}$, will be set if one of the following conditions is met:

1) the command is executed and the Q Response is zero,
2) the addressed SCC detected an error in the command message,
3) no SCC accepted the command.

Bit two, SX, will be set if one of the following conditions is met:

1) the command is executed and the X Command Accepted response is zero,

2) the addressed SCC detected an error in the command message,

3) no SCC accepted the command.

Bit 3, ERR, will be set if the addressed SCC detected an error in the command message.

Bit 4, DERR, will be set if the previous command sent to the addressed SCC contained a parity error or the X Command Accepted response to the last Dataway command executed by the SCC was zero.

Bit 5, ADNR, will be set if no crate accepts the command message transmitted by the SHD. This indicates that the addressed crate is in the bypass mode or the crate address in the Command message was damaged during transmission.

Bit 6, LPE, is set if a longitudinal (column) parity error is detected in the reply message. This indicates that the Reply message was damaged in transmission and cannot be considered valid; that is, bits 1 through 5 of the register must be ignored and Read data, if any, cannot be considered valid. For information on error recovery procedures, refer to the Error Recovery section of this manual.

The states of LAM Status bits 7 through 12 are updated asynchronously, whenever the event described by a bit occurs.

Bit 7, TMO, indicates that 350 milliseconds has elapsed since the SD transmitted the Command message and no Reply or turned around message (command message not accepted by any SCC), has been received.

Bit 8, TPE, indicates that a transverse parity error was detected in a Reply message. This indicates that the Reply message was damaged during transmission and cannot be considered valid.

Bit 9, RDY, indicates that the Command message has been transmitted and either the Reply or turned around Command message has been received or the time-out period has elapsed. This bit is set by the occurrence of SHR.$\overline{\text{CMD}}$ (Serial Highway Ready and not Command). The state of SHR.$\overline{\text{CMD}}$ is also available via the Q test command, F(27).A(1).

Bit 10, XMR, indicates that the last byte of the Command message has been transmitted. This bit is used when operating in the pipeline mode. Refer to the Operating Procedure section of this manual for further information.

Bit 11, DMD, indicates that a Demand message has been received.

Bit 12, SERR, indicates that a SYNC error has occurred. In bit mode, this means that an improper configuration of start and stop bits has been detected for several bytes. In byte mode, this means that the received byte clock was missing for four bytes transmitted.

The LAM Status Register can be read with the F(1).A(12) command. It will be cleared by the F(11).A(12) command and can be selectively cleared by the F(23).A(12) command.

LAM Mask

The LAM Mask Register is used to determine which of the LAM Status bits will cause a LAM Request in the local crate. A LAM Status bit is masked "on" by setting the respective bit in the LAM Mask register. Four Dataway commands are available for accessing the LAM Mask register.

1) F(11).A(13) Clear LAM Mask
2) F(17).A(13) Write LAM Mask
3) F(19).A(13) Selectively set LAM Mask
4) F(23).A(13) Selectively clear LAM Mask

OPERATING PROCEDURES

MODES OF USE

Single Command Execution

The Single Command execution mode, specified by bits 15 and 16 of the Command register being zero, is generally used for executing random lists of commands and transferring blocks of data. Within this mode the user has the choice of two operating procedures, Conservative or Pipeline operation.

Conservative Operation

Conservative operating procedure implies that only one Serial Highway transaction will be taking place at one time; that is, after initiating a Command message transmission another will not be initiated until a Reply or Turned around Command message has been received or Time-out has occurred. This procedure allows the user to implement error recovery routines if a transmission error occurs during the transaction. Typically this procedure is used when executing random lists of commands. This procedure must be used when executing destructive Read commands, such as reading a FIFO memory.

Flowchart one details the procedure used when operating in the Single Command Execution mode. When following the Conservative operating procedure, the driving software will enter the flowchart at point A and leave via point D. When the exit condition is reached, SHR - Serial Highway Ready Flag true for polling software or RDY - Ready LAM set for interrupt-driven software, the user will determine whether the transaction was completed successfully and continue accordingly. Refer to the Operation Status section of this manual for further information.

Pipeline Operation

The Pipeline operating procedure implies that several Serial Highway transactions will be taking place at one time; that is, after initiating one Command message transmission another will be initiated as soon as the first has been sent; that is, do not wait for the Reply message. This procedure improves serial system throughput but denies the user the opportunity to recover from an error in a single transmission. This procedure is primarily used when transferring a block of data

to or from a memory in a serial crate. This procedure must not be used when executing destructive Read Commands, such as reading a FIFO memory.

Pipeline Operation, Write Block

Flowchart one details the procedure used when operating in the Single Command Execution mode. When writing a block of data using the Pipeline operating procedure, the software sequencer will follow flowchart one in the following manner. Initial entry will occur at point A, establishing the CAMAC command and address. Software will loop between points B and C, initiating Write Command messages and waiting until the message transmitter is ready, until the write data block has been exhausted. Also, software must count the Reply messages and check to see that no errors have occurred. (See Operation Status section of this manual.) If any Reply messages are missing or any transmission errors detected, the entire block must be retransmitted.

Pipeline Operating, Read Block

When reading a block of data using the Pipeline operating procedure, the software will follow flowchart one in the following manner. The software will loop between points A and C, initiating Read Command messages and waiting until the message transmitter is ready until a predetermined number of Read Commands have been sent. Also, the user must count the Reply messages and store the read data as replies are received. If any replies are missing or any transmission errors detected, the entire operation must be repeated.

In some cases the use of the F(16).A(2) command to write the lower 16 bits of the Command register will improve system throughput when executing a group of commands in the same serial crate.

MR - Repeat Command Mode

The Repeat Command Mode, specified by bit 15 being one and bit 16 being zero in the Command register, is generally used for reading a block of data. By definition, this mode operates using the conservative procedure.

Read Block

Flowchart two details the procedure used when operating in the MR - Repeat Command Mode. When operating in this mode, the software sequencer will follow flowchart two in the following manner. Initial entry will occur at point A. First, the CAMAC command and address to be used while in the repeat mode are loaded in the Command register. The repeat mode is specified by setting bit 15 to one in the Command register. Serial Write commands cannot be used in this mode. If a Write command is loaded in the Command register, the 3992 will wait for write data at B, and the software sequencer will never find SHR or RDY at D. If a Read or Control command is loaded in the Command Register, the 3992 will format and transmit the serial Command message specified in the Command Register. The software sequence will detect SHR, for polling software, or RDY, for interrupt-driven software, when the Serial Highway transaction has been completed. The user must check transaction status. (For further information, refer to Operation Status section of this

manual.) If no error occurred, the serial read data should be read using the F(0).A(0) command and stored. In the MR - Repeat Command Mode, the F(0).A(0) command will initiate another Command message transmission by the 3992.

There are two types of transfers which this mode will be used for, Q Stop transfers and Word Count transfers.

Q Stop

The Q Stop procedure is used for reading blocks of unknown length. Typically, this procedure is used when reading a FIFO memory which will respond with a Q Response of zero when the FIFO is empty. When using this method, the operation is terminated by leaving the sequence via E after detecting a serial Q Response of zero.

Word Count

The Word Count procedure is used for reading blocks of known length. When the last Serial Highway transaction has been completed, the software sequence indicates that the Command register is loaded with a 'dummy' write command specifying Single Command Execution mode. Write data is <u>not</u> loaded. This allows the Read Data register to be read without initiating another Command Message transmission.

<u>MQ - Q Scan Mode</u>

The Q or Address Scan mode, specified by bits 15 and 16 of the Command register being one, is used for transferring data from an array of CAMAC modules to the 3992. This mode provides an efficient method for reading a group of similar modules. Typically, it is used for retrieving data from a group of multichannel modules, such as A/D converters or counters. The user specifies the CAMAC Read Function code to be used, F(0) through F(7), the address of the serial crate the scan will be executed in and the initial Station Number and Subaddress and the mode in the Command register.

The Address Scan

During the Address Scan operation, the 3992 uses the Q Response from the previous command to determine the station number and subaddress in the current station has been read. The 3992 responds to a Q Response of zero by incrementing the station number and resetting the subaddress. A Q Response of one indicates that the data from the last command was valid and should be stored. The 3992 responds to a Q Response of one by incrementing the Subaddress, or, if the Subaddress was 15, it is reset to zero and the Station Number is incremented. If, due to a programming error, the 3992 increments the Station Number to 32, the Serial Crate Address will be reset, and the next Command message transmitted will not be accepted by any Serial Crate, resulting in an error.

Procedure

Flowchart three details the procedure followed for Q Scan operation. Initial entry is made at A. The Read Function Code, Serial Crate Address and mode specification are loaded in the Command register along with the initial Subaddress and Station

Number. When the serial transaction has been completed, the 3992 sets the SHR flag and RDY LAM Status bit. The user must check the operation status to determine whether an error has occurred. If no error occurred and this is not the last transfer, the read data will be read using the F(0).A(0) command. When in the Q Scan mode, the F(0).A(0) command will cause the 3992 to update the Station Number and Subaddress and initiate a new serial Command message transmission.

If the Q Response to the read was one, the data read was valid and should be stored. If the Q Response was zero, the data is not valid and should be ignored. The serial Q and X Responses are sent on crate Q and X Buses when an F(0).A(0) to the 3992 station is executed.

If no error has occurred and the Reply to the last transfer has been received, a 'dummy' write command should be loaded in the Command register. The 'dummy' command specifies Single Command Execution mode. Write data is <u>not</u> loaded, so that command is not executed. This allows the Read data register to be read with the F(0).A(0) without initiating another serial Command message transmission.

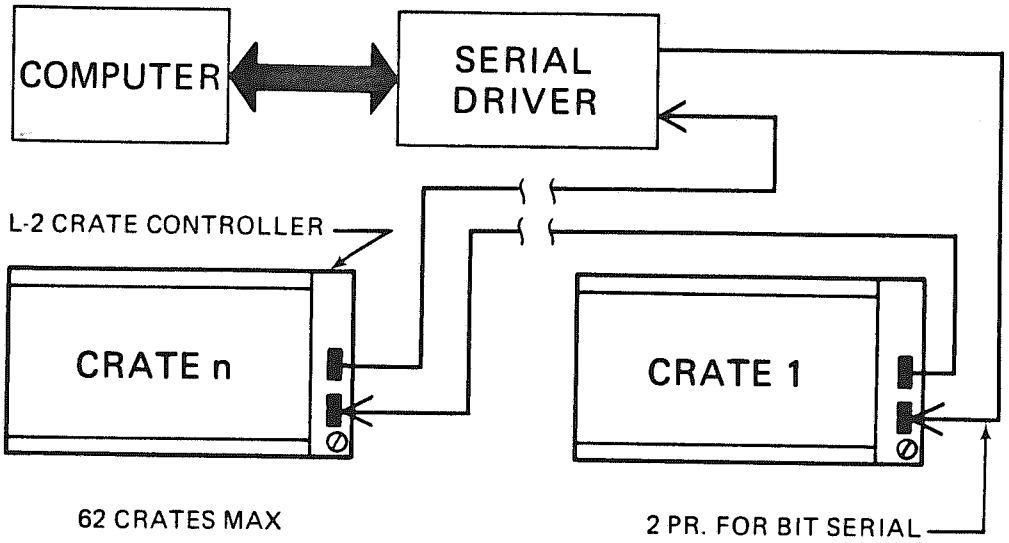


Figure 1 -- Typical CAMAC Serial Highway

Clock Rate	Bit Serial	Byte Serial
100K	1200 μs	120 μs
250K	520 μs	52 μs
500K	220 μs	25 μs
1M	130 μs	14 μs
2.5M	52 μs	6 μs
5M	26 μs	3.7 μs

Figure 2 -- Message Length Vs. Clock Rate

These are undefined ports - - not fixed by CAMAC specification.

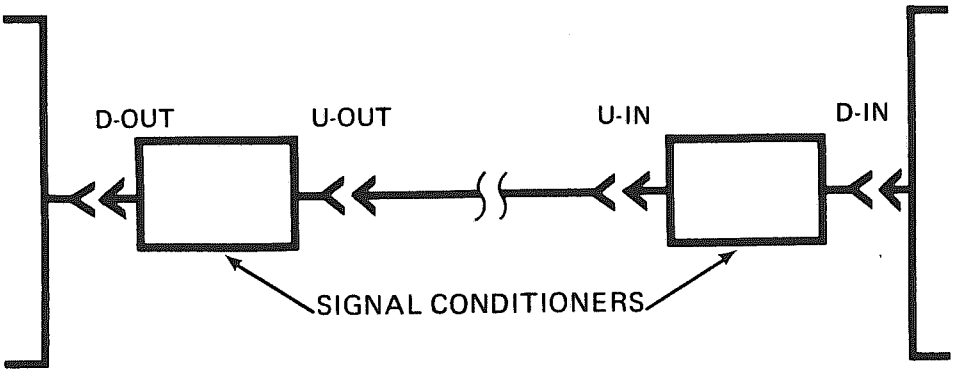


Figure 3 -- U-Port Signal Conditioners

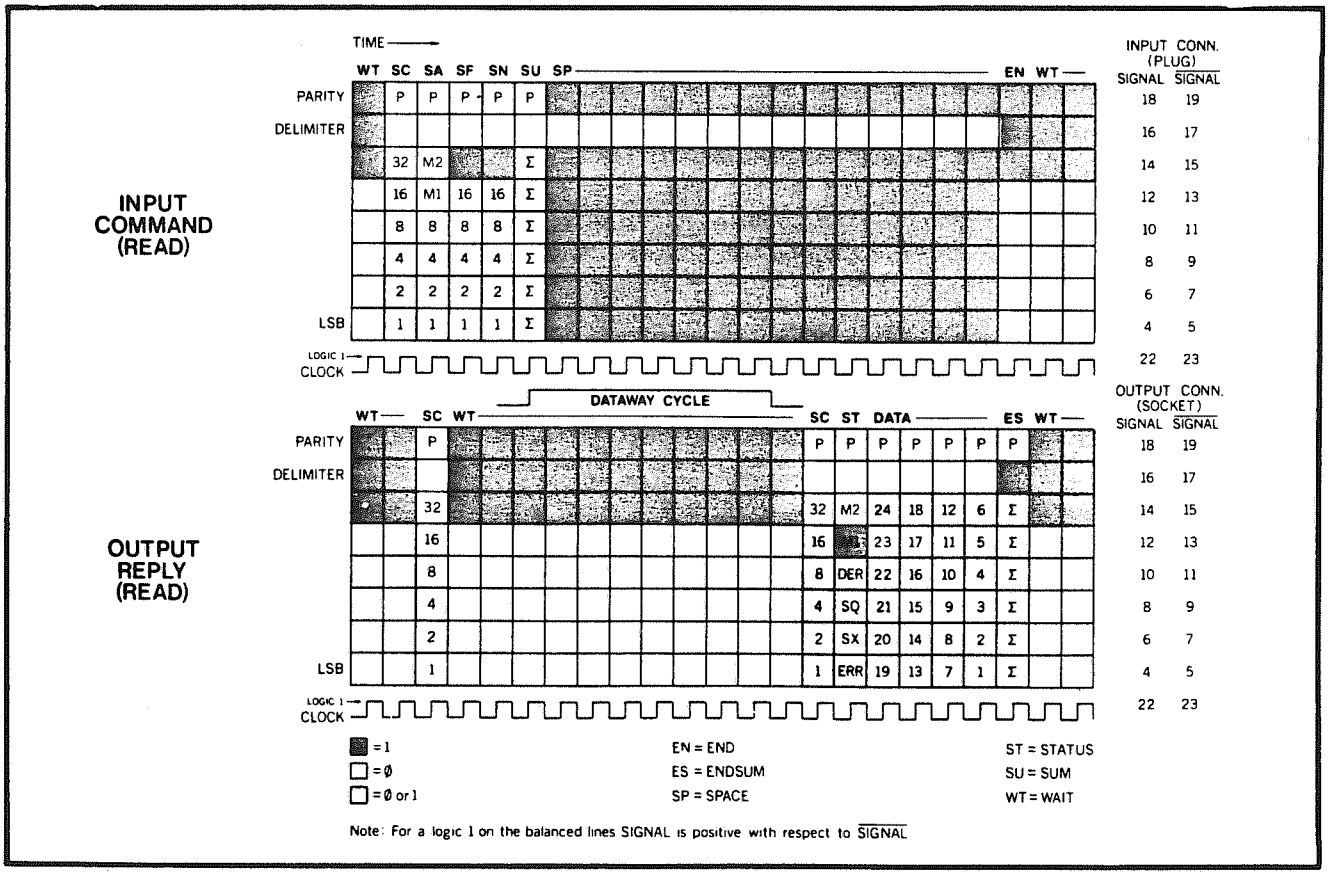
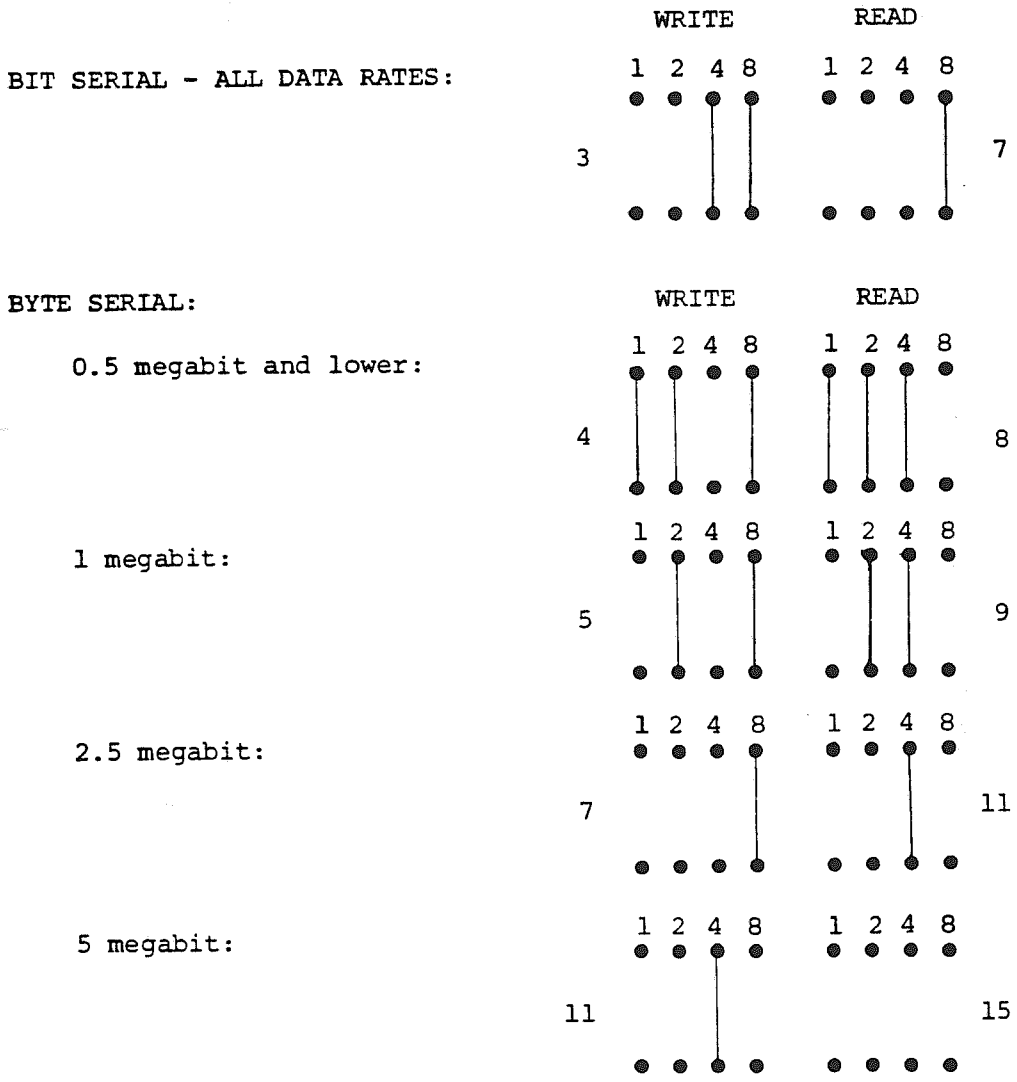


Figure 4 -- Command Reply Sequence



Notes:

1) Remove ground shield on 3992 (right side of module) to access straps.

2) Selection is made (binary bit TRUE) by removal of strap.

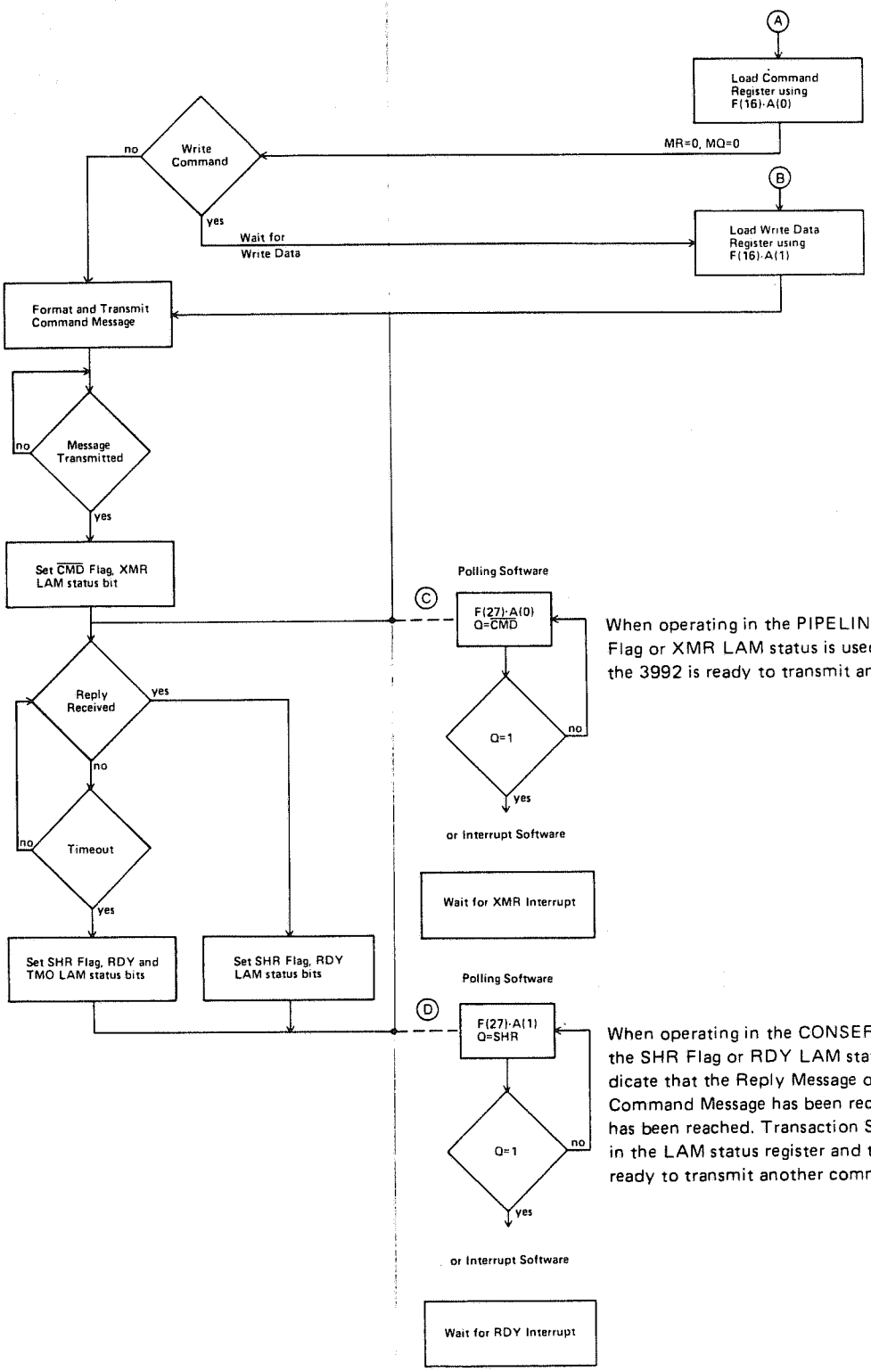
3) System will work properly with too many space bytes; however, message will be longer than needed.

4) For margin of safety, one more space byte than specification minimum is shown for byte serial operation.

Figure 5 -- Space Byte Selection

3992 Hardware Sequence

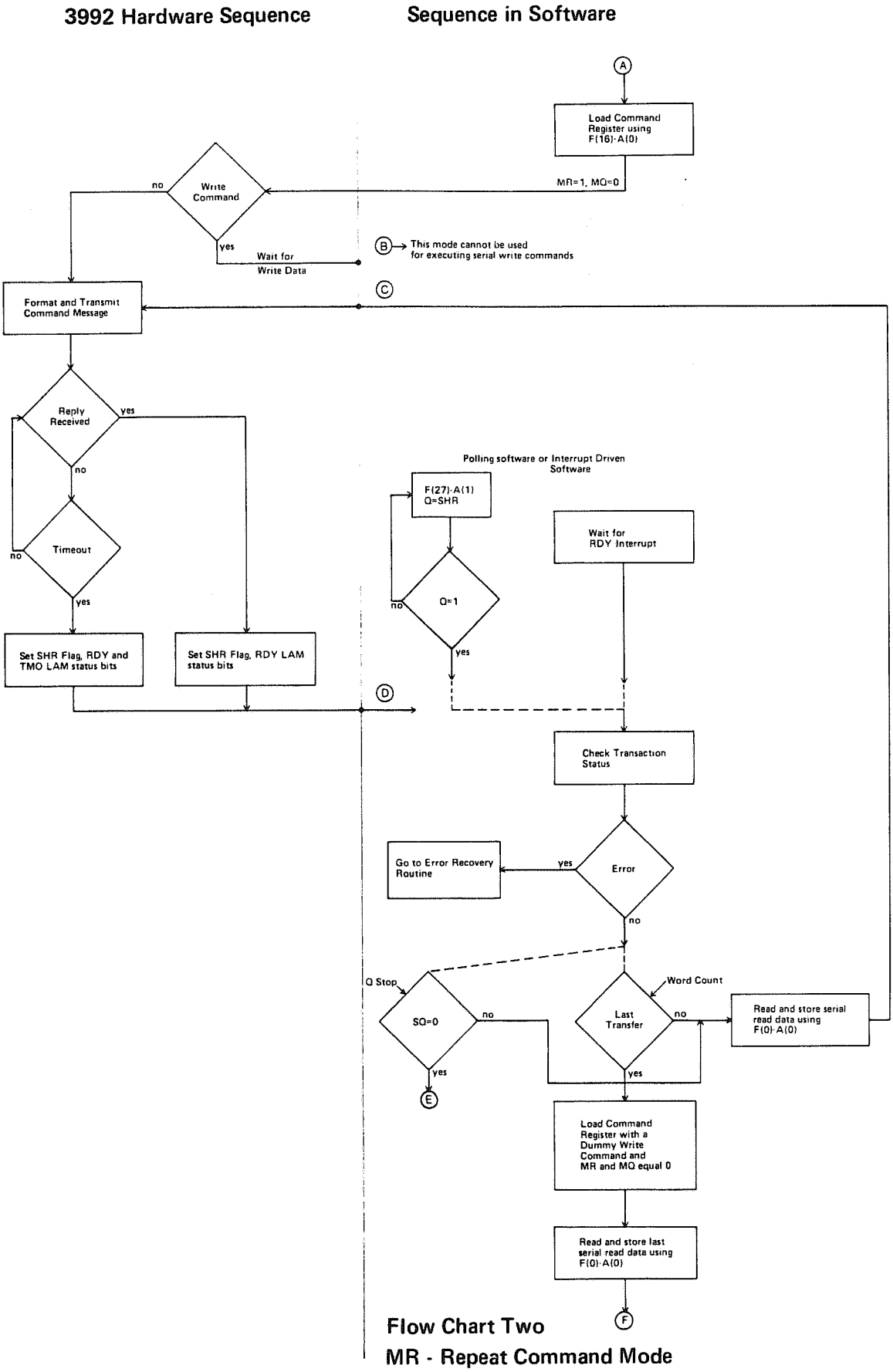
Sequence in Software



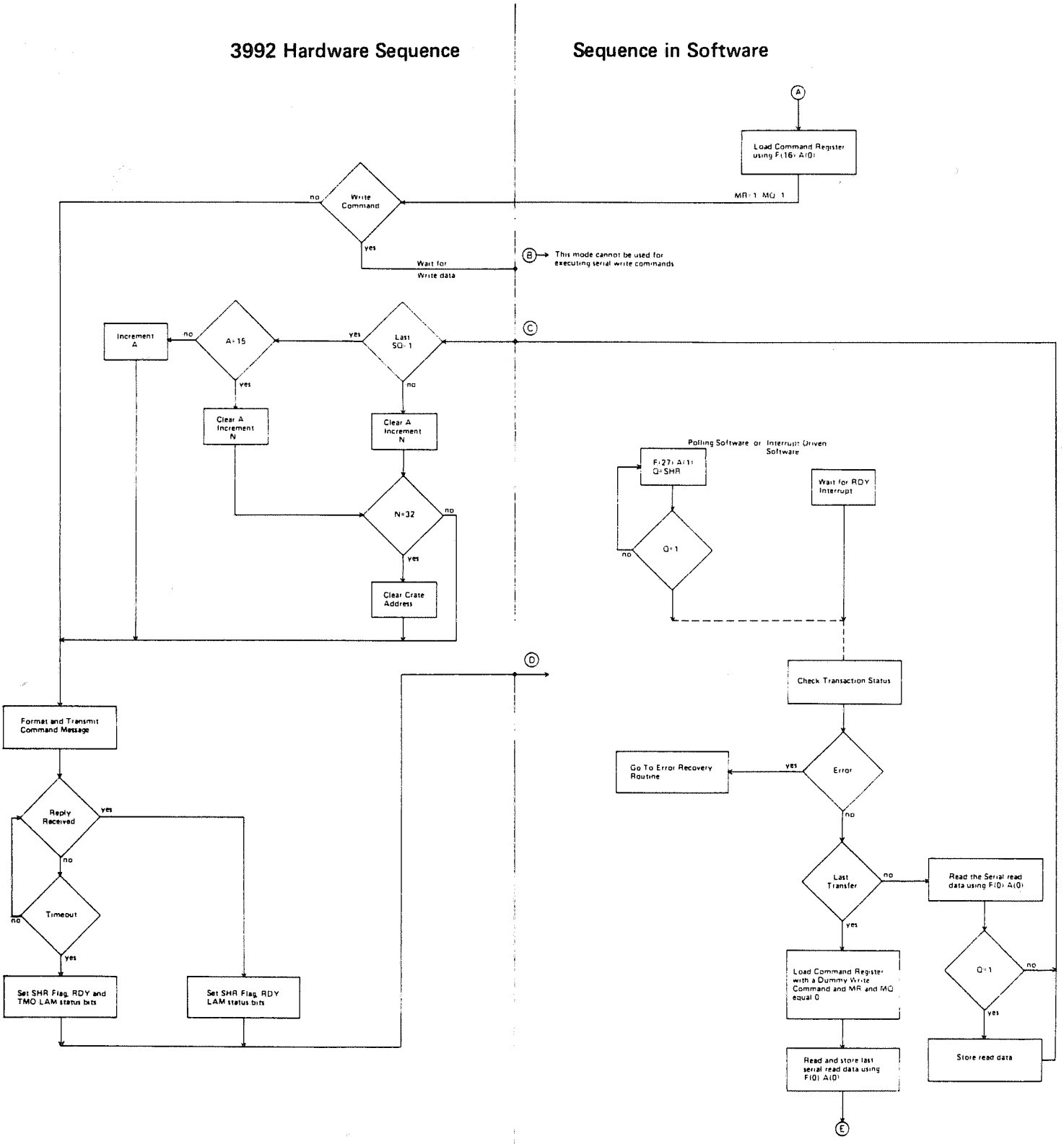
When operating in the PIPELINE mode the $\overline{CMD}$ Flag or XMR LAM status is used to indicate that the 3992 is ready to transmit another command.

When operating in the CONSERVATIVE mode the SHR Flag or RDY LAM status is used to indicate that the Reply Message or Turned around Command Message has been received or Timeout has been reached. Transaction Status is available in the LAM status register and the Driver is ready to transmit another command message.

Flow Chart One
Single Command Execution using the Model 3992



Flow Chart Two
MR - Repeat Command Mode



Flow Chart Three
MR - MQ Q Scan Mode

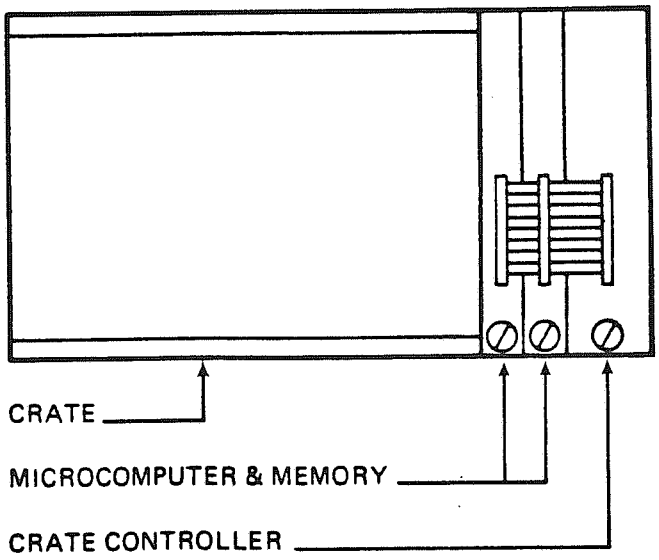
APPENDIX A

CAMAC Computer Interface Alternatives

1. Microcomputer in crate
2. Use of computer interface bus
3. CAMAC parallel branch highway
4. CAMAC serial highway

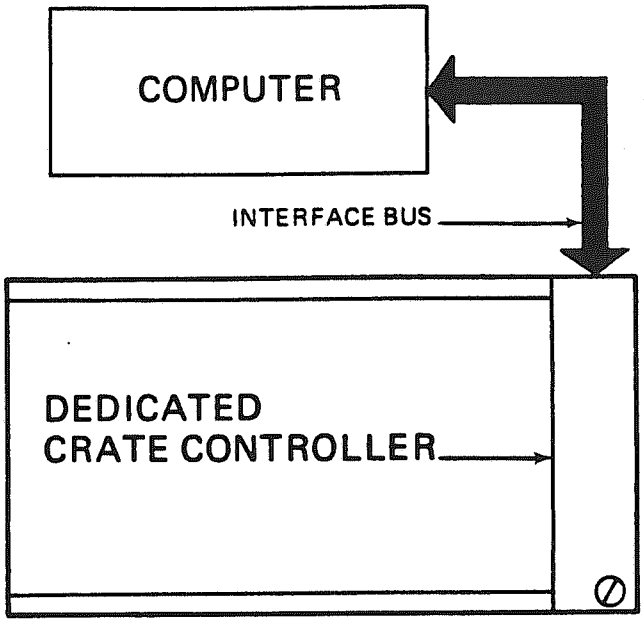
1

Microcomputer in Crate



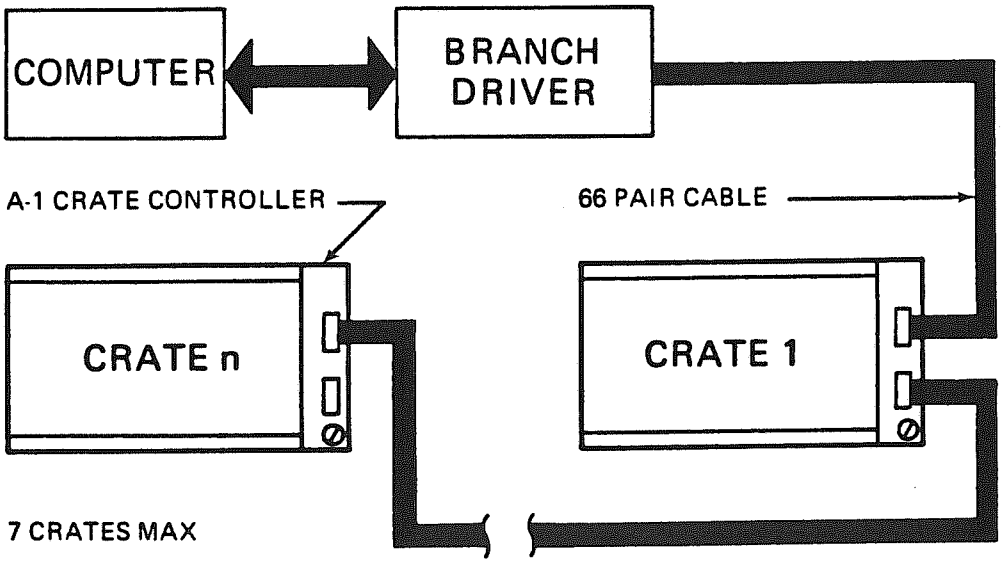
2

Use of Computer Interface Bus



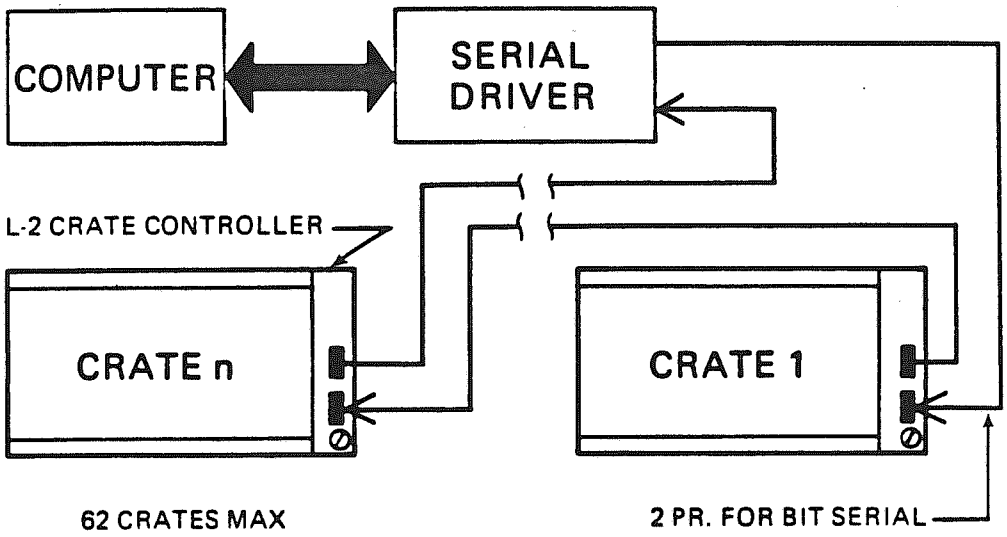
3

CAMAC Parallel Branch Highway



4

CAMAC Serial Highway



5

Features of the CAMAC Serial Highway System

1. It can support up to 62 crates on one loop.

2. Distance between crates is limited only by the transmission media used.

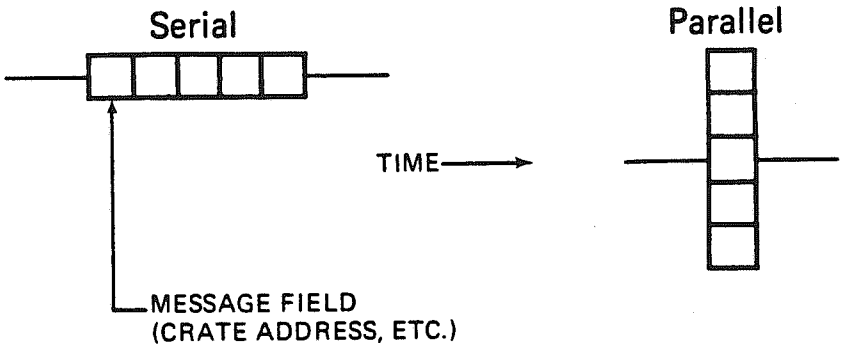
3. It can operate in very noisy environments.

4. Messages can be sent very rapidly.

6

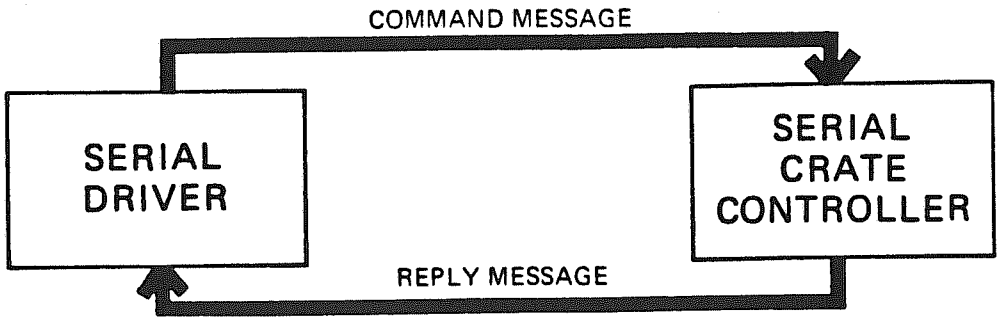
Why is it called a "serial" highway?

Because the message fields are sent one-by-one in sequence.



7

Message Path around the Loop



8

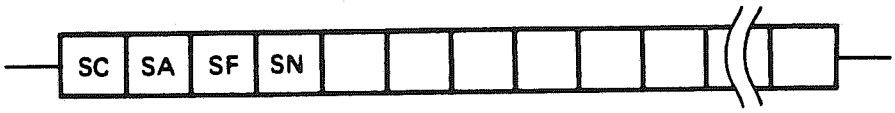
Fields in a Command Message

SC - - Serial crate to be addressed (1 to 62)

SA - - Subaddress of command to module (0 to 15)

SF - - Function code of command to module (0 to 31)

SN - - Slot number of remote module (1 to 31)



9

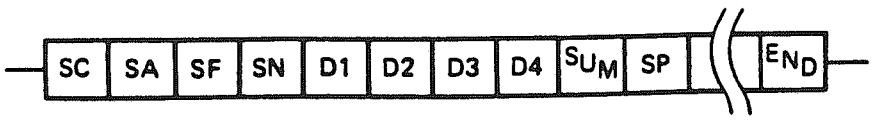
Command Message Fields - - - - continued

DATA - - If Write command, three fields (24 bits)

SUM - - Column parity check field

SPACE - - Makes space for reply message

END - - Indicates end of message



10

Fields in a Reply Message

SC - - Serial Crate that was addressed

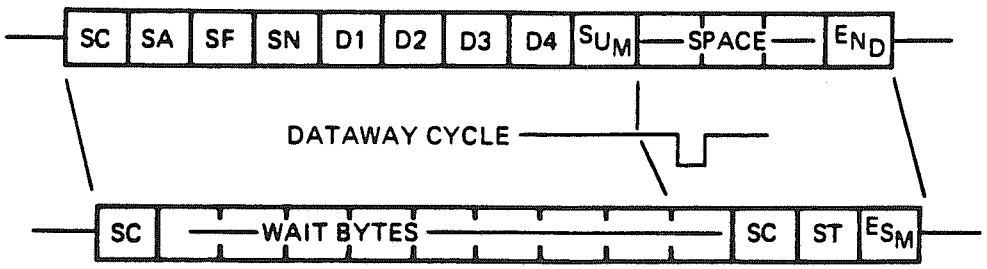
STATUS - - Q, X and error status

DATA - - If Read command, four fields (24 bits)

ENDSUM - - Column parity and end of Reply

11

Command/Reply Relationship (Write Command)



12

How are the Message Fields Subdivided?

Each message field is an 8-bit byte.

For example, the SC field:

Bit	Use
1	SC1
2	SC2
3	SC4
4	SC8

Bit	Use
5	SC16
6	SC32
7	Delimiter
8	Parity

13

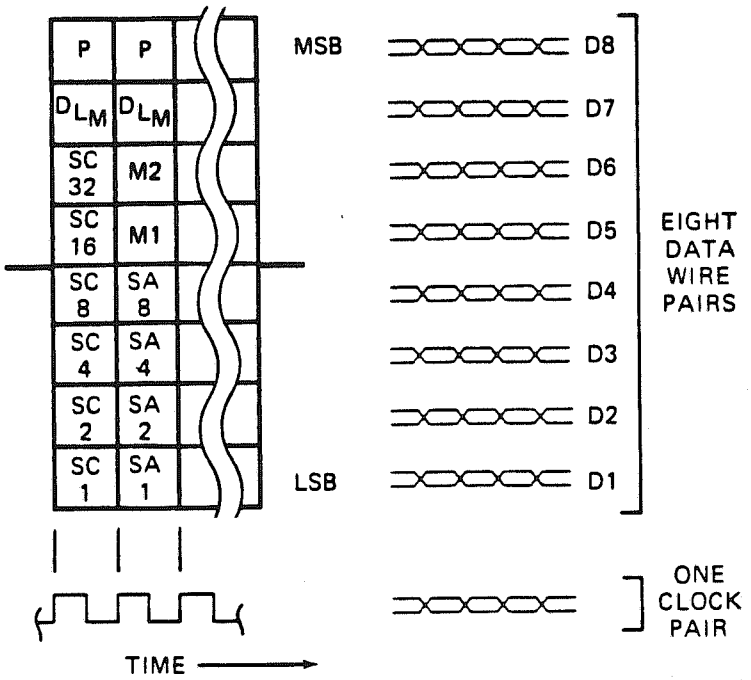
How are the Message Fields Transmitted?

1. Byte serial - - **each 8-bit byte** is transmitted "all bits at once".

2. Bit serial - - **each bit** in a byte is transmitted one-at-a-time.

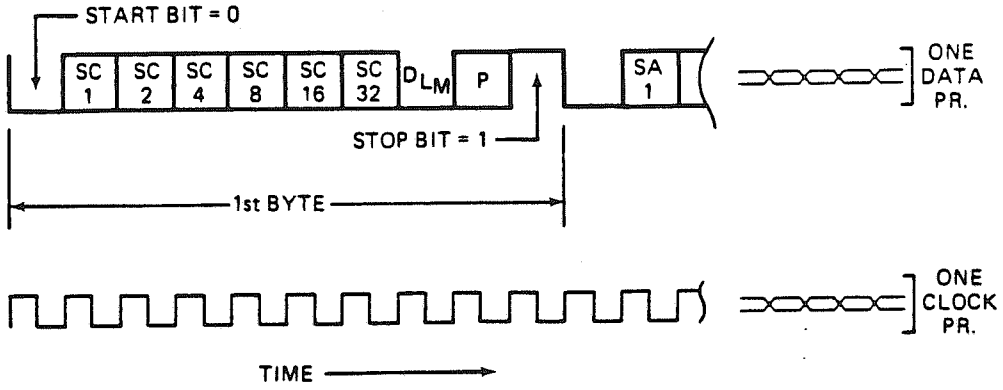
14

Byte Serial Transmission



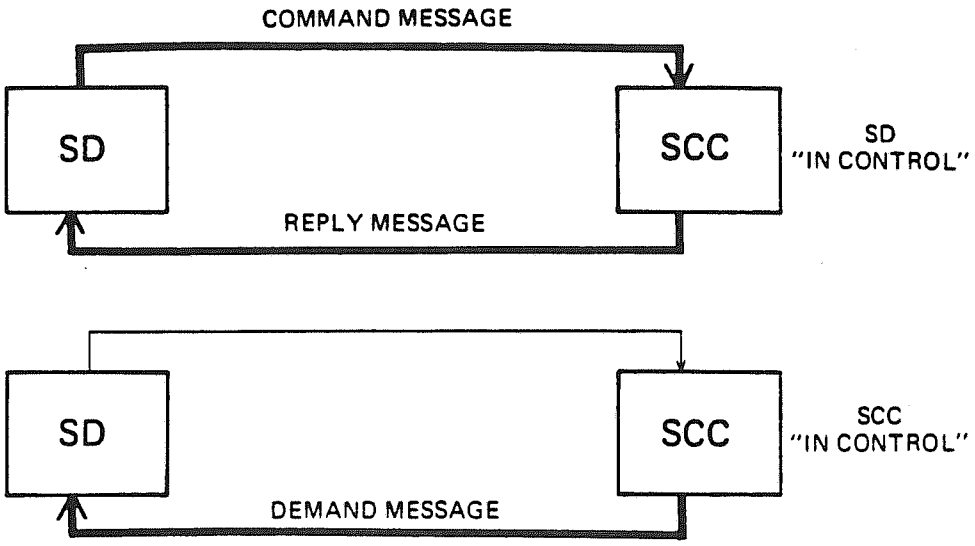
15

Bit Serial Transmission



16

Another Message Type, the Demand Message



17

Demand Message Details

A Demand Message is sent as a "request for action" from a LAM becoming true.

Demand Message fields (bytes):

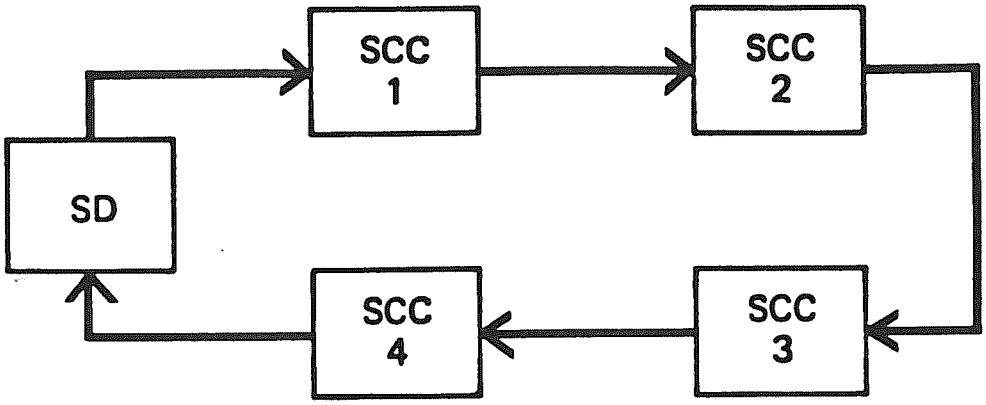
SC - - Serial Crate generating the Demand

SGL - - Serial Graded L field

ENDSUM - - Column parity and end of Demand

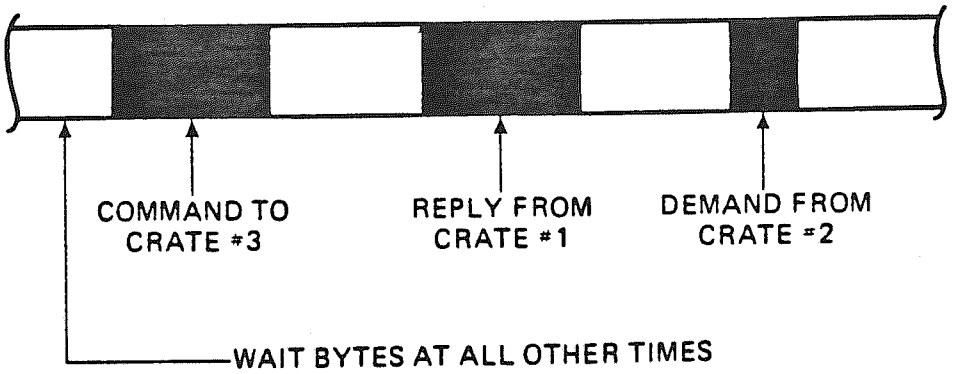
18

Command/Reply Path in a Multi-crate System



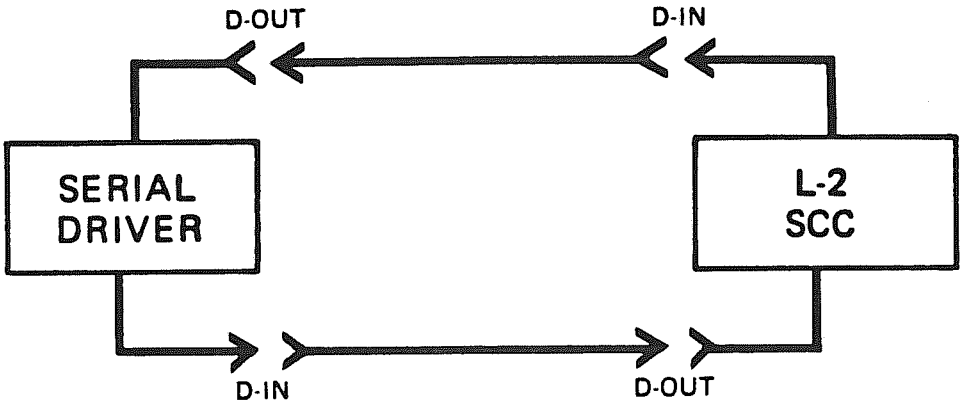
Crate #3 is addressed, others are "transparent".

Highway Traffic between Crates #2 and #3



How are the serial driver and serial crate controllers connected in a system?

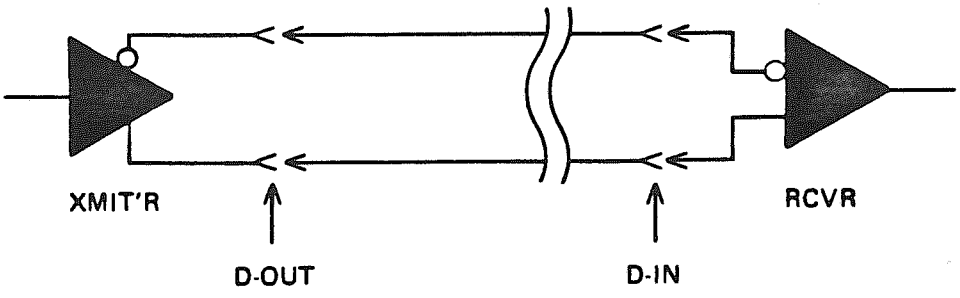
The simplest connection is called "D-Port".



21

What are the signals like?

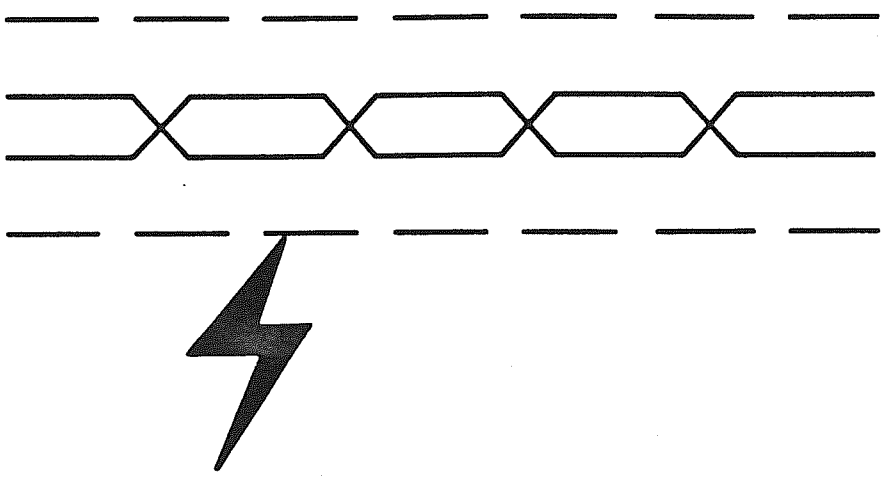
Clock and data are each RS-422 balanced signals.



22

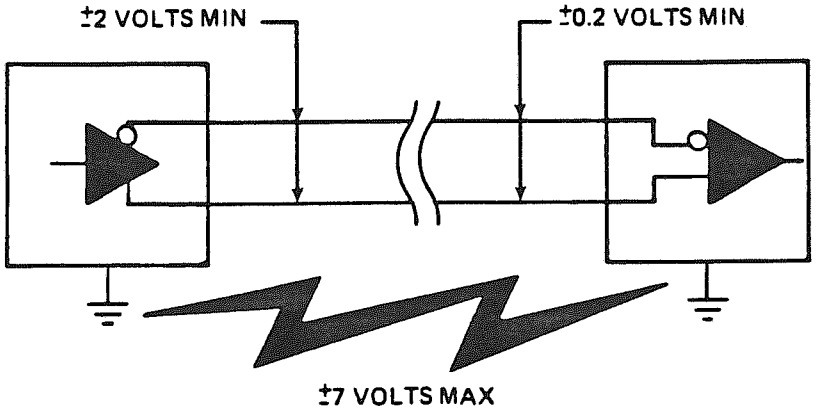
What kind of cable should be used?

The cable should be twisted pair with shield grounded at both ends.



23

What are the characteristics of serial highway signals?

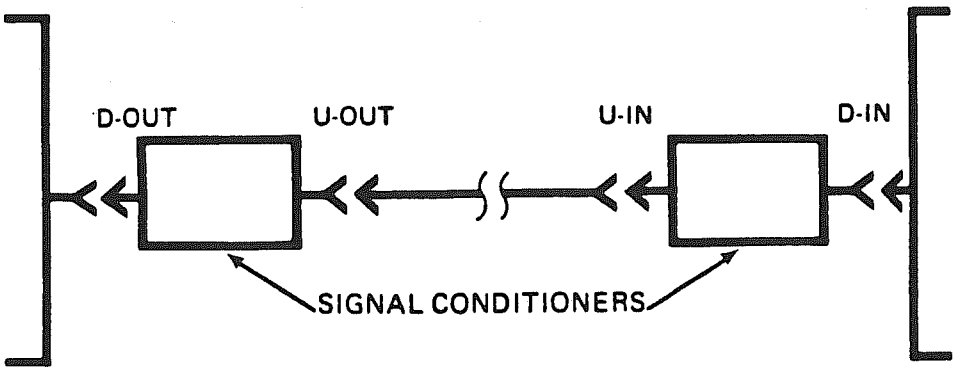


Also, a clock rate from zero to five megabits per second.

24

What are U-Ports?

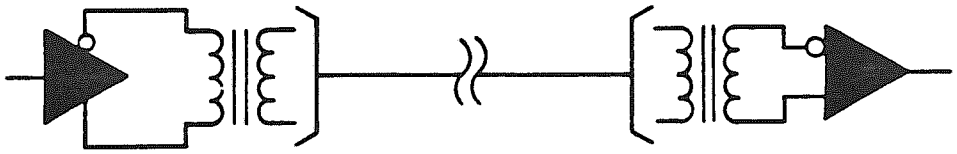
These are undefined ports - - not fixed by CAMAC specification.



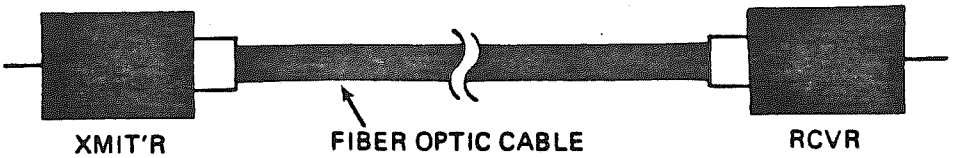
25

What are the basic types of U-Port adapters?

1. Transformer isolated:

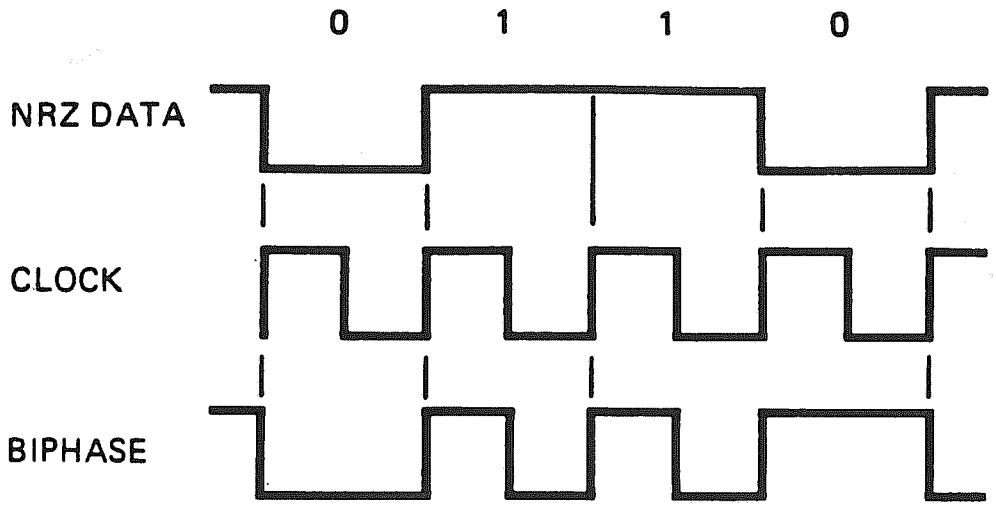


2. Fiber optic:



26

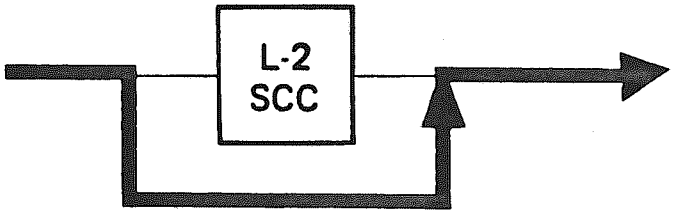
How are clock and data sent over one path?



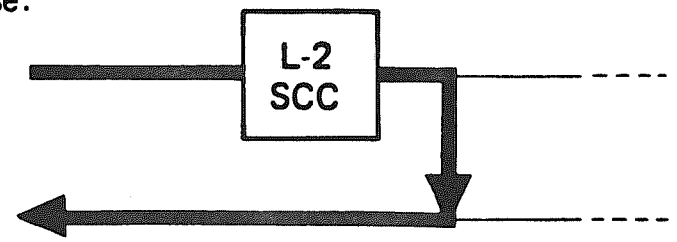
27

What are other features of transformer-type U-Port adapters?

1. Bypass:



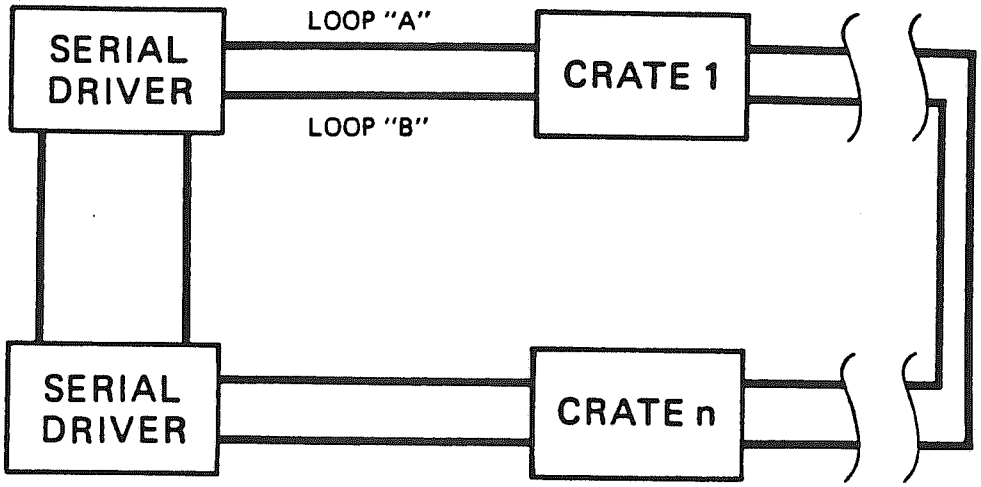
2. Loop Collapse:



28

Features of transformer-type U-Ports (continued)

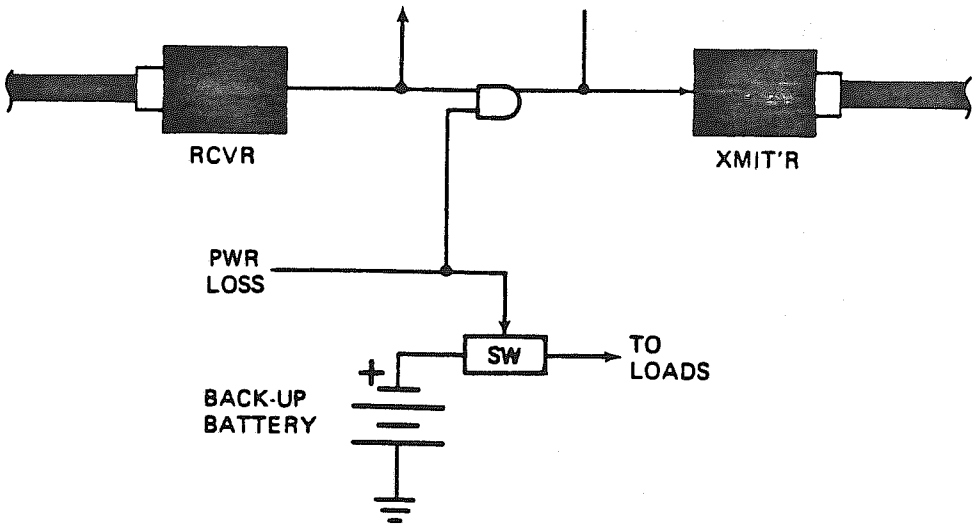
3. Dual-computer and/or dual-loop:



29

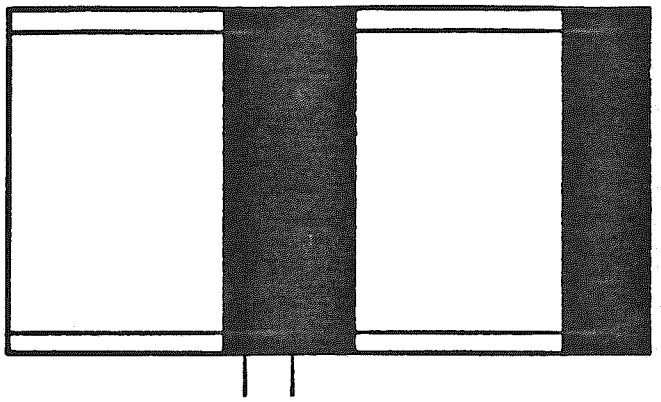
What are other features of fiber optic U-Ports?

Battery backup:



30

Serial Driver Modules for General Use



The KSC Model 3992 is a serial driver and also a module in "main" crate.

The 3994 can be used to provide block transfers.

How does clock rate relate to message rate?

Clock Rate	Maximum Messages per sec	
	Bit Serial	Byte Serial
1M Bit	7,500	73,000
2.5M Bit	15,000	130,000
5M Bit	30,000	250,000

For a system with 10 remote crates and a 1000 ft. loop (5M Bit clock), max. rate is 28,000 and 125,000.

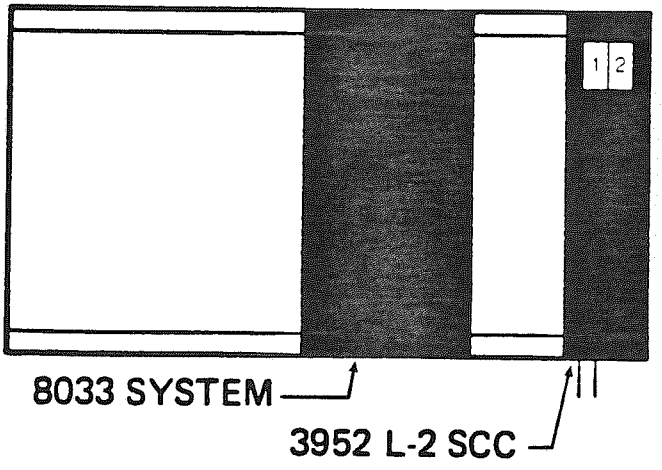
How long can the serial highway be?

Clock Rate	Wire Cable		Fiber Optic
	22ga.	18ga.	
1M Bit	250m	1000m	1000m
2.5M Bit	140m	500m	1000m
5M Bit	70m	250m	500m

The above assumes the following:

1. Distance is between "repeats".
2. Distance is for U-Port adapters; reduce to 60% for D-Port.
3. Cable types: 22ga. is 5800/5801; 18ga. is RG-22; Fiber optic is 5802.

How is Remote Intelligence provided?



L-2 SCCs support auxiliary crate controllers with their associated computers.

DEMAND HANDLING IN THE CAMAC SERIAL SYSTEM

The Type L-2 Serial Crate Controller (SCC) has the ability to alert the Serial Highway Driver (SHD) that a CAMAC LAM (look-at-me) is pending by asynchronously generating and transmitting a Demand message on the serial highway.

This ability allows serial systems to have certain operations interrupt driven as opposed to polled. The Demand message is unique with respect to all other serial highway messages since it is the only one which is not generated by the SHD, or as a result of a message from the serial highway driver.

The Demand Message

The Demand message transmitted by the serial crate controller uses the following format:

Byte #	Bit:	8	7	6	5	4	3	2	1
1		T	0	C32	C16	C8	C4	C2	C1
2		T	0	1	SG16	SG8	SG4	SG2	SG1
3		T	1	LE	LE	LE	LE	LE	LE

Byte One

Bits one through six of byte one indicates which SCC (1 through 62) transmitted the demand message. Bit seven, the delimeter bit, is set to zero to indicate this is a message byte. Bit eight is set to one or zero to maintain an odd number of one's in byte one.

Byte Two

Bits one through five of byte two are the Serial Grader LAM (SGL) bits. The meaning of the SGL bits depends on how the serial crate is configured. When the SCC is used in conjunction with a LAM Graded (KSC Model 3924) these bits will indicate the slot number (1 through 24) of the highest priority LAM pending. Bit six, the message identifier bit, is set to one to indicate that this is a demand message. Bits seven and eight have the same meaning as in byte one.

Byte Three

Bits one through six are set to one or zero to maintain an even number of one's in their respective columns. Bit seven is set to one indicating that this is the last byte of the message. Bit eight is set to one or zero to maintain an odd number of one's in byte three.

The "HUNG" Demand Message

Since demand messages are generated asynchronously by the SCC provisions are made for the case where a demand message has been transmitted, corrupted in transmission and therefore ignored by the SHD. The repeat timer on the SCC allows selection of a nominal delay between transmission of the initial demand message and transmission of the "hung" demand message. This delay is strap selectable. A nominal time delay of 1 msec, 10 msec, 100 msec or 10 seconds may be selected. A "hung" demand message is differentiated from a normal demand message by setting all of the SGL bits in byte two of the demand message to one. The repeat timer may be disabled.

The SGL Encoder Connector

The SCC may be configured for stand-alone demand message generation by appropriately "patching" the SGL Encoder connector on the back of the Type L-2 SCC.

These patches may be incorporated using the 5942-Z1A connector included with the Model 3952 SCC or optionally on a Model 2010 SGL Adapter.

The signals present on the SGL Encoder connector are listed in the table below.

SGL-ENCODER CONNECTOR

Contact	Signal	Direction	Contact	Signal	Direction
1	Demand Busy	Out	2	L1	Out
3	SGLE1	In	4	L2	Out
5	SGLE2	In	6	L3	Out
7	SGLE3	In	8	L4	Out
9	SGLE4	In	10	L5	Out
11	SGLE5	In	12	L6	Out
13	External Repeat	In	14	L7	Out
15	——		16	L8	Out
17	——		18	L9	Out
19	Time-out	Out	20	L10	Out
21	Demand Message Initiate	In	22	L11	Out
23	Start timer	In	24	L12	Out
25	Selected L's present	In	26	L13	Out
27	——		28	L14	Out
29	Auxiliary Controller Lockout	Out	30	L15	Out
31	Byte Clock	Out	32	L16	Out
33	——		34	L17	Out
35	——		36	L18	Out
37	——		38	L19	Out
39	——		40	L20	Out
41	SCC Busy	Out	42	L21	Out
43	N1	In	44	L22	Out
45	N2	In	46	L23	Out
47	N4	In	48	L24	In/Out
49	N8	In	50	L-SUM	Out
51	N16	In	52	Gnd	——

The even contacts between 2 and 48, inclusive, provide access to dataway LAM lines L1 through L24. The 24 LAM lines provide each individual slot with the ability to interrupt the SCC. L24 may be set by bit 10 of the SCC status register providing a means of testing the demand handling process.

Contact 50, L-SUM, is the logical "OR" of all of the LAM lines.

Contacts 3, 5, 7, 9, 11, SGLE-1 through SGLE-5, provide the contents for the five-bit SGL field in byte two of the DEMAND message.

Contact 21, Demand Message Initiate, DMI, initiates the generation of a DEMAND MESSAGE at a 0 to 1 transition. This assumes all other necessary conditions are met. These conditions are discussed later in the text.

Contact 25, selected L's present controls bit 16 of the SCC status register. Meaning of this bit will depend on serial crate configuration.

The signal on contact 1, Demand Busy, is generated by the SCC and used by the LAM Grader, if present, to staticize SGLE 1 - SGLE 5 during demand message generation.

Contact 13, External Repeat, must be asserted by the LAM Grader to generate a "hung" demand message. This signal is used by separate LAM Graders only.

Contact 31, Byte Clock, is provided for use by external LAM Graders.

Contact 23, Start Timer, is used to control the repeat timer in the SCC. This signal is used when "hung" demand message generation is desired.

Contact 19, Time-Out, is the output from the repeat timer in the SCC. This signal may be used to initiate "hung" demand message generation.

Contact 41, SCC Busy, provides a signal which indicates the SCC is engaged in a Command/Reply transaction.

Contacts 43, 45, 47, 49 and 51, N1 through N16, are used by separate auxiliary crate controllers to provide the N field of a dataway command.

Contact 29, Auxiliary Controller Lockout, indicates the SCC requires use of the dataway. This signal is used in multiple crate controller configurations.

Patching The SGL Encoder Connector For Stand-Alone Use

The following connections allow the SCC to generate demand messages.

1. Connect contact 50, L-SUM to contact 23, Start Timer.
2. Connect contact 19, Time-Out to contact 21, Demand Message Initiate.

These connections will cause the SCC to generate a Demand message when demands are enabled (bit 9 in the SCC status register set to one) and a transition from the state of L-SUM false (no LAMs pending) to L-SUM true (one or many LAMs pending) occurs.

If L-SUM is true when bit 9 in the SCC status register is set to one a demand message will be generated.

If the repeat timer on the SCC is disabled no more demand messages will be transmitted until either bit 9 in the SCC status register is cleared and set (disabling and re-enabling demand generation) or all pending LAMs are cleared, thereby setting L-SUM false.

If the repeat timer is enabled the normal demand message will be generated when L-SUM initially goes true and hung demand messages will be generated at the selected rate if L-SUM does not go false (all LAMs cleared) before the repeat timer times out. No hung demand will be generated if L-SUM goes false before time-out occurs. If time-out does occur hung demands will continue to be generated at the repeat timer interval until L-SUM goes false or bit 9 of the SCC status register is set to zero, disabling demands.

Additional connections are required to define the contents of the SGL field in the demand message. It is necessary to connect a single LAM line (L1-L24) to each of the five SGLE lines which the user wishes to define. Any SGLE line not connected will result in a zero being transmitted in that bit position. It should be noted that if all five are used a situation where all five LAMs go true together will result in a demand message which appears to be a hung demand.

The fact that only five LAMs can be patched into the SGL field does not limit the user to five modules which can source LAM interrupts. If a LAM which is not patched into the SGL field occurs a demand message with all SGL bits set to zero will be generated. To determine which LAMs are pending at any time an F(1) A(12) N(30) command may be used to read the state of the twenty-four LAM lines.