Model 4022/4054

8-64 Channel Transient Recorder

INSTRUCTION MANUAL

April, 1992

Model 4022-S001

*** Special Option ***

April 1987

Special Option

Model 4022-S001

The 4022-S001 is a 4022-M1A with the input connectors for channels one through four implemented as isolated, single pin LEMO type connectors (shell size "00"). The positive leg of the input signal is connected to the center pin of the LEMO, and the negative leg of the input signal is tied to the connector shell.

April 1987

*****Special Option*****

Model 4022-S003

8 to 64-channel Transient Recorder

April, 1996

SPECIAL OPTION

Model 4022-S003

The Model 4022-S003 is the same as the 4022-M1A except this option has strap selection and overall offset trimmed for an input range of ±5V.

CONTENTS

TABLES

FIGURES

KineticSystems Corporation

Standardized Data Acquisition and Control Systems

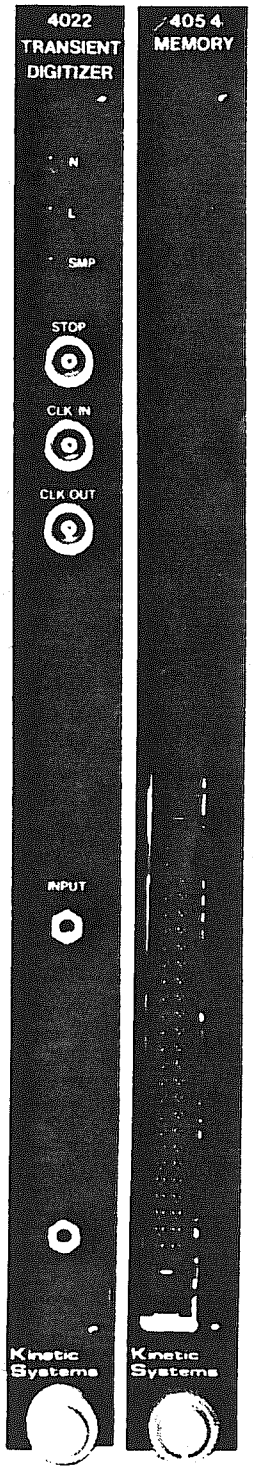
4022/4054

8 to 64-channel Transient Recorder

(Rev. 12/93)

FEATURES

- Twelve-bit resolution
- Sample rates to 250 kilosamples per second (one active channel)
- Eight input channels, expandable to 64 with eight 4022s
- Active channels are programmable from the Dataway
- Options available with 'D' or 2-pin LEMO input connectors
- Excellent dynamic accuracy
- Differential input for common-mode rejection
- Up to four megasamples with one memory module
- Memory expandable to sixteen megasamples
- Active memory size is programmable down to two kilosamples
- Memory data in offset binary or two's complement
- Memory readout at full Dataway speed
- Direct readout for "present value" monitoring
- Pretrigger, post-trigger intervals are programmable
- Programmable selection of internal clock (5 hertz to 250 kilohertz)
- External clock input connector



GENERAL DESCRIPTION

The Models 4022 and 4054 are each single-width CAMAC modules. The 4022 is an 8-channel transient digitizer containing a 12-bit ADC, a multiplexer, and eight track/hold amplifiers for simultaneous sampling. The recorder can be expanded to 64 channels by using eight 4022s.

The maximum sampling rates per channel for all combinations of number of active channels and number of interconnected 4022s are shown below:

Maximum Sampling Rates

Active Channels	Number of 4022s			
	1	2	4	8
1	250 KHz	250 KHz	200 KHz	140 KHz
2	125 KHz	125 KHz	110 KHz	90 KHz
4	62.5 KHz	62.5 KHz	55 KHz	50 KHz
8	31.25 KHz	31.25 KHz	30 KHz	28 KHz

The 4054 is a high-capacity memory module with memory size options of one, two, or four megasamples. Up to four 4054s can be connected to one transient recorder, giving a total memory capacity of sixteen megasamples. For smaller memory requirements, a 4050 memory module may be substituted for the 4054. However, 4050 and 4054 modules may not be used together in a system.

(continued on following page)

11 Maryknoll Drive • Lockport, IL 60441 • (815) 838 0005 • TWX 910 638 2831 • FAX (815) 838 4424

GENERAL DESCRIPTION *(continued)*

The input signal for each channel is received on a 2-pin LEMO connector (4022-M1A) or for all channels on a 25-contact 'D' connector with sockets (4022-D1A). The sample rate is controlled by a programmable internal clock that is selectable from 5 hertz to 250 kilohertz or by an external TTL-level clock connected to a front-panel LEMO connector. A clock-out LEMO connector is provided.

The pretrigger and post-trigger sample sizes are programmable. The Stop (event trigger) LEMO connector accepts a TTL-level signal. When an event trigger pulse is received, the recorder continues sampling until the end of the post-trigger period is reached. A LAM can be set at that time.

For each 4054 the amount of active memory (the size of the recording "loop") is programmable down to two kilosamples. Memory readout is strap-selectable to provide offset binary or two's complement. In the latter case, the sign is extended to 16 bits. Samples for each channel can be read out contiguously by an F(2)·A(0) command [preceded by an F(17)·A(0) channel command]. Readout can also occur in a streaming fashion (channel data interleaved) by using the F(2)·A(1) command. Both single-channel and streaming readout can be at full Dataway speed.

As an aid in system setup, "present value monitoring" Read commands are included. Each 4022 contains an eight-word memory, readable from the Dataway with F(1)·A(0) through F(1)·A(7). This feature is usable in both the sample and nonsample states. The data update is controlled by the internal or external clock.

A Start Sample CAMAC command causes the digitizer to begin sampling after readout of the previous samples. Additionally, a Stop Sample CAMAC command allows a software emulation of the external event trigger. This feature is useful for system diagnostics as well as for applications where a periodic waveform is being monitored.

When more than one 4054 memory module is used, each 4054 must have four megasamples capacity. The available memory per channel is the total memory divided by the number of active channels. The active memory is programmably selectable in powers of 2 increments from two kilosamples to the maximum available memory. The ratio of active memory used for pretrigger samples is programmable from 0/8 to 8/8 in 1/8 increments.

FRONT PANEL INDICATORS (on Model 4022)

N:	Flashes when the module is addressed.
L:	Indicates that a LAM request is pending.
SMP:	Indicates that the digitizer is in the Sample state.

CONNECTORS

Eight two-pin LEMO connectors (or optionally a 25-contact 'D' socket connector) are used for the analog input. The stop trigger, clock-in and clock-out connectors are single-pin LEMOs, TTL level. Refer to ORDERING INFORMATION for the intermodule flat ribbon cables required.

FUNCTION CODES (N = module slot for the 4022 transient recorder. See Note 6.)

Command		Q	Action
F(0)·A(0)	RD1	$\overline{\text{SAMPLE}}$	Reads the Control register.
F(1)·A(i)	RD2	1	Reads the present value, selected channel. (See Note 5.)
F(2)·A(0)	RC1	DAV	Reads the waveform data, selected channel.
F(2)·A(1)	RC1	DAV	Reads the waveform data in streaming (interleaved) form for all channels.
F(3)·A(0)	RCM	$\overline{\text{SAMPLE}}$	Reads the Module Identifier (R1-R8).
F(8)·A(0)	TLM	LR	Tests whether a LAM request is present.
F(9)·A(0)	CL1	$\overline{\text{SAMPLE}}$	Starts digitizing (places in SAMPLE state) and clears the LAM Status.
F(9)·A(1)	CL1	$\overline{\text{SAMPLE}}$	Resets the address pointer to the first memory location written with data.
F(10)·A(0)	CLM	$\overline{\text{SAMPLE}}$	Clears the LAM status.
F(16)·A(0)	WT1	$\overline{\text{SAMPLE}}$	Writes the Control register.
F(17)·A(0)	WT2	$\overline{\text{SAMPLE}}$	Selects the channel for waveform readout (1 to 64). Uses F(2)·A(0) for memory readout. (See Note 7.)
F(24)·A(0)	DIS	1	Disables the LAM request.
F(25)·A(0)	XEQ	SAMPLE	Stops digitizing (places in the $\overline{\text{SAMPLE}}$ state after completion of the post-trigger samples).
F(25)·A(1)	XEQ	$\overline{\text{SAMPLE}}$	Places the address pointer at start-of-block for streaming (interleaved) readout. (Used if a sample block read was not completed and a reread is desired).
F(25)·A(2)	XEQ	SAMPLE	Stops digitizing (places in $\overline{\text{SAMPLE}}$ state immediately. Used if waveform data is undesirable).
F(26)·A(0)	ENB	1	Enables the LAM request.
F(27)·A(0)	TST	LS	Tests whether the LAM status is set.
Z	CZ		Places the digitizer in the $\overline{\text{SAMPLE}}$ state, clears the LAM status, disables the LAM request, clears the Control register.

Notes: 1. X = 1 for all valid addressed commands.

2. All valid addressed commands except F(1)·A(i) and F(25)·A(0) give a Q = 0, X = 1 response when the digitizer is in the digitizing (SAMPLE) state and no action is taken in response to these commands.
3. If the unit is digitizing (in the SAMPLE state), an F(25)·A(0) command will give a Q = 1 response. Any subsequent F(25)·A(0) commands (while the unit is not sampling) will give a Q = 0 response.
4. The F(2)·A(0) and F(2)·A(1) commands will give a Q = 1 response provided that:
   a. the unit is not sampling;
   b. in the case of the F(2)·A(0) command, the F(17)·A(0) channel selection command has been executed;
   c. the end-of-sample has not been reached (i.e., Q = 0 after the last word is read).
5. Subaddress (i) can range from 0 to 7 to select Channel 1 to 8.
6. In the case of multiple 4022s, all commands are addressed to the "master" 4022 except for the F(1) commands. For these latter commands, the 4022 containing the channel to be read is accessed.
7. Data for the F(17)·A(0) command can range from 0 to 63 to select Channel 1 to 64.
8. The F(9)·A(1) command is used when it is necessary to start reading data at the first memory location written with data. One condition requiring this command is when the sampling process is terminated prior to all active memory being loaded.

SPECIFICATIONS

Item	Specifications
Number of Inputs:	Eight per 4022, 64 maximum
Type:	Differential
Impedance:	One megohm minimum
Full-scale Range:	±5 volts, ±10 volts, strap-selectable
Conversion Rate:	DC to 250 kilosamples per second. Maximum rate depends upon the number of active channels
Internal Clock:	Crystal-controlled with programmable rates of 5, 10, 25, 50, 100, 250, 500 hertz; 1, 2.5, 5, 10, 25, 50, 100, 250 kilohertz
Resolution:	12 bits (1 part in 4096)
Output Code:	Offset binary or two's complement, strap-selectable
Aperture Uncertainty:	±150 ps typical
Accuracy:	±1 LSB maximum error from best fit over entire range

POWER REQUIREMENTS

Model	+6 volts	−6 volts	+24 volts	−24 volts
4022-x1A	1.4 A	—	200 mA	200 mA
4054-Z1B	2.0 A	—	—	—
4054-Z2B	2.1 A	—	—	—
4054-Z3B	2.6 A	—	—	—

ORDERING INFORMATION

Model 4022-D1A — 12,bit, 8-channel Transient Recorder "D" Connector Input
Model 4022-M1A — 12,bit, 8-channel Transient Recorder, LEMO Connector Input
Model 4022-Z1A — 12,bit, 8-channel Transient Recorder, Skt/Skt LEMO Connector Input
Model 4054-Z1B — Transient Memory, One megasample x 12-bit Capacity
Model 4054-Z2B — Transient Memory, Two megasample x 12-bit Capacity
Model 4054-Z3B — Transient Memory, Four megasample x 12-bit Capacity
Model 4050-Z1B — Transient Memory, 64 kilosample Capacity
Model 4050-Z2B — Transient Memory, 256 kilosample Capacity

Weight: Model 4022
.6 kg. (1 lb. 6 oz.)
Weight: Model 4054
.6 kg. (1 lb. 6 oz.)

Weight: Model 4050
.6 kg. (1 lb. 6 oz.)

Accessories — Model 5910-Z1A Single-pin LEMO Connector
Model 5911-Z1A Two-pin LEMO Connector (Model 4022-M1A)
Model 5933-Z1A 25-Contact "D" Connector (Model 4022-D1A)
Model 5852-A/C/E Series Cable Assemblies

The following data bus cables must be ordered to ensure proper operation:

Model 5845-w000 Front Memory Bus

4054 Memory Modules	2	3	4
Suffix (-w000)	A	B	C

Note: The memory bus is not required if only one 4054 is used.

Model 5846-w000 Rear Data Bus

Total 4022 + 4054	2	3	4	5	6	7	8	9	10	11	12
Suffix (-w000)	A	B	C	D	E	F	G	H	J	K	L

SYSTEM SET-UP

In this manual, the word "system" will be used to refer to a group of one to eight Model 4022 Transient Digitizers connected to one to four Model 4054 Memory modules.

In each system there will be one master 4022 which controls all modules attached to it. All but one of the CAMAC commands to the system (the F(1)A(i) Read Present Value command) must be addressed to the master 4022. The largest possible system consists of eight Model 4022 Transient Digitizers and four Model 4054 Memory modules.

The first step in setting up the system is setting the strap options. See the section of this manual on strap options for information on strap meaning and placement. Note that while any number of 4022s (from one through eight) can be in the system, the master 4022 must be strapped for one, two, four, or eight 4022s.

After the straps have been set, the modules can be installed in the CAMAC crate.

C A U T I O N

Always turn crate power off

when inserting or removing modules

Once installed, the rear connectors on all modules in the system should be connected with a Model 5846-Series 40-conductor ribbon cable. In a system containing more than one 4054, the front panel connectors of the 4054s should be connected with a Model 5845-Series 50-conductor ribbon cable.

When an external Stop Trigger and/or external Clock are used, they need only be connected to the master 4022 in the system. This is done with single-pin LEMO connectors (either a Model 5910-Z1A or a Model 5857-Series Cable Assembly).

The final step in system set-up is the connection of the signals to be measured. The connector pinout charts have detailed information on the front panel connectors of the 4022. See the section on channel addressing on page 13 of this manual to determine the channel numbers in a system containing more than one 4022.

PRESENT VALUE MONITOR

Each Model 4022 Transient Digitizer has an eight word memory which stores the most recent data read from each of its channels. The memory is read with an F(1)A(i) command (i = 0 to 7) to the 4022 containing the desired channel. This is the only command which may directly address any 4022 other than the master 4022 in a system. The present value monitor data is updated constantly and can be read whether or not the system is in the sample state. After power-up or a "Z" to the crate; only the channel 1 (A = 0) present value may be read. To read the present value of other channels, it is necessary to set the number of active channels in the

Control/Status Register on page 7. The Model 4054 Memory module is not necessary for the present value monitor and need not be attached to the system, thus one or more Model 4022 Transient Digitizers can be connected together and used as a scanning A/D.

PRE-TRIGGER SELECTION

The pre-trigger sample size is programmable through the control register. The pre-trigger sizes vary in 1/8th increments from 0/8th to 8/8th. This is the fraction of active memory and not the total memory. For example, if the pre-trigger size is set for 3/8th with 16K of active memory, a total of 6144 addresses will contain data prior to the stop or trigger pulse, and the remaining 10240 locations will follow the trigger pulse. Each 1/8th in this situation will be 2048 address locations. A setting of 0/8th pre-trigger will result in all of the active memory being written after the trigger pulse. An 8/8th setting will result in no more samples being stored after the trigger pulse is received.

RECORDING INPUT SIGNALS

Before recording, the control register must be set to the desired configuration. See the section on Control/Status on page 7 to determine the desired settings. The control register is set with an F(16)A(0) command to the slot containing the Master 4022.

The system begins storing data in the 4054 memory after an F(9)A(0) command, the Start Sample command. To stop sampling, the master 4022 must receive an F(25)A(0) command or a Stop Trigger signal on its front panel connector. Once the Stop Sampling has been initiated, the system will continue to record the input signals until the post-trigger samples have been stored, then the Sample state is cleared and LAM status is set.

READ INSTRUCTIONS

There are two ways to read the data from the memory: selected channel or streaming (interleaved). To read the data from a selected channel, the desired channel must be set with an F(17)A(0) command with data of 0 to 63 (corresponding to channels 1 to 64). The data can be read with successive F(2)A(0) commands until a Q response of zero is returned indicating end-of-memory. The memory can be reset at any point with an F(25)A(1) command thus allowing the data to be read again.

After the sample is completed, the memory address is set to the first address after the last written address. The first value read will give the value at this beginning address. The address will be incremented automatically to the next appropriate address after a read is performed. The beginning address is stored in a register to be reloaded by the user to allow the memory to be read from the beginning. An F(25)A(1) command is used to load this address directly to allow F(2)A(1) commands to read the data. The F(17)A(0) command loads the beginning address plus an offset. This allows a specific channel to be selected. After an F(17)A(0) command, the address will be incremented an amount equal to the number of channels being digitized every time an F(2)A(0) command is performed. The module will be disabled from this mode of increment by an F(2)A(1), F(25)A(1), F(9)A(0) or a CAMAC Z command.

Q = 0 is returned if any read is attempted while a sample is in progress. Data returned will be zero. Q = 0 and data = 0 is also returned if more data is attempted to be read than what is available in active memory.

CONTROL/STATUS REGISTER

16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
ERR FLG	PRE 4	PRE 3	PRE 2	PRE 1	ACT 4	ACT 3	ACT 2	ACT 1	CHN 3	CHN 2	CHN 1	CLK 4	CLK 3	CLK 2	CLK 1

Bit 16 **Error Flag** - set when scanning is halted before entire active memory has been written. In this state, data read from the memory will be invalid for an unknown number of reads, until the location where sampling started is reached.

Bits 15-12 **Pre-trigger Size** - select the ratio of pre-trigger memory to active memory as shown in the following table.

Bit 15	14	13	12	(Pre-trigger/Active) RATIO
0	0	0	0	0/8
0	0	0	1	1/8
0	0	1	0	2/8
0	0	1	1	3/8
0	1	0	0	4/8
0	1	0	1	5/8
0	1	1	0	6/8
0	1	1	1	7/8

Bits 11-8 **Active Memory Size** - select the total amount of memory to be used while scanning.

Bit 11	10	09	08	Active Memory Size (12 Bit Words)
0	0	0	0	2K (2048)
0	0	0	1	4K (4096)
0	0	1	0	8K (8192)
0	0	1	1	16K (16384)
0	1	0	0	32K (32768)
0	1	0	1	64K (65536)
0	1	1	0	128K (131072)
0	1	1	1	256K (262144)
1	0	0	0	512K (524288)
1	0	0	1	1 Meg (1048576)
1	0	1	0	2 Meg (2097152)
1	0	1	1	4 Meg (4194304)
1	1	0	0	8 Meg (8388608)
1	1	0	1	16 Meg (16777216)

NOTE: The active memory size is limited by the size and number of the Model 4054 memory modules in the system.

NOTE: Alternate active memory sizes are possible as a special order option.

Bits 7-5 **Number of Channels** - selects the number of active channels for each interconnected Model 4022.

Bit 07 06 05	Active Channels
0 0 0	1
0 0 1	2
0 1 1	4
1 1 1	8

Bits 4-1 **Sample Clock** - select the frequency of the internal sample clock, or enable the external sample clock.

Bit 04	03	02	01	Frequency
0	0	0	0	5 Hz
0	0	0	1	10 Hz
0	0	1	0	25 Hz
0	0	1	1	50 Hz
0	1	0	0	100 Hz
0	1	0	1	250 Hz
0	1	1	0	500 Hz
0	1	1	1	1 KHz
1	0	0	0	2.5 KHz
1	0	0	1	5 KHz
1	0	1	0	10 KHz
1	0	1	1	25 KHz
1	1	0	0	50 KHz
1	1	0	1	100 KHz
1	1	1	0	250 KHz
1	1	1	1	EXTERNAL

NOTE: Other frequencies are available from the internal sample clock, see the section on Internal Clock Frequencies on page 17 for details.

4022 STRAP OPTIONS

There are five sets of straps on the Model 4022. Figure 1 shows their locations on the board. In a system of more than one 4022 attached to the same memory, only the module address and A/D input range need to be set on 4022s other than the master 4022.

Module ID - Eight straps set the eight bit binary number read with an F(3)A(0) command. Intended to give the user a method of identifying the module, these straps can be set to any position. These straps need only be set on the master 4022.

2's Complement - One strap sets the output data format to either 2's complement, with sign extended to 16 bits, or offset binary. This strap need only be set on the master 4022.

Number of 4022s - Three straps select the number of 4022s connected in a system as shown in the following table. These straps need only be set on the master 4022.

Strap 4 2 1	Number of 4022's
0 0 0	1
0 0 1	2
0 1 1	4
1 1 1	8

NOTE: When there are three 4022s in the system, the number of 4022 straps must be set to 4 (011). When there are five, six, or seven 4022s, the straps must be set to 8 (111).

Module Address - Three straps select the address of the Model 4022 in a system of one through eight 4022s, as shown in the following table. These straps must be set on all 4022s in the system.

Strap 4 2 1	Number Address	
0 0 0	1	MASTER
0 0 1	2	
0 1 0	3	
0 1 1	4	
1 0 0	5	
1 0 1	6	
1 1 0	7	
1 1 1	8	

NOTE: Module addresses in any system of 4022s must start at module address one (1), which is the master 4022, and the addresses must be continuous.

A/D Input Range - Two straps select the input range of the analog to digital converter. The straps must be placed in the same position, ±5V or ±10V. These straps must be set on all 4022s in a system.

4054 STRAP OPTIONS

A-B Strap should always be loaded in B position, not A. Position A is used for testing purposes only.

AC0-AC1 These straps are loaded at the factory and should not be removed.

MSTR-SLV With the strap loaded at location MSTR, the 4054 becomes a master. This gives it full control of the front-panel memory bus. All other 4054s should have straps loaded at location SLV to make them slave units.

If only one 4054 is used in the digitizing system, it should be strapped to be a master.

MB0-MB1 These straps select the number of megasamples of memory the system will access.

MB1	MB0	Megasample Number
OUT	OUT	1- 4 (also 1M and 2M)
OUT	IN	5- 8
IN	OUT	9-12
IN	IN	13-16

EXAMPLE: With two 4054s each having the required 4 Megasample of memory, the master would have both MB0 and MB1 not loaded, and the slave would have MB0 loaded and MB1 removed.

16-EX These straps determine whether 16-bit data or extended 12-bit data is to be read. When using a 4022 digitizer, these straps should always be loaded in the EX position.

NOTE: If a 4054-ZXA option (16-Bit) is being used and these straps are strapped to 16 Bits, 13-15 of the DATA will reflect the module address of the DATA, Bit 16 will be read as zero.

4024 strap should be loaded when the 4054 is not used with a 4024. This strap is **only** to be removed when the 4054 is used with a 4024.

A spare strap location is provided to the left of strap location MB1.

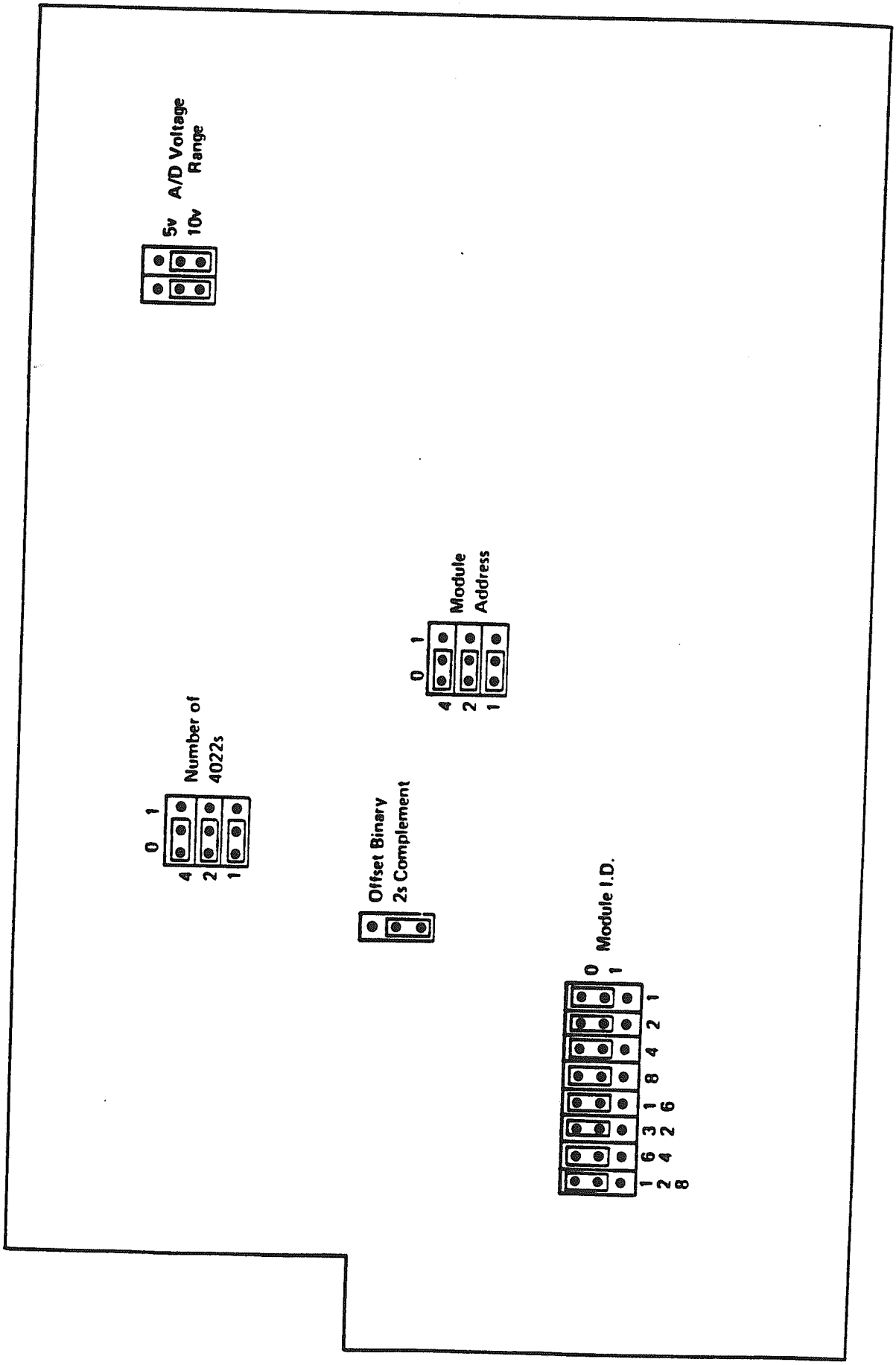
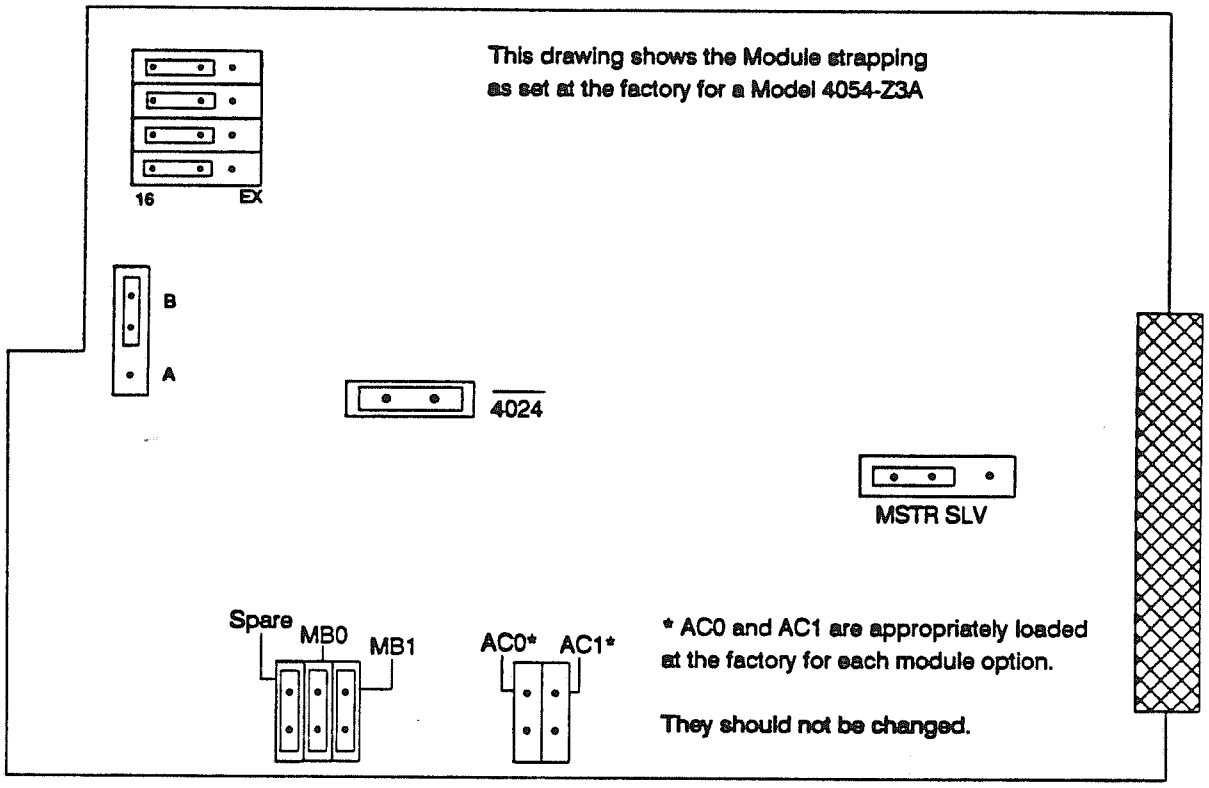


FIGURE 1

4022 STRAP LOCATIONS



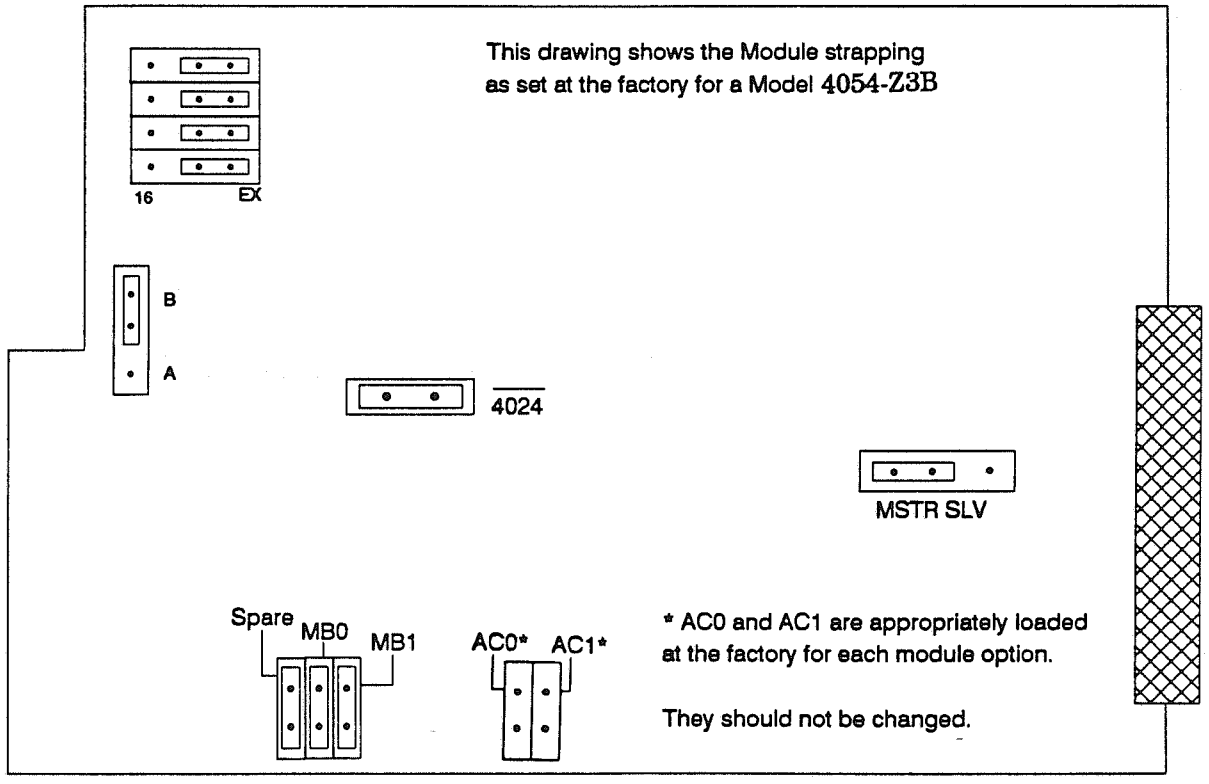


FIGURE 2

MODEL 4054 STRAP LOCATIONS

CHANNEL ADDRESSING

The following tables show the channel address layout in systems containing more than one 4022. The numbers listed in the column labeled "4022 Channel" correspond to the channels on the individual 4022 (one through eight). The numbers listed in the row labeled "4022 Address" correspond to the module address strap settings of the 4022s in the system. The numbers listed in the columns under the label "Data" are the data that must be written to the master 4022 with an F(17)A(0) command in order to access the indicated channel. They also show the order in which input data is stored in the memory.

NOTE: While it is possible to have three, five, six, or seven 4022s in a system, the master 4022 must be strapped for one, two, four, or eight 4022s. Memory and channel numbers are always allocated as if there were one, two, four, or eight 4022s.

TABLE 1

One 4022

4022 Address	000
4022 Channel	Data
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7

TABLE 2

Two 4022s

4022 Address	000	001
4022 Channel	Data	
1	0	1
2	2	3
3	4	5
4	6	7
5	8	9
6	10	11
7	12	13
8	14	15

TABLE 3

Four 4022s

4022 Address 4022 Channel	000 Data	001	010	011
1	0	1	2	3
2	4	5	6	7
3	8	9	10	11
4	12	13	14	15
5	16	17	18	19
6	20	21	22	23
7	24	25	26	27
8	28	29	30	31

TABLE 4

Eight 4022s

4022 Address 4022 Channel	000 Data	001	010	011	100	101	110	111
1	0	1	2	3	4	5	6	7
2	8	9	10	11	12	13	14	15
3	16	17	18	19	20	21	22	23
4	24	25	26	27	28	29	30	31
5	32	33	34	35	36	37	38	39
6	40	41	42	43	44	45	46	47
7	48	49	50	51	52	53	54	55
8	56	57	58	59	60	61	62	63

OFFSET RECALIBRATION

The 4022 has been designed with separate non-interacting gain adjustments for ±5V and ± 10V input range selections as well as individual offset trims for each of the eight channels. There is an additional overall offset trim which compensates for offset variations when switching from one input range to the other. All adjustments for both input ranges are properly set at the factory before shipping. The module is shipped with strap selections and overall offset trimmed for the ±10V input range.

If the ±5V input range is desired, the following simple procedure should be performed to ensure peak results.

1. Properly place the range jumper straps to the 5V range position.

2. Apply 0 volts to any channel (e.g., short both differential inputs to ground).

3. Perform Present Value Monitor read operation on the selected channel.

4. Adjust potentiometer PT3 (near pin 32 of the ADC chip) until the proper 0 volt reading is obtained.

MEMORY DESCRIPTION

The Model 4054 can be configured to provide 1M to 16M words of memory for use with the Model 4022. Individual 4054s can contain 1M, 2M or 4M words of memory. To obtain larger amounts of memory, either 2 or 4 4054s can be connected together to provide 8M or 16M words of memory.

The actual amount of memory used to store data can be equal to or less than the total amount of memory loaded in the digitizing system. This amount of memory is called the active memory and is programmable through the control register ranging from 2K to 16M words in increments of powers of 2.

The twelve-bit data words received from the 4022 are stored in sequential order. This is independent of the actual number of channels that are active, whether it is one or 64. The data stored can be read in sequential order over the CAMAC Dataway using the F(2)A(1) command. Or if desired, each individual channel can be read by using an F(2)A(0) command that was preceded by an F(17)A(0) containing the channel number to be read.

The data received from the 4022 is double-buffered in the 4054 to allow hidden refreshes, to the dynamic memory, every 10 microseconds. Chip U48 controls the sequence of writes and refreshes to the dynamic memory.

At the beginning of a sample when more than one 4054 is used, the higher megaword is written first. The next highest megaword is written until all of the memory is written and the address rolls over again to the initial megaword of memory. The memory will be continually written until the sample is completed.

MASTER/SLAVE OPERATION OF 4054

When there is more than one 4054, all but one has to be strapped to be a slave with only one being the master. Even if the active memory is set to only 2K active words and 16 megawords are loaded, only one 4054 is to be master.

The master 4054 responds to the Dataway commands addressed to the master 4022 and controls all the other 4054s through the front-panel 50-pin bus. On this bus are the control signals for the dynamic RAMs and the 24 address lines. If more than one 4054 were a master, both modules would attempt to drive these lines.

FRONT PANEL CONNECTORS 4022

On all options of the 4022, there are three single-position LEMO socket connectors. In any system of one through eight 4022s, only the master 4022 should have any connections to these three points. On all other 4022s these connectors are inactive. The connector labels and their functions are listed below.

STOP - TTL input with 470 Ohm resistor pull-up to +5 Volts followed by a series 47 Ohm resistor preceding diode clamps to ground and +5 Volts. A transition from TTL low to high on this connector will cause the 4022 to leave the sample state after reading the post-trigger samples. The Low or High period must be greater than 100 ns.

CLK IN - TTL input with 470 Ohm resistor pull-up to +5 Volts followed by a series 47 Ohm resistor preceding diode clamps to ground and +5 Volts. When the 4022 is set for external clock, a transition from TTL low to high on this connector will initiate the A/D conversion process. The Low or High period must be greater than 100 ns.

CLK OUT - TTL output of the internal or external sample clock depending upon which is selected. This signal can be used to pass the sample clock to other 4022/4054 systems.

The 4022-M1A has eight two-position LEMO connectors for the input signals. These connectors are labeled on the front panel with their channel numbers. Position one (socket) of each LEMO is the low side of the input signal and position two (pin) is the high side.

The 4022-D1A has one 25-socket D connector for (DB25S) the input signals. See the connector layout on page 14 for pin numbers.

INTERNAL CLOCK FREQUENCIES

Internal clock frequencies other than those provided are available when the 74S288 PROM in location U45 is changed. Locations 0 through 15 in the PROM correspond to the sample clock bits in the control register. The following table shows the output data necessary for the optional frequencies.

TABLE 5

DATA									DATA								
D7	D6	D5	D4	D3	D2	D1	D0	FREQ.(Hz)	D7	D6	D5	D4	D3	D2	D1	D0	FREQ.(Hz)
1	0	0	0	0	0	0	1	250K	1	0	0	0	1	1	1	0	33.3
1	0	0	0	0	1	0	1	200K	1	0	0	0	1	0	0	1	25
1	0	0	0	0	0	1	1	166.6K	1	0	0	0	1	1	0	1	20
1	0	0	0	0	1	0	0	100K	1	0	0	0	1	0	1	1	16.6
1	0	0	0	0	1	1	1	83.3K	1	0	0	0	1	1	0	0	10
1	0	1	0	0	0	1	0	50K	1	0	0	0	1	1	1	1	8.3
1	0	1	0	0	1	1	0	33.3K	1	0	1	0	1	0	1	0	5
1	0	1	0	0	0	0	1	25K	1	0	1	0	1	1	1	0	3.3
1	0	1	0	0	1	0	1	20K	1	0	1	0	1	0	0	1	2.5
1	0	1	0	0	0	1	1	16.6K	1	0	1	0	1	1	0	1	2
1	0	1	0	0	1	0	0	10K	1	0	1	0	1	0	1	1	1.66
1	0	1	0	0	1	1	1	8.3K	1	0	1	0	1	1	0	0	1
1	0	0	1	0	0	1	0	5K	1	0	1	0	1	1	1	1	0.83
1	0	0	1	0	1	1	0	3.3K	1	0	0	1	1	0	1	0	0.5
1	0	0	1	0	0	0	1	2.5K	1	0	0	1	1	1	1	0	0.33
1	0	0	1	0	1	0	1	2K	1	0	0	1	1	0	0	1	0.25
1	0	0	1	0	0	1	1	1.6K	1	0	0	1	1	1	0	1	0.20
1	0	0	1	0	1	0	0	1K	1	0	0	1	1	0	1	1	0.16
1	0	0	1	0	1	1	1	833.3	1	0	0	1	1	1	0	0	0.1
1	0	1	1	0	0	1	0	500	1	0	0	1	1	1	1	1	0.083
1	0	1	1	0	1	1	0	333.3	1	0	1	1	1	0	1	0	0.05
1	0	1	1	0	0	0	1	250	1	0	1	1	1	1	1	0	0.033
1	0	1	1	0	1	0	1	200	1	0	1	1	1	0	0	1	0.025
1	0	1	1	0	0	1	1	166.6	1	0	1	1	1	1	0	1	0.02
1	0	1	1	0	1	0	1	100	1	0	1	1	1	0	1	1	0.016
1	0	1	1	0	1	1	1	83.3	1	0	1	1	1	1	0	0	0.01
1	0	0	0	1	0	1	0	50	1	0	1	1	1	1	1	1	0.0083
									0	1	X	X	X	X	X	X	EXTERNAL

MEMORY BUS

Pin No.	Name	Function
1	REF(L)	Refresh in Progress
2	GND	Ground
3	R/C	Row/Column Select
4	GND	Ground
5	CAS(L)	Column Address Strobe
6	GND	Ground
7	RAS(L)	Row Address Strobe
8	GND	Ground
9	READ(L)	CAMAC Read {F(2)·[A(0)+A(1)]}
10	GND	Ground
11	CLK1	Register 1 Clock
12	GND	Ground
13	EN1(L)	Register 1 Enable
14	GND	Ground
15	CLK0	Register 0 Clock
16	GND	Ground
17	EN0(L)	Register 0 Enable
18	GND	Ground
19	A1	Address Bit 1
20	A2	Address Bit 2
21	A23	Address Bit 23
22	A3	Address Bit 3
23	A4	Address Bit 4
24	GND	Ground
25	A5	Address Bit 5
26	A6	Address Bit 6
27	A24	Address Bit 24
28	A7	Address Bit 7
29	A8	Address Bit 8
30	GND	Ground
31	A9	Address Bit 9
32	A10	Address Bit 10
33	GND	Ground
34	A11	Address Bit 11
35	A12	Address Bit 12
36	GND	Ground
37	A13	Address Bit 13
38	A14	Address Bit 14
39	GND	Ground
40	A15	Address Bit 15

MEMORY BUS (Continued)

Pin No.	Name	Function
41	A16	Address Bit 16
42	GND	Ground
43	A17	Address Bit 17
44	A18	Address Bit 18
45	GND	Ground
46	A19	Address Bit 19
47	A20	Address Bit 20
48	GND	Ground
49	A21	Address Bit 21
50	A22	Address Bit 22

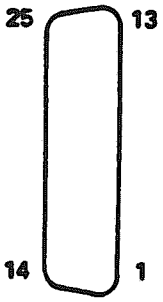
All signals are high-true except those labeled (L), which are low-true.

DATA BUS

Pin No.	Name	Function
1	LATCH	Data Latch
2	B1	Data Bit 1
3	B2	Data Bit 2
4	B3	Data Bit 3
5	B4	Data Bit 4
6	B5	Data Bit 5
7	B6	Data Bit 6
8	B7	Data Bit 7
9	B8	Data Bit 8
10	B9	Data Bit 9
11	B10	Data Bit 10
12	B11	Data Bit 11
13	B12	Data Bit 12
14	MA1	Module Address 1
15	MA2	Module Address 2
16	MA4	Module Address 4
17	GND	Ground
18	2's cmpl.	2's Complement Select
19	SEL1	# of 4022's 1
20	SEL2	# of 4022's 2
21	SEL4	# of 4022's 4
22	GND	Ground
23	DCLK	Data Clock
24	GND	Ground
25	CA1	Channel Address 1
26	CA2	Channel Address 2
27	CA4	Channel Address 4
28	GND	Ground
29	CNVT	Convert
30	GND	Ground
31	T/H	Track/Hold
32	GND	Ground
33	Sample	Sample in Progress
34	GND	Ground
35	TRG	Stop Trigger
36	GND	Ground
37	N(L)	N line from Master 4022
38	GND	Ground
39	EOM	End-of-Memory
40	GND	Ground

4022/4054 SOCKET WIRE LIST

FRONT-PANEL CONNECTOR - 4022-D1A

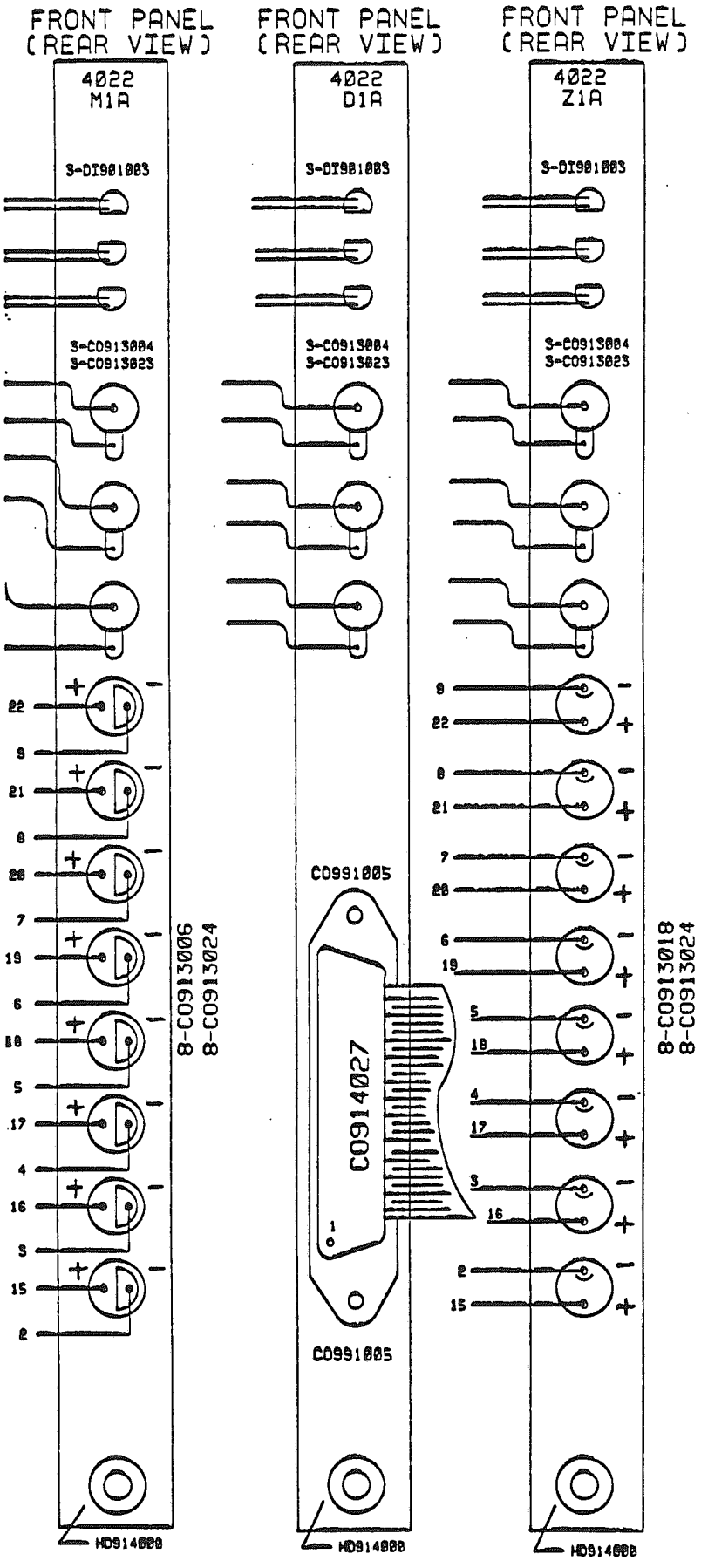


Socket/Wire List

25 SOCKET 'D'

SOCKET NO.	
25	
24	
23	GND
22	CHAN 1 (+)
21	CHAN 2 (+)
20	CHAN 3 (+)
19	CHAN 4 (+)
18	CHAN 5 (+)
17	CHAN 6 (+)
16	CHAN 7 (+)
15	CHAN 8 (+)
14	GND

SOCKET NO.	
13	
12	
11	
10	GND
9	CHAN 1 (-)
8	CHAN 2 (-)
7	CHAN 3 (-)
6	CHAN 4 (-)
5	CHAN 5 (-)
4	CHAN 6 (-)
3	CHAN 7 (-)
2	CHAN 8 (-)
1	GND


FRONT PANEL
(REAR VIEW)
4022
M1A
S-DI981003
S-C0913004
S-C0913023
22
9
21
8
20
7
19
6
18
5
17
4
16
3
15
2
8-C0913006
8-C0913024
HD914000
FRONT PANEL
(REAR VIEW)
4022
D1A
S-DI981003
S-C0913004
S-C0913023
C0991005
C0914027
C0991005
HD914000
FRONT PANEL
(REAR VIEW)
4022
Z1A
S-DI981003
S-C0913004
S-C0913023
9
22
8
21
7
20
6
19
5
18
4
17
3
16
2
15
8-C0913018
8-C0913024
HD914000
FRONT VIEW
RED KEY UP

WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

The product warranty may vary outside the United States and does not include shipping, customs clearance, or any other charges. Consult your local authorized representative or reseller for more information regarding specific warranty coverage and shipping details.

PRODUCT SPECIFICATIONS AND DESCRIPTIONS IN THIS DOCUMENT SUBJECT TO CHANGE WITHOUT NOTICE.

KINETICSYSTEMS SPECIFICALLY MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR ANY OTHER WARRANTY EITHER EXPRESSED OR IMPLIED, EXCEPT AS IS EXPRESSLY SET FORTH HEREIN. PRODUCT FAILURES CREATED BY UNAUTHORIZED MODIFICATIONS, PRODUCT MISUSE, OR IMPROPER INSTALLATION ARE NOT COVERED BY THIS WARRANTY.

THE WARRANTIES PROVIIDED HEREIN ARE THE PURCHASER'S SOLE AND EXCLUSIVE REMEDIES ON ANY CLAIM OF ANY KIND FOR ANY LOSS OR DAMAGE ARISING OUT OF, CONNECTED WITH, OR RESULTING FROM THE USE, PERFORMANCE OR BREACH THEREOF, OR FROM THE DESIGN, MANUFACTURE, SALE, DELIVERY, RESALE, OR REPAIR OR USE OF ANY PRODUCTS COVERED OR FURNISHED BY KINETICSYSTEMS INCLUDING BUT NOT LIMITED TO ANY CLAIM OF NEGLIGENCE OR OTHER TORTIOUS BREACH, SHALL BE THE REPAIR OR REPLACEMENT, FOB FACTORY, AS KINETICSYSTEMS MAY ELECT, OF THE PRODUCT OR PART THEREOF GIVING RISE TO SUCH CLAIM, EXCEPT THAT KINETICSYSTEMS' LIABILITY FOR SUCH REPAIR OR REPLACEMENT SHALL IN NO EVENT EXCEED THE CONTRACT PRICE ALLOCABLE TO THE PRODUCTS OR PART THEROF WHICH GIVES RISE TO THE CLAIM. IN NO EVENT SHALL KINETICSYSTEMS BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING LOSS OF PROFITS.

Products will not be accepted for credit or exchange without the prior written approval of KineticSystems. If it is necessary to return a product for repair, replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center prior to shipping the product to KineticSystems. The following steps should be taken before returning any product:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com