KineticSystems

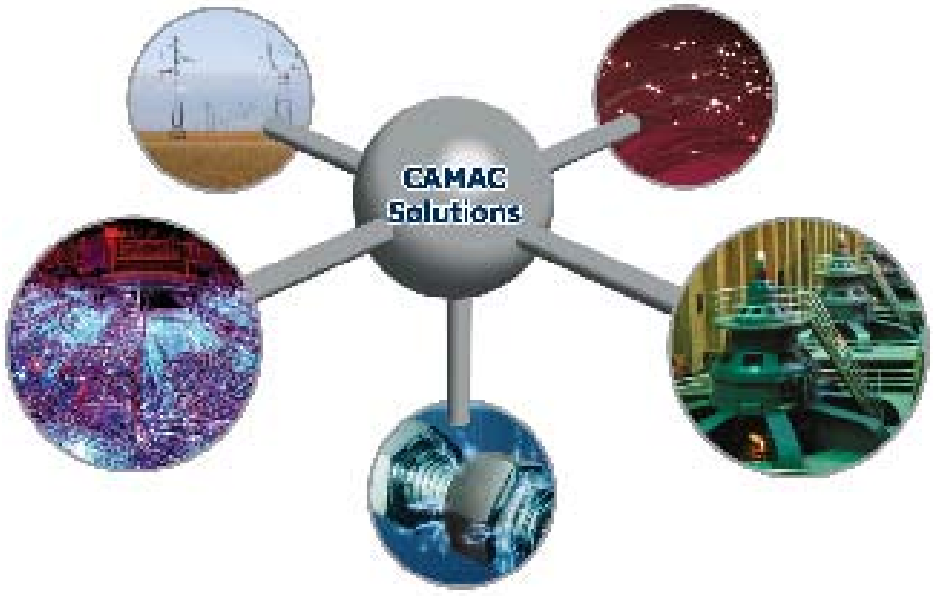
CAMAC Equipment

CAMAC, Computer Automated Measurement And Control, is an IEEE-standard (583), modular, high-performance, realtime data acquisition and control system concept.

Since 1969, CAMAC has been used in many thousands of scientific, industrial, aerospace, and defense test systems around the world.

3596

24-Bit, 16-Channel Sigma-Delta ADC



The Model 3596 CAMAC module functions as either a single-scan or continuously active 16-channel Sigma-Delta ADC.

FEATURES

- 16-channels, 24-bit data fields (up to 19 bits single-shot esolution-more with sampling averaging)
- Automatic tracking filtering (-3dB at 0.262 sample rate)
- Channel-by-channel programmable pre-gain (1 or 100)
- Channel-by-channel programmable post-gain (1 through 128)
- Continuous scan mode at 9.76 Hz to 1.028 kHz sampling rates (per channel)
- Single-Scan mode through synchronizing front-panel trigger (in and out) or CAMAC command (F(25)•A(0) or CAMAC "C" Clear operation)
- Two calibration modes: internal zero/full-scale references or external (front-panel LEMO) full-scale reference

GENERAL DESCRIPTION

The Model 3596 CAMAC module functions as either a single-scan or continuously active 16-channel Sigma-Delta ADC. Sigma-Delta conversion is a technique which attains its very high accuracy by digitally decimating/filtering the output of a fast, single-bit converter. This eliminates the need for expensive tracking filter, sample/hold, and gain functions allowing a simple ADC-per-channel structure. This further eliminates the need to multiplex inputs to a common ADC and thereby reduces crosstalk effects to negligible levels. Another important consequence of the digital filtering is that filter notches are produced which can be made to coincide with 60 Hz (or 50 Hz) power line frequencies and their harmonics. Thus, even in environments with severe signal corruption due to power line noise, very good results are possible.

The 3596 module provides for independently selectable post-gains of 1 to 128 on differentially-received inputs which accept up to 10 volts full-scale. A common sampling rate should be chosen for all channels and may range from 9.76 Hz to 1.028 kHz. These frequencies also define the first notch in the build-in lowpass tracking filters. The -3dB bandwidth is consequently always 0.262 times the selected sampling rate. The effective resolution of each channel is derated by increased gain and sampling rate, and ranges from 19 bits at a gain of one and a 10 Hz rate to 8 bits at a gain of 128 and a 1 kHz rate. For all gains at rates of 100 Hz and below, resolution is at least 15 bits. In addition, a channel-by-channel programmable pre-gain of 100 may be selected with only minimal reduction of effective resolution. The effect on resolution under various sampling rate conditions is described in the table below.

SIGNALS/CONNECTORS

CLK OUT	10 MHz TTL master clock Connector type: Single-pin LEMO
CLK IN	TTL input for common 10 MHz clock Connector type: Single-pin LEMO
DATA RDY	Data available to read out on all channels (coincides with LAM Status indication) TTL output; falling-edge active (800 nsec low pulse) Connector type: Single-pin LEMO
TRIG OUT	Resync/Initiate Single-Scan trigger output TTL output; falling-edge active (1600 nsec low pulse) Connector type: Single-pin LEMO
TRIG IN	Resync/Initiate Single-Scan trigger input TTL input; falling-edge active (100 nsec minimum low pulse) Connector type: Single-pin LEMO
REF IN	Positive full-scale reference voltage for use in full-system channel calibration Up to volts (depending on setting of channel gain) Connector type: 2-contact pin ()/ socket (-) LEMO
JI	Differential analog channel inputs (ESD and overvoltage protected) Up to 10 volt signal range (depending on setting of channel gain) Connector type: 36-socket AMP Rectangular connector

When a Single-Scan operation is triggered, a single conversion cycle takes place and one sample point for each channel recoded. The channels are first synchronized so that these samples correspond to the same point in time. This synchronization process causes the data to remain invalid for four sample intervals of the selected sample rate. When all 16 channel samples have been recorded after this interval, a LAM Request signal, if enabled, is issued to indicate that the channels are ready for read-out. Alternatively, the LAM Status condition may be polled by waiting for a valid "Q" response to an F(27)•A(0) CAMAC command to indicate that data is available. In addition to LAM, a TTL "DATA RDY" trigger output is provided on the front panel which may be used to trigger a CAMAC list-processing device like the KineticSystems Model 3982 module.

The 3596 module provides for two mechanisms of offset and gain calibration. A self-calibration mode uses a mid-scale (0 volts) and positive full-scale reference internal to each channel's Sigma-Delta converter to calculate offset and gain for that converter. Alternatively, a system calibration mode may be selected which connects mid and full-scale voltages through the entire front-end circuitry of each channel for greater absolute accuracy. This method uses the module's analog ground as the mid-scale voltage and an external full-scale reference through the REF IN front-panel, two-conductor LEMO connector.

The LAM and Overwrite Status commands may be used to avoid rereading "stale" data and to indicate if samples were missed (overwritten before being read). A full complement of clock and trigger inputs and outputs are available to allow synchronous data-taking over multiple 3596 modules.

Command	Q	Action
F(0)•A(i)[1] **RD1**	1	Read the Converted Data Memory for channel i 1.
F(1) •A(0) **RD2**	1	Reads a 16-bit Pre-Gain Register for all channels. Bit "x" = 1 indicates a gain of 100 on channel "x".
F(8) •A(0) **TLM**		Tests if a LAM request is set.
F(10) •A(0) **CLM**	1	Clears the LAM Status bit.
F(16) •A(i)[1, 3] **WT1**	/ACTV*RDY	Writes the Control Word for channel i 1.
F(17) •A(0) **WT2**	1	Reads a 16-bit Pre-Gain Register for all channels. Bit "x" = 1 indicates a gain of 100 on channel "x".
F(18) •A(0)[3] **SS1**	/ACTV*RDY	Writes a common Control Word to all 16 channels.
F(24) •A(0) **DIS**	1	Disables the LAM Request.
F(24) •A(1) **DIS**	1	Disables Active-Scan mode.
F(24) •A(2)[3] **DIS**	/ACTV*RDY	Disables External Calibration mode.
F(25) •A(0)[2, 3] **XEQ**	RDY	Initiates a Single-Scan operation, resynchronizes the converters, clears the LAM Status bit, asserts TRIG OUT.
F(25) •A(1)[3] **XEQ**	/ACTV*RDY	Initiates a single scan of the Control Words (accessible via F(0) commands), asserts TRIG OUT.
F(26) •A(0) **ENB**	1	Enables the LAM Request
F(26)A(1)[2] **ENB**	RDY	Enables Active (continuous)-Scan mode, resynchronizes the converters, clears the LAM status bit, asserts TRIG OUT.
F(26) •A(2)[3] **ENB**	/ACTV*RDY	Enables External Calibration mode.
F(27) •A(0) **TST**	LS	Tests if the LAM Status bit is set. "Q" response indicates data is available.
F(27) •A(1) **TST**	RDY	Tests (through the "Q" response) if module is ready for further commands.
F(27) •A(2) **TST**	/OVRWT	Test (through the "Q" response) if channel data has not been overwritten since the last F(10) •A(0) Clear LAM command (or F(25) •A(0), F(26)A(1), CAMAC "Z" commands).
Z*S2[3] **Z**	0	Disables Active-Scan mode, clears LAM Status, disables LAM Request, disables External Calibration mode, clears the Pre-Gain Register.
C*S2 **CZ**	0	Resynchronizes channel scanning.

Notes:

1. Channel numbers 1 to 16 correspond to i = 0 to 15.
2. Issuing these commands while Active-Scan mode is enabled resynchronizes the converters, clears the LAM Status bit, and asserts "TRIG OUT" without otherwise affecting Active Scanning.
3. These commands require more than 1 sec to perform their functions and, consequently, produce a NOT READY (/RDY) condition until they are completed.

Item	Description
Number of inputs	16
Type of inputs	Differential
Input impedance	10^{10} ohms || 35 pF
Full-scale range	10 volts @ unity gain
Conversion data rate	10...25...30...50...60...100...250...500...1028 Hz; programmable as 19531.25/n where n = {19, 20, ..., 2000}
Resolution	19 bits minimum (10 Hz data rate, Gain = 1) 18 bits minimum (30 Hz data rate, Gain = 1) 17 bits minimum (60 Hz data rate, Gain = 1)
Missing codes	None below 60 Hz data rate
Cross-talk	< 0.00002% FSR (measured at unity gain with full-scale change applied to adjacent channels)
Programmable gain	**Pre** : 1 or 100 0.025% uncalibrated
	Post: 1,2,4,8,16,32,64,128
Pre-gain change settling time	140 µsec to 0.01%
Offset drift error	0.4 3/G µ V/deg C typical
50 Hz normal-mode attenuation	100 dB minimum (@ 50, 25,..., 50/N data rates)
60 Hz normal-mode attenuation	100 dB minimum (@ 60, 30,..., 60/N data rates)
Common-mode rejection ratio	80 dB minimum (DC to 60 Hz at all data rates
Effective bandwidth (-3dB)	0.262 x converter data rate (e.g., 2.62 Hz @ 10 Hz rate)

WEIGHT

0.7 kg. (1 lb., 9 oz.)

POWER REQUIREMENTS

+6 volts	1700 mA
-6 volts	24 mA
+24 volts	110 mA
-24 volts	80 mA

ACCESSORIES

Model 5910-Z1A	1-contact LEMO mating connector
Model 5911-Z1A	2-contact LEMO mating connector
Model 5944-Z1A	36P AMP Rectangular mating connector
Model 5857-Hxyz	1-contact LEMO to BNC shielded cable
Model 5857-Gxyz	2-contact LEMO to BNC shielded cable
Model 1992-Z1A	Rack Mount Isothermal Panel
Model 5855-Bxyz	50S Amphenol Ribbon to 36P Rectangular AMP Connector Cable

ORDERING INFORMATION

MODEL	DESCRIPTION
3596-Z1A	24-bit, 16 channel Sigma-Delta ADC Module
3596-Z1B	24-bit, 16 channel Sigma-Delta ADC Module with Sonsor Power

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