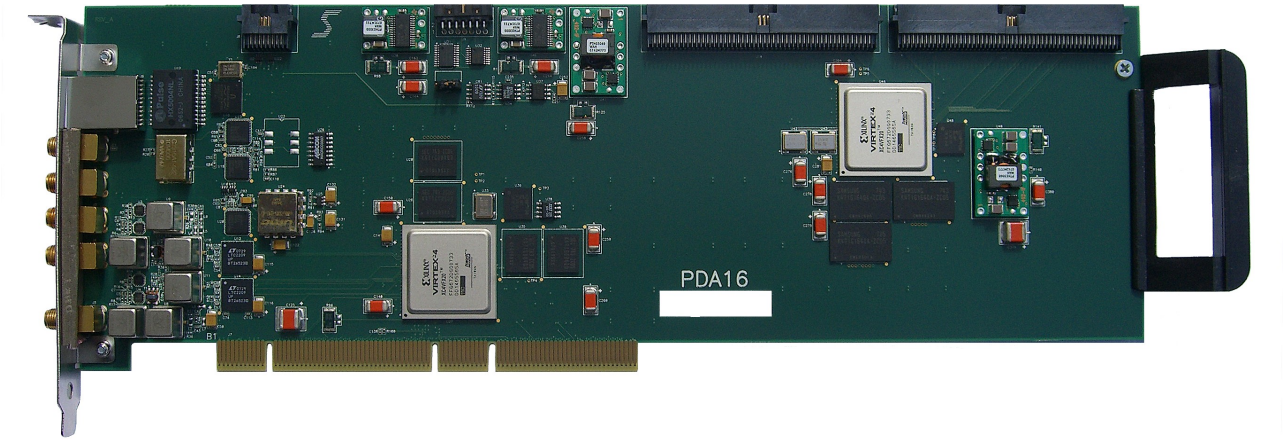
Product Information Sheet

PDA16

2 Channel, 16-Bit Waveform Digitizer



FEATURES

- 2 Analog Channels at up to 160 MHz Sample Rate per Channel
- 16 Bits of Resolution
- Bandwidth from 100 KHz to 700 MHz
- 512 Megabytes of On-Board Memory
- 500 MB/s Transfer via Signatec Auxiliary Bus (SAB)
- 640 MB/s Continuous Transfer Over PCI-X Bus
- PCI/PCI-X 64-Bit PCI-X Plug and Play Compatible Board
- Available Product Options:
  - Xilinx Virtex-4 FX20/60 FPGA
  - Option for Onboard Customer Programmable FPGA
  - Ample Support for User HW and SW Customized Processing Functionality
  - Xilinx Compatible JTAG Port Simplifies Development of User FPGA Processing

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
  - Medical Diagnostics
  - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PDA16 is a dual channel waveform capture board that provides a remarkable combination of high speed and high resolution sampling along with a very large memory capacity. Signal frequencies up to 700 MHz can be accurately captured either in baseband or in higher order Nyquist zones using under-sampling techniques.

The PDA16 is a PCI/PCI-X 64-bit compatible board equipped with standard 'Plug and Play' features common in PCI systems. The entire 512 MB memory may be used as an exceptionally large FIFO for acquiring data directly to either the SAB or PCI bus continuously non stop. In either Buffered Acquisition Mode (where the 512 RAM FIFO is used) or Data Transfer Mode it is capable of sustaining 500 megabyte/sec transfers over the SAB and 640 megabyte/sec transfers over the PCI-X bus. Significant test data has shown that recordings with this large FIFO buffering the recording process can be continuous at the card's full sampling rate even when operating in traditional non real-time environments such as the Windows operating system.

The Signatec Auxiliary Bus (SAB) allows for the high-speed transfer of data to fast processor boards, such as Signatec's PMP1000, or other peripherals, independent of the host PCI-X bus. In addition to facilitating data transfers, the SAB can be used for operational control as well.

The PDA16 was designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range. Six voltage ranges are implemented with full scale input levels from 267 mV to 2.5 volts with two of these ranges implementing a transformer coupled input direct to the ADC for best possible signal performance (2.5 V and 1.67 V).

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any clock value up to 160 MHz, offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, 5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

Up to three PDA16 boards may be interconnected in a Master/Slave configuration via a ribbon cable that connects at the top of the board. In this configuration the clock and trigger signals from the Master drive the Slave boards so that data sampling on all boards occurs simultaneously. The PDA16 supports single shot, segmented, and pretrigger triggering modes.

HARDWARE DESCRIPTION

Overview

The block diagram shows a simplified mechanization for the PDA16. The input signals are AC coupled. Six voltage ranges are implemented for each channel. The upper range is 2.5 volts full scale while the lower range is 267 millivolts FS. See the specification section at the end of this data sheet for the actual voltage range values.

The upper two ranges are transformer coupled to the ADC with no amplification and no filtering. These ranges have the highest performance level with respect to SFDR and SNR. The transformer coupled ranges have a higher minimum operating frequency and a lower maximum operating frequency than the amplifier ranges.

The lower four voltage ranges are implemented with multiple high-performance amplifiers and relay switches. The amplifiers have a bandwidth greater than 1 GHz with their outputs connected to a third order Bessel low pass filter. The purpose of this filter is to reduce the noise bandwidth of the amplifiers to no more than required to capture the maximum input signal frequency. The PDA16 is offered with no filter or standard filter cutoffs of 120 MHz or 210 MHz. With no filter, the channel bandwidth is limited by the ADC to about 700 MHz.

ADC data can be captured in dual channel or single channel mode. In single channel mode the entire signal memory can be used to capture data from channel 1 only.

The Pretrigger Samples FIFO can be thought of as a programmable length shift register with a maximum length of 4k samples and can be used to capture signal data before the trigger event. Before a trigger is received, the digitizers are active and data is continuously written into the shift register. After receiving a trigger, data samples are then written into the Acquisition FIFO. See the section "Trigger Modes and Options" for trigger mode details.

Data is written into the SDRAM via the Acquisition FIFO and read from RAM via the I/O FIFO. The double-data-rate RAM operates at a clock rate of 200 MHz yielding a total transfer bandwidth capability of 1600 MB/s in and out of the onboard RAM.

Operating Modes

The PDA16 has 8 operating modes as follows:

1. Standby – the only passive mode with no data activity.
2. RAM Acquisition – waveform data is captured into the on-board RAM.
3. PCI Acquisition – waveform data is passed to PCI bus, bypassing the on-board RAM (limited to small acquisition sizes).
4. PCI Buffered Acquisition – waveform data is passed to the PCI bus, using the on-board 512 MBs of RAM as a FIFO.
5. SAB Acquisition – waveform data is passed to SAB bus, bypassing the on-board RAM.
6. PCI Transfer – transfer data to the PCI bus after a RAM Acquisition.
7. SAB Transfer – transfer data to the SAB bus after a RAM Acquisition.
8. PCI Write RAM – Used to test RAM. Use PCI transfer mode to read back the data.

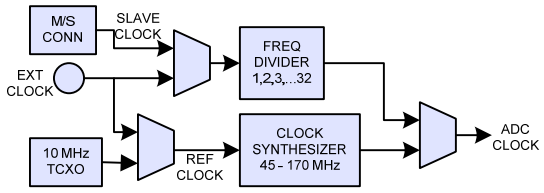
Of particular interest is the PCI buffered acquisition mode, where the SDRAM is operated as a large FIFO for acquiring data directly to the PCI bus. A large FIFO is necessary when acquiring large amounts of data to the PCI bus in order to prevent data loss due to the host system's intermittent PCI bus activity. Data may be put into RAM at a maximum rate of 640 MB/s (2 channels at 160 MHz) while also being extracted at this same rate by interleaving the write and read data packets from the onboard PDA16 RAM.

External Inputs/Outputs

Besides the signal data inputs, the PDA16 also provides SMA connections for a clock input, a trigger input, and a digital input/output signal. The clock input can be used to supply the source clock for the ADCs or a 10MHz reference clock for the internal synthesized clocks. The digital I/O connector will typically be used for outputting clock and trigger signals along with possible custom capabilities.

ADC Clock Circuit

An internal synthesized clock is the primary clock source for the ADCs. This synthesized clock on the PDA16 allows for users to dial in almost any frequency possible for the onboard ADCs with resulting sampling clock performance that matches or beats most fixed crystal oscillator performance. The ADC clock can also be supplied from the external clock input or from the Slave clock at the Master/Slave connector. The figure below shows the functionality of the ADC clock circuitry.



The synthesizer can generate any frequency from 45 to 128 MHz and most frequencies from 128 to 170 MHz. See the specification section for the range of un-settable frequencies.

If the external clock input is the ADC clock source, it may be divided by any integer value from 1 to 32. For Master/Slave board combinations the slave board(s) derive(s) the ADC clock from the Master/Slave connector via a ribbon cable connection. For slave boards the frequency divider should be set to 1 to match the slave clock to the master clock.

For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second divider can be set from 2 to 32 in factors of 2.

When the synthesized clock is selected, ADC clock jitter is extremely low at about 200 fS RMS. The jitter is independent of the clock divider setting. Clock jitter can reduce the SNR of the captured signal at high frequencies. Due to the low synthesizer clock jitter, degradation does not occur until the signal frequency is typically greater than 100 MHz.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied reference clock. The internal reference clock is accurate to better than 5ppm. This sets the ADC clock accuracy to also be within 5ppm.

HARDWARE DESCRIPTION (Continued)

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. This is a digital input with TTL signal level. Triggering may be set to occur on either the positive or negative going edge of the signal.

Acquisition may also be set to occur based on the amplitude level of either of the two input signals exceeding a programmed trigger level. The triggering threshold is a digital value that is compared against the digitized signal. The detection is edge based with either positive or negative excursion being selectable.

Digital Output

The digital output is a user selectable signal. The digitizer clock and an acquisition start signal are available as outputs. The complete list of functions is TBD, with typical uses for this connector involving the possibility for custom I/O capabilities for user applications

Trigger Modes and Options

In data acquisition mode, two triggering modes are available: single shot or segmented. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. The PCI buffered acquisition mode can be combined with the segmented trigger mode for creating high-speed continuous segment recordings.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – In the "post-trigger modes" this is the number of samples that will be taken after which the memory will be considered "full" and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt or send an interrupt over the SAB. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 512 megabytes in steps of 8 bytes. In buffered acquisition modes it is also possible to operate in a "free run" mode whereby data is collected until the board is commanded to terminate the acquisition.

Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – In Single Shot or Segmented Modes, this is the number of samples that will be recorded into RAM that occurred before the trigger.

Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

Time Stamps

In Segmented Mode "time stamps" allow for storing the time relationship between the memory segments. Time Stamps are 32 bit timer values with a clock resolution of 7.5 nanoseconds, and are accumulated in a 2048 element FIFO memory separate from the data. If necessary, time stamps may be read during acquisition in order to prevent overflow. This is possible in any acquisition mode.

SAB Operation

The PDA16 can perform SAB data transfers at 64 bits, or at 32 bits over either the high (SABH) or low (SABL) bus ports. This provides flexibility when multiple boards are incorporated into a system. At 64 bits the maximum transfer rate is 500 MB/s.

PCI Operation

The PDA16 is capable of sustaining a long-term data-transfer rate, over the PCI-X 100MHz bus, of 640 megabytes per second when installed in a 64 bit PCI-X slot. The PDA16 can also be optionally configured to operate at slower PCI-X 66MHz or PCI 33MHz rates when installed in a 64-bit PCI-X slot for compatibility with systems containing shared slots with other cards running at these slower rates.

Under-Sampling and Anti-alias Filtering

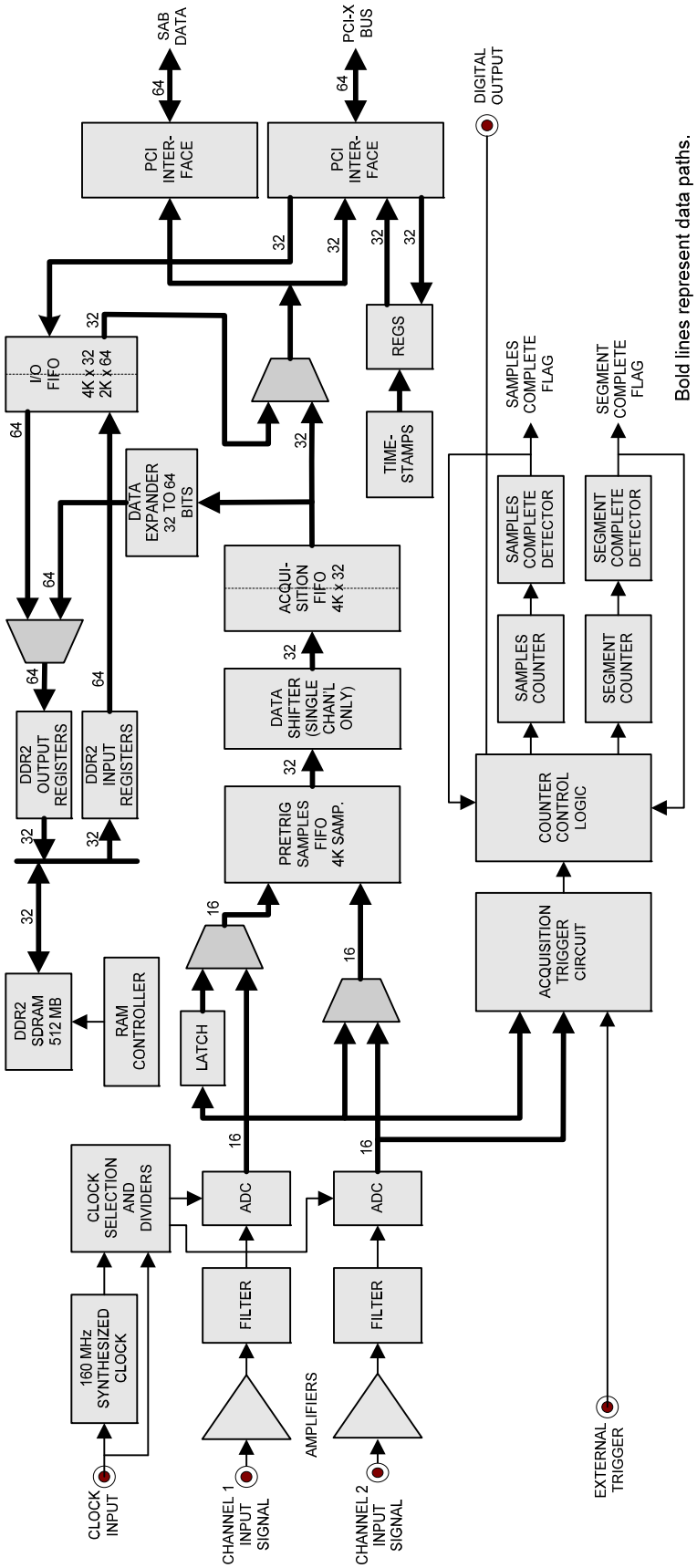
The PDA16 has a maximum digitization rate of 160 MHz but has an analog bandwidth (unfiltered) of 700 MHz. The wide analog bandwidth provides the capability of acquiring signals at frequencies well beyond the first Nyquist zone of the converter. Assuming a maximum digitizing rate of 160 MHz, the actual bandwidth of signals that can be captured is still limited to a maximum of 80 MHz but that band can be located anywhere in the 100 KHz to 700 MHz space, subject to the limitations imposed by the sampling frequency itself. Capturing signal frequencies that are more than one-half the sample rate is referred to as Under-Sampling.

At a sample rate of 160 MHz the PDA16 is capable of capturing 9 Nyquist zones (frequency bands, all numbers in Megahertz):

0 – 80	80 - 160	160 - 240	240 - 320
320-400	400 - 480	480 - 560	560 - 640
640 - 700			

Operation in any of the frequency bands requires that signal frequencies from outside the band not be allowed to reach the ADC. This may involve the application of external band-pass filters to properly reject the out-of-band signals.

To capture frequency bands that span across two of the bands as shown in the table above, the ADC clock frequency would need to be reduced to shift the resulting Nyquist bands so as to completely capture the desired frequency range. Reducing the sampling frequency will reduce the bandwidth that can be captured.



PDA16 FUNCTIONALALITY

INTEGRATED SIGNAL PROCESSING VIA on card FPGA

Overview

Signatec's PDA16 enables users to add customized signal processing into the output data flow via Xilinx® Virtex FPGAs with embedded PowerPC processors. Standard development environments can be used to program for this device, such as Xilinx ISE™ and System Generator with MATLAB software tools. To accommodate its customers' varied performance requirements, Signatec designed the PDA16 to utilize the Virtex-4 FX20 (standard) or FX60 device, delivering a processing performance range from 19,224 logic cells/1,224 kbits block RAM/32 DSP slices/1 Power PC to 56,880 logic cells/4,176 kbits block RAM/128 DSP slices/2 Power PCs, respectively. Processed data results can be sent to the PC or across the PDA16 SAB bus to other system devices, such as Signatec's parallel processing DSP board: PMP1000.

The processing capabilities are located in the SAB FPGA (as shown in the pictorial of the board layout in this data sheet). Shown below is the functionality of the SAB Interface with data flow and processing structures.

Acquired data from the System FPGA can be passed to the SAB Interface via the Parallel data bus or via some combination of the 4 serial data channels. The parallel bus can sustain 1 Billion bytes per second. Each serial channel is capable of transferring approximately 500 Million bytes per second. System data transferred via the parallel bus can be passed through directly to the SAB bus or can be routed into the processing circuitry via the data bus bridge.

The processing functionality consists of user generated hardware circuit functions and user processing software running on the Power PC. The PDA16 is supplied with a library of hardware and software signal processing functions.

*Option: User Processing – Hardware

The hardware development process is simplified by using commercial tools such as MATLAB and System Generator. Applications are developed by dragging and dropping logic blocks and connecting them to an input gateway block and an output gateway block (provided by Signatec). Up to 128 XtremeDSP slices are available for creating super-fast operations such as filtering and FFTs. After the logic blocks have been connected MATLAB can be used to run simulations on the design. After a successful simulation the logic can optionally be debugged on the FPGA running at full speed using *chipscope*.

*Option: User Processing – Software

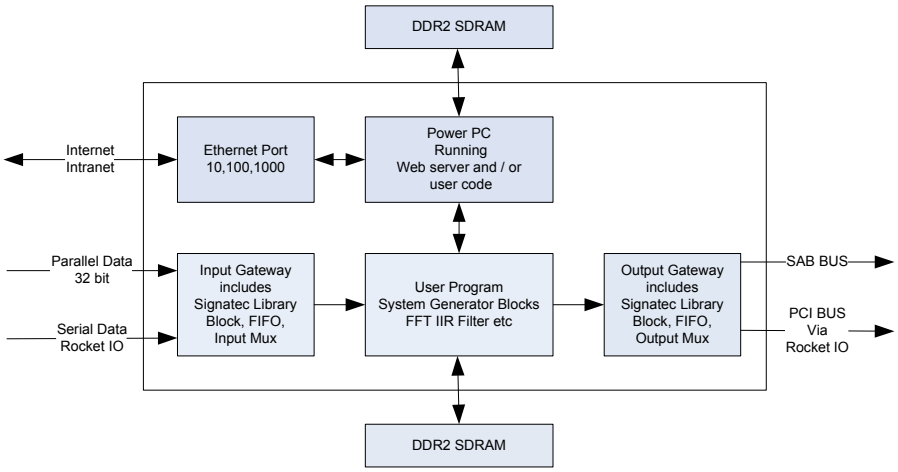
Using the Embedded Development Kit (EDK) simplifies software development for the on-chip Power PC. The software can be changed without rebuilding the logic, which greatly speeds up development. The EDK generates drivers for all the peripherals, resulting in the developer designing the application rather than the lower level code.

Using peripherals designed and provided by Signatec, users have the option of performing PDA16 board settings and monitoring various flags from this embedded Power-PC versus the traditional method of using the host system, thus making the PDA16 a true real-time acquisition, monitoring and processing system.

*Option: FPGA User Program Interface

Developing logic and Power PC code for the PDA16 is greatly simplified by Signatec's user development kit and use of standard off the shelf development programs that are familiar to today's FPGA programmers. The PDA16 user FPGA has a JTAG interface that is compatible with Xilinx ISE and other similar or related Xilinx family of development programs, including System Generator, which works with MATLAB for providing a library of easy to use signal processing functions.

The Signatec user development kit includes instructions for using the supported Xilinx software/tools, sample source files for Xilinx projects, sample source files using System Generator and MATLAB for signal processing, component peripherals that the Power PC can use for controlling the PDA16 and Power PC example programs.



FPGA SAB Typical Configuration

SOFTWARE, SYSTEM, AND PERFORMANCE DETAILS

Software

The PDA16 is supplied with the following software:

- Windows and Linux Drivers
- C Function Library with source code
- Software manual that describes how to use the available library of functions to create larger applications or systems.
- Multiple Coding examples
- Full Windows Scope Application

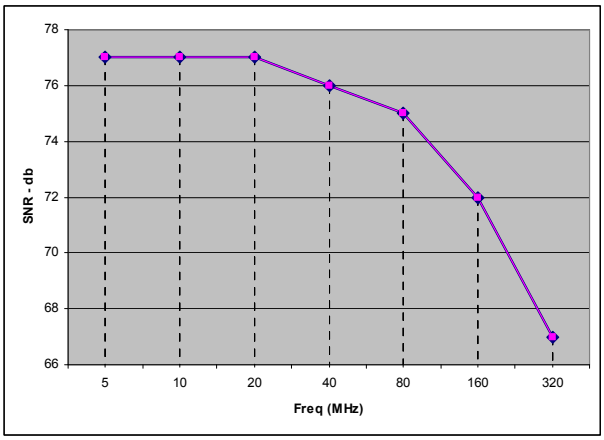
System Capabilities

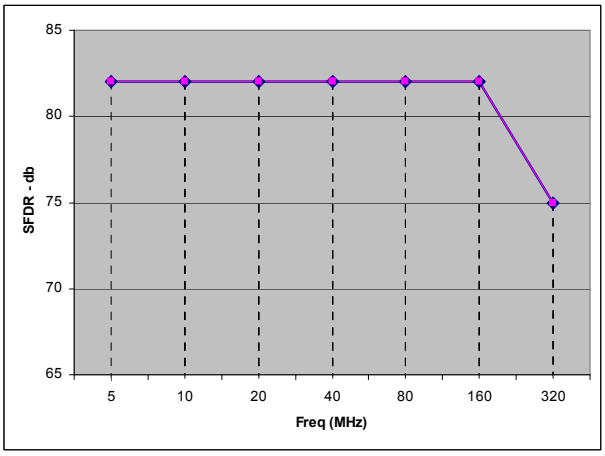
The system solution offered by Signatec is based on supplying a comprehensive range of products incorporating the Signatec Auxiliary Bus. This 64-bit bus provides transfer rates up to 500 MB/s. SAB boards act as modular building blocks for constructing high performance systems that mechanize a wide variety of applications. Shown in the figure below are elements of such a system. Many systems can be constructed using standard desktop PC's. For demanding applications Signatec can supply a total turnkey system utilizing one of our industrial computer systems.

Devices connected to the SAB may communicate via SAB interrupt and control lines. This allows the boards to accomplish multiple acquisition, transfer, and processing cycles under control of the signal processor device, without PC intervention. Bypassing the host bus and operating system can significantly improve system performance.

Typical Performance

The following charts depict anticipated PDA16 typical performance at this time. These charts will be updated upon full PDA16 production release.





DEFINITION OF TERMS

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

PDA16 SPECIFICATIONS AND ORDERING INFORMATION

External Signal Connections

Analog Input, Channel 1	: SMA
Analog Input, Channel 2	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Digital Output	: SMA
Ethernet	: RJ45

Analog Inputs

Full Scale Volt. Ranges	: 2.50V, 1.67V, 1.00V, 667mV,
	: 400mV, 267mV
Impedance	: 50 ohms
Bandwidth	: 100 KHz to 700 MHz (with no LP filter)
Coupling	: AC

External Trigger

Signal Type	: digital, TTL signal level
Impedance	: >10k ohms
Bandwidth	: 50 MHz

Internal Synthesized Clock

Frequency range	: 45.0 - 170 MHz
Resolution	: better than 5 PPM
Accuracy	: better than 5 PPM
Unsettable ranges	: 128.9-129.8, 140.6-142.8, 154.7-158.7 MHz

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance : 50 ohms	
Frequency	: 10 MHz to 160 MHz
Amplitude	: 100 mV p-p to 2.0 V p-p

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32

Reference Clock

Internal	: 10.0 MHz, ± 5 ppm max.
External	: 10.0 MHz, ± 50 ppm max (required for lock)

Digital Output

Type	: TTL Logic Level
Max. Frequency	: 160 MHz
Suggested Load	: 1k ohms

Digitizer

Resolution	: 16 bits
Aperture Jitter	: 0.07 pS typical
Clock Rate	: 1.0 to 160 MHz

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pretrigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pretrigger Samples	: samples prior to trigger are stored; Single Channel: 8k max.; Dual Channel: 4k max per channel
Delayed Trigger	: delay from trigger to data storage; Up to 64k digitizer clock cycles

Memory

Active Size	: Up to 256 MegaSamples
Segment Size	: Up to 128 Megasamples
Segment re-arm time[1]	: 150 nanoseconds
Addressing	: DMA transfer from starting address

I/O Addressing

PCI Controller Address	: 64 bytes, Plug and Play selected
Control/Status Registers	: 32 bytes, Plug and Play selected

Signatec Auxiliary Bus

Data Transfer Modes	: Block
Data Transfer Rates	: up to 640 MB/s max @ 64 bits
Data Direction	: output only

Power Requirements

+12V	: 400 mAmps max.
+5V	: 1.5 Amps max.
+3.3V	: 2.3 Amps max.

Absolute Maximum Ratings

Analog Inputs	: 5 volts peak to peak
Trigger Input	: -0.2 to +4.0 volts DC
Clock Input	: 5 volts peak to peak
Ambient Temperature	: 0 to 50 C

PDA16 Part Numbers

PDA16-[*FX*]-[*LPF*]-[*INTERFACE*]-[*MS*]

[*FX*]: **20** = Virtex-4 FX20 device.
60 = Virtex-4 FX60 device.

[*LPF*] = Cutoff frequency for the low pass filter in MHz. Standard options are **120** and **210 (default)**. For no upper cutoff, this [LPF] should be **0**.

[*INTERFACE*]: **P33** = PCI 64-bit 33MHz.
X66 = PCI-X 64-bit 66MHz.
X100 (default) = PCI-X 64-bit 100MHz.

[*MS*] = Add **MS** for Master/Slave configuration requirement.

Example Part Order Numbers (**-MS** may be added to any of these numbers):

PDA16-20-0-P33, PDA16-20-0-X66, PDA16-20-0-X100
PDA16-20-120-P33, PDA16-20-120-X66, PDA16-20-120-X100
PDA16-20-210-P33, PDA16-20-210-X66, PDA16-20-210-X100
PDA16-60-210-P33, PDA16-60-210-X66, PDA16-60-210-X100

SAB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

Master-Slave Cables

The PDA16 may be software configured to operate as a Master or a Slave in a multiple board system. For Master/Slave operation a 26-pin ribbon cable is required to connect the boards. To specify master/slave configuration, order part number with ending of **–MS**. Master/Slave boards must occupy adjacent slots. The maximum number of boards to be connected is one master and two slaves.

Documentation & Accessories

The PDA16 is supplied with a comprehensive operator's manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to libraries and examples.

Product Warranty

All Signatec products carry a full 1-year warranty. During the warranty period, DynamicSignals will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or abuse of the products.

Notes:

1. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

DynamicSignals reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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