KineticSystems Company, LLC
Preston Scientific
PRESYS 1000
User's Manual

June, 2004

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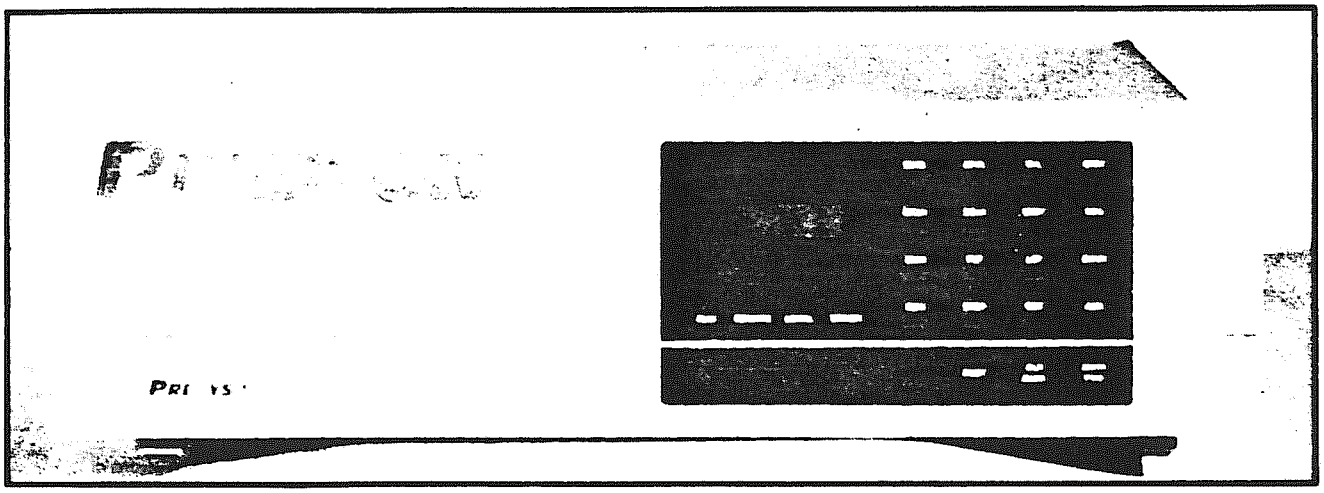
PRESYS 1000 SYSTEMS

USER MANUAL

PRESTON

PRESSYS 1000

Analog and Digital Input and Output Data Processing Sub-System

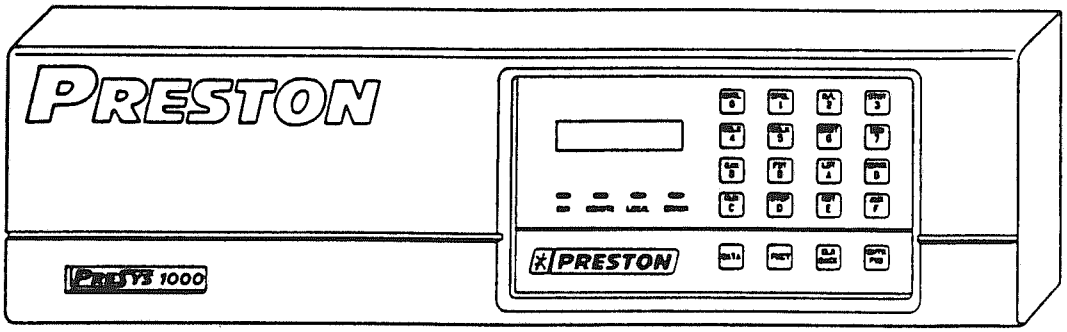


PRESSYS 1000 the data processing sub-system that combines multi-channel A/D Conversion, D/A Conversion, Digital Input and Output multiplexing all in ONE instrumentation package.

We turn the key . . . from A to D

PRESYS 1000

PRESYS 1000, Preston's newest data conversion system is organized as an "Analog and Digital, Input and Output" Data Processing Sub-System that combines multi channel A/D Conversion, D/A Conversion, Digital Input and Output multiplexing all in one easily interfaced instrumentation package.



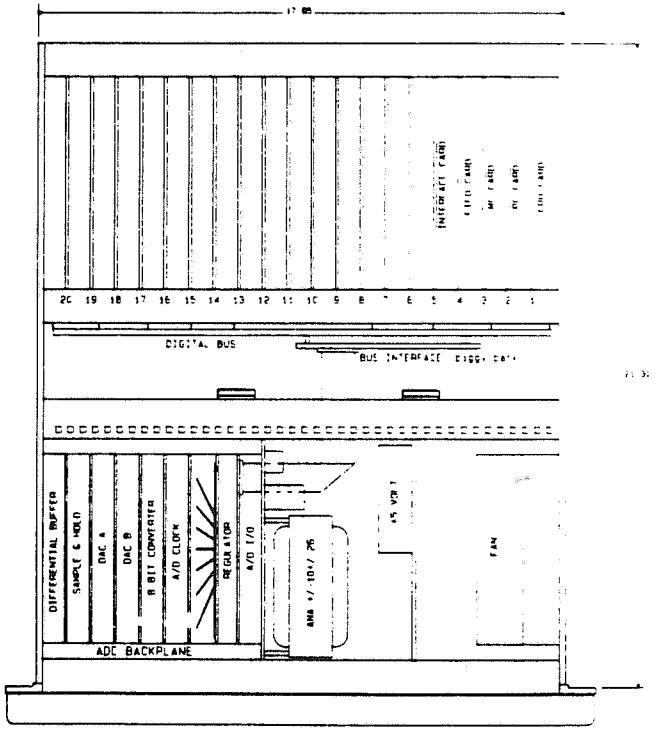
PRESYS 1000 Control Panel

The basic system includes space for high-speed A/D Converter, combined input/output DATA BUS featuring Analog Bus structure for Analog inputs and Digital Bus structure for Digital Inputs and Digital Outputs (Memory expansion, multiple computer interfaces and D/A Converters). Further the basic PRESYS 1000 System Chassis includes the UPC controller, 30K word channel address memory, 128K FIFO memory, basic computer interface, front panel control system and separate power supplies for Analog and Digital modules.

PRESYS 1000 Systems provide easily configured Analog and Digital Data Acquisition; Analog and Digital data Output; all in one compact Instrumentation package. System interface options are offered for most micro, mini and super-mini computers and Array Processors with the possibility to interface one or more computers for control and/or simultaneous data Output.

PRESYS 1000 systems will offer most Preston's existing GM, EM, LC, SDAC Series, A/D and D/A conversion channels. Most circuit boards are being repackaged to fit the PRESYS 1000 BUS concept therefore the multiplexer, amplifier, Sample-and-Hold, DAC's and filter plug-in cards cannot be moved from the existing GM systems to PRESYS 1000 systems.

The PRESYS 1000 Chassis includes UPC controller, ADC backplane and the Input/Output backplane. There is also an expander chassis that can be configured with Bus/Address expansion electronics to expand PRESYS 1000 Input/Output channel capability.



PRESYS 1000 Master Chassis

PRESYS 1000 Basic Chassis has space for 15 card modules which contain either Analog Input Channels, Digital Input Channels and/or Digital and Analog Output Channels (D/A Converters).

This same Card space will also accept other System functions. . .additional Computer Interfaces, FIFO expansion, and Chassis expansion electronics (the logic necessary to attach the PRESYS 1000 Expansion Chassis).

Any of these 15 Card Slots will accept any of the following Input or Output Channels or System Control Functions. . .

Analog Multiplexer 16 Channels/Module, Sim Sample-and-Hold 8 Channels/Module, Digital Inputs 16 Bits/Module, Digital Outputs 16 Bits/Module, Analog Outputs 1-4 Channels/Module, FIFO Buffer 128K to 1 Meg/Module, Computer Interface 1 or 2 Modules/Interface, and Bus Expansion 2 to 4 Modules/Chassis.

PRESYS 1000 Expansion Chassis has 16 Card Slots available to accept either Analog Input Channels, Digital Input Channels and/or Digital and Analog Output Channels. Any of these 16 Card Slots will accept any of the input or output channels as previously defined. There are 4 additional Card Slots that are dedicated to service bus expansion needs for attaching the PRESYS 1000 Expansion Chassis to the PRESYS 1000 Basic System Chassis.

PRESYS 1000 Basic System

STANDARD CONFIGURATION

Master Chassis has 15 Card Slots for accepting Analog and Digital, Inputs and Outputs as noted here-in.

ANALOG INPUTS. . .

PMX Series Multiplexer
PSH8 Sample-and Hold
Amp-Filter-Mux
Filter-MUX

DIGITAL MODULES AND ANALOG OUTPUTS. . .

PDAC Series D/A Converters
(Choice of 7 models)
FIFO Memories
Digital Inputs
Digital Outputs
Computer Interfaces

PRESYS 1000 A/D CONVERSION(*)

PAD 15-1 A/D Converter, 15 Bits @ 1 MHz
PAD 15-2 A/D Converter, 15 Bits @ 500 kHz
PAD 15-3 A/D Converter, 15 Bits @ 307 kHz
PAD 16-3 A/D Converter, 16 Bits @ 307 kHz
PAD 13-1 A/D Converter, 13 Bits @ 1 MHz
PAD 13-2 A/D Converter, 13 Bits @ 500 kHz
PAD 13-3 A/D Converter, 13 Bits @ 307 kHz

(*) Plugs into dedicated ADC Backplane as shown in the PRESYS 1000 Master Chassis drawing.

OTHER PRESYS 1000 FEATURES. . .

The PRESYS 1000 Bus system was created to eliminate custom chassis configuration, custom backplanes and custom wiring. This is achieved by bringing all data and control signals to a Mecca type Bus. The Bus uses a 96 pin DIN connector and will incorporate many of the functions of Preston's older MCLS Control System while providing for custom design implementations as well.

Although the Bus concept has been the primary design objective of the PRESYS 1000 System, the standardized form factors, off the shelf power supplies, accessories and modularity of components have been just as important. The connectors and chassis are all Euro-card form factor. PRESYS 1000 Systems have two Power Supplies, one for Analog and one for Digital. The initial PRESYS 1000 Systems utilize existing GM Series ADC with backplane which is mounted in the front row of the chassis. The back of the chassis will house the MUX, other Analog Input Modules, the interface cards and digital Input/Output modules. The ADC and power supplies occupy the front row. There are three dedicated card slots in the rear row that have electronics associated with UPC control. Two additional card slots are required for a simple type computer interface (i.e. DRQ3B, 12006A or DR11W, etc. . .) and FIFO Memory (16 Bit X 128K).

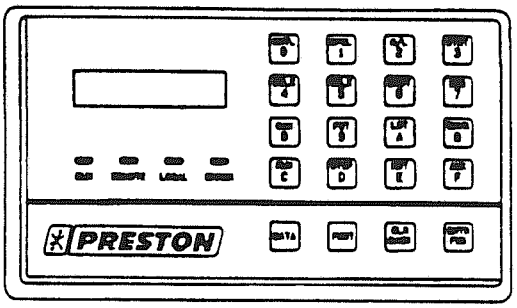
The remaining 15 Card Slots in the rear row are configured to accept Input/Output channels.

PRESYS 1000

PRESYS 1000

The PRESYS 1000 Basic Chassis is 5.22 inches high and mounts in standard 19 inch cabinets. Cooling is provided to the chassis by drawing air in from the top and back while exhausting air out the side (there will be 1 small AC fan). A center plentum will allow for improved air circulation and will maintain a constant air flow over the ADC regardless of board configuration. The total wiring of the system comprise mostly power and ground with perhaps 3 or 4 header cable interconnections, thus eliminating special custom inter-module wiring.

The front panel has a hex pad and some control to provide the ability to select hex, decimal, octal or binary display and local verse remote control. The display will be an LCD type with alpha-numeric capability. There is a front panel indication of remote or local operation RUN or ERROR conditions. In addition to displaying data in hex and decimal (counts) the output of converted analog data can be displayed in volts. Binary display of output data is not available.



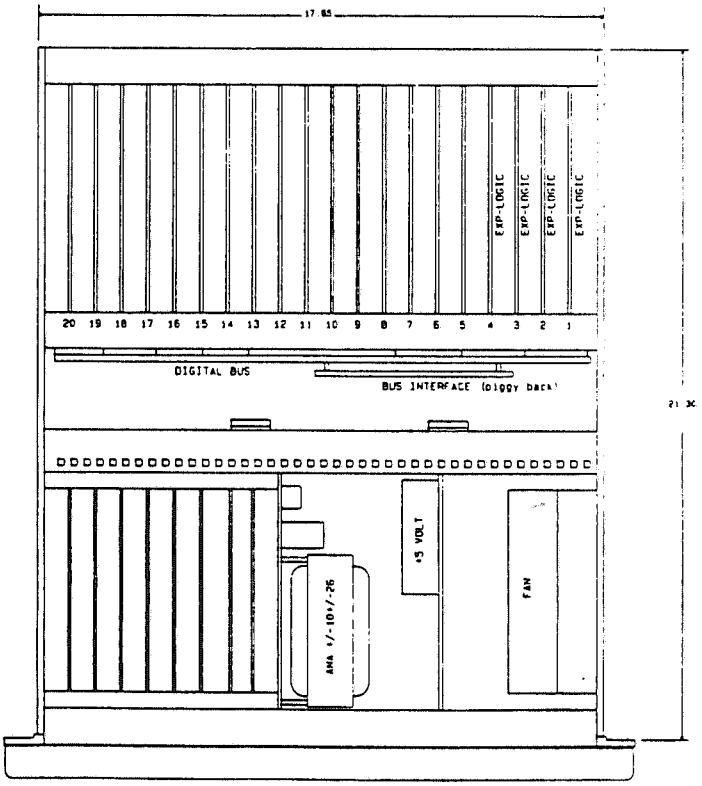
The basic control electronics is configured using PLD modules mounted on printed circuit cards and includes most of the functions of the existing MCLS Control Systems.

The UPC Controller will also manage the internal Input/Output Bus structures in determining channel type, system configurations and channel sequencing.

Interfacing to PRESYS 1000 will actually be very similar to the existing GM-System interface except much easier to change interface configurations. The main virtue of PRESYS 1000 system is to allow much easier integration of a variety of Analog and Digital Channels with multiple computer interfaces, expanded FIFO's, etc. plus the ability to easily reconfigure those systems by adding or exchanging either Input or Output modules.

PRESYS 1000 can be totally reconfigured in a matter of minutes. Change interfaces, add input or output channels, even add expansion chassis all in less than 45 minutes.

This data sheet covers only the beginning of the PRESYS 1000 story. . . more comes later in updates and supplements to this brochure.



EXPANDER CHASSIS

PRESTON
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FAX (714) 632-7355 Telex. 5101004596

SYSTEM CONFIGURATIONS AND CHANNEL IDENTIFICATION

Each PRESYS system must contain one Master chassis, and may include one or more Expansion chassis. When ac power is applied, the system scans the cards installed for type and location. The resulting information is used to generate a channel numbering table which is stored in a non-volatile memory. FIGURE 3-9A defines the standard numbering sequence.

The following list summarizes the number of channels on most standard cards.

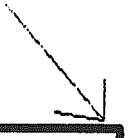
* 16 channel analog multiplexers
* 8 channel simultaneous sample-and-holds
* 4 channel simultaneous sample-and-hold
* 4 channel analog output card
* 8 channel analog output card
* 2 channel programmable gain amplifier
* 1 channel (16 line) digital input
* 1 channel (16 line) digital output
* 2 channel (32 line) digital input
* 2 channel (32 line) digital output
* 1 channel counter (16 bit)
* 2 channel counter (32 bit)

As indicated in FIGURE 3-9, numbering usually begins in the Master chassis. The following configurations, indicate channel numbering for systems as delivered. Note that if cards with different locations are switched, channel numbering for all succeeding cards will be changed when the system is next powered "ON".

Channel numbering begins with 0 in the highest numbered slot containing a user I/O card. Empty slots are ignored. Interfaces, sub-multiplexers, and control cards are also ignored

REAR OF CHASSIS

TOP VIEW



20
19
18
17
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14
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12
11
10
9
8
7
6
5
4
3
2
1
AC POWER SWITCH WIRING

PRESYS 1000 & 4000 CHASSIS

BACK ROW

NOTE:

THE SYSTEM DETECTS THE NUMBER OF CHANNELS ON CARDS INSTALLED, WHEN POWERED ON.

IN PRESYS 1000 SYSTEMS, CHANNEL ADDRESSES BEING WITH 0 ON CARD IN HIGHEST NUMBERED SLOT & INCREASE AS SLOT NUMBERS DECREASE.

IN PRESYS 4000 SYSTEMS, CHANNEL ADDRESSES BEGIN WITH 0 ON CARD IN LOWEST NUMBERED SLOT AND INCREASE AS SLOT NUMBERS INCREASE.

ADDRESSES ARE NOT ASSIGNED TO UNUSED SLOTS.

IN MULTIPLE CHASSIS SYSTEMS, CHANNEL 0 USUALLY BEGINS IN THE MASTER CHASSIS.

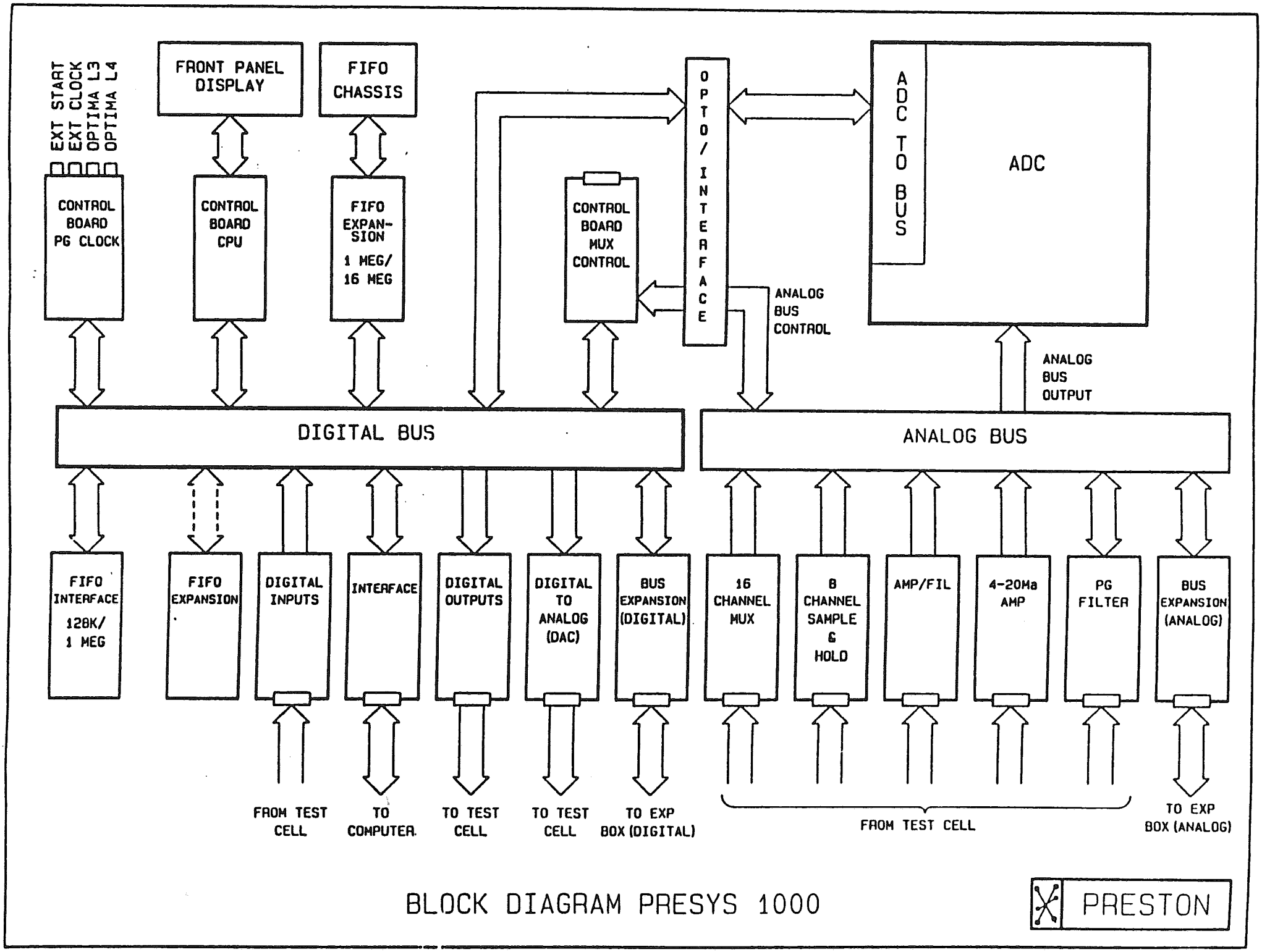
PRESYS 1000 SYSTEM EXAMPLE

SLOT	CARD INSTALLED	ADDRESSES
20	16 CHANNEL MUX	0 - 15
19	8 CHANNEL S/H	16 - 23
18	EMPTY	---------
17	2 CHANNEL D/A	24 - 25

PRESYS 4000 SYSTEM EXAMPLE

SLOT	CARD INSTALLED	ADDRESSES
20	4 CHANNEL ADC	4 - 7
19	2 CHANNEL ADC	2 - 3
18	EMPTY	---------
17	2 CHANNEL ADC	0 - 1

FIGURE 3-9A



BLOCK DIAGRAM PRESYS 1000

PRESTON

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PRESYS BUS/BACKPLANE OVERVIEW

This document presents a generalized "OVERVIEW" of the backplane connections related to the various types of I/O cards used in both PRESYS 1000 and PRESYS 4000 systems. It does not discuss bus timing, define control signals, or list pin assignments.

PRESYS 1000 systems use a single ADC preceded by an analog multiplexer. They are intended to scan multiple channels with relatively low conversion rates per channel. Depending upon the ADC installed they may be clocked for aggregate rates of up to 1MHz. Channel selection is programmable.

PRESYS 4000 systems use an ADC per channel cards with outputs digitally multiplexed into a single data stream. They are intended to scan multiple channels with relatively high conversion rates per channel. Since all channels are clocked simultaneously, time correlated data is generated.

The maximum clock rates depends upon the type and number of ADC per channel cards included in the system. All cards installed will be scanned in sequence determined by physical location. The maximum aggregate data rate is 5MHz.

N O T E:

If the maximum aggregate rate of the PRESYS 4000 system is below 1MHz, it may be factory configured as a PRESYS 1000 system which includes all of the channel selection options.

The backplane extends across all 20 slots of the back row of the PPESYS chassis. The description herein applies only to the slots available for user connections (5 - 20).

There are two basic sections of the backplane; ANALOG and DIGITAL. To minimize system noise, each section is connected to a separate power supply. Reference Figure BUS_OVER. User I/O cards may be plugged into any of the referenced slots. The only make connections to the appropriate power supplies.

Most analog cards require control signals generated by digital cards located in slots 1 - 3. Since these signals are referenced to the digital power supply they are routed through an optical isolator assembly mounted on the rear side of the backplane.

ANALOG cards include: (Reference Figure BUS_ANA)

* 16 channel differential multiplexers
* 16 channel single-ended, buffered multiplexers
* 8 channel simultaneous sample-and-holds
* 2 channel programmable gain amplifiers
* 1 channel programmable gain, filter amplifiers

DIGITAL cards include: (Reference Figure BUS_DIG)

* 1 channel, 16 line digital input
* 2 channel, 16 line digital input
* 1 channel, 16 line digital output
* 2 channel, 16 line digital output
* Assorted computer compatible interfaces (SCSI, IEEE-488, DR11-W, etc.)

Two other types of cards used in PRESYS systems are:

* Analog-to-Digital converter per channel: (Reference Figure BUS_ADC)

  * 1 channel, 16 bit Analog-to-Digital converter
  * 2 channel, 16 bit Analog-to-Digital converter
  * 4 channel, 12 bit Analog-to-Digital converter

* Digital-to-Analog converter (Reference Figure BUS_DAC)

  * 8 channel, 12 bit Digital-to-Analog converter
  * 4 channel, 16 bit Digital-to-Analog converter

These two groups of cards connect to both the ANALOG and DIGITAL sections of the backplane. Unless they include onboard optical isolation, the ANALOG and DIGITAL power supplies will no longer be isolated. Since this is acceptable in many systems, optical isolation on these cards is available as an option, and not included as a standard feature.

The Analog-to-Digital converter per channel cards use the ANALOG power supplies on input sides. The outputs connect to the digital data bus which is referenced to DIGITAL ground. Optional optical isolators on these cards break this connection.

The Digital-to-Analog converter cards receive input data and control signals from the DIGITAL section of the backplane but require voltages from the ANALOG power supplies on outputs. Optional optical isolators on digital I/O lines break connections between the ANALOG and DIGITAL power supplies.

The ANALOG section is common to slots 4 through 20, but analog cards normally plug into slots 6 - 20. It basically consists of:

* Analog power supply

* Analog bus connected to multiplexer switch outputs on analog plug-in cards. This is also connected to the input of the Analog-to-Digital converter located in the front row of the PRESYS 1000 systems. It is not used on PRESYS 4000 systems.

* Isolated address and control lines needed by Analog cards

The DIGITAL section is common to the entire 20 slots, but user connections are limited to slots 5 - 20. It basically consists of:

* Digital power supply (+5 volts)

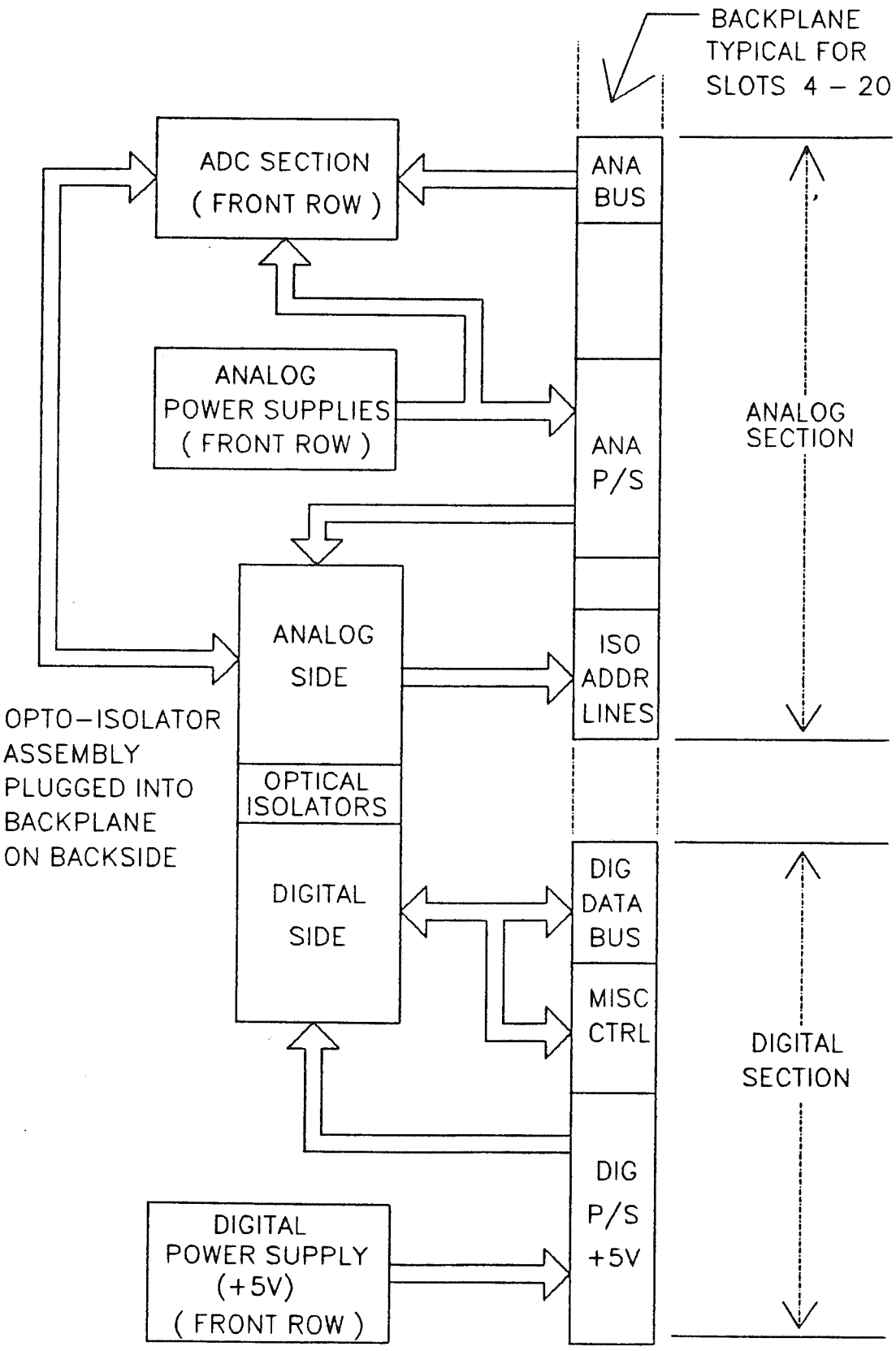
* 16 line digital data bus

* Miscellaneous control lines

Reference Figures:

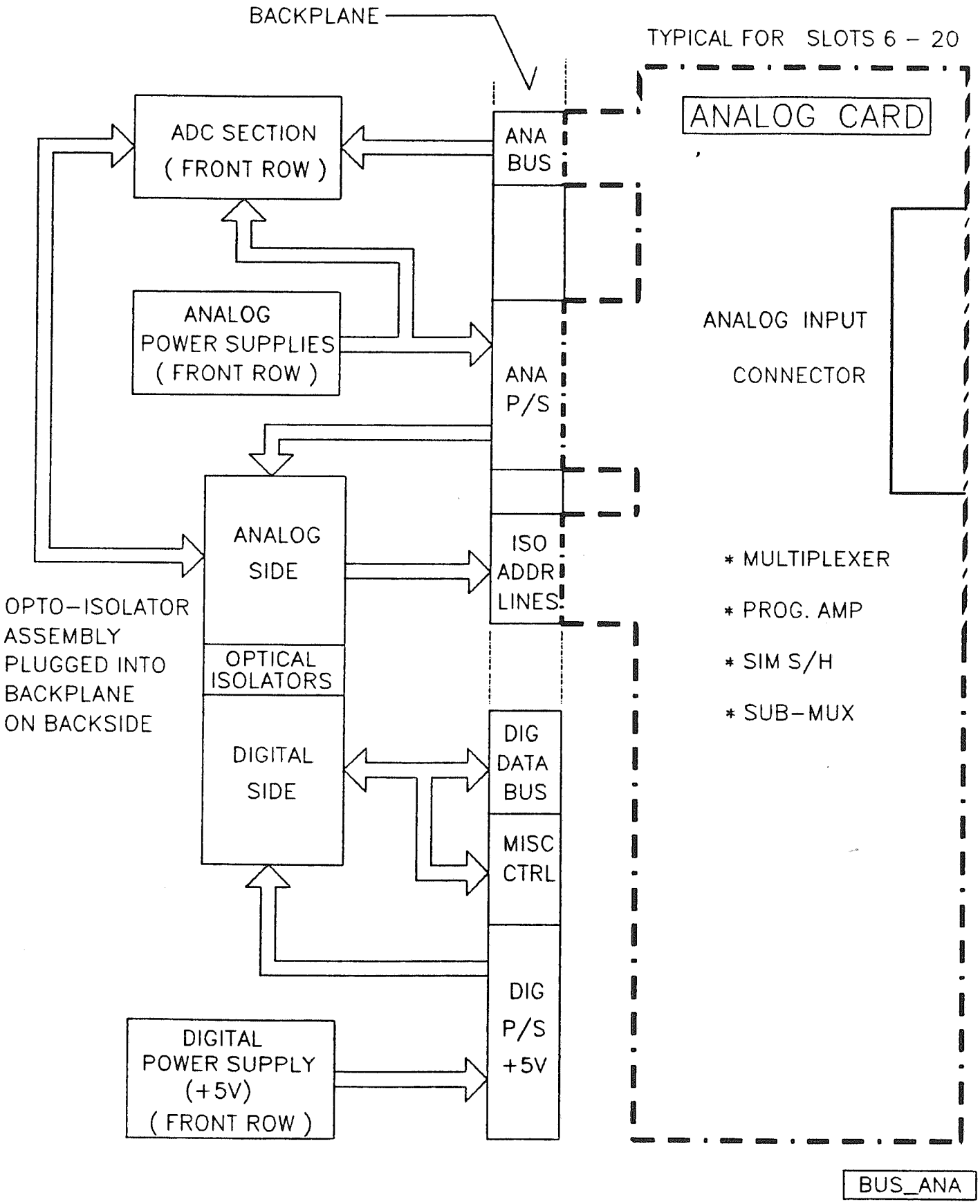
FIGURE 3-9A
BUS_OVER
BUS_ANA
BUS_DIG
BUS_ADC
BUS_DAC

PRESYS BUS / BACKPLANE OVERVIEW

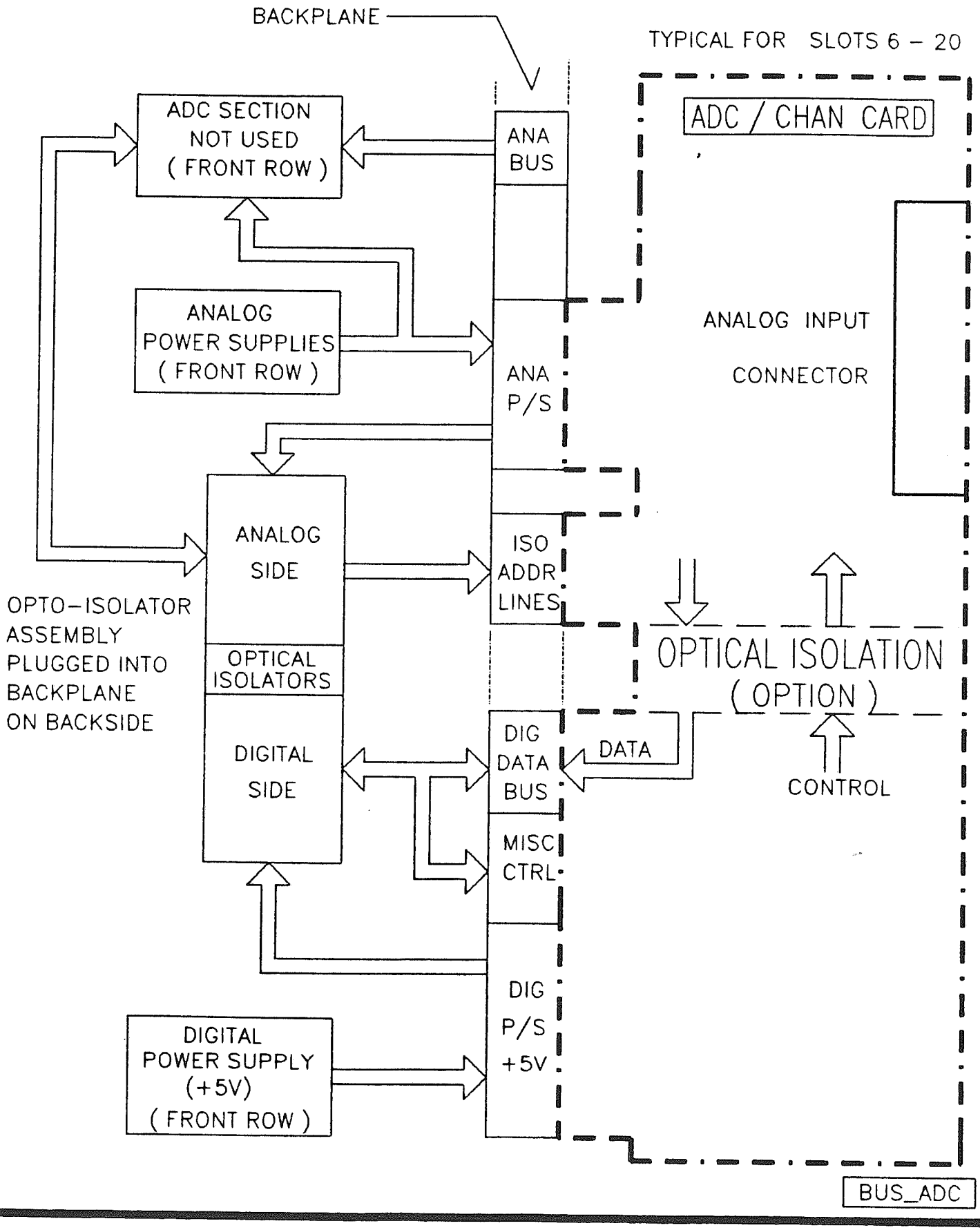


BUS_OVER

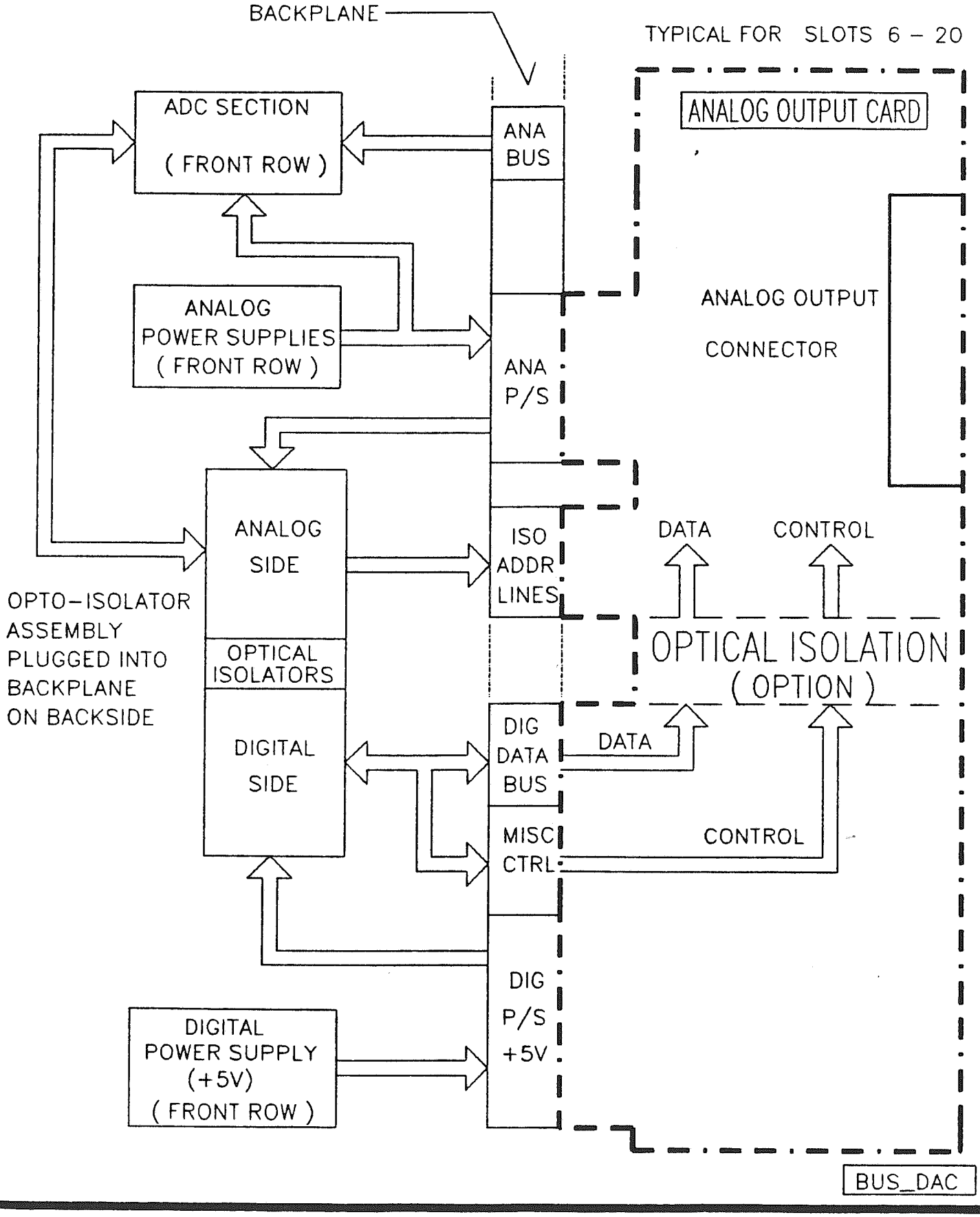
PRESYS BUS / BACKPLANE OVERVIEW



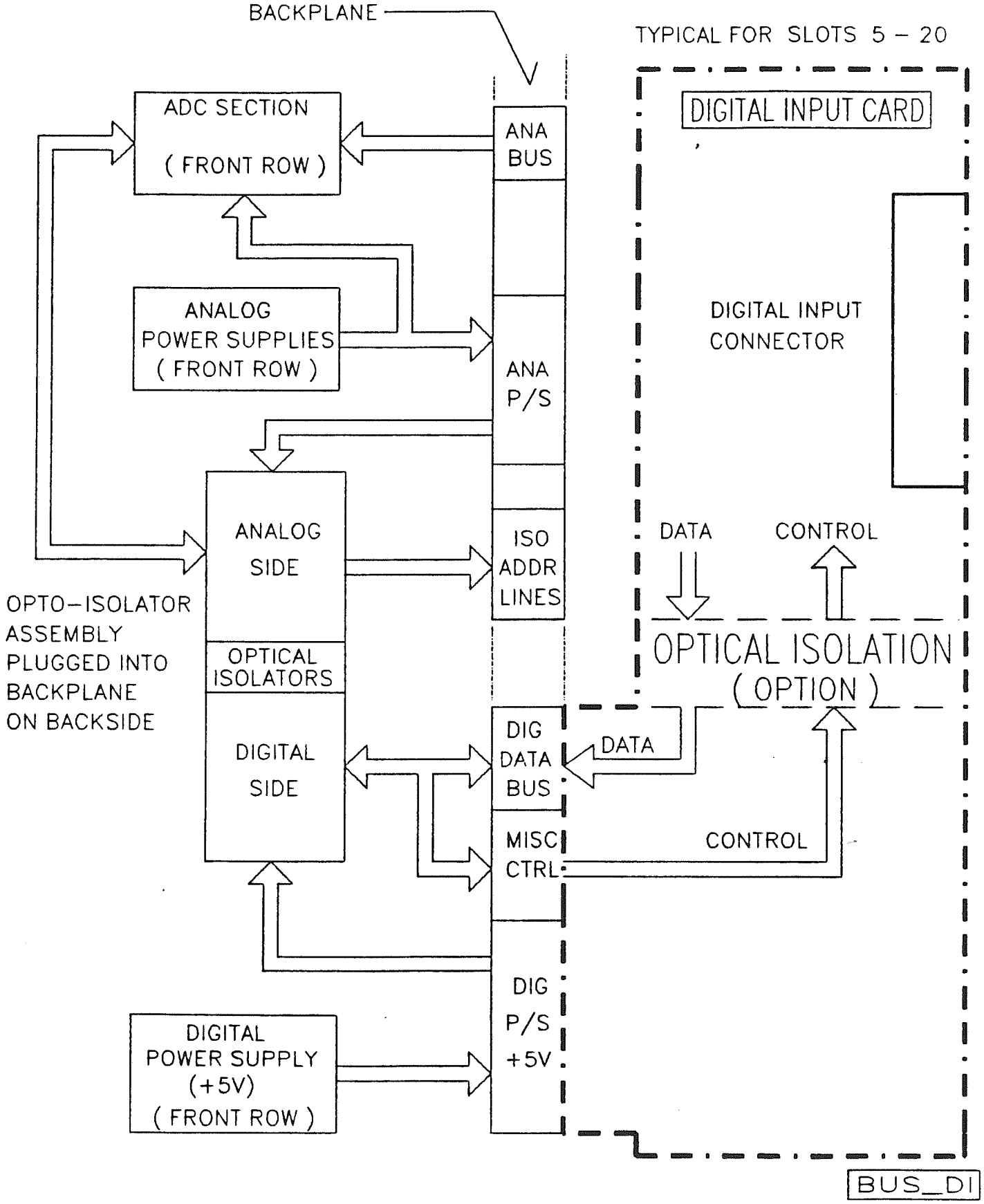
PRESYS BUS / BACKPLANE OVERVIEW



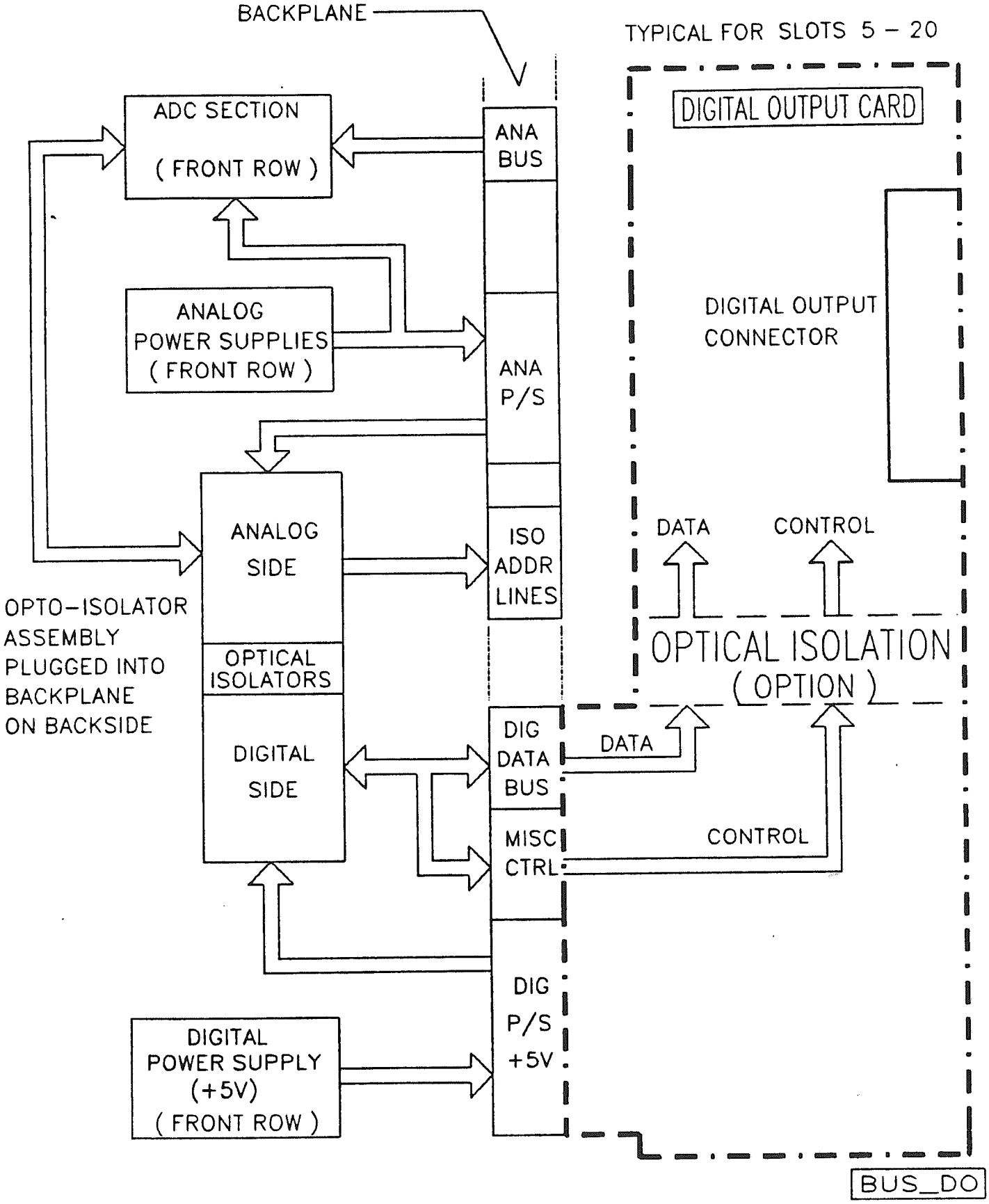
PRESYS BUS / BACKPLANE OVERVIEW



PRESYS BUS / BACKPLANE OVERVIEW



PRESYS BUS / BACKPLANE OVERVIEW



INSTALLATION

The figure on the following page indicates the preferred method for mounting a PRESYS system chassis into a cabinet. Rails, as indicated, or some alternate device are required to support the weight.

Since the PRESYS systems may be installed into many types of cabinets the rails are NOT supplied by Preston.

The top cover of the PRESYS chassis has slots for airflow. A spacer panel of at least 1.75 inches in height(minimal RETMA standard) should be installed directly above this unit. This assures that the airflow in the unit will be approximately the same when installed in a rack as on the bench where calibration was performed.

Blank panels are installed in all empty slots in the rear of the chassis to block airflow through these openings and keep all input air passing over the cards installed. If some new item should be added the corresponding blank cover must first be removed. If a card is removed, one should be installed. If not available, use some other temporary material to cover the resulting opening.

It would be good practice to save the blank panels if an item is removed. If some other module is removed for any reason this cover can be installed in its place. It is also a good idea to save the shipping container in case the unit should need be sent back to the factory or some other authorized service center.

All user connections to the PRESYS are made via connectors mounted on the back of the plug in cards.

After the PRESYS 1000 chassis has been installed in the cabinet the following procedure is recommended:

* A: Verify power switch is in the OFF position. If not place it to the OFF position.

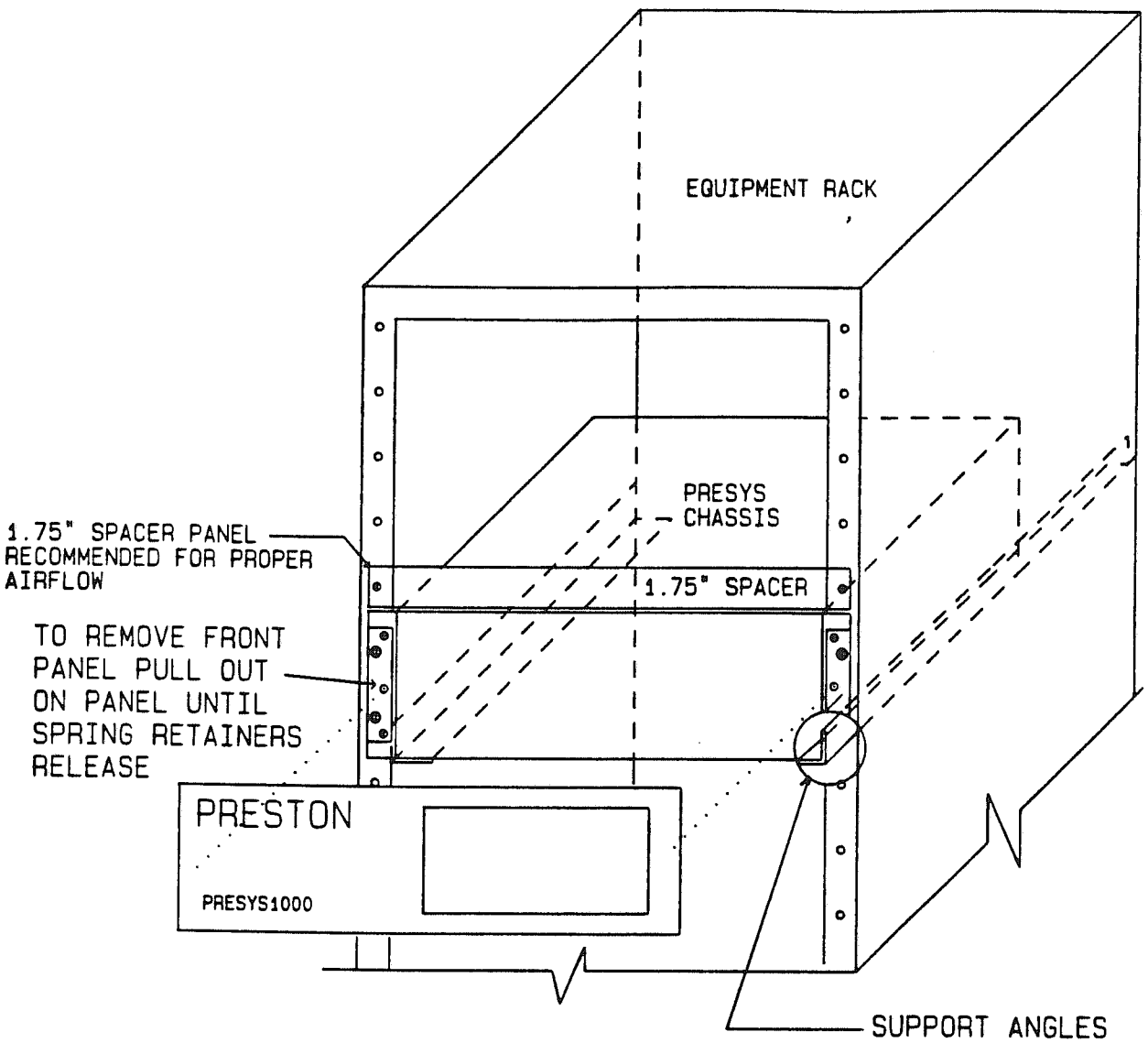
* B: Verify that input ac voltage in the cabinet agrees with that indicated on power tag mounted above power cord.

* C: With input signal sources set to nominal 0 volt levels make appropriate connections to input signals.

* D: Connect interface cables to computer or external controller.

* E: Place power switch to the ON position and allow a 1 hour warm up period to guarantee rated accuracy.

* F: During the warm up time the system is operational and may be used for all functions but at a lesser degree of accuracy from the analog components.



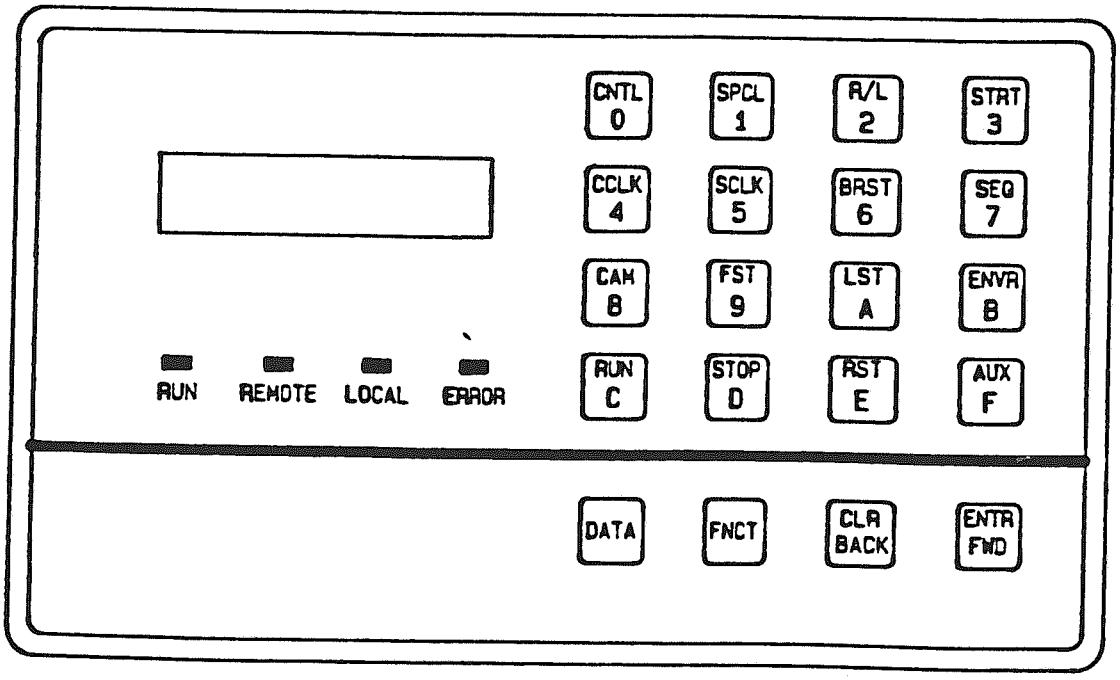
PRESYS 1000 INSTALLATION

FILE: PRE_INST

PRESTON SCIENTIFIC

PRESYS 1000

FRONT PANEL QUICK REFERENCE



OPERATOR KEY DESCRIPTIONS

Must press this key for any DATA entry. Makes keys the hexidecimal value black screened on the keys. Sometimes this key is used to move to another display.

This key places all keys back to their FUNCTION mode, the white screened lettering on the key.

This key CLEARS an entry leaving that display unchanged or scrolls a display BACKWARD.

This key causes system to accept an ENTRY or scrolls a display FORWARD.

KEY DEFINITIONS

KEY	DESCRIPTION	FIGURE
CNTL 0	Display / change CONTROL WORD or EXTENSION WORD . .	100
	Display individual CONTROL BITS or EXTENSION BITS. .	101
SPCL 1	Load User defined defaults	102
R/L 2	Change modes REMOTE / LOCAL	103
STRT 3	Display / change INTERNAL or EXTERNAL START mode . .	104
CCLK 4	Display / change BURST CHANNEL RATE CLOCK or . . . . PRESCALE CLOCK divisor	105
SCLK 5	Display / change SCAN CLOCK divisor or . . . . . CLOCK SOURCE	106
BRST 6	Display / change BURST or NON-BURST mode	107
SEQ 7	Display / change SEQUENTIAL or RANDOM mode	108
CAM 8	Display / change CAM ENABLED or CAM DISABLED mode. .	109
	Display / change CAM ADDRESS or CAM DATA	110
FST 9	Display / change FIRST CHANNEL ADDRESS or . . . . . 2nd, 3rd, 4th PARTITION FIRST ADDRESSES	111
LST A	Display / change LAST CHANNEL ADDRESS or . . . . . 2nd, 3rd, 4th PARTITION LAST ADDRESSES	112

KEY DEFINITIONS

KEY	DESCRIPTION		FIGURE
ENVR B	Display / change ENVIROMENT information		
	Display WAITING FOR information	(env 1) .	113
	Display ERROR LIST	(env 2) .	114
	Display PROM REV and DATE	(env 3) .	115
	Display / change ADC DATA DISPLAY FORMAT .	(env 4) .	116
	Display / change CAM DATA DISPLAY FORMAT .	(env 5) .	117
	Display / change MISCELLANEOUS SETTINGS . .	(env 6) .	118
	ADC RESOLUTION		
	ADC OFFSET		
	ADC FULLSCALE		
	REMAKE DEFAULTS		
	CRYSTAL FREQUENCY		
	EXTERNAL MUXCLK source with EXT BURST CLOCK		
	STOP* CLOCK SOURCE		
	MASTER or SLAVE chassis		
	EXTERNAL START EDGE		
	EXTERNAL CLOCK EDGE		
	STOP* or COIN START		
	SIMULTANEOUS HOLD CAM ENABLE		
	CAM RESTART EDGE		
	DIAGNOSTICS		
RUN C	Place system into a LOCAL RUN condition		121
	Display ADC DATA or DIGITAL IN DATA		
STOP D	Place system into a LOCAL STOPPED condition		122
RST E	Place system into a RESET condition		123
	Put system into FACTORY DEFAULT state (poweron reset)		124
AUX F	Display / change BUS TALK DATA or ANALOG BUS DATA . .		125

■ DISPLAY CONTROL WORD or EXTENSION WORD

[FNCT] [CNTL 0] "CONTROL WORD"

or

[FNCT] [CNTL 0] [CNTL 0] "EXTENSION WORD"

■ CHANGE CONTROL WORD or EXTENSION WORD

Use above steps to get the desired display, then press

[DATA] followed by [CNTL 0] or [SPCL 1] as required, then press

[ENTR FWD]

use [CLR BACK] to restore to original state

use [FNCT] to put panel in function mode

figure 100

■ DISPLAY CONTROL WORD or EXTENSION WORD

[FNCT] [CNTL 0] "CONTROL WORD"

or

[FNCT] [CNTL 0] [CNTL 0] "EXTENSION WORD"

■ DISPLAY CONTROL BITS or EXTENSION BITS

Use above steps to get the desired display, then press

[ENTR FWD] to scroll Forward through the control bits , or

[CLR BACK] to scroll Backward through the control bits.

use [FNCT] to put panel in function mode

figure 101

■ LOAD USER DEFINED DEFAULTS

FNCT | SPCL 1 | ENTR FWD | DATA | SPCL 1 | ENTR FWD

figure 102

■ CHANGE MODES REMOTE / LOCAL

FNCT | R/L 2 "REMOTE REGISTERS"

or

FNCT | R/L 2 "LOCAL REGISTERS"

use FNCT to put panel in function mode

figure 103

DISPLAY START MODE

FNCT STRT 3 "INT START" or "EXT START"

CHANGE START MODE

FNCT STRT 3 "INT START" or "EXT START" ENTR FWD

use FNCT to put panel in function mode

figure 104

■ DISPLAY BURST CHANNEL RATE CLOCK or PRESCALE DIVISOR

FNCT CCLK 4 "BURST CHAN CLK"

or

FNCT CCLK 4 CCLK 4 "CLOCK PRESCALE"

■ CHANGE BURST CHANNEL RATE CLOCK or PRESCALE DIVISOR

Use above steps to get the desired display, then press

DATA followed by the Divisor value desired , then press

ENTR FWD

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 105

■ DISPLAY SCAN CLOCK DIVISOR or CLOCK SOURCE

FNCT SCLK 5 "SCAN RATE CLK"

or

FNCT SCLK 5 "SCAN RATE CLK" ENTR FWD "INTERNAL SOURCE" or "EXTERNAL SOURCE"

■ CHANGE SCAN CLOCK DIVISOR or CLOCK SOURCE

To change the Divisor press . FNCT SCLK 5 then press DATA followed by the Divisor value desired . then press ENTR FWD

To change clock source press .

FNCT SCLK 5 ENTR FWD "INTERNAL SOURCE" or "EXTERNAL SOURCE" ENTR FWD

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 106

DISPLAY BURST MODE

FNCT BRST 6 → "BURST MODE" or "NON-BURST MODE"

CHANGE BURST MODE

FNCT BRST 6 → "BURST MODE" or "NON-BURST MODE" → ENTR FWD

use FNCT to put panel in function mode

figure 107

DISPLAY SEQUENCE MODE

FNCT SEQ 7 "RANDOM MODE" or "SEQUENCE MODE"

CHANGE SEQUENCE MODE

FNCT SEQ 7 "RANDOM MODE" or "SEQUENCE MODE" ENTR FWD

use FNCT to put panel in function mode

figure 108

DISPLAY CAM MODE

FNCT CAM 8 "ENABLE CAM" or "DISABLE CAM"

CHANGE CAM MODE

FNCT CAM 8 "ENABLE CAM" or "DISABLE CAM" ENTR FWD

use FNCT to put panel in function mode

figure 109

DISPLAY CAM DATA

FNCT CAM 8 DATA "CAM ADDR = "
"CAM DATA = "

ENTR FWD to scroll Forward through CAM list , or

CLR BACK to scroll Backward through CAM list.

CHANGE CAM DATA

- METHOD 1: CHANGE OF DATA BETWEEN FIRST AND LAST

Use above steps to advance to desired location, press DATA

DATA followed by the desired data value, then press ENTR FWD

- METHOD 2: .CHANGE OF DATA AT ANY LOCATION

Use above steps to get to CAM display, then press DATA

followed by the desired address value, then press ENTR FWD

Next press DATA DATA followed by the data value desired,

then press ENTR FWD

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 110

■ DISPLAY FIRST CHANNEL ADDRESS or FIRST PARTITION ADDRESSES

[FNCT] [FST 9] "FIRST ADDRESS"

or

[FNCT] [FST 9] [FST 9] "FRST PART ADDR2"

or

[FNCT] [FST 9] [FST 9] [FST 9] "FRST PART ADDR3"

or

[FNCT] [FST 9] [FST 9] [FST 9] [FST 9] "FRST PART ADDR4"

■ CHANGE FIRST CHANNEL ADDRESS or FIRST PARTITION ADDRESSES

Use above steps to get the desired display, then press

[DATA] followed by the Address value desired , then press

[ENTR FWD]

use [CLR BACK] to restore to original state

use [FNCT] to put panel in function mode

figure 111

■ DISPLAY LAST CHANNEL ADDRESS or LAST PARTITION ADDRESSES

FNCT LST A "LAST ADDRESS"

or

FNCT LST A LST A "LAST PART ADDR2"

or

FNCT LST A LST A LST A "LAST PART ADDR3"

or

FNCT LST A LST A LST A LST A "LAST PART ADDR4"

■ CHANGE LAST CHANNEL ADDRESS or LAST PARTITION ADDRESSES

Use above steps to get the desired display, then press

DATA followed by the Address value desired , then press

ENTR FWD

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 112

■ DISPLAY WAITING FOR INFORMATION.

FNCT ENVR B "ENVIROMENT = 1" ENTR FWD "WAITING FOR"

figure 113

■ DISPLAY ERROR LIST

FNCT ENVR B DATA R/L 2 ENTR FWD "ERR 1 = "

ENTR FWD to scroll Forward through the list

CLR BACK to scroll Backward through the list

figure 114

■ DISPLAY PROM REVISION AND DATE

FNCT ENVR B DATA STRT 3 ENTR FWD "PROM1 9988-XX"

ENTR FWD "PROM2 9989-XX"

use FNCT to put panel in function mode

figure 115

DISPLAY ADC DATA FORMAT FOR DISPLAY

FNCT ENVR B DATA CCLK 4 ENTR FWD "SIGNAL = "

CHANGE ADC DATA FORMAT FOR DISPLAY

Use above steps to get to the format display, then press DATA followed by the value corresponding to the desired display format. Then press ENTR FWD

figure 116

DISPLAY CAM DATA FORMAT FOR DISPLAY and DATA ENTRY

FNCT ENVR B DATA SCLK 5 ENTR FWD "CAM DATA = "

CHANGE CAM DATA FORMAT FOR DISPLAY and DATA ENTRY

Use above steps to get to the format display, then press DATA followed by the value corresponding to the desired display format. Then press ENTR FWD

figure 117

DISPLAY MISCELLANEOUS ENVIROMENT SETTINGS

FNCT ENVR B DATA BRST 6 ENTR FWD "ADC RESOLUTION"

ENTR FWD to scroll Forward through the list settings, or

CLR BACK to scroll Backward through the list settings.

CHANGE MISCELLANEOUS ENVIROMENT SETTINGS

Use above steps to get to the desired setting, then press DATA followed by the value corresponding to the desired setting, then press ENTR FWD

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 118

DISPLAY BOARD DEFINITION TABLE

FNCT | ENVR 8 | DATA | SEQ 7 | ENTR FWD "BD 0 TYPE 8000"

ENTR FWD to scroll Forward through the list settings, or

CLR BACK to scroll Backward through the list settings.

CHANGE BOARD DEFINITION TABLE

Use above steps to get to the desired board, then press DATA followed by the value corresponding to the desired setting, then press ENTR FWD . If the data for the setting is already as desired then press CLR BACK to skip to the next setting for that board.

use CLR BACK to restore to original state

use FNCT to put panel in function mode

figure 119

■ DISPLAY REMOVED BOARD LIST

[FNCT] [ENVR B] [DATA] [CAM B] [ENTR FWD] "REMOVED BOARD 0"

[ENTR FWD] to scroll Forward through the list, or

[CLR BACK] to scroll Backward through the list.

■ CHANGE REMOVED BOARD LIST

Use above steps to get to the removed board display, press [DATA] followed by the starting address value of the removed board, then press [ENTR FWD] . Now enter the board length (number of channels on the board or 0), then press [ENTR FWD] Use 0 as the length to remove board from list.

use [FNCT] to put panel in function mode

figure 120

■ PLACE SYSTEM INTO LOCAL RUN CONDITION or DISPLAY ADC DATA or DIGITAL IN DATA

[FNCT] [RUN C] "CHANNEL = 0"

[ENTR FWD] to scroll Forward through the active channels, or

[CLR BACK] to scroll Backward through the active channels

■ CHANGE CHANNEL DISPLAYED

Use above steps to get to the channel display, then press [DATA] followed by the address of the channel to display, then press [ENTR FWD] . Data will only be displayed on those channels scanned.

use [FNCT] to put panel in function mode

figure 121

■ PLACE SYSTEM INTO A LOCAL STOP CONDITION

FNCT STOP D "SYSTEM STOPPED"

figure 122

■ PLACE SYSTEM INTO A RESET CONDITION

FNCT RST E "TO RESET SYSTEM" ENTR FWD "RESET COMPLETE"

figure 123

■ PUT SYSTEM INTO FACTORY DEFAULT STATE

Hold the RST E while powering up the system.

use FNCT to put panel in function mode

figure 124

DISPLAY BUS TALK DATA

[FNCT] [AUX F] "ID ADDRS = "
"BUS DATA = "

[ENTR FWD] to send data as shown on display to the Bus.

If ID = 100, the data will also be sent to the Analog Data Bus.

CHANGE ID or BUS DATA

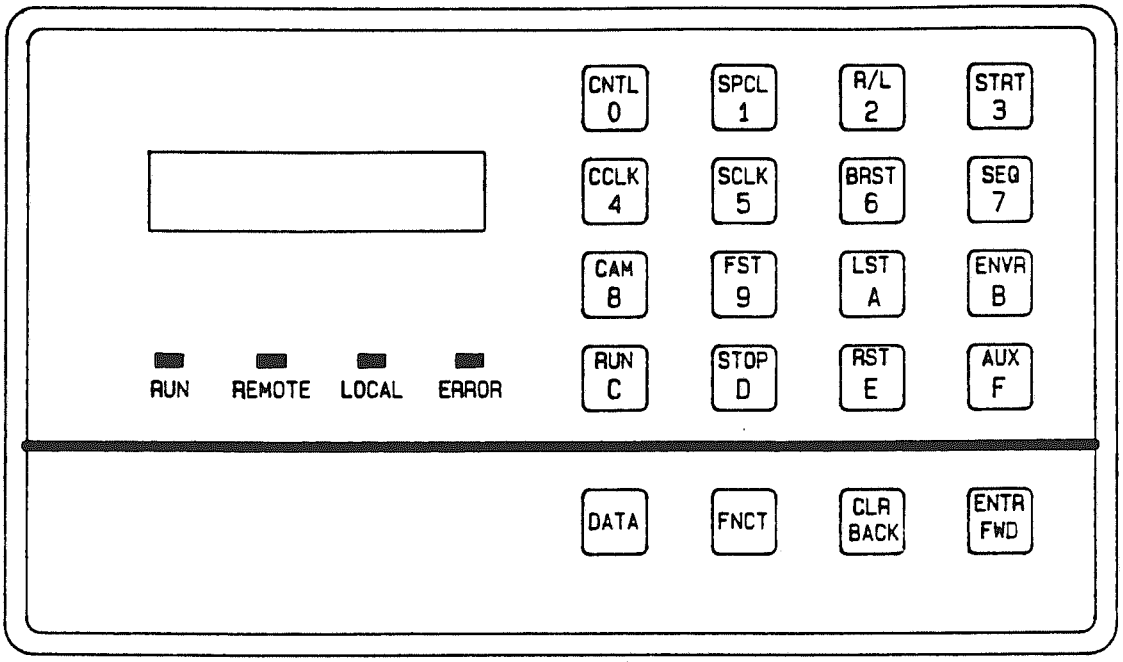
- To change the ID address, use steps above to get to the ID BUS display, then press [DATA] followed by ID data, then press [ENTR FWD]

- To change the BUS data, use the steps above to get to the ID BUS display, then press [DATA] [DATA] followed by BUS data, then press [ENTR FWD]

use [CLR BACK] to restore to original state

use [FNCT] to put panel in function mode

figure 125



PRESYS 1000

FRONT PANEL CONTROLS

CONTROL PANEL KEY STROKES

The sequence of keystrokes is based on the assumption that the user is always starting from the "FUNCTION" level (first level) which can be reached by pressing the key labeled "FNCT". In general, except when the system is waiting for data to be entered, the system will remain at the "FUNCTION" level.

When a display is followed by an "L" or an "R", this will remind the user that the information displayed is from the "Local" or from the "Remote" registers. Only formatting and display parameters may be entered in the "REMOTE" mode while all parameters may be entered in the "LOCAL" mode. If the computer has set the "LOCAL LOCKOUT" bit in the 'CONTROL WORD" then the "LOCAL" mode will be restricted to the same entries as the "REMOTE" mode.

The keys are designated as follows:

KEY	FUNCTION	DESCRIPTION
0	CNTL	Command Control Word
1	SPCL	Special Control Functions
2	R/L	Remote Local Register Mode Control
3	STRT	Start Mode and Start Control
4	CCLK	Clock Prescaler and Burst Channel Rate
5	SCLK	Scan Rate Clock
6	BRST	Burst or Non-Burst Mode
7	SEQ	Sequence or Random Mode
8	CAM	Cam Enable/Disable and Data
9	FST	First Channel Data
A	LST	Last Channel Data
B	ENVR	Set System Environment
C	RUN	Start System and Read Channel Data
D	STOP	Stop the System
E	RST	Reset the System
F	AUX	Auxiliary Functions
CB	CLR BACK	Clear Entry or Backspace
DA	DATA	Enable Data Display and Entry
EF	ENTR FWD	Enter Data or Step Forward
FN	FNCT	Return to the FUNCTION Level

The functional description of each control panel key is described in the following paragraphs. A hexadecimal coding is used to number the paragraphs so that the number of the each paragraph represents the sequence of keystrokes necessary to reach the described function. In addition to the sixteen data keys are the four control keys, "DATA", "FNCT", "CLR BACK", and "ENTR FWD". These four keys are abbreviated to "DA", "FN", "CB", and "EF". A double dot (..) following a key indicates one or more repeat pressings of that key.

0 The "CNTL" key.

The "CNTL" key performs three functions, view the Command Word, change the Command Word, and view the decoded bits of the Command Word.

Pressing the "CNTL" (0) key will cause the first line of the display to read "CONTROL WORD" followed by an "L" or an "R". On the second line of the display is the 16 bit Command Word displayed in binary notation.

0.DA The Control Word data entry mode in "LOCAL" only.

In this mode a flashing cursor appears over one of the binary bits of the displayed Control Word. The data bit can be changed or the cursor moved.

0.DA.0 Cause the data bit at the cursor to be a zero and the cursor to move to the right to the next bit that the user is permitted to change.

0.DA.1 Cause the data bit at the cursor to be a one and the cursor to move to the right to the next bit that the user is permitted to change.

0.DA.n.CB Where "n" is a "0" or a "1", pressing the "CLR BACK" key will cause the cursor to move to the left to the next previous bit that the user is permitted to change.

0.DA.n.EF Where "n" is any number of "0", "1", or "CLR BACK" key pressings, pressing the "ENTR FWD" key will cause the modified Control Word to be entered.

0.CB Cause the first line of the display to read "BIT NUMBER 1" followed by "L" or "R". The second line of the display will display the decoded control function together with it's state.

0.CB.. Subsequent pressing of the "CLR BACK" key will cause the bit number to increment through the bits of the control word displaying the state and function of each bit.

0.EF Cause the first line of the display to read "BIT NUMBER 15" followed by "L" or "R". The second line of the display will display the decoded control function together with it's state.

0.EF.. Subsequent pressing of the "ENTR FWD" key will cause the bit number to decrement through the bits of the control word displaying the state and function of each bit.

0.n.. Where "n" is any number of "ENTR FWD" and "CLR BACK" key pressings will increment and decrement through the bits of the control word displaying the state and function of each bit.

1 The "SPCL" key.

The "SPCL" key reloads the default system parameters in "LOCAL" only.

Pressing the "SPCL" (1) key will cause the first line of the display to read "SPECIAL FUNCTION". The second line of the display will read "PRESS ENTR/FWD".

1.EF Pressing the "ENTR FWD" key will cause the first line of the display to read "DEFLT PARAMTRS". The second line of the display will read "0=NO 1=YES.

1.EF.DA Pressing the "DATA" key will cause the blinking cursor to appear at the end of the second line in "LOCAL" only.

1.EF.DA.0 Pressing the "0" key will display a "0" at the blinking cursor.

1.EF.DA.0.EF Pressing the "ENTR FWD" key will cause the control word to be displayed as in step 0 without change.

1.EF.DA.1 Pressing the "1" key will display a "1" at the blinking cursor.

1.EF.DA.1.EF Pressing the "ENTR FWD" key will cause the control word to be changed to the default value and displayed as in step 0.

2 The "R/L" key.

Pressing the "R/L" (2) key will cause the mode of the other keys to change between displaying (only) the data stored in the remote registers and displaying and changing, if desired, the data stored in the local registers. Each time this key is pressed the mode will change. The first line of the display will read "LOCAL REGISTERS" or "REMOTE REGISTERS" as applicable.

3 The "STRT" key.

The "STRT" key will display and change the start mode of the system between internal and external start.

Pressing the "STRT" (3) key will cause the first line of the display to read "INT START" or "EXT START", depending on the current mode of the system, followed by an "L" or an "R". If the display is in the remote mode and an "R" is displayed, the second line of the display will remain blank. If the display is in the local mode and an "L" is displayed then the second line will read "PRESS ENTR/FWD".

3.EF Pressing the "ENTR FWD" key when in the local display mode will cause the system to switch to the alternate mode which will be displayed.

4 The "CCLK" key.

The "CCLK" key will display and change the Burst Mode Channel Rate Clock and the Master Clock Prescaler. Pressing this key repetitively will cause the display to toggle between the Burst Mode Channel Rate Clock and the Master Clock Prescaler.

Pressing the "CCLK" (4) key will cause the first line of the display to read "BURST CHAN CLK", followed by an "L" or an "R". The second line of the display will read "DIV = nnn", where "nnn" is the decimal value of the divisor that divides the System Operating Clock down to the Burst Channel Clock rate.

4.DA Pressing the "DATA" key while in the "LOCAL" mode will cause the second line of the display to read "DIV =" only with a flashing cursor at the position of the first digit of the divisor value.

4.DA.n.. Pressing the keys "0" through "9" will record a new value for the Burst Channel Clock Divisor.

4.DA.n..CB Pressing the "CLR BACK" key will delete the new entry, retaining the old divisor value, and change the display to be the same as prior to pressing the "DATA" key.(PRS4).

4.DA.n..EF Pressing the "ENTR FWD" key will cause the new divisor to be entered into the system.

4.4 Pressing the "CCLK" key a second time will cause the first line of the display to read "CLOCK PRESCALE", followed by an "L" or an "R". The second line of the display will read "DIV = nnn", where "nnn" is the decimal value of the divisor that divides the System Operating Clock down to the Prescaler Clock rate.

4.4.DA Pressing the "DATA" key while in the "LOCAL" mode will cause the second line of the display to read "DIV =" only with a flashing cursor at the position of the first digit of the divisor value.

4.4.DA.n.. Pressing the keys "0" through "9" will record a new value for the Prescaler Clock Divisor.

4.4.DA.n..CB Pressing the "CLR BACK" key will delete the new entry, retaining the old divisor value, and change the display to be the same as if the 4.4 key stroke had been pressed.

4.4.DA.n..EF Pressing the "ENTR FWD" key will cause the new divisor to be entered into the system, and change the display to be the same as if the 4.4 key stroke had been pressed.

5 The "SCLK" key.

The "SCLK" key will display and change the Scan Rate Clock which is the clock that sets the rate at which the Burst Scans occur in the Burst Mode and the rate at which the channels are scanned in the non-burst mode.

Pressing the "SCLK" (5) key will cause the first line of the display to read "SCAN RATE CLK", followed by an "L" or an "R". The second line of the display will read "DIV = nnn", where "nnn" is the decimal value of the divisor that divides the System Operating Clock down to the Scan Rate Clock.

5.DA Pressing the "DATA" key in the "LOCAL" mode will cause the second line of the display to read "DIV =" only with a flashing cursor at the position of the first digit of the divisor value.

5.DA.n.. Pressing the keys "0" through "9" will record a new value for the Scan Rate Clock Divisor.

5.DA.n..CB Pressing the "CLR BACK" key will delete the new entry, retaining the old divisor value, and change the display to be the same as if a "5" key stroke had been pressed.

5.DA.n..EF Pressing the "ENTR FWD" key will cause the new divisor to be entered into the system.

5.EF Pressing the "ENTR FWD" key in the "LOCAL" mode will cause the source of the scan clock to switch between internal and external.

6 The "BRST" key.

The "BRST" key will display and change the running mode of the system between burst mode and non-burst mode.

Pressing the "BRST" (6) key will cause the first line of the display to read "BURST MODE" or "NON-BURST MODE", depending on the current mode of the system, followed by an "L" or an "R". If the display is in the remote mode and an "R" is displayed, the second line of the display will remain blank. If the display is in the local mode and an "L" is displayed then the second line will read "PRESS ENTR/FWD".

6.EF Pressing the "ENTR FWD" key when in the local display mode will cause the system to switch to the alternate mode.

7 The "SEQ" key.

The "SEQ" key will display and change the running mode of the system between the sequence mode and the random mode.

Pressing the "SEQ" (7) key will cause the first line of the display to read "SEQUENCE MODE" or "RANDOM MODE", depending on the current mode of the system, followed by an "L" or an "R". If the display is in the remote mode and an "R" is displayed, the second line of the display will remain blank. If the display is in the local mode and an "L" is displayed then the second line will read "PRESS ENTR/FWD".

7.EF Pressing the "ENTR FWD" key when in the local display mode will cause the system to switch to the alternate mode.

8 The "CAM" key.

The "CAM" key will display and change the enabled or disabled status of the channel address memory and display and enter data into the memory.

Pressing the "CAM" (8) key will cause the first line of the display to read "ENABLE CAM" or "DISABLE CAM", depending on the current mode of the system, followed by an "L" or an "R". If the display is in the remote mode and an "R" is displayed, the second line of the display will remain blank. If the display is in the local mode and an "L" is displayed then the second line will read "PRESS ENTR/FWD".

8.DA Pressing the "DATA" key will cause the first line of the display to read "CAM ADDR= nnnn", where "nnnn" is the First Address, and the second line of the display to read "CAM DATA= dddd", where "dddd" is the data stored in the addressed memory location. The address "nnnn" is always displayed in decimal notation and the data "dddd" is displayed in the format selected in the Environment entry function.

8.DA.DA Pressing the "DATA" key a second time will cause the first line of the display to read "CAM ADDR=", with the cursor placed at the position to enter a new address.

8.DA.DA.DA Pressing the "DATA" key a third time in the "LOCAL" mode will cause the first line of the display to read "CAM ADDR= nnnn", where "nnnn" is the current address, and the second line of the display to read "CAM DATA=" with the cursor placed at the position to enter the new cam data. The data must be entered in the same format as the data is displayed.

8.DA.DA.DA.n.. Pressing the keys "0" through "7", "0" through "9", or "0" through "F", will record a new value for the cam data.

8.DA.DA.DA.n..CB Pressing the key "CLR BACK" will delete the new value, retaining the old value, and change the display to be the same as if 8.DA.DA.n..EF key strokes had been pressed.

8.DA.DA.DA.n..EF Pressing the key "ENTR FWD" will cause the data to change to the entered value, and change the display to be the same as if 8.DA.DA.n..EF key strokes had been pressed.

8.DA.DA.n.. Pressing the keys "0" through "9" will record a new value for the address to be displayed.

8.DA.DA.n..CB Pressing the key "CLR BACK" will delete the new value, retaining the old value, and change the display to be the same as if 8.DA.DA key strokes had been pressed.

8.DA.DA.n..EF Pressing the key "ENTR FWD" will cause the address to change to the entered value, and change the display to be the same as if 8.DA.DA key strokes had been pressed.

8.DA.EF Pressing the "ENTR FWD" key will cause the cam address to advance to the next address and display that data.

8.DA.EF.. Pressing the "ENTR FWD" key additional times will cause the address to advance each time and display that data. When the Last Address has been reached the address will wrap around to the First Address.

8.DA.EF..DA Pressing the "DATA" key after any number of "ENTR FWD" keys is the same as key strokes 8.DA.DA for the displayed address (PRS4).

8.EF Pressing the "ENTR FWD" key when in the local display mode will cause the system to switch to the alternate mode.

9 The "FST" key.

The "FST" key will display and change the First Channel which is the first sequencer position of any multiplexer scan.

Pressing the "FST" (9) key will cause the first line of the display to read "FIRST CHANNEL", followed by an "L" or an "R". The second line of the display will read "CHAN = nnn", where "nnn" is the decimal value of the current first channel.

9.DA Pressing the "DATA" key in the "LOCAL" mode will cause the second line of the display to read "CHAN =" only with a flashing cursor at the position of the first digit of the address value.

9.DA.n.. Pressing the keys "0" through "9" will record a new value for the First Channel.

9.DA.n..CB Pressing the "CLR BACK" key will backspace, deleting the most recently entered digit.

9.DA.n..EF Pressing the "ENTR FWD" key will cause the new first channel value to be entered into the system.

A The "LST" key.

The "LST" key will display and change the Last Channel which is the last sequencer position of any multiplexer scan.

Pressing the "LST" (A) key will cause the first line of the display to read "LAST CHANNEL", followed by an "L" or an "R". The second line of the display will read "CHAN = nnn", where "nnn" is the decimal value of the current last channel.

A.DA Pressing the "DATA" key in the "LOCAL" mode will cause the second line of the display to read "CHAN =" only with a flashing cursor at the position of the first digit of the address value.

A.DA.n.. Pressing the keys "0" through "9" will record a new value for the Last Channel.

A.DA.n..CB Pressing the "CLR BACK" key will backspace, deleting the most recently entered digit.

A.DA.n..EF Pressing the "ENTR FWD" key will cause the new Last channel value to be entered into the system.

B The "ENVR" key.

The "ENVR" (B) key will display and change the Environment variables of the system. The environment variables include System Status, Error Status, date and version of the operating system, ADC data display format, CAM data display format, system default settings, the resolution of the ADC, the full scale and offset of the ADC in millivolts, and chassis setup information.

Pressing the "ENVR" key will cause the first line of the display to read "ENVIRONMENT = 1" and the second line of the display to read "PRESS ENTR/FWD".

B.DA Pressing the "DATA" key will cause the digit "1" to be replaced by the cursor.

B.DA.n Pressing keys "2" through "8" will select the desired ENVIRONMENT to view or change.

ENV #	ENVIRONMENT
1	EXPECTED COMMAND
2	ERROR HISTORY
3	PROM PART NUMBER, VERSION, AND DATE
4	ADC DATA FORMAT
5	CAM DATA FORMAT
6	ADC RESOLUTION, OFFSET, FULL SCALE, REMAKE RESET, SET CRYSTAL FREQUENCY, EXTERNAL CLOCKS, STOP CLOCK SOURCE, MASTER/SLAVE, START PULSE EDGE, CLOCK PULSE EDGE, START, SIM CAM BIT, CAM RESTART EDGE, DIAGNOSTIC CAM MODE.
7	CHASSIS CIRCUIT BOARD LIST
8	REMOVED BOARD LIST

B.DA.1.EF Pressing the B.DA.1.EF key sequence provides the user with the present state of the system in terms of the sequence of commands. If the system is running, the first line of the display will read "SYSTEM RUNNING". If the system is not running then the first line of the display will read "WAITING FOR" and the second line of the display will usually read "CONTROL WORD". In the event that an incomplete sequence of commands has been sent from the host

computer then the second line of the readout may read "CAM DATA", "CLOCK DIV", "FST CHAN", "LST CHAN", "RUN ENABLE", or "START".

B.DA.2.EF Pressing the B.DA.2.EF key sequence provides the user with a readout of up to 32 error codes. After 32 error codes have been recorded, any further errors will be disregarded until the 32 recorded error codes have been erased. ' Errors due to incorrect keyboard entries are not recorded.

If there are no errors recorded then the first line of the display will read "NO ERRORS".

If there are errors then the first line of the display will read "ERROR 1 = nn" where "nn" is the error code.

B.DA.2.EF.. Additional pressing of the "ENTR FWD" key will cause the display to read the subsequent errors up to error number 32. After the last recorded error has been displayed, the first line of the display will read "TO CLEAR ERRORS", an the second line of the display will read "PRESS ENTR/FWD". if the "ENTR FWD" key is then pressed the recorded errors will be cleared from memory and the display will read "ERRORS CLEARED". Prior to erasing the errors, they should be recorded for diagnostic purposes.

B.DA.2.EF..CB Pressing the "CLR BACK" key will cause the display to read the previous error.

B.DA.3.EF Pressing the B.DA.3.EF key sequence provides the user with information about the operating system software. The first information is about the first PROM. The first line of the display will read "PROM1 nnnn-nn" where "nnnn-nn" is the part number of the PROM. The second line of the display will read "REV nn DATE mmyy" where "nn" is the revision number of the software on the PROM and "mmyy" is the month and year that the PROM was produced.

B.DA.3.EF.EF Pressing the "ENTR FWD" key a second time will give information about the second PROM. The first line of the display will read "PROM2 nnnn-nn" where "nnnn-nn" is the part number of the PROM. The second line of the display will read "REV nn DATE mmyy" where "nn" is the revision number of the software on the PROM and "mmyy" is the month and year that the PROM was produced.

B.DA.3.EF.EF.EF Pressing the "ENTR FWD" key a third time will toggle back to give information about the first PROM.

B.DA.4.EF Pressing the B.DA.4.EF key sequence will display the format for displaying the ADC data. The first line of the display will read "SIGNAL = fffff" where "fffff" is "HEX, "OCTAL", "DEC", or "VOLTS".

B.DA.4.EF.DA Pressing the "DATA" key will cause the second display line to read "O=0 H=1 D=2 V=3" followed by a cursor.

B.DA.4.EF.DA.n Pressing a key from "O" to "3" will select one of the formats.

B.DA.4.EF.DA.n.CB Pressing the "CLR BACK" key will cancel the entry without changing the format.

B.DA.4.EF.DA.n.EF Pressing the "ENTR FWD" key will enter the new format into the system.

B.DA.5.EF Pressing the B.DA.5.EF key sequence will display the format for displaying the CAM data. The first line of the display will read "CAM DATA = fffff" where "fffff" is "HEX, "OCTAL", or "DEC".

B.DA.5.EF.DA Pressing the "DATA" key will cause the second display line to read "O=0 H=1 D=2" followed by a cursor.

B.DA.5.EF.DA.n Pressing a key from "O" to "2" will select one of the formats.

B.DA.5.EF.DA.n.CB Pressing the "CLR BACK" key will cancel the entry without changing the format.

B.DA.5.EF.DA.n.EF Pressing the "ENTR FWD" key will enter the new format into the system.

B.DA.6.(n)EF Pressing the B.DA.6 key sequence followed by (n) pressings of the "ENTR FWD" key will cause the following displays to appear:

(n)	DISPLAY	DATA
1	"ADC RESOLUTION" "BITS =nn"	NUMBER OF ADC BITS
2	"ADC OFFSET" " MV =nnnnn"	OFFSET FROM ZERO OF THE MIDPOINT OF THE RANGE

3	"ADC FULL SCALE" " MV =nnnnn"	ONE HALF OF THE ADC RANGE
4	"UPDATE DEFAULTS" "0=NO 1=YES"	"YES" WILL LOAD CURRENT PARAMETERS INTO DEFAULTS
5	"CRYSTAL FREQ" "DATA =nn"	DESIRED CRYSTAL FREQUENCY 1, 4, 5, OR 10 MEGAHERTZ
6	"EXT MUX-BRST CLK" "DATA=0"	"1" OR "YES" WILL USE THE EXTERNAL CLOCK
7	"STOP CLOCK SRC" "DATA=0"	"1" OR "YES" WILL USE STOP* AS A CLOCK SOURCE
8	"MASTER OR SLAVE" "DATA=1"	SELECT "0" FOR SLAVE AND "1" FOR MASTER
9	"EXT START EDGE" "DATA =1"	SELECT "1" FOR "POS" OR "0" FOR "NEG" CLOCK EDGE
10	"EXT CLOCK EDGE" "DATA=1"	SELECT "1" FOR "POS" OR "0" FOR NEG CLOCK EDGE
11	"STOP-COIN START" "DATA=1"	SELECT "1" FOR STOP* OR "0" FOR COIN* START
12	"SIM HOLD CAM ENB" "DATA=0"	"1" OR "YES" WILL ENABLE SIM HOLD CAM BIT
13	"CAM RESTART EDGE" "DATA=1"	SELECT "1" FOR "POS" OR "0" FOR "NEG" CAM RESTART EDGE
14	"DIAGNOSTICS" "DATA =0"	SELECT DIAG. CAM MODE 1=REPLACE OUTPUT DATA WITH 16 BIT COUNTER 2=READ MICROPROCESSOR MEMORY 3=READ MICROPROCESSOR PORT

B.DA.6.(n)EF.CB.. Pressing the "CLR BACK" key after the B.DA.6.(n)EF key sequence will decrement the value of (n) for each pressing of the "CLR BACK" key.

B.DA.6.(n)EF..DA Pressing the "DATA" key will cause the cursor to appear.

B.DA.6.(n)EF.DA.nn Pressing keys from "0" to "9" will enter the desired data.

B.DA.6.(n)EF.DA.n.CB Pressing the "CLR BACK" key will cancel the entry without changing the format.

B.DA.6.(n)EF.DA.n.EF Pressing the "ENTR FWD" key will enter the new resolution into the system.

B.DA.7.(n)EF Pressing the B.DA.7 key sequence followed by (n) pressings of the "ENTR FWD" key will display and permit editing and entering the list of boards in the system together with their listen and talk addresses. The first line of the display will read "BD ddd TYPE hhhh", where "ddd" is the decimal position of the entry, in the list beginning with zero, and is equal to (n)-1, and "hhhh" is the type of board in hexadecimal notation. The second line of the display will read "LADD lll TADD ttt", where "lll" is the listen address in hex and "ttt" is the talk address in hex.

B.DA.7.(n)EF.CB.. Pressing the "CLR BACK" key after the B.DA.7.(n)EF key sequence will decrement the value of (n) for each pressing of the "CLR BACK" key.

B.DA.7.(n)EF.DA Pressing the "DATA" key will cause the cursor to appear instead of "hhhh",the board type.

B.DA.7.(n)EF.DA.n.. Pressing keys from "0" to "F" will enter the type code for board number "ddd".

B.DA.7.(n)EF.DA.n..CB Pressing the "CLR BACK" key will cancel the entry without changing the board type. The cursor will replace the listen address, "lll".

B.DA.7.(n)EF.DA.n..EF Pressing the "ENTR FWD" key will enter the new board type. The cursor will replace the listen address, "lll".

B.DA.7.(n)EF.DA.n..EF.n.. Pressing keys from "0" to "F" will enter the listen address of the board "ddd".

B.DA.7.(n)EF.DA.n..EF.n..CB Pressing the "CLR BACK" key will cancel the entry without changing the listen address. The cursor will replace the talk address, "ttt".

B.DA.7.(n)EF.DA.n..EF.n..EF Pressing the "ENTR FWD" key will enter the new listen address. The cursor will replace the talk address, "ttt".

B.DA.7.(n)EF.DA.n..EF.n..EF.n.. Pressing keys from "0" to "F" will enter the talk address for board number "ddd".

B.DA.7.(n)EF.DA.n..EF.n..EF.n..CB Pressing the "CLR BACK" key will cancel the entry without changing the board type. The cursor disappear.

B.DA.7.(n)EF.DA.n..EF.n..EF.n..EF Pressing the "ENTR FWD" key will enter the talk address. The cursor will disappear.

B.DA.8.(n)EF Pressing the B.DA.8 key sequence followed by (n) pressings of the "ENTR FWD" key will display and permit editing and entering the list of input boards that have been removed from the system. By entering the multiplexer address and the number of channels on the board, space will be saved in the channel sequence for the removed board. This removes the requirement for the user to reconfigure the host computer for the channel locations of the removed board. When this key sequence is pressed the first line of the display will read "REMOVED BOARD" and the second line of the display will read "FCH=ffff LGT=ll", where "ffff" is the decimal number of the first channel on the board. "ll" is the number of channels on the board in decimal notation. If (n) is one, then the board with the lowest first channel will be displayed. As (n) increases, the display will step through the list in the order of increasing first channel number.

B.DA.8.(n)EF.CB.. Pressing the "CLR BACK" key after the B.DA.8.(n)EF key sequence will decrement the value of (n) for each pressing of the "CLR BACK" key.

B.DA.8.(n)EF.DA Pressing the "DATA" key will cause the data in the second line of the display to disappear and the cursor to appear in place of the first channel number "ffff".

B.DA.8.(n)EF.DA.n.. Pressing keys from "0" to "F" will enter the first channel number of the

board, "ffff".

B.DA.8.(n)EF.DA.n..CB Pressing the "CLR BACK" key will cancel the entry without changing the first address. The cursor will appear in place of the length, "11".

B.DA.8.(n)EF.DA.n..EF Pressing the "ENTR FWD" key will enter the new first address and the cursor will replace the length, "11".

B.DA.8.(n)EF.DA.n..EF.n.. Pressing keys from "0" to "F" will enter the length of the board "11".

B.DA.8.(n)EF.DA.n..EF.n..CB Pressing the "CLR BACK" key will cancel the entry without changing board length, "11".

B.DA.8.(n)EF.DA.n..EF.n..EF Pressing the "ENTR FWD" key will enter the new board length, "11". If the board length is zero then the board will not be entered into the list. If the first channel number is an existing entry in the list then a length of 0 will cause the entry to be deleted from the list.

B.EF Pressing the key sequence B.EF is the same as press-ing the key sequence B.1.EF.

C The "RUN" key.

The "RUN" key will place the system into a run condition if it is in the "LOCAL" Mode. In both the "LOCAL" and "REMOTE" Modes, if the system is running, as indicated by the "RUN" LED being illuminated but not flashing, then the data for a selected channel will be displayed.

Pressing the "RUN" (C) key will cause the first line of the display to read "CHAN = nnnn " where "nnnn" is the decimal value of the channel that was previously read, or a channel within the first channel to last channel range. The second line of the display will read "SIGNAL = ". If the system is running then after channel "nnnn" has been digitized the second line of the display will read "SIGNAL = dddd " where "dddd" is the data for that channel displayed in the format selected using the "ENVR" key.

C.CB Pressing the "CLR BACK" key will cause the channel display to decrement. If the First Channel had been displayed then the display will wrap around to the Last Channel. When the displayed channel is digitized, the data for that channel will be displayed.

C.DA Pressing the "DATA" key will cause the cursor to appear in place of the channel number.

C.DA.nnnn Pressing keys "0" through "9" will enter the desired channel number in decimal format.

C.DA.nnnn.CB Pressing the "CLR BACK" key will delete the entered channel number and return to the previous channel number.

C.DA.nnnn.EF Pressing the "ENTR FWD" key will enter the new channel number and after that channel has been digitized its data will be displayed.

C.EF Pressing the "ENTR FWD" key will cause the channel display to increment. If the Last Channel had been displayed then the display will wrap around to the First Channel. When the displayed channel is digitized, the data for that channel will be displayed.

D The "STOP" key.

The "STOP" key will stop a running system if it is in a local mode and turn off the "RUN" LED. Pressing the "STOP" (D) key will stop the system and cause the first line of the display to read "SYSTEM STOPPED" if the system is in the local control mode. If the system is in the remote mode the first line of the display will read "SYSTEM STOPPED" or "SYSTEM RUNNING" as required.

E The "RST" key.

The "RST" key will reset the system variables.Pressing the "RST" (E) key will cause the first line of the display to read "TO RESET SYSTEM". The second line of the display will read "PRESS ENTR/FWD".

E.EF Pressing the "ENTR FWD" key will cause the system to reset and clear the display.

NOTE: If the "RST" key is held depressed while the AC system power is being turned on, a MASTER RESET will occur that will set the system defaults to a very slow generic operating mode.

F The "AUX" key.

The "AUX" key is a spare key reserved for special use and is not implemented in this system.

CB **The "CLR BACK" key.** The key code is 18.

The "CLR BACK" key has two uses depending on what Control Panel Function is being used. When the "ENTR FWD" key is used to step forward through a list of items, the "CLR BACK" key may be used as a backspace key to step backwards through the list. When data or addresses are being entered, if "CLR BACK" is pressed instead of the "ENTR FWD" key then the entered data will be cleared and no new information will be recorded.

DA **The "DATA" key.** The key code is 16.

The "DATA" key has two functions, for those Control Panel Functions that allow both mode control and data entry, pressing the "DATA" key will switch to the data display mode. For those Control Panel Functions that are already in the data display mode or have been switched to the data display mode, pressing the "DATA" key will cause the cursor to appear to allow data to be entered.

EF **The "ENTR FWD" key.** The key code is 19.

The "ENTR FWD" key has two uses depending on what Control Panel Function is being used. The "ENTR FWD" key can be used to step forward through a list of items, this use is normally prompted by the "PRESS ENTR/FWD" display. When data or addresses are being entered, pressing the "ENTR FWD" key will cause the new information to be recorded.

FN **The "FNCT" key.** The key code is 17.

The "FNCT" key is used to return the control entry to the "FUNCTION" or first level. At this level, the white notation on keys "0" through "F" is in effect and pressing one of those keys will enter the noted function. Since some functions automatically return to the "FUNCTION" level upon completion and other functions do not, it is suggested that every key stroke sequence commence with pressing the "FNCT" key until the user is familiar with the system. In the event that an incorrect sequence of key strokes are entered, the user can always return to the "FUNCTION" level by pressing the "FNCT" key.

REPORTED ERRORS CODES

ERROR 2 Fatal, status read from TTL card not correct. Possible supply problem in the ADC block or Opto communication problem.

ERROR 3 Fatal, setup not completed. Missing Opto/Interface or MC board.

ERROR 4 Fatal, setup not completed. Not receiving response from Opto/Interface board.

ERROR 5 Warning, Remote BCRC not matching hardware. Only Reported on powerup. (CCLK)

ERROR 6 Fatal, Resolution not matching hardware. Correct jumpers on TTL card to match hardware. (BITS)

ERROR 7 Data type or offset not matching hardware. Correct jumpers on TTL card to match hardware or Correct environment table to match jumpers on TTL card.

ERROR 8 Full Scale not matching hardware. Correct jumpers on TTL card to match hardware or correct environment table to match jumpers.

ERROR 9 Fatal, wrong TTL OUTPUT card, mode not supported. Install TTL card for the ADC type being used.

ERROR 10 Fatal, not defined operating mode, TTL card jumpers ?

ERROR 11 Fatal, Bad Crystal Freq choosen. Correct environment table.

ERROR 12 Warning, Remote PRE-CLOCK not equal to 1. Only reported on powerup. (SNCKRE)

ERROR 13 Scan length is greater than 30K MAXIMUM LIMIT, or First > last channel. (Removed on 9989-02).

ERROR 14 Coin for counter #1 is negative.
First > last channel. (Removed on 9989-02).

ERROR 15 Coin for counter #2 is negative.
First > last channel. (Removed on 9989-02).

ERROR 16 Coin for counter #3 is negative.
First > last channel. (Removed on 9989-02).

ERROR 17 Coin for counter #4 is negative.
First > last channel. (Removed on 9989-02).

ERROR 18 Crystal frequency is illegal in the Environment. Legal values are: 10Mhz, 5Mhz, 4Mhz, and 1Mhz. (20Mhz and 2Mhz legal on 9989-03).

ERROR 19 Pre-Mux divisor too large for crystal used.

ERROR 20 Pre-Burst divisor too large for crystal used.

ERROR 21 CAM write scan length is greater than 30K, or first > last channel. (Removed on 9989-02).

ERROR 22 Poll* stuck Hi. (No channels recorded in config)

ERROR 23 Poll* stuck Lo.

ERROR 24 Bus talk to system area, not allowed.

ERROR 25 ADC timing not consistent with ADC type identified.

ERROR 26 ADC block Mux Delay circuit not working.

ERROR 27 Yanker card not responding or not installed if diagnostic mode 19 invoked.

ERROR 27 ID/SIZE array overflow. Over 272 cards identified. This error reported if diagnostic mode 19 is NOT invoked.

ERROR 28 Fatal, prom dash mismatch.

ERROR 29 An attempt was made to adjust a digital TC pot, consult the factory if such an adjustment is required.

ERRORS 30-127 NOT DEFINED.

ERROR 128 (CPU) SRESET1* HI. (will not go LO).

ERROR 129 (CPU) SRESET1* F/F WILL NOT REMEMBER LO.

ERROR 130 ERR128 AND ERR129

ERROR 131 (CPU) SRESET1* LO. (will not go HI).

ERROR 132 ERR128 AND ERR131

ERROR 133 ERR129 AND ERR131

ERROR 134 ERR130 AND ERR131

ERROR 135 (CPU) RESET2* STUCK LO.

ERROR 136 (CPU) RESET2* STUCK HI.

ERROR 137 ERR135 AND ERR136

ERROR 138 (CPU) RESET3* STUCK LO.

ERROR 139 (CPU) RESET3* STUCK HI.

ERROR 140 ERR138 AND ERR139

ERROR 141 (FIDIA) OVERRUN* NOT WORKING. (FIFO-TO-CPU)

ERROR 142 (FIDIA) FIFO SIZE ERROR (FIFO NOT 128K, 256K, 512K, OR 1MEG).

ERROR 143 (FIDIA) READ TIME OUT FROM FIFO.

ERROR 144 (CPU) CLRMXPRSNT* DID NOT CLEAR MUX PRESENT F/F.

ERROR 145 (CPU) MUX CLOCK DID NOT SET MUX PRESENT F/F.

ERROR 146 ERR144 AND ERR145

ERROR 147 (FIDIA) COMPARISON ERROR BETWWEEN FIFO DATA & CPU.

ERROR 148 (CPU) STOP* HI. (will not go LO).

ERROR 149 (CPU) STOP* LO. (will not go HI).

ERROR 150 ERR148 AND ERR149

ERROR 151 (FIDIA) CANNOT CLEAR DECOM F/F (FIFO ALWAYS TALKING?)

ERROR 152 (CPU) STMORE is HI. (will not go LO).

ERROR 153 (CPU) STMORE is LO. (will not go HI).

ERROR 154 ERR152 AND ERR153

ERROR 156 (CPU) DECOM is HI. (will not go LO).

ERROR 157 (CPU) STMORE is HI. (will not go LO).

ERROR 158 (CPU) ERROR READING INT5.5. (will not go LO).

ERROR 159 (CPU) CANNOT SET DECOM. (will not go HI).

ERROR 160 (CPU) INT5.5 is LO. (will not go HI).

ERROR 161 (MC) MC CAM TEST FAILED COUNT TEST.

ERROR 162 (MC) MC CAM TEST FAILED 5's TEST.

ERROR 163 (MC) MC CAM TEST FAILED A's TEST.

ERROR 164 COMPARE ERROR --- LSB BYTE OF ADC TO OPTO TO BUS

ERROR 165 COMPARE ERROR --- MSB BYTE OF ADC TO OPTO TO BUS

ERROR 166 MC CARD NOT INSTALLED OR BROKEN

ERROR 167 COMPARE ERROR WITH MC CARD ADD LINES

ERROR 168 FIFO NOT RESPONDING

INTRODUCTION.

This system is interfaced using the IEEE-488 interface protocol and therefore has special considerations regarding the system control and operation. This section of the manual details these considerations.

The basic programming steps indicated herein are compatible with the MCLS controlled systems now in use.

The IEEE-488 Bus structure as implemented by Preston follows the rules set by the IEEE-488 handbook. The Preston IEEE-488 Bus interface board uses a Fairchild 96LS488 controller chip to interpret the IEEE-488 bus signals and transmit data to and from a PRESYS 1000 Controller.

The Controller transmits and receives 16-bit words which are broken into bytes by the 96LS488 for bus transmission. The interface will respond to any IEEE-488 bus command. The most commonly used commands are: SERIAL POLL (Status), WRITE (data to PRESYS), READ (data from PRESYS), and CLEAR (initialize interface).

The signals TRANSMIT TERMINATE and READ TERMINATE must be disabled, as READ TERMINATE is not generated by the PRESYS bus, and TRANSMIT TERMINATE causes false data to be transmitted to the PRESYS controller.

4.0 PROGRAMMING

Programming the PRESYS 1000 through the IEEE-488 Bus:

1. Before attempting to transmit data to the PRESYS 1000 system, a Device Clear MUST be sent to the PRESYS 1000 system address, in order to set the byte steering logic in the proper direction for data transmission.

2. It should be noted that most computers send and receive data in reverse order from Hewlett-Packard computers. This is true, for example, for Digital Equipment Corporation computers. The sequence in which the bytes are sent can be reversed by changing straps on the IEEE-488 Control board, part number 201060.

   This eliminates the need to reverse the sequence of bytes through software in the computer. The standard factory settings for the various dash number variations of the 201060 board are given in the following table:

IEEE-488 INTERFACE BOARD
P. C. ASSEMBLY PART NUMBER 201060
DASH NUMBER TABULATION

DASH NO.	STRAP	NOTES
-00	A-B, C-D, E-F, G-H	SENDS HIGHER-ORDER BYTE FIRST
-01	A-D, B-C, E-H, G-F	SENDS LOWER-ORDER BYTE FIRST

5.0 STATUS BITS

The status bits are defined in the following table:

STATUS BIT TABLE

BIT NUMBER	BIT DEFINITION	
1	EMPTY*	(Fifo status)
2	OVERRUN*	(Fifo status)
3	FULL*	(Fifo status)
4	STOP*	(Presys status)
5	HALF FULL*	(Fifo status)
6	MISC.0	(future use, tied HI)
7	( )	(IEEE for polling)
8	ERROR*	(CPU status)

REQUEST SERVICE (RSV) LINE

Installing jumper W10 will connect the IEEE request service (RSV) input line to the fifo OVERRUN* signal. OVERRUN* is asserted when ADC data tries to write to a full fifo. If RSV is to be used with some other status, say EMPTY* for example, a wire-wrap wire must be used to complete the connection. See schematic 201061-T for connection possibilities.

6.0 CONTROL WORD BIT 2.

Bit 2, handshake enable bit. This bit should be programmed true insuring the ability to always transmit data. If this bit is false TXRDY will be left false possibly inhibiting data transmission.

DIP SWITCH SETTINGS.

Setting the Device addresses

Two 5-position dip switches set the TALK and LISTEN addresses. These dip switches are located on the top edge of the IEEE-488 Interface printed circuit board, part number 201060-00.

Dip switch "TAD SW3" sets the talk address. Switch position number 5 is the MSB, and switch position number 1 is the LSB. Closure of a switch sets a zero bit in the address, while opening the switch sets a one bit in the address.

Dip switch "LAD SW2" sets the listen address. Switch position number 5 is the MSB, and switch position number 1 is the LSB. Closure of a switch sets a zero bit in the address, while opening the switch sets a one bit in the address.

In the extended-address mode, the talk and listen addresses are one and the same. This extended address is 10 bits long. The extended address is set by the combination of dip switches SW3 and SW2. SW3 sets the PRIMARY ADDRESS, and SW2 sets the SECONDARY ADDRESS.

IEEE-488 OPERATING MODES.

The Preston IEEE-488 interface has 13 modes of operation. Four mode bits, M0 through M3, make up a 4-bit input code that defines the operating mode. Of the 16 possible combinations of four bits, three combinations are unused. The remaining 13 combinations are all valid operating modes for the interface.

Dip switch "MOD SW1" (MODE SELECT) is a 4-position dip switch that sets the operating mode of the interface. This switch is located on the IEEE-488 Interface printed circuit board, part number 201060-00. Switch positions 1 through 4 of dip switch "MOD SW1" correspond to mode bits M0 through M3, respectively. Closure of a switch sets a zero for the corresponding mode bit, while opening the switch sets a one for the corresponding mode bit.

The following table defines each valid setting of the four switch positions of dip switch "MOD SW1", and the corresponding interface operating mode and function:

MODE INPUTS M0	M1	M2	M3	OPERATING MODE	NOTE	FUNCTION
0	0	0	0	OFF LINE		THE DEVICE CANNOT TAKE PART IN ANY IEEE-488 OPERATIONS
0	0	0	1	TON(LOW SPEED)	1	THE DEVICE GOES DIRECTLY TO THE TALK-ADDRESSED STATE
0	0	1	0	LON		THE DEVICE GOES DIRECTLY TO THE LISTEN-ADDRESSED STATE
0	0	1	1	TON(HI SPEED)	1	THE DEVICE GOES DIRECTLY TO THE TALK-ADDRESSED STATE (HI SPEED)
0	1	0	0	T(LOW SPEED)	1	TALKER SINGLE-ADDRESS MODE
0	1	0	1	TE(LOW SPEED)	1	TALKER EXTENDED-ADDRESS MODE
0	1	1	0	T(HI SPEED)	1	TALKER SINGLE-ADDRESS MODE
0	1	1	1	TE(HI SPEED)	1	TALKER EXTENDED-ADDRESS MODE
1	0	0	0	L		LISTENER SINGLE-ADDRESS MODE
1	0	0	1	LE		LISTENER EXTENDED-ADDRESS MODE
1	1	0	0	T/L(LOW SPEED)	1,2	TALKER/LISTENER DUAL-ADDRESS MODE
1	1	0	1	TE/LE(LOW SPEED)	1	TALKER/LISTENER EXTENDED-ADR MODE
1	1	1	0	T/L(HI SPEED)	1,2	TALKER/LISTENER DUAL-ADDRESS MODE *

NOTES:

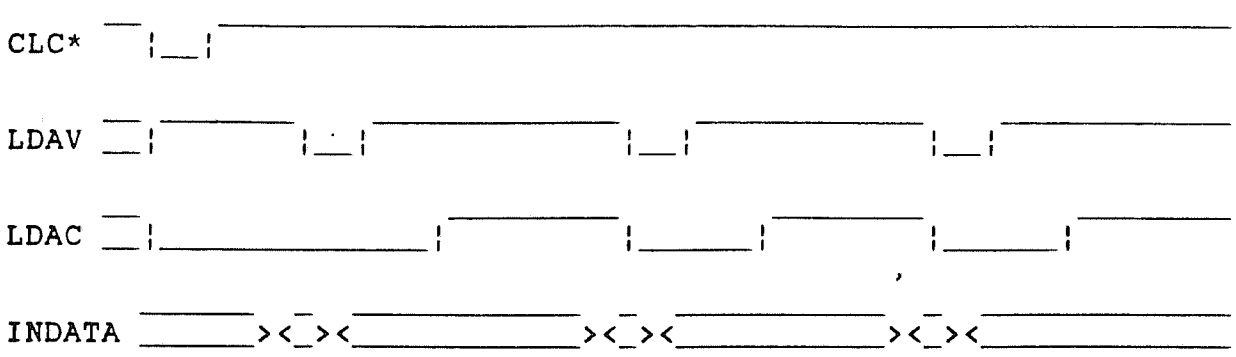
1. The LOW SPEED TALKER option is selected where open-collector data drivers are used. The delay from putting valid data on the bus to DAV* going true is 2.0 microseconds. The HI SPEED option is selected where tri-state drivers are used. The settling delay (data to DAV*) is 1.1 microseconds for the first byte sent after a LOW to HI transition of ATN*, and 500 nanoseconds for subsequent bytes.

2. For dual-address talker and listener modes, the talk and listen addresses can be different.

3. In the "Operating Mode" column above, T=Talker, and L=Listener.

* SET AT FACTORY.

INTERFACE HOST-TO-PRESYS INPUT TIMING.



Description:

1) CLC* goes LO, generating RESET1*, and pre-setting the interface handshake signals.

2) The computer then sends the first byte of data.

3) LDAV goes LO clocking in the first byte of data.

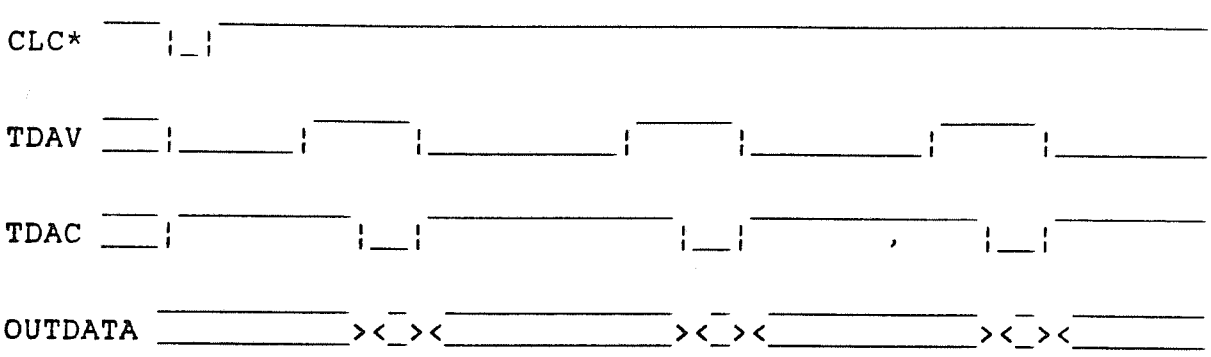
4) The computer then sends the second byte of data.

5) LDAV goes HI clocking in the second byte of data, the interface board transmits the entire word to the CPU card.

6) The transmission of the word to the CPU card generates LDAC.

7) LDAC going HI signals the computer to send the next word.

INTERFACE PRESYS-TO-HOST OUTPUT TIMING.



Description:

1) CLC* goes LO, generating RESET1*, and pre-setting the interface handshake signals.

2) Presys sends a word to the interface then raises TDAV.

3) TDAC goes LO transmitting the first byte of data to IEEE.

4) TDAC goes HI transmitting the second byte to IEEE, and taking away TDAV.

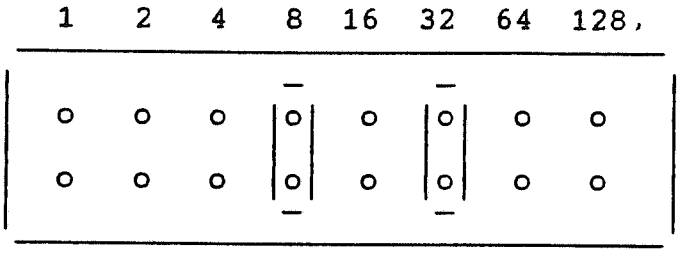
5) TDAC going HI requests another word from the Presys fifo by generating an LMORE* (not shown).

6) Repeat sequence starting at step (2).

TALKER ADDRESS SELECTION.

The following strap configuration establishes the link between the IEEE interface card and the CPU card within a Presys system. Normally the CPU card is at address 40, so the IEEE card must be talking to address 40 for the CPU card to listen.

Shown below is the jumpers for TALK ADDRESS of 40.

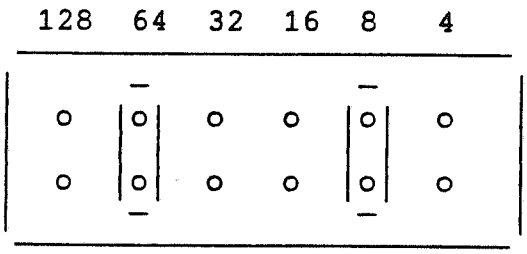


IEEE488 INTERFACE BOARD TALKER ADDRESS JUMPERS

LISTEN ADDRESSING.

The following strap configuration establishes the link between the FIFO card and the IEEE interface card inside a Presys system. Normally the FIFO card talks to address 72, so the IEEE card must be listening to address 72 for ADC data to reach the IEEE card.

Shown below is the jumpers for LISTEN ADDRESS of 72.



IEEE488 INTERFACE BOARD LISTEN ADDRESS JUMPERS

JUMPERS
PRESTON BUS MISCELLANEOUS LINES

The miscellaneous lines have standard functions associated with them, installing a jumper below will connect the "function" to the IEEE status register. If a function cannot be strapped to the proper status bit, then a wire-wrap connection is needed.

Jumper	Connects	default	Signal Name
JP1	MISC 0 to STATUS 6	OMIT	(future use)
JP2	MISC 1 to STATUS 8	INSTALL	(ERROR*)
JP3	MISC 2 to LMORE*	INSTALL	(handshake)
JP4	MISC 3 to STATUS 1	INSTALL	(EMPTY*)
JP5	MISC 4 to STATUS 5	INSTALL	(HFULL*)
JP6	MISC 5 to STATUS 3	INSTALL	(FULL*)
JP7	STOP* to STATUS 4	INSTALL	(STOP*)
JP8	MISC 6 to STATUS 2	INSTALL	(OVERRUN*)
JP9	TMORE* to MISC 7	INSTALL	(handshake)
JP10	MISC 6 to RSV	INSTALL	(OVERRUN*)

The IEEE interface may send/receive the MOST significant 8 bits first, or the LEAST significant 8 bits first. The following four jumpers will determine the order:

Installing: A-D, B-C, E-H, G-F Sends low byte first.

Installing: A-B, C-D, E-F, G-H Sends high byte first.

---------- Revision D boards and later ----------

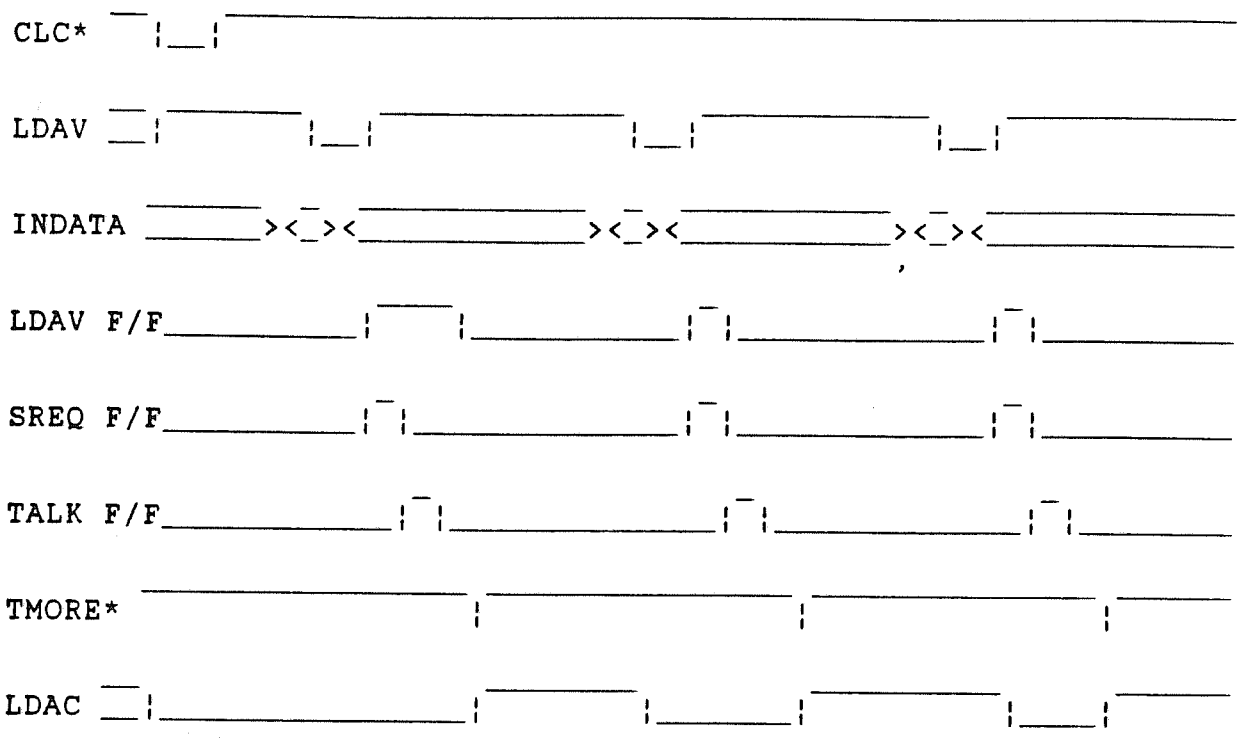
JP11 and JP12 change the way the interface card is reset.

JP12 (normally installed) is used when the fifo is cleared during setup (control word, etc...). When the ADC is setup, whoever is slowest to finish (Presys or Host) requests the first word out of the fifo. In "loop mode" the fifo is not cleared between runs.

JP11 clears the fifo between Go commands (on "loop mode" systems). Unfortunately, during "non-looping mode" runs, a fast host computer can request an old word out of a yet to be cleared fifo. To prevent this, the host computer sends two RSO run commands as the last program step. The host computer waits for the handshake from the first RSO run command (by this time the fifo is cleared) before sending the second RSO (which is ignored but handshaked), then finally requesting the first word out of the fifo.

JP11	OMIT	loop mode, clears fifo between Go's
JP12	INSTALL	loop mode, no fifo clear between Go's

INTERNAL PRESYS IEEE CARD-TO-CPU TIMING



Description:

1) CLC* goes LO, generating RESET1*, and pre-setting the interface handshake signals.

2) The computer sends two bytes of data.

3) LDAV goes HI clocking in the second byte of data, the LDAV flip-flop is set.

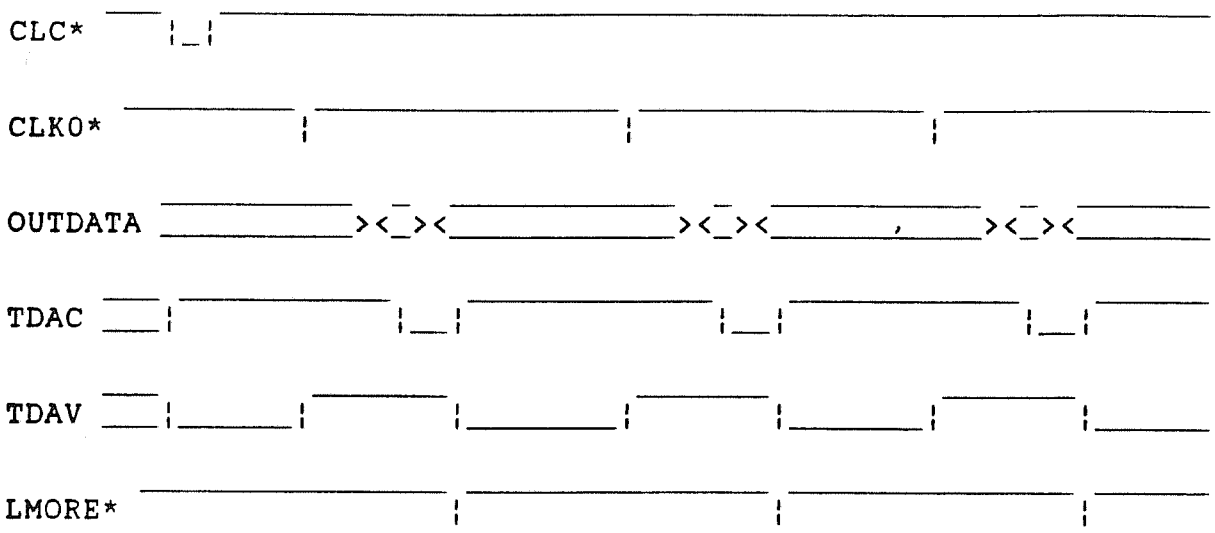
4) The interface card generates a service request (SREQ) to the protocol logic. The bus protocol logic sets the TALK flip-flop and the word is transferred to the CPU card.

5) When the CPU is finished processing the word, the CPU acknowledges by sending a TMORE* signal to the interface card.

6) The TMORE* signal generates the IEEE acknowledge by asserting the LDAC signal.

7) Repeat this sequence starting at step (2).

INTERNAL FIFO-TO-PRESYS IEEE CARD TIMING



Description:

1) CLC* goes LO, generating RESET1*, and pre-setting the interface handshake signals.

2) Presys sends a word to the interface generating a CLK0*, and raising TDAV.

3) TDAC goes LO transmitting the first byte of data to IEEE.

4) TDAC goes HI transmitting the second byte to IEEE, and taking away TDAV.

5) TDAC going HI requests another word from the Presys fifo by generating an LMORE*.

6) Repeat sequence starting at step (2).

REMOTE PROGRAMMING

Table of Contents

1.0 INTRODUCTION:

This is a description of the remote programming features of the UPC control system which are not interface dependent. Because of the modular flexibility of the PRESYS 1000 system, some features of the UPC control system will not be used on a specific PRESYS 1000 system. They are included to show the potential for field enhancement of the PRESYS system.

Every PRESYS 1000 system contains an interface card or cards. The additional information necessary to program with a specific interface is included in the documentation for that interface.

The UPC system generates all necessary signals to control an A/D converter and its associated input modules such as analog multiplexers, simultaneous sample-and-holds, and preamplifiers. It can also control digital I/O data words and DAC's. While most systems include an A/D converter and analog multiplexer it is possible to configure a system with only digital I/O and/or DAC's.

UPC DESCRIPTION:

The UPC Control system is designed to allow the user to both:

* Set up the system.

  This is accomplished by down loading a series of data words from the host device, such as a host computer, to the UPC control system. The Set-up operation utilizes an interrupt driven microprocessor in the PRESYS system. Since a command may require many internal steps to process, each command is therefore comparatively slow. A time of 60 to 4000 microseconds per word is required.

* Control the start of data transfer.

  In the internal start mode, the system will start to run and to transfer data as soon as a GO command is received. In the external start mode, the system must receive a GO command followed by the selected edge of the external start signal.

2.0 UPC PROGRAMMING

2.1 SEQUENCE

The UPC programming procedure consists of three steps:

1. The Host controller sends the SOFTWARE RESET command.

2. The Host controller sends a data array containing a CONTROL WORD followed by necessary setup data. Step 2 and steps 1 and 2 can be repeated as necessary.

3. The Host controller sends RUN command.

2.2 HARD RESET COMMAND

Some computer interfaces require a hard reset to stop or clear the interface handshake before sending the software reset command. See the interface section of the manual for further information.

2.3 SOFTWARE RESET COMMAND

A SOFTWARE RESET command consists of one 16-bit word of all one's (FFFF). This word interrupts the UPC, causing it to stop the ADC's analog-to-digital conversion process, clear the FIFO data memory and to listen for a new control word. The RESET command does not change any memory or register settings previously programmed.

2.4 CONTROL WORD AND SETUP DATA

The word following the RESET command is interpreted as the CONTROL WORD. This 16-bit word contains setup data and consists of three parts:

1. The 8 MSB's contain the control information
2. The next 2 bits control the run mode
3. The 6 LSB's determine both the data needed for a complete setup and whether the RUN command requires a handshake. With the exception of the Handshake (bit2), at least one data word will be required for each bit that is HI. These words must appear in the same order as the bits, for example:

```
CONTROL WORD
CLOCK DIVISOR
FIRST ADDRESS
LAST ADDRESS
CAM DATA FOR CAM FIRST ADDRESS
 :
 :
CAM DATA FOR CAM LAST ADDRESS
EXTENSION CONTROL WORD
```

2.5 EXTENSION CONTROL WORD AND SETUP DATA

If enabled, the word following the last data word of the COMMAND WORD is interpreted as the EXTENSION CONTROL WORD. This 16-bit word contains additional setup data and consists of three parts:

1. The 3 MSB's contain the mode selection information. At present there are only the 3 bits. The REDIRECT MODE bit if set, will take precedence over the other 2. The DIAGNOSTIC MODE bit if set, may or may not effect the operation of system depending on the value of the DIAGNOSTIC WORD. The PARTITION MODE bit if set, will only have its effect if system is programmed to use the CAM table.

   Once a mode has been programmed, that mode will continue until a Reset Command followed by a primary Control Word are sent to the PRESYS System, at this time the Extension Control word will be cleared. A new Extension Control word will have to be sent if a mode within the Extension Control word is desired.

   Note: Sending a Reset Command followed by a Run Code will not modify the previously programmed extension mode.

2. The next 6 bits are not used.

3. The 8 LSB's determine the data needed for a complete setup. At least one data word will be required for each bit that is HI. These words must appear in the same order as the bits, for example:

```
   :
   :
EXTENSION CONTROL WORD
CPU REDIRECT WORD
ENVIRONMENT WORD
REDIRECT ADDRESS
DIAGNOSTIC WORD
FIRST ADDRESS OF FIRST PARTITION
LAST ADDRESS OF FIRST PARTITION
   :
   :
FIRST ADDRESS OF FOURTH PARTITION
LAST ADDRESS OF FOURTH PARTITION
PRE SCALE CLOCK DIVISOR
BCRC CLOCK DIVISOR
EXTENSION CONTROL WORD
```

2.6 RUN COMMAND

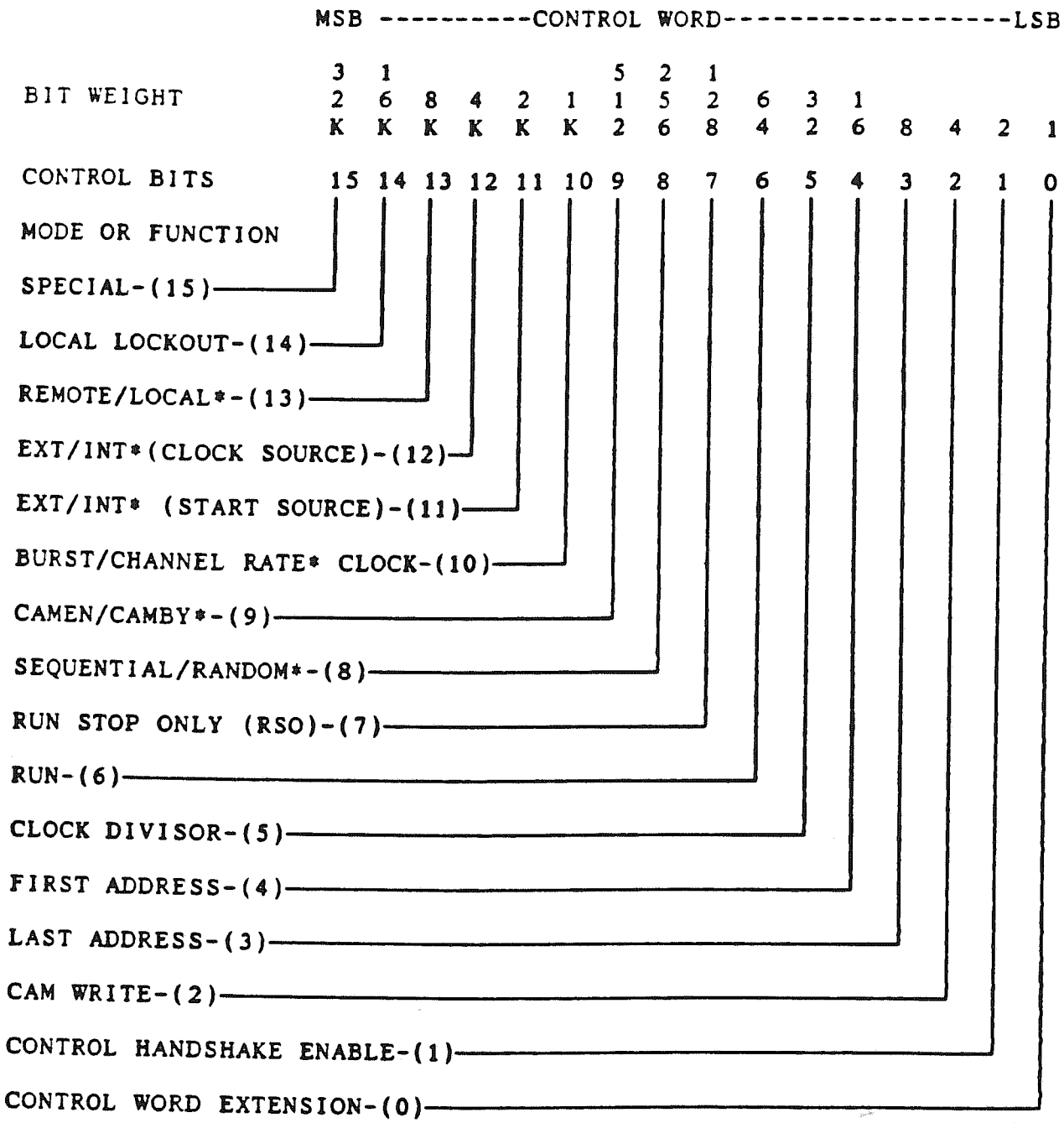
The last word in the programming block must be a RUN command. The RUN command is actually a control word that completes the setup and switches the system to the RUN condition.

3.0 CONTROL WORD DEFINITION

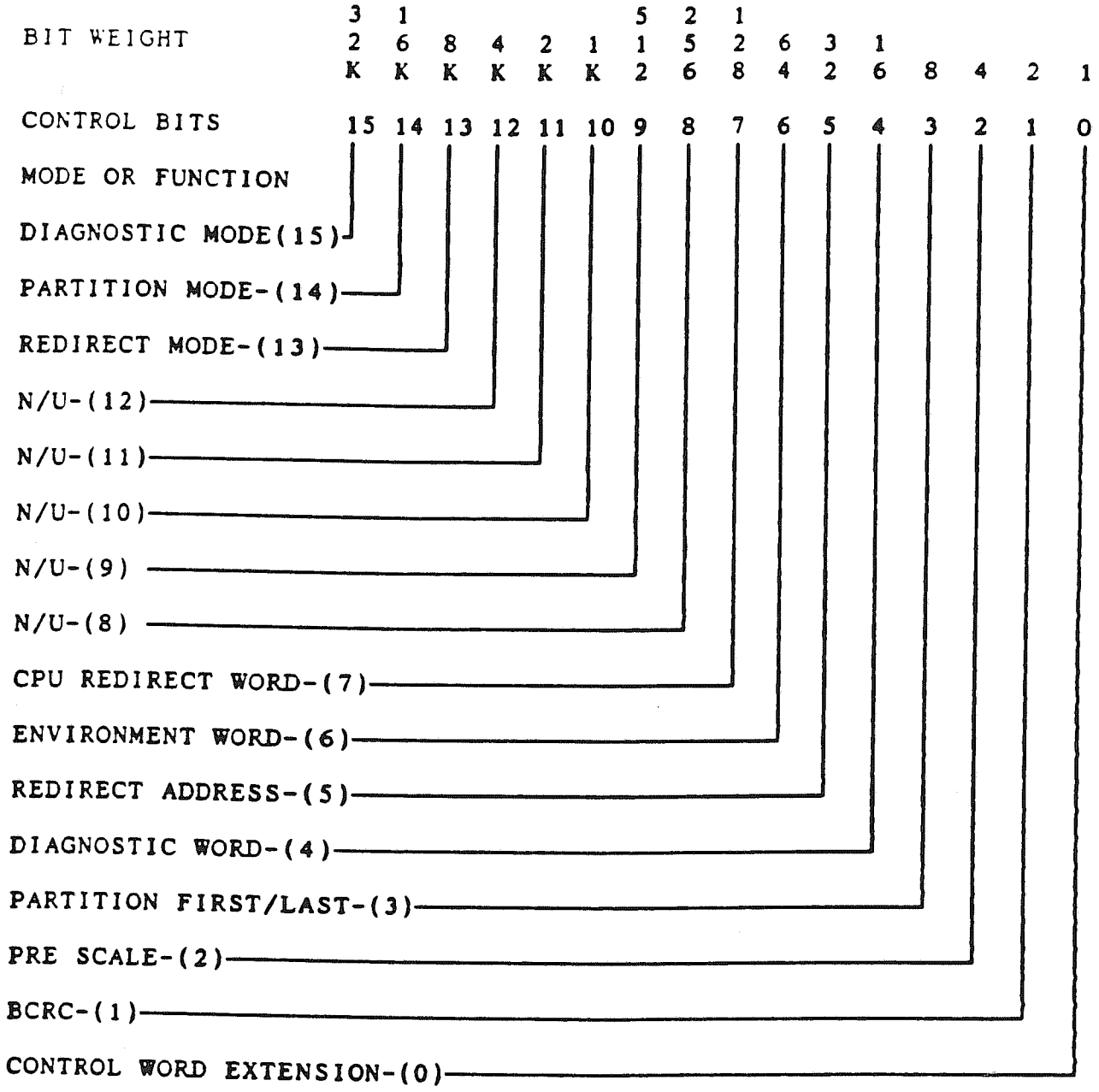
The CONTROL WORD containing 16 bits is sent from the host controller to the UPC Control System. This CONTROL WORD determines the operating modes and functions of the PRESYS 1000 System. The CONTROL WORD is sent to the UPC in what is known as COMMAND MODE.

All Control bits are ACTIVE HIGH unless otherwise noted.

* The names of CONTROL BITS which contain a "/" and are followed by a "*" indicate that this is a dual function bit. The name preceding the slash is active when that bit is high, the name following the slash is active when that bit is low.


MSB ----------CONTROL WORD----------LSB
BIT WEIGHT
32K 16K 8K 4K 2K 1K 512 256 128 64 32 16 8 4 2 1
CONTROL BITS
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MODE OR FUNCTION
SPECIAL-(15)
LOCAL LOCKOUT-(14)
REMOTE/LOCAL*-(13)
EXT/INT*(CLOCK SOURCE)-(12)
EXT/INT* (START SOURCE)-(11)
BURST/CHANNEL RATE* CLOCK-(10)
CAMEN/CAMBY*-(9)
SEQUENTIAL/RANDOM*-(8)
RUN STOP ONLY (RSO)-(7)
RUN-(6)
CLOCK DIVISOR-(5)
FIRST ADDRESS-(4)
LAST ADDRESS-(3)
CAM WRITE-(2)
CONTROL HANDSHAKE ENABLE-(1)
CONTROL WORD EXTENSION-(0)

MSB --------EXTENSION CONTROL WORD----------LSB



NOTE: "N/U" INDICATES UNUSED BITS WHICH SHOULD BE PROGRAMMED AS ZEROS.

4.0 CONTROL WORD BIT DEFINITIONS

4.1 SPECIAL BIT 15 (32K or SIGN)

This bit is used to give access to special registers and functions not normally accessed by the UPC. The following definitions are in effect when this bit is zero.

4.1.1 LOCAL LOCKOUT BIT 14 (16K)

The LOCAL LOCKOUT bit allows the host controller to "LOCKOUT" the front panel controls. This means the LOCAL/REMOTE switching cannot be electrically changed to the LOCAL position. The UPC has been instructed to ignore LOCAL control. All the remote registers can be accessed and displayed but not changed from the front panel keyboard.

4.1.2 REMOTE/LOCAL* BIT 13 (8K)

The REMOTE/LOCAL* bit selects between the remotely programmed or locally (front panel) programmed registers for the Clock Divisor, First Address, Last Address, and Burst Channel Rate Clock Divisor.

4.1.3 EXT/INT* CLOCK SOURCE BIT 12 (4K)

The EXT/INT* CLOCK SOURCE bit selects between the internally generated clock source, or an externally supplied clock source (via the EXTERNAL CLOCK SOURCE BNC connector). Unless otherwise specified, the EXTERNAL CLOCK SOURCE input requires a TTL level signal with a positive going edge. The maximum external clock frequency is 10 MHz.

4.1.4 EXT/INT* START SOURCE BIT 11 (2K)

The EXT/INT* START SOURCE bit selects between an Internal or External START function. The External START requires that a RUN condition has been programmed. Unless otherwise specified, the EXTERNAL START input requires a positive going signal having TTL levels.

4.1.5 BURST/CHANNEL RATE* BIT 10 (1K)

The BURST/CHANNEL RATE* bit allows the clock to be operated either in the scan rate mode (BURST), or in the channel rate mode (NON-BURST).

4.1.5.1 CHANNEL RATE MODE

When bit 10 is programmed LO, the UPC clock will run in the channel rate mode, with the ADC/MUX scanning continuously through the programmed channels. The Clock Divisor will be used to program the channel-to-channel period.

4.1.5.2 BURST MODE

When bit 10 is programmed HI, the UPC clock will run in the burst mode. In the burst mode, the ADC/MUX will run from first address to last address at the maximum rate and then stop, waiting for the next clock to start another burst of data. The minimum length burst is 2 channels.

The burst rate is determined by the clock (internal) or by the EXTERNAL CLOCK signal (external). In BURST mode, the clock divisor will be used to program the period of the burst scan. The period of the burst scan will include all the channel times plus a minimum of one channel spacing between the burst scans. The minimum clock divisor is determined by (no. of channels + 1) multiplied by the minimum clock divisor for the ADC or the BCRC divisor if the BCRC has been programmed.

4.1.5.3 EXTERNALLY-CLOCKED SINGLE-BURST MODE

The externally-clocked single burst mode is used when the user wants to synchronize the data conversion process to an external signal. This signal will start the burst mode. The UPC clock will pulse for the number of times necessary to convert from first address to last address. Then it will stop and wait for the next rising edge on the EXTERNAL CLOCK BNC. The clock divisor for this mode must be programmed to 1!

4.1.5.4 EXTERNALLY ENABLED BURST MODE

This mode is used when the UPC internal burst start clock is to be enabled by an external signal. The first burst will occur after the start signal is received. Succeeding bursts will be generated by the UPC clock. The minimum clock divisor for this mode is determined (# of channels +1) * minimum UPC clock divisor or the BCRC divisor if the BCRC is programmed. For further details on how to use this mode refer to the corresponding computer interface description.

4.1.6 CAMEN/CAMBY* BIT 9 (512)

Selects the CAM (Channel address memory). The CAM allows the programmer to select a random list of channels to be converted. These channels will always be converted in the order in which they are entered. The first address and last address will determine the area of CAM to be used. The addresses programmed into this area will be the actual channel addresses used by the MUX/ADC. The cam use is transparent to the MUX/ADC. See the CAM WRITE (bit 2) for further information on this function.

4.1.7 SEQUENTIAL/RANDOM* BIT 8 (256)

This bit should always be programmed HI. It is included for software compatibility with previous systems where it selected between the sequential address or the random channel address mode.

4.1.8 RUN STOP ONLY (RSO) BIT 7 (128)

This is one of the two run bits, RUN STOP ONLY and RUN, that are used to start and stop the system. If this bit is high the system will ignore all other bits in the COMMAND WORD except for RUN (bit 7), EXTERNAL START (bit 11) and SPECIAL (bit 15).

4.1.9 RUN BIT 6 (64)

Causes the system to enter the RUN condition. If this bit is programmed HI when the RSO (bit 7) is HI, the system will enter the Run condition. The system is stopped by entering a SOFTWARE RESET.

4.1.10 CLOCK DIVISOR BIT 5 (32)

A function bit that allows system to accept clock divisor data. Programming the clock divisor bit in the control word HI will allow the user to change the previously-programmed clock divisor. When power is applied to the system, the system sets the clock divisor to the system's minimum value. Once programmed to a new value, however, this new value will remain until reprogrammed.

When the clock divisor data has been entered BIT 5 will turn off on the control word front panel display.

4.1.10.1 CLOCK DIVISOR BASE FREQUENCY

Refer to test report found in interface manual. The standard value is 10 mHz.

4.1.10.2 MINIMUM CLOCK DIVISOR

The minimum clock divisor using the internal clock will usually be determined by the maximum conversion rate of the ADC. For example, in a system that includes an ADC with a 1 mHz maximum conversion rate and a 10MHz internal clock, the minimum divisor will be 10. With a 5MHz internal clock the minimum divisor will be 5. The divided rate must not exceed the maximum conversion rate of the A/D converter.

4.1.10.3 MAXIMUM CLOCK DIVISOR

The maximum clock divisor is 65534 which is represented by the hex word FFFE. If a divisor of 65535, as represented by the hex word FFFF were used, it would be interpreted as a SOFTWARE RESET.

4.1.10.4 BURST CLOCK

See Paragraph 4.1.5.2 BURST MODE for programming this clock divisor in the BURST MODE.

4.1.11 FIRST ADDRESS BIT 4 (16)

A function bit that sets up the system to accept first channel, or first memory position, address data.

When the first address data has been entered BIT 4 will turn off on the control word front panel display.

4.1.12 LAST ADDRESS BIT 3 (8)

A function bit that sets up the system to accept last channel, or last memory position, address data.

When the last address data has been entered BIT 3 will turn off on the control word front panel display.

4.1.13 CAM WRITE BIT 2 (4)

A function bit that sets up the system to accept channel address data sequentially entered into the CAM channel address memory. This function requires sending a First Address and a Last Address to determine the area in the CAM that the data is going to be stored in before sending that data to the channel address memory. Enough data must be sent to move the address pointer from the first address to the last address. After the CAM has been loaded, any portion of it can be used. The CAM can be used with any conversion mode.

When all of the CAM data (first to last) has been entered, BIT 2 will turn off on the control word front panel display.

4.1.14 CONTROL HANDSHAKE ENABLE BIT 1 (2)

If this bit is programmed HI, all control words and data words will be acknowledged with an UPC generated handshake. If this bit is programmed LO, all but the RUN command will be acknowledged with an UPC handshake. See the interface section of the manual for a further description of the handshake signals involved and the specific programming of this bit.

4.1.15 CONTROL WORD EXTENSION BIT 0 (1)

This bit is used to give access to the functions controlled by the extension control word. When this bit of the COMMAND WORD is HI then, after all data has been sent as required by this COMMAND WORD, the following word will be interpreted as an extension COMMAND WORD.

When the EXTENSION CONTROL WORD has been entered, then after all data has been sent as required by this EXTENSION COMMAND WORD, BIT 0 will turn off on the control word front panel display.

4.2 SPECIAL BIT 15 (32K or SIGN)SPECIAL COMMANDS

This bit is used to give access to special registers and functions not normally accessed by the UPC. All the remaining bit definitions are the same as when this bit is LO except for the following definitions which are modified by the bit being HI.

4.2.1 RUN BIT 6 (64)

Causes the system to enter the special RUN condition for those systems utilizing the special CAM STOP BIT option. If this bit is programmed HI when the SPECIAL (bit 15) is HI and the RSO (bit 7) is HI, the system will enter the Run condition. The system will then be stopped by encountering a bit in the CAM table called the CAM STOP BIT. The system can also be stopped by entering a SOFTWARE RESET.

4.2.2 BCRC DIVISOR BIT 5 (32)

This function bit allows the user to reprogram the BURST CHANNEL RATE CLOCK. This is the clock rate that determines the time between channels within the BURST period. When control word bit 15 (SPECIAL) is programmed HI and bit 5 (CLOCK DIVISOR) is programmed HI, data for the clock function will be used for the BURST CHANNEL RATE CLOCK Divisor. See also Paragraph 4.3.9.

This Clock Divisor defaults to the system's maximum channel rate when power is applied. Once programmed to a new value, however, this new value will remain until reprogrammed. Once programmed to a new value, on power up, error 5 will be reported as a non fatal warning error.

4.2.3 SPECIAL CAM WRITE BIT 2 (4)

A function bit that sets the system to accept data that is destined for specific I/O cards such as Programmable Gain Input Amplifiers, DACs, AND Digital Output Cards. This function requires sending a First Address and a Last Address to establish the area in the I/O addresses where the data is going to be stored, before sending that data. Enough data must be sent to move the address pointer from first address to last address. When the last data word has been entered BIT 2 will be turned off on the front panel display of the COMMAND WORD. If there are channels, that cannot accept data included in the list of channels between FIRST and LAST, then dummy data can be sent to those channels to ease programming.

If First and Last addresses are offset by 32K, then all data sent as described above will instead be ported to the RS232 port within PreSys. This feature will then allow user to program external devices via the RS232 option. All data words are sent as 2 bytes.

4.2.4 CONTROL WORD EXTENSION BIT 0 (1)

This command called the SPECIAL EXTENSION OUTPUT is used for chaining chassis together. It is invoked by sending a control word of 8001. This mode redirects all inputs from a primary interface card to an output device at a listener address of 48. The output device could be another interface, a digital output card, a DAC , or some other device that can listen. The primary intent is to have the input data to a chassis redirected to a digital output type of device so that the data can become the input to another chassis. To exit this mode requires a HARDWARE RESET.

4.3 CONTROL WORD EXTENSION BIT 0 (1)

This bit is used to give access to the functions controlled by the extension control word. When this bit of the COMMAND WORD is HI then, after all data has been sent as required by the COMMAND WORD, the following word will be interpreted as an EXTENSION COMMAND WORD with the following bit definitions:

4.3.1 DIAGNOSTIC MODE BIT 15 (32K)

This bit must be set HI when running any diagnostic that causes data to be output to the Host Controller.

4.3.2 PARTITION MODE BIT 14 (16K)

With this bit set HI, when system reaches a run condition, it will cause the CAM to work in a partition mode. This mode of operation allows up to 4 soft partitions of the CAM memory. Shifting from the primary partition to a secondary or third or fourth is done by the setting of the MSB bit in the CAM table. When ever the MSB bit is set in a CAM data word, that entire word is replaced with a word from the next level.

4.3.3 REDIRECT MODE BIT 13 (8K)

With this bit set, and when a RSO code is sent to the PRESYS system, (RSO STOP for Redirect No RUN, RSO RUN for Redirect RUN) additional input sent to the system will be redirected to the port address defined by user using the REDIRECT ADDRESS BIT 6 and the redirect data word. The user may address any device above the system (0-63 are system addresses). The purpose of this mode is to allow high speed data transfer bypassing the UPC. To exit this mode, and to return to communication with the UPC, requires a HARDWARE RESET. With the redirect mode, input can be redirected to any system port address 64 to 255.

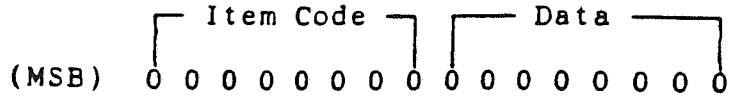
4.3.4 CPU REDIRECT WORD BIT 7 (128)

When set, a word following the command word must be sent. The data sent will be directed to the port defined by the redirect address. If bit 5 in the EXTENSION COMMAND WORD is set, the CPU REDIRECT WORD will be remembered until data for bit 5 (REDIRECT ADDRESS) is sent. The remembered data will be transferred to the proper port. If in diag mode 14, then data is sent to PreSys memory area where the redirect address is the segment of memory and the msb of the redirect word is offset to memory. The lsb of the redirect word is the data to be stored to memory. This mode should only be used by the experenced user. Also this mode may not be portable to prom updates.

4.3.5 ENVIRONMENT WORD BIT 6 (64)

Setting this bit permits changing the environment of the PRESYS system. Some elements of the environment only affect the front panel readout while others affect the remote operation. The setting of this bit requires the user to send an additional word where the MSB byte is an Item Code and where the LSB byte is data for that selected Item.

Environment Word

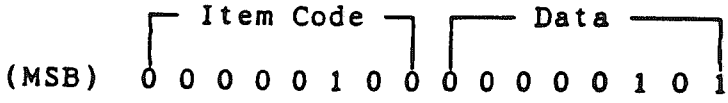


Item Code is the position value of the item as found in the environment table.

Item Code	Description
0	ADC RESOLUTION IN BITS
1	ADC OFFSET (see Data Byte description)
2	ADC FULL SCALE (see Data Byte descript.)
3	(no action)
4	CRYSTAL FREQUENCY IN mHz
5	EXT MUXCLK source with EXT BURST CLOCK
6	STOP* CLOCK source
7	MASTER or SLAVE chassis
8	EXTERNAL START EDGE
9	EXTERNAL CLOCK EDGE
10	STOP* or COIN* START
11	SIMULTANEOUS HOLD CAM ENABLE
12	CAM RESTART EDGE

Data is the value desired for that item code. In the cases of item code 1 and 2, see Data Byte description below.

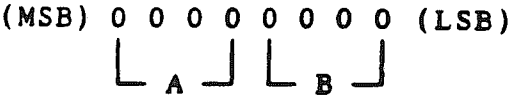
EXAMPLE: If you wanted to change the base crystal frequency from the default value of 10 mHz to 5 mHz, then the environment word to send would be:



Data Byte description

When choosing Item Codes 1 or 2, the data byte has a special format as shown below.

Data Byte



The MSB nibble "A" represents the number of 1000(s) of mV(s)
The LSB nibble "B" represents the number of 24(s) of mV(s)

EXAMPLE: A byte value of 0AAH would represent 10x1000 + 10x24 for a Full scale or Offset value of 10240 mV or 10.240 volts.

4.3.6 REDIRECT ADDRESS BIT 5 (32)

When this bit is HI a word following this COMMAND WORD must contain a value from 64 to 255 which will be the redirected port address.

4.3.7 DIAGNOSTIC WORD BIT 4 (16)

When this bit is HI a word following this COMMAND WORD must contain a Diagnostic Word value as shown in the following table. This word value will set the diagnostic mode of the system. The following list shows the diagnostic modes and the required setting of the Diagnostic Mode (bit 15).

Diag Mode Bit	Diag Word Value	
X	0	- Run time data is as primary and extension control words dictate. Run time data is not modified in any way. The state of the diagnostic bit is unimportant, can be HI or LO.
Set	1	- In this mode when the system reaches a run condition, the ADC data is replaced with counter data. This count data starts at zero and counts to 64K-1 and then loops back to zero. This mode verifies the data path from the ADC block's TTL output card through the ribbon to the opto card, through the opto card to the bus, through the FIFO, through the PRESYS interface and then through the cable to the host controller's interface into the host controller system.
X	2	- This makes the Cam Display Function into a System Memory Read Function.
X	3	- This makes the Cam Display Function into a System Port Read Function.
Set	4	- This outputs, in place of ADC data, Address Counter data or Cam data. The number of words transferred is determined by the setting of First and Last remote registers. This data is output when a run code is sent. The type of data sent is determined by the CAMEN/CAMBY* bit of the primary CONTROL WORD.
X	5	- This mode modifies the Front panel Control word display to be INPUT WORD. This display will show the most recent word sent to the

PRESYS system. Also, while in this mode, the acknowledge for an input word sent to the PRESYS system by an interface will only occur if the <ENTR/FWD> key is pressed. With this mode it is possible to see each word sent to the PRESYS system. Use the <ENTR/FWD> key for a Handshake response to the input word sent, and view each word at the INPUT WORD display. Set to mode 5 while in Local mode for the most straight forward results. If you program this remotely, as soon as you do you will need to press the <ENTR/FWD> key.

Set 6 - FIFO Echo Mode. This mode when a run condition is reached takes data sent by the Host controller and echos it back to the Host through the PRESYS FIFO then PRESYS interface. No ADC data is sent to the Host. The number of words sent to the PRESYS prior to reading them back is dependent on the SIZE of the PRESYS FIFO. FFFFH data not allowed.

Set 7 - Interface Echo Mode. This mode when a run condition is reached will take data sent by the Host controller and echos it back to the Host through the PRESYS interface. No ADC data is sent to the Host. Each word sent by the Host must be read immediately by the Host (no fifo). FFFFH data not allowed.

Set 8 - Error List Header. In this mode when a run condition is reached, the first 32 words sent to the FIFO will be the error list table. After the 32 words have been sent, the ADC will be placed into the described run condition and after the ADC has started, ADC data will be sent to the FIFO.

Set 9 - Setup Data Header. Works as described in mode 8 except the first 32 words sent are setup information. See table for order of setup information.

Set 10 - System Environment Header. Works as described in mode 8 except the first 96 words sent are environmental setup information. See table for what data and order sent.

Set 11 - Error/Setup Header. Works as described in mode 8 except there are 64 words sent at first. 32 for Error list, 32 for Setup. Each list is appended to the next in the order noted.

Set 12 - Error/Setup/Environment Header. Works as described in mode 8 except there are 160 words sent at first. 32 for Error list, 32 for Setup and 96 for Environment data. Each list is appended to the next in the order noted.

Set 13 - Device Code Data Header. Works as described in mode 8 except Device Code Data is sent. The number of header words is equal to the number of channels in the system. This value can be read via mode 10 or 12. It is the last value read. The order of the data sent is from the first channel polled in system to the last channel polled in system.

14 - This modifies the CPU Redirect mode to send data to PreSys memory and load trim pots. See memory map and special trim pot instructions. These may not be included with your system.

15 - Not defined.

16 - Not defined.

X 17 - Data from Host is sent to the RS232 port. This allows remote monitoring of setup data. This mode must be programmed locally.

X 18 - This causes system to Power On Reset immediately after receiving this code. This allows user to have system reinitialize and perform the power on diagnostics. This function causes interface handshake control to work erratically, therefore immediately following output of this diagnostic word, user must wait a period of 5 seconds to allow the power on tests to complete.

X 19 - Power On check for Yanker Card.

X 20 - Power On test of FIFO and Cam. Tests the devices at time of power on with different data patterns to decide if the devices are operating correctly.

X 21 - Power On test of FIFO. Same as mode 20 but only checks FIFO.

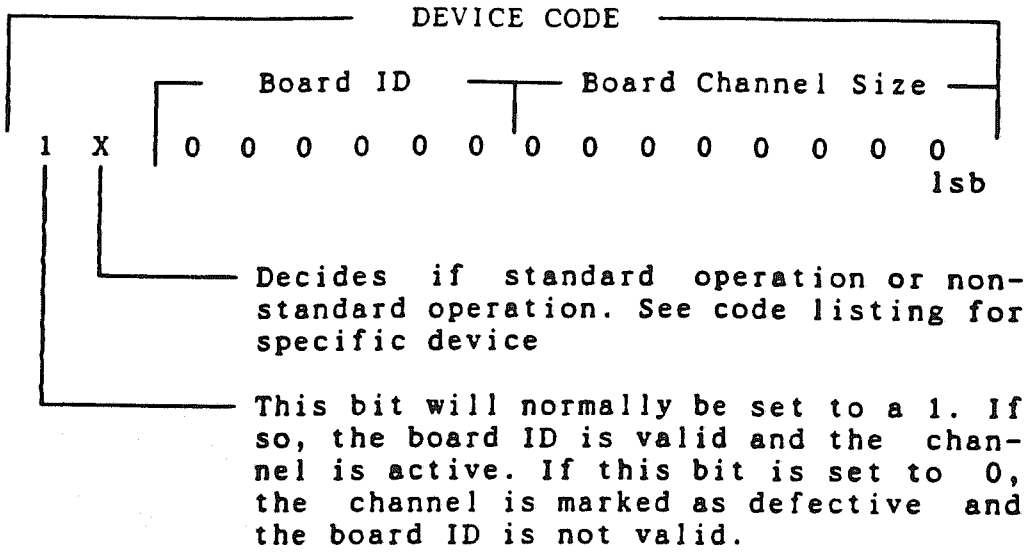
X 22 - Power On test of Cam. Same as mode 20 but only checks Cam.

23 - Not Defined

Table for Modes 8, 9, 10.

Mode 8 (Error List)	Mode 9 (Setup Data)			Mode 10 (Environmental Data)		
Word #	Word #			Word #		
1	Code	(33) 1	Control Word	(65) 1		DBL0 FCH
2	"	(34) 2	Scan Clock	(66) 2		DBL0 Length
3	"	(35) 3	First Chn		.	
4	"	(36) 4	Last Chn		.	
5	"	(37) 5	Extension Word		.	
6	"	(38) 6	0000	(79) 15		DBL7 FCH
7	"	(39) 7	0000 future use	(80) 16		DBL7 Length
8	"	(40) 8	0000 zero's for	(81) 17		BD0 Type
9	"	(41) 9	0000 now.	(82) 18		BD0 Listen Addr
10	"	(42) 10	0000	(83) 19		BD0 Talk Addr
11	"	(43) 11	0000		.	
12	"	(44) 12	0000		.	
13	"	(45) 13	0000		.	
14	"	(46) 14	0000	(138) 74		BD19 Type
15	"	(47) 15	0000	(139) 75		BD19 Lstn Addr
16	"	(48) 16	0000	(140) 76		BD19 Talk Addr
17	"	(49) 17	0000	(141) 77		ADC Resolution
18	"	(50) 18	0000	(142) 78		ADC Offset
19	"	(51) 19	0000	(143) 79		ADC Full Scale
20	"	(52) 20	0000	(144) 80		Crystal
21	"	(53) 21	0000	(145) 81		Ext Mx-Brst Ck
22	"	(54) 22	0000	(146) 82		Stp Clk Source
23	"	(55) 23	Redirect Address	(147) 83		Master/Slave
24	"	(56) 24	Diagnostic Word	(148) 84		Ext Start Edge
25	"	(57) 25	Partition First 2	(149) 85		Ext Clock Edge
26	"	(58) 26	Partition Last 2	(150) 86		Stp-Coin Start
27	"	(59) 27	Partition First 3	(151) 87		Sim Hld Cam En
28	"	(60) 28	Partition Last 3	(152) 88		Cam Rstrt Edge
29	"	(61) 29	Partition First 4	(153) 89		Diagnostic Wrd
30	"	(62) 30	Partition Last 4	(154) 90		0000
31	"	(63) 31	Prescale Clock	(155) 91		0000
32	Code	(64) 32	BCRC	(156) 92		0000
				(157) 93		0000
				(158) 94		0000
Word # if mode 11 or 12				(159) 95		0000
				(160) 96		# of Channels
				Word # if mode 12		

Table for Mode 13.



For the following codes, the value shown for S is the value returned for Standard Operation of that card.

16 Channel cards

ID#	S	Board Description
63	1	16 channel differential multiplexer card

8 Channel cards

ID#	S	Board Description
63	1	HL-8 8 Channel Sample and Hold
42	0	PDAC812 12 Bit DAC

4 Channel cards

ID#	S	Board Description
1	0	PDAC416-A 16 Bit DAC
42	0	PDAC412 12 Bit DAC

2 Channel cards

ID#	S	Board Description
0	1	PGA-4/FILTER card
1	0	PDAC216-A 16 Bit DAC
42	0	DO card
63	1	DI card

1 Channel cards

ID#	S	Board Description
0	1	PGA/PGF
1	0	PDAC116-A 16 Bit DAC
12	1	Single Channel 500KHz 16-Bit ADC
42	0	DO card
63	1	DI card

4.3.8 PARTITION FIRST/LAST BIT 3 (8)

Setting of this bit requires user to send 4 pairs of First and Last data words. The first pair sent are for the primary list of the partitioned cam. The second pair sent are for secondary list 2 of the partitioned cam. The third pair sent is for secondary list 3 and the fourth pair is for secondary list 4. The user must send four pairs of first and last, even if the user only intends to use only two partitions. 8 words are sent in all.

4.3.9 PRESCALE BIT 2 (4)

Setting of this bit requires user to send a Prescale clock divisor data word. This divisor will pre-divide the crystal frequency to the Burst Clock counter or the Mux clock counter, depending of mode of system. If this divisor is not programmed to 1 then a non fatal warning error code of 12 will be reported on power up.

4.3.10 BCRC DIVISOR BIT 1 (2)

A function bit that sets up the system to allow the user to reprogram the BURST CHANNEL RATE CLOCK. This is the clock rate that determines the time between channels within the BURST period.

This Clock Divisor defaults to the system's maximum channel rate when power is applied. Once programmed to a new value, on power up, error 5 will be reported as a non fatal warning error.

4.3.11 CONTROL WORD EXTENSION BIT 0 (1)

This bit is used to give access to the functions controlled by a second extension control word. When this bit of the first EXTENSION COMMAND WORD is HI then, after all data has been sent as required by this first EXTENSION COMMAND WORD, the following word will be interpreted as a second EXTENSION COMMAND WORD. This function is not currently implemented so this bit should be held LO.

5.0 OTHER COMMANDS

5.1 SOFTWARE RESET COMMAND (FFFF)

Entering all one's (FFFF) as a data word at any time resets the system. This resetting of the system includes:

- o Stopping of the system handshake almost immediately.
- o Does not change the previously-programmed control settings.
- o Resets the FIFO and other digital I/O devices.
- o Places the system in the command mode, ready to receive a new COMMAND WORD.

If the system receives an FFFF word while it is in the middle of a programming sequence, the system will exit the task. In this case the user will have to begin programming again, starting with the COMMAND WORD. This could be used as an emergency exit during either the data entry or running modes. Because the data can contain the code FFFF, the SOFTWARE RESET will not be active during the data entry period of functions such as the CAM load or SPECIAL CAM WRITE sequence. The specified number of entries, first to last, must be made before the SOFTWARE RESET will be recognized..

5.2 RUN COMMANDS

A RUN command is a COMMAND word that has bit 7 (RUN STOP ONLY) programmed HI and is not a RESET command.

If bit 7 (RUN ONLY) is programmed HI, then all other bits except bit 6 (RUN), bit 11 (EXTERNAL START), and bit 15 (SPECIAL) will be ignored, except on a SOFTWARE RESET.

5.2.1 RUN COMMAND 1

When bit 7 (RUN STOP ONLY) and bit 6 (RUN) are HI and bit 15 (SPECIAL) is LO, the system will enter the RUN condition. If the system is to be internally started it will start as soon as it has finished its setup routine.

If the system is in the external start mode the external start input circuit will be enabled. The system may then be started with an input to the EXTERNAL START BNC.

This command must be followed by a RESET command after the measurement or test is completed, in order to stop the system and return it to the command mode, ready to receive the next COMMAND WORD.

5.2.2 RUN COMMAND 2

When bit 7 (RUN STOP ONLY) is HI and bit 6 (RUN) is HI and bit 15 (SPECIAL) is HI, the system will enter a special RUN condition. This RUN command is for those systems

using the CAM STOP BIT option. With this option, the system will start as in RUN COMMAND 1 above but will stop when a STOP BIT is detected in the CAM data.

This command must be followed by a RESET command after the measurement or test is completed, in order to return the system to the command mode, ready to receive the next control word.

6.0 DAC CONTROLLER PROGRAMMING

6.1 GENERAL

The DAC Controller card is used to control DACs or Digital outputs. This card plugs on the back of the main backplane and therefore will not use up a slot. The controller has two operating modes. These are:

1) ADC/DAC Simulator Mode
2) DAC only Mode
3) Pre-ADC DAC Entry Mode

In Mode (1), the ADC and DACs share the control hardware example, clock, and address generator. In this mode a FIFO for the DACs is not a requirement. A scan of ADC data is read in, the Host does some crunching, then data is sent to the DACs.

In Mode (2), the DACs have their own controller chassis. This allows any form of DAC timing without consideration for ADC timing unless the DAC system is used in conjunction with an ADC. This mode gets best performance with a FIFO, although it can work without one.

In Mode (3), the data to the DACs is loaded during the setup time to establish the pre-run conditions for the ADC

6.2 PROGRAMMING MODE 1 - ADC/DAC SIMULATOR

In Mode (1), user must program into the CAM table, the ADC sequence followed by the DAC sequence. All DAC channels following the ADC channels must have the STOP BIT set (2k bit). System must be programmed for Burst and the RSO2 run code must be used to invoke the STOP BIT logic and allow system to start.

When the system starts, system will start converting from first channel to the first stop bit. Here the system is stopped on the first DAC channel. The system will remain stopped on that channel until data has been transferred to that channel from the Host, then system advances to the next stop bit, which is the next DAC channel. Again, the system remains stopped until data has been transferred, then moves to the next stop bit. This process is repeated until last channel is reached and data is transferred to that channel.

What happens next is a function of some options that deal with simulation time distortions. If the DACs are dual ranked and time distortion is not much of a problem, COIN XFR may be used at this point to load the second rank of all DACs. This approach is the most straight forward and most simply allows a way to give DACs time to settle before the next ADC scan of channels. See figure 1.

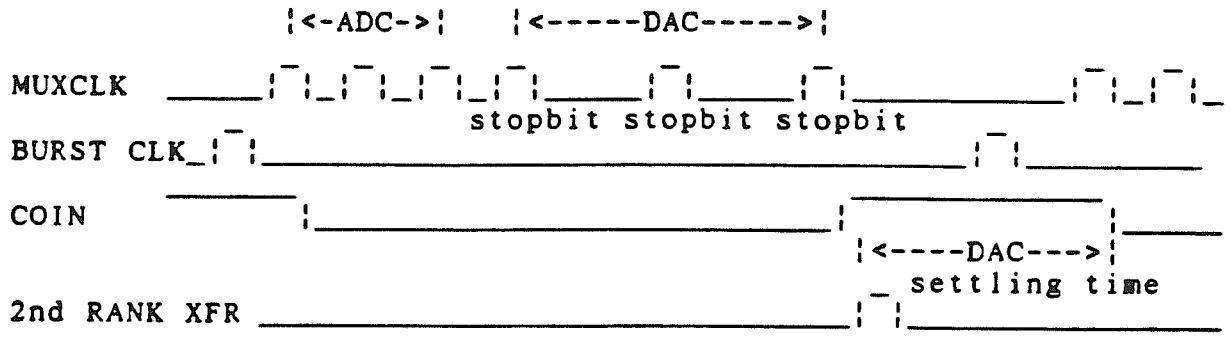


FIGURE 1

If user needs to minimize time distortions, then the Controller must be strapped for Burst Clk transfer. This will cause the second rank of DACs to update at the precise rate of Burst Clk. This however removes DAC settling time. Since the DACs need some time to settle prior to the next ADC scan, user must program into the CAM table some number of extra channels that precede the ADC channels. The number of extra channels required depends on the ADC speed and the DAC settling time. The EXTRA channels should be one of the DAC channels reselected the required number of times and not having the stop bit set. See Fig 2.

Number extra channels = DAC settling time / ADC channel time
(rounded up)

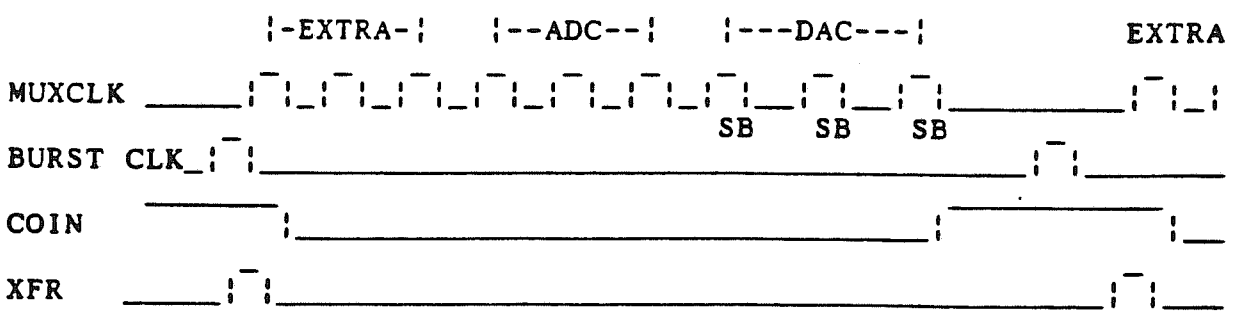


FIGURE 2

If system is operating with Sim Sample & Holds, and extra channels are inserted into the CAM list, then Sim Hold needs to come from Burst Clk with extra delay to occur at first ADC channel or the Sim Enable Bit must be put to use.

6.3 PROGRAMMING MODE 2 - DAC ONLY

In Mode (2), use of the CAM table is an option. User must program the system for Burst mode and use the standard RSO run code. If DAC data is ported directly to the DACs, not through a FIFO, the user must also turn off the Handshake Bit. Transfer rate will be that of the Burst Clock. System must be set up to use the COIN START option of the PC card.

After system receives a run code, the first rank of the DAC channels will be loaded. When the first rank of the last channel loads, the system will either:

1) Start Burst Clock and transfer data to second rank.

or

2) Wait for FIFO Half Full or Full then start Burst clock and transfer data to second rank.

After the Burst Clock is started, it is up to the user to make sure that the data rate to the first rank is fast enough to keep up with the Burst rate programmed.

Transfer rates to a DAC is approximately 700KHz (1.4 uSec). Faster rates might be achieved under special conditions.

FIFO write to DAC	200	-0 +100 nSec	300 max
Muxclk width	500		500
DAC read to LMORE	255		250
DAC CNTRL TMORE to Muxclk	255		250
other accumulated delays	100		100
			=========
Total Time			1.4 uSec

7.0 PROGRAMMING EXAMPLES

7.1 EXAMPLE - BURST RATE CLOCK RE-PROGRAM

A typical programming word string to change the BCRC would be

```
FFFF  RESET COMMAND
A020  CONTROL WORD - Special, Remote, Clock
nnnn  Desired burst channel rate clock divisor.
```

This string would then be followed by the normal UPC setup string of data words.

An alternate method of programming the BCRC is to include it the normal UPC setup string by using the EXTENSION bit.

FFFF	RESET COMMAND
233F	CONTROL WORD - Remote, CAM Enab, Burst, Sequential, Clock, First, Last, CAM Write, Handshake & Extension
0100	CLOCK DIVISOR (Burst)
0000	FIRST CAM LOCATION
0002	LAST CAM LOCATION
000F	CAM DATA FIRST MUX ADDRESS
000E	CAM DATA SECOND MUX ADDRESS
000D	CAM DATA LAST MUX ADDRESS
0002	EXTENSION CONTROL WORD - BCRC
0010	BURST CHANNEL RATE CLOCK DIVISOR
00C0	RUN COMMAND 1

7.2 EXAMPLE - CAM ADDRESS ENTRY

The chart below gives an example of the programming sequence for CAM address entry:

FFFF	RESET COMMAND
231E	CONTROL WORD - Remote, CAM Enab, Burst, Sequential, First, Last, CAM Write, & Handshake
0000	FIRST CAM LOCATION
0002	LAST CAM LOCATION
000F	CAM DATA FIRST MUX ADDRESS
000E	CAM DATA SECOND MUX ADDRESS
000D	CAM DATA LAST MUX ADDRESS
00C0	RUN COMMAND 1

When this program has been entered into the UPC the system will run on the channels indirectly addressed through the channel address memory.

7.3 EXAMPLE - SEQUENTIAL OPERATION WITH INTERNAL CLOCK

This example illustrates sequential operation using the internal clock, starting on Channel 0 and resetting to Channel 0 after converting Channel 3. The system will run continuously after receiving the run command until stopped by a RESET command from the host controller. The UPC clock will start approximately 4 milliseconds after the run command is received.

FFFF	RESET COMMAND
213A	CONTROL WORD - Remote, Sequential, Clock, First Last, & Handshake
0080	CLOCK DIVISOR
0000	FIRST CHANNEL ADDRESS
0003	LAST CHANNEL ADDRESS
00C0	RUN COMMAND 1

7.4 EXAMPLE - PROGRAMMING GAIN OF PPGA-4 AMPLIFIER

This example illustrates the gain programming of a device such as a PPGA-4 amplifier. For this example assume that 8 channels of PPGA-4 amplifiers are at multiplexer address locations 16 through 23.

FFFF	RESET COMMAND
A11C	CONTROL WORD - Special, Remote, Sequential, First, Last & CAM Write
0010	FIRST ADDRESS (16)
0017	LAST ADDRESS (23)
0000	GAIN CODE FOR PPGA-4 CHANNEL 16
0001	GAIN CODE FOR PPGA-4 CHANNEL 17
0001	GAIN CODE FOR PPGA-4 CHANNEL 18
0004	GAIN CODE FOR PPGA-4 CHANNEL 19
0005	GAIN CODE FOR PPGA-4 CHANNEL 20
000B	GAIN CODE FOR PPGA-4 CHANNEL 21
0001	GAIN CODE FOR PPGA-4 CHANNEL 22
0000	GAIN CODE FOR PPGA-4 CHANNEL 23

7.5 EXAMPLE - CAM PARTITION MODE PROGRAMMING

As an example of a partitioned CAM, assume that there is a need to have the following scan requirements:

9 channels at 833.33 kHz per channel (12 uSec period)
7 channels at 27.778 kHz per channel (36 uSec period)
7 channels at 6.9444 kHz per channel (144 uSec period)
10 channels at 0.6944 kHz per channel (1440 uSec period)

This can be accomplished by building the following table in the CAM

Primary List	Secondary list 1	Sec list 2	Sec list 3
pos#1	pos#1	pos#1	pos#1
2	2	2	2
3	X3	3	3
X4	4	X4	4
5	5	5	5
12uS 6	36uS 6	144uS 6	1440uS 6
7	X7	7	7
X8	8	8	8
9	9		9
10		(x4)	10
11	(x3)		
X12			(x10)

x = Bit 16 of CAM DATA is set

The above table assumes a 1uS per channel ADC. Each time an x is encountered in the primary list, that data word is replaced with data at the next level. In this way, it is possible to build a CAM table to incorporate Hi speed channels, those of the primary list, with those of slower speeds, list 2, 3 and 4. The ratio between the lists is the total number of X's in the preceding list divided into the number of channels for the list of interest.

Example: Secondary list 1 has 9 channels. How long does it take to go through one scan of all these channels?

Solution: The preceding list, the primary list shows there are 3 X's, or 3 times per scan of the primary list, data is replaced by the secondary list. Since there are 9 items in the secondary list, it will take 3 passes of the primary list to get through all 9 items, thus

9 / 3 = 3 (times longer than primary)

where 9 is number of channels in list,
where 3 is number of X's in preceding list.

Answer is then 3 x 12uSec or 36uSec.

Note: The time to scan the primary list is dictated by mode burst or non-burst and scan clock divisor.

The following commands will program the PRESYS system to perform this function:

FFFF	RESET COMMAND
2101	CONTROL WORD - Remote, Sequential & Extension
4004	EXTENSION CONTROL WORD - Partition Mode, Partition First/last
0000	PRIMARY PARTITION FIRST (0)
000B	PRIMARY PARTITION LAST (11)
0010	SECONDARY 1 PARTITION FIRST (16)

0018	SECONDARY 1 PARTITION LAST (24)
0020	SECONDARY 2 PARTITION FIRST (32)
0027	SECONDARY 2 PARTITION LAST (39)
0030	SECONDARY 3 PARTITION FIRST (48)
0039	SECONDARY 3 PARTITION LAST (57)
211C	CONTROL WORD - Remote, Sequential, First, Last, CAM Write
0000	FIRST PRIMARY CAM LOCATION (0)
000B	LAST PRIMARY CAM LOCATION (11)
0000	CAM DATA FIRST MUX ADDRESS (0)
0001	CAM DATA SECOND MUX ADDRESS (1)
0002	CAM DATA THIRD MUX ADDRESS (2)
8000	CAM DATA SHIFT
0003	CAM DATA FOURTH MUX ADDRESS (3)
0004	CAM DATA FIFTH MUX ADDRESS (4)
0005	CAM DATA SIXTH MUX ADDRESS (5)
8000	CAM DATA SHIFT
0006	CAM DATA SEVENTH MUX ADDRESS (6)
0007	CAM DATA EIGHTH MUX ADDRESS (7)
0008	CAM DATA NINTH MUX ADDRESS (8)
8000	CAM DATA SHIFT
211C	CONTROL WORD - Remote, Sequential, First, Last, CAM Write
0010	FIRST SECONDARY 1 CAM LOCATION (16)
0018	LAST SECONDARY 1 CAM LOCATION (24)
0009	CAM DATA FIRST MUX ADDRESS (9)
000A	CAM DATA SECOND MUX ADDRESS (10)
8000	CAM DATA SHIFT
000B	CAM DATA THIRD MUX ADDRESS (11)
000C	CAM DATA FOURTH MUX ADDRESS (12)
000D	CAM DATA FIFTH MUX ADDRESS (13)
8000	CAM DATA SHIFT
000E	CAM DATA SIXTH MUX ADDRESS (14)
000F	CAM DATA SEVENTH MUX ADDRESS (15)
211C	CONTROL WORD - Remote, Sequential, First, Last, CAM Write
0020	FIRST SECONDARY 2 CAM LOCATION (32)
0027	LAST SECONDARY 2 CAM LOCATION (39)
0010	CAM DATA FIRST MUX ADDRESS (16)
0011	CAM DATA SECOND MUX ADDRESS (17)
0012	CAM DATA THIRD MUX ADDRESS (18)
8000	CAM DATA SHIFT
0013	CAM DATA FOURTH MUX ADDRESS (19)
0014	CAM DATA FIFTH MUX ADDRESS (20)
0015	CAM DATA SIXTH MUX ADDRESS (21)
0016	CAM DATA SEVENTH MUX ADDRESS (22)
211C	CONTROL WORD - Remote, Sequential, First, Last, CAM Write
0030	FIRST SECONDARY 3 CAM LOCATION (48)
0039	LAST SECONDARY 3 CAM LOCATION (57)
0017	CAM DATA FIRST MUX ADDRESS (23)
0018	CAM DATA SECOND MUX ADDRESS (24)
0019	CAM DATA THIRD MUX ADDRESS (25)
001A	CAM DATA FOURTH MUX ADDRESS (26)

001B	CAM DATA FIFTH MUX ADDRESS (27)
001C	CAM DATA SIXTH MUX ADDRESS (28)
001D	CAM DATA SEVENTH MUX ADDRESS (29)
001E	CAM DATA EIGHTH MUX ADDRESS (30)
001F	CAM DATA NINTH MUX ADDRESS (31)
0020	CAM DATA TENTH MUX ADDRESS (32)
233C	CONTROL WORD - Remote, CAM Enab, Burst, Sequential, Clock, First, Last & Handshake
000A	CLOCK DIVISOR (10)
0000	PRIMARY PARTITION FIRST (0)
000B	PRIMARY PARTITION LAST (11)
00C0	RUN COMMAND 1

7.6 EXAMPLE - DAC CONTROLLER PROGRAMMING

MODE 1 - ADC/DAC SIMULATION

Assume there is a system of 8 analog channels and 4 DAC channels to be run in the simulation mode. Send the following command string:

FFFF	RESET COMMAND
273F	CONTROL WORD - Remote, Burst, Cam Enable, Sequential, Clock, First, Last, Cam Write, Handshake & Extension
0008	BURST CLOCK DIVISOR (8 mSec)
0000	FIRST ADDRESS (0)
000B	LAST ADDRESS (11)
0000	CAM DATA FIRST MUX ADDRESS (0)
0001	CAM DATA SECOND MUX ADDRESS (1)
0002	CAM DATA THIRD MUX ADDRESS (2)
0003	CAM DATA FOURTH MUX ADDRESS (3)
0004	CAM DATA FIFTH MUX ADDRESS (4)
0005	CAM DATA SIXTH MUX ADDRESS (5)
0006	CAM DATA SEVENTH MUX ADDRESS (6)
0007	CAM DATA EIGHTH MUX ADDRESS (7)
0108	CAM DATA FIRST CAM ADDRESS + STOP BIT (2048+8)
0109	CAM DATA SECOND CAM ADDRESS + STOP BIT (2048+9)
010A	CAM DATA THIRD CAM ADDRESS + STOP BIT (2048+10)
010B	CAM DATA FOURTH CAM ADDRESS + STOP BIT(2048+11)
1024	EXTENSION CONTROL WORD - Redirect Mode, Redirect Address, & Prescale
0064	REDIRECT ADDRESS TO DAC (100)
2710	PRESCALE DIVISOR (10000) CONVERT 10 mHz TO 1kHz
80C0	SPECIAL RSO RUN FOR STOP BIT

READ 8 WORDS OF ADC DATA

OUTPUT 4 WORDS OF DAC DATA

Loop back to "READ 8 WORDS OF ADC DATA"

MODE 2 - DAC ONLY

Assume there is a system of 8 analog channels and 4 DAC channels to be run in the DAC only mode. Send the following command string:

FFFF	RESET COMMAND
WAIT 1 mSec	
FFFF	RESET COMMAND
273F	CONTROL WORD - Remote, Burst, Cam Enable, Sequential, Clock, First, Last, Cam Write, Handshake & Extension
03E8	CLOCK DIVISOR (1000) BURST CLOCK
0000	FIRST ADDRESS (0)
0003	LAST ADDRESS (3)
0008	CAM DATA FIRST CAM ADDRESS (8)
0009	CAM DATA SECOND CAM ADDRESS (9)
000A	CAM DATA THIRD CAM ADDRESS (10)
000B	CAM DATA FOURTH CAM ADDRESS (11)
1066	EXTENSION CONTROL WORD - Redirect Mode, Environment Word, Redir. Addr, Prescale, & BCRC
0A00	FORCE COIN START
0040	REDIRECT ADDRESS TO DACs FIFO (64)
0001	PRESCALE DIVISOR (1)
0000	BCRC
00C0	RUN COMMAND

OUTPUT DAC DATA

DACs will output data after the required amount of data has been entered into the FIFO.

MODE 3 - Pre-ADC DAC Entry

Assume there is a system of 8 analog channels and 4 DAC channels to be run in the Pre-ADC DAC entry mode. Send the following command string:

FFFF	RESET COMMAND

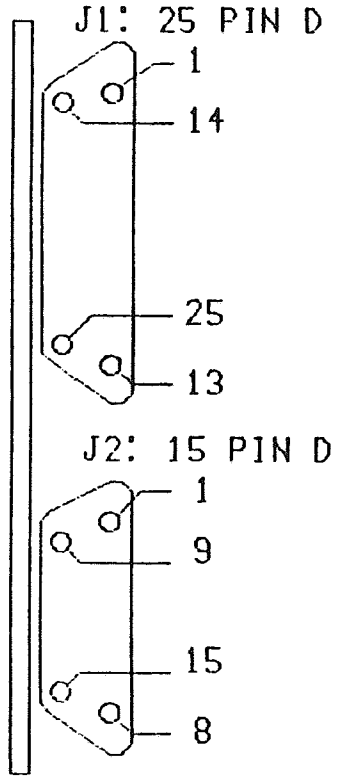
WAIT 1 mSec

A11E	CONTROL WORD - Special, Remote, Sequential, First, Last, Cam Write & Handshake
0008	FIRST ADDRESS (8) OF DAC0
000B	LAST ADDRESS (11) OF DAC3
dddd	CAM DATA FOR FIRST CAM - DAC0
dddd	CAM DATA FOR SECOND CAM - DAC1
dddd	CAM DATA FOR THIRD CAM - DAC2
dddd	CAM DATA FOR FOURTH CAM - DAC3
FFFF	RESET COMMAND

THE DACs ARE NOW OUTPUTTING THE REQUIRED DATA

OUTPUT THE COMMANDS TO RUN THE ADC IN THE DESIRED MODE

CONNECTOR PIN ASSIGNMENTS



REAR VIEW

J1 ANALOG INPUTS

PIN	SIGNAL	PIN	SIGNAL
1	CH0 HI	7	CH4 HI
2	CH0 LO	8	CH4 LO
14	CH0 GND	20	CH4 GND
15	CH1 HI	21	CH5 HI
16	CH1 LO	22	CH5 LO
3	CH1 GND	9	CH5 GND
4	CH2 HI	10	CH6 HI
5	CH2 LO	11	CH6 LO
17	CH2 GND	23	CH6 GND
18	CH3 HI	24	CH7 HI
19	CH3 LO	25	CH7 LO
6	CH3 GND	12	CH7 GND
		13	PWR GND

J2 SIM S/H CONTROL

PIN	SIGNAL
1	Y1
9	GND
2	Y2
10	GND
3	Y3
11	GND
4	Y4
12	GND
5	Y5
13	GND
6	Y6
14	GND
7	Y7
15	GND

ANALOG SUB-MUX, P/N 200520-T

200520-T

MODEL PMX-2B

PRESYS 1000 BUFFERED MUX

INTRODUCTION:

The model and PMX-2B buffered multiplexer cards provide high input impedance to user input signals and low output impedance to drive a single-ended CMOS multiplexer integrated circuit. This isolates user amplifier outputs from multiplexer switching transients.

For additional information on multiplexing errors refer to the Preston application note entitled "Dynamic Input Characteristics of Analog Multiplexers used in Analog to Digital Conversion Systems".

They are packaged on standard PRESYS 1000 plug in cards with 37 pin D type connectors mounted on the rear for user inputs and are directly interchangeable with the PMX multiplexer cards. The model PMX-2B may be used with any of the PRESYS A/D converters except models which operate at 1MHz conversion rate.

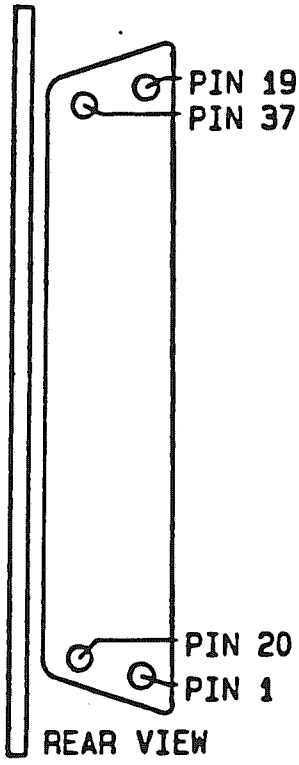
BASIC SPECIFICATIONS:

Input channels:	16 single-ended (quasi-differential)
Full-scale:	+/- 10 volts
Maximum Input:	+/- 15 volts without damage
Zero Offset:	+/- 125 microvolts
Gain Error:	+/- .005%
Tempco:	15 microvolts per degree C RTI
Input Impedance:	Greater than 10 megohms shunted by 50 pf maximum
Settling time:	2 microseconds

PRESTON

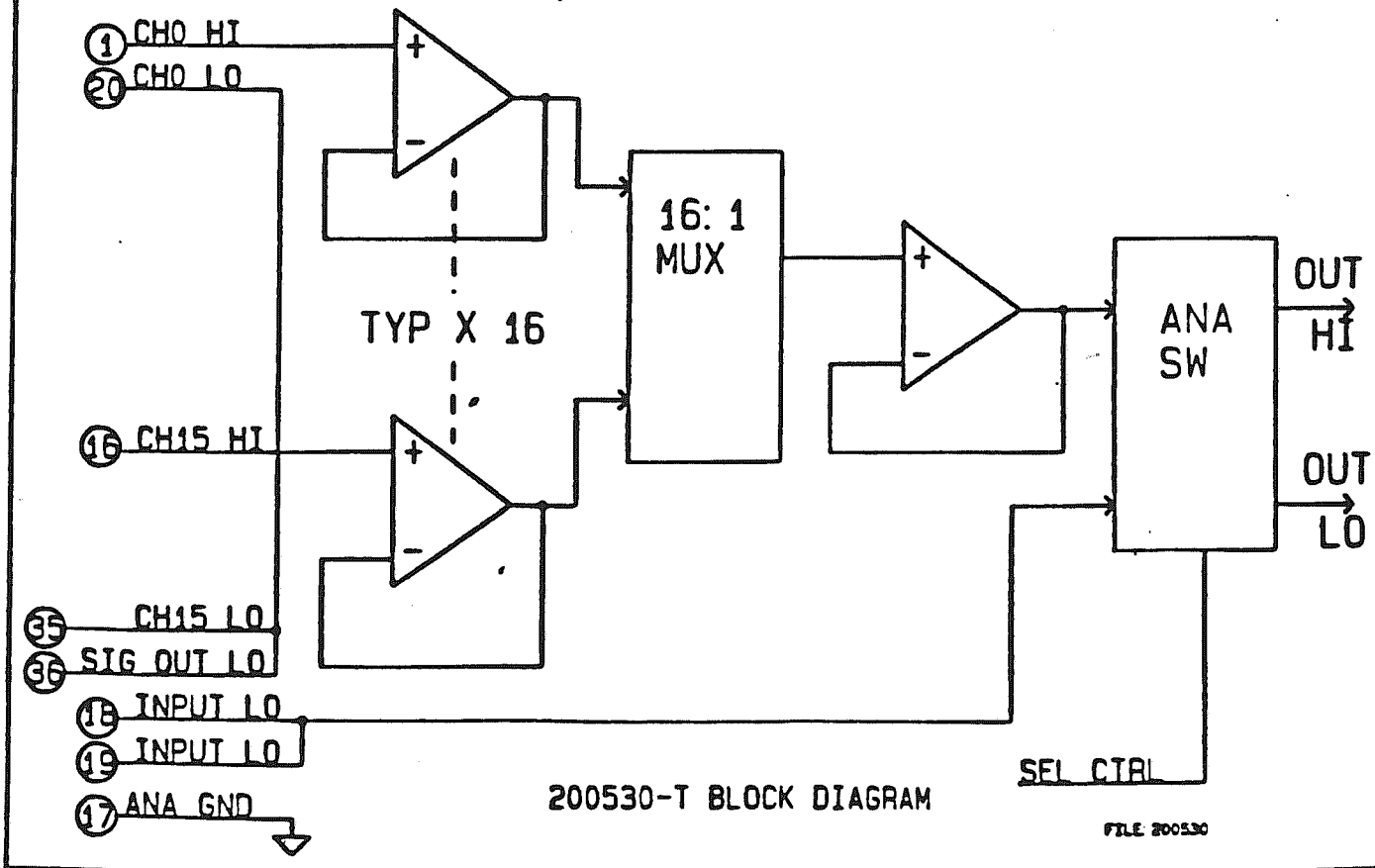
Preston Scientific
1180 N. Blue Gum Street, Anaheim, CA 92806
Tel: (714) 632-3700 FAX: (714) 632-7355

BUFFERED MULTIPLEXER 16 CHN
P/N 200530-00,-01 (PMX-2B)



SIGNAL	PIN#
PWR GND	37
SIG OUT LO	36
CH 15 SH/LO	35
CH 14 SH/LO	34
CH 13 SH/LO	33
CH 12 SH/LO	32
CH 11 SH/LO	31
CH 10 SH/LO	30
CH 9 SH/LO	29
CH 8 SH/LO	28
CH 7 SH/LO	27
CH 6 SH/LO	26
CH 5 SH/LO	25
CH 4 SH/LO	24
CH 3 SH/LO	23
CH 2 SH/LO	22
CH 1 SH/LO	21
CH 0 SH/LO	20

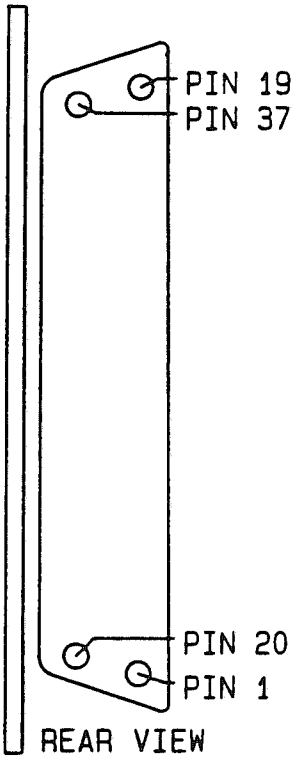
PIN#	SIGNAL
19	INPUT LO
18	INPUT LO
17	ANA GND
16	CH 15 HI
15	CH 14 HI
14	CH 13 HI
13	CH 12 HI
12	CH 11 HI
11	CH 10 HI
10	CH 9 HI
9	CH 8 HI
8	CH 7 HI
7	CH 6 HI
6	CH 5 HI
5	CH 4 HI
4	CH 3 HI
3	CH 2 HI
2	CH 1 HI
1	CH 0 HI



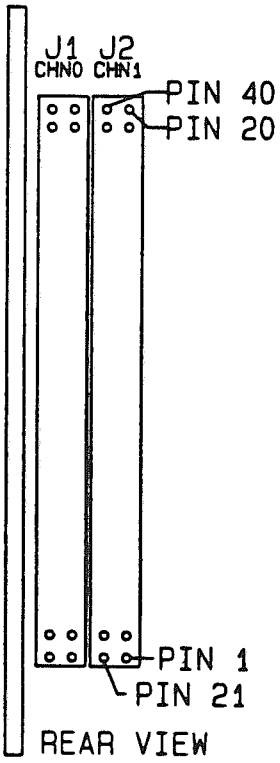
200530-T BLOCK DIAGRAM

FILE 200530

DIGITAL INPUT 201125-T



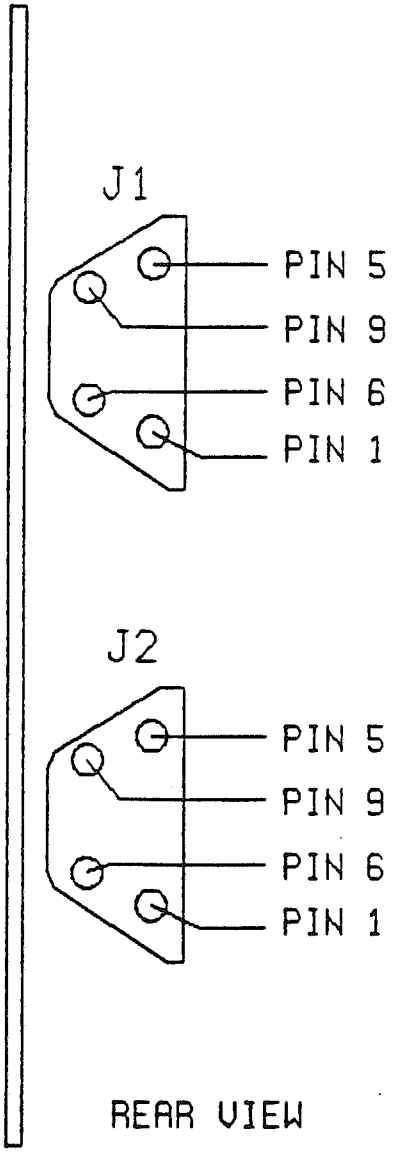
SIGNAL	PIN	PIN	SIGNAL
BUSGND	37	19	ACKOUT0
BUSGND	36	18	INSTB0
BUSGND	35	17	FRZOUT0
BUSGND	34	16	INDATA 1
BUSGND	33	15	INDATA 2
BUSGND	32	14	INDATA 4
BUSGND	31	13	INDATA 8
BUSGND	30	12	INDATA 16
BUSGND	29	11	INDATA 32
BUSGND	28	10	INDATA 64
BUSGND	27	9	INDATA 128
BUSGND	26	8	INDATA 256
BUSGND	25	7	INDATA 512
BUSGND	24	6	INDATA 1K
BUSGND	23	5	INDATA 2K
BUSGND	22	4	INDATA 4K
BUSGND	21	3	INDATA 8K
BUSGND	20	2	INDATA 16K
		1	INDATA 32K



J1 CHANNEL 0				J2 CHANNEL 1			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
BUSGND	40	20	N/C	BUSGND	40	20	N/C
BUSGND	39	19	ACKOUT0	BUSGND	39	19	N/C
BUSGND	38	18	INSTB0	BUSGND	38	18	INSTB1
BUSGND	37	17	FRZOUT0	BUSGND	37	17	FRZOUT1
BUSGND	36	16	INDATA 1	BUSGND	36	16	INDATA 1
BUSGND	35	15	INDATA 2	BUSGND	35	15	INDATA 2
BUSGND	34	14	INDATA 4	BUSGND	34	14	INDATA 4
BUSGND	33	13	INDATA 8	BUSGND	33	13	INDATA 8
BUSGND	32	12	INDATA 16	BUSGND	32	12	INDATA 16
BUSGND	31	11	INDATA 32	BUSGND	31	11	INDATA 32
BUSGND	30	10	INDATA 64	BUSGND	30	10	INDATA 64
BUSGND	29	9	INDATA 128	BUSGND	29	9	INDATA 128
BUSGND	28	8	INDATA 256	BUSGND	28	8	INDATA 256
BUSGND	27	7	INDATA 512	BUSGND	27	7	INDATA 512
BUSGND	26	6	INDATA 1K	BUSGND	26	6	INDATA 1K
BUSGND	25	5	INDATA 2K	BUSGND	25	5	INDATA 2K
BUSGND	24	4	INDATA 4K	BUSGND	24	4	INDATA 4K
BUSGND	23	3	INDATA 8K	BUSGND	23	3	INDATA 8K
BUSGND	22	2	INDATA 16K	BUSGND	22	2	INDATA 16K
BUSGND	21	1	INDATA 32K	BUSGND	21	1	INDATA 32K

FILE: 201125

16 / 32 BIT COUNTER
P/N 201215-T



J1

PIN#	SIGNAL
1	CLOCK 0 HI
2	START 0 HI
3	CLEAR 0 HI
4	NOT USED
5	NOT USED
6	CLOCK 0 LO
7	START 0 LO
8	CLEAR 0 LO
9	NOT USED

J2

PIN#	SIGNAL
1	CLOCK 1 HI
2	START 1 HI
3	CLEAR 1 HI
4	NOT USED
5	NOT USED
6	CLOCK 1 LO
7	START 1 LO
8	CLEAR 1 LO
9	NOT USED

FILE 201215

Table of Contents

Introduction:
The 16/32 Bit Counter Card contains two (2) 16 bit counters which can be used independently, or connected together to form one (1) 32 bit counter. When used as one (1) 32 bit counter the 16 LSBs are addressed as channel 0 and the 16 MSBs are addressed as channel 1. Each counter has its own clock, start, and clear inputs. Each counter has circuitry which freezes the output value prior to reading, after the counter is read, it is restored to normal operation. During the count "freeze" period the counter itself does not miss any clock pulses.

Input drive requirements:
All external inputs to the counter card are optically isolated and must be capable of driving the isolator's LED which is about 5.1mA at 5 volts or about 12.5mA at 10 volts.
Do not exceed 12 volts on any isolated input!
If higher or lower logic voltages are used you will need to select a new resistor value for R1 through R6. The formula (Resistor = Vhigh/0.0125) can be used to calculate R1 through R6. Where Vhigh is the high logic level voltage. R1-R6 are series current limit resistors for the isolator LED. Example: if 28 volt logic is used then R = 28/0.0125 = 2240 ohms, so use 2.2k.

Counter Clock:
Each counter clock features back to back LED's for clock pulse polarity correction. The maximum allowable clocking frequency is 1MHz and the minimum clock pulse width is 500nS. This clocking limitation is due to the filtering that goes on at the input for noise rejection. The CLOCK HI input is pin 1, and the "CLOCK LO" input is pin 6 on the user connector.

Counter Clear:
Each counter can be internally, externally, or never cleared (Reset to 0000h), depending on jumper selections made on the card.

Internal-clear: When jumper selected, is one of the following:
  RESET1* (the interface reset)
  RESET2* (the System FFFFh reset)
  RESET3* (a special user defined reset)
External-clear: When jumper selected, occurs when the user provides a pulse to the "External Clear" pin on the user connector. The external clear function can be made active hi, or active lo by the proper jumper selection.

Counter Start:
Each counter can be internally, or externally started. The start signal is only used once the counter has been cleared. The counter only looks at the edge of the start signal (which is edge selectable) to start. The start edge will be ignored if the "clear" signal is active.

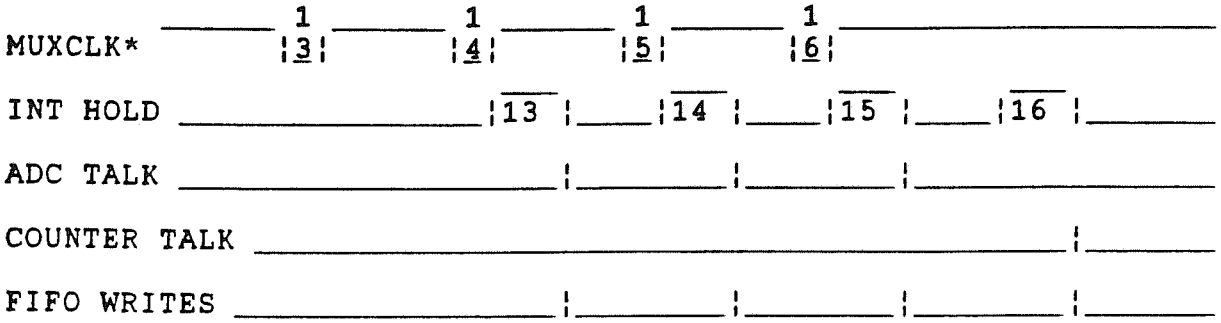
Internal-start: when selected, triggers on the RSO RUN COMMAND.
External-start: when selected, triggers when the user provides a start edge (+/- edge selectable) at the "External Start" pin.

Data transfer modes:
The two read modes, used to transfer Counter data to the PreSys Fifo, will be referred to as "CHANNEL MODE" AND "SQUEEZE MODE".

CHANNEL MODE:
The counter will transmit its data when the system addresses the Counter as a channel. Like an ADC analog channel, this method uses up one channel time per channel.

"Channel Mode" example: 3 ADC channels, and 1 counter channel. The entire scan takes 4 channel times.

CHANNEL MODE TIMING:



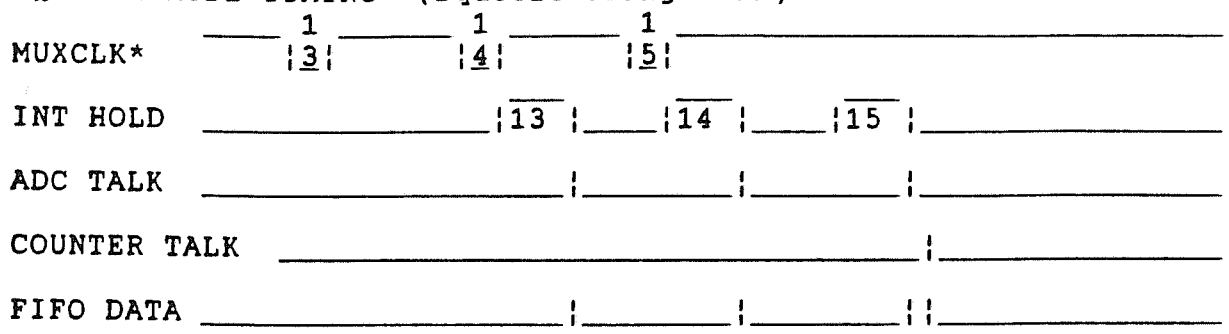
In this example data from the system is in the following order:

1) Channel #13 ADC data
2) Channel #14 ADC data
3) Channel #15 ADC data
4) Channel #16 Counter data

SQUEEZE MODE:
The counter transmits its data AFTER a "Channel Mode" device has transmitted its data word. Unlike a "Channel Mode" device, this method does not use up a channel time. The user chooses "when" the counter is to squeeze its data into the data stream by using either the COIN signal, or a CAM bit (32k, 16k, 8k, 4k). Choosing COIN will place the Counter data after the last addressed channel in a scan. Using a CAM bit allows you to place the counter channel anywhere in a scan. NOTE: Squeeze mode will not work in an expansion chassis.

"Squeeze mode" example: 3 ADC channels, and 1 counter channel. The entire scan now only takes 3 channel times.

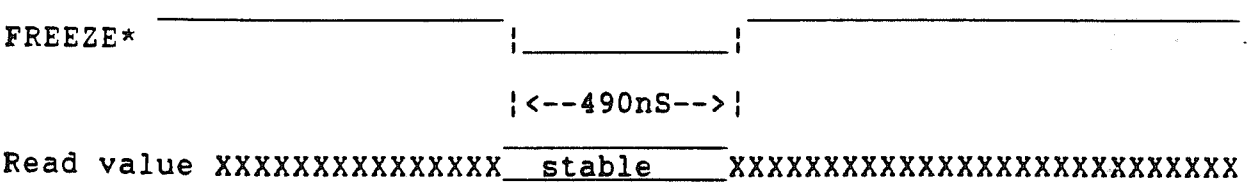
SQUEEZE MODE TIMING (Squeeze using COIN).



In this example data from the system is in the following order:

1) Channel #13 ADC data
2) Channel #14 ADC data
3) Channel #15 ADC data
4) Counter data

Counter "read" register freeze:
Each counter has a "read" register which is normally allowed to follow the value of the counter. Moments prior to reading the "read" register, a freeze signal is generated to tell the read register to hold its contents steady. The "read" register is not allowed to update while the freeze signal is asserted. Clock pulses are counted during this time, however they are not allowed to affect the value in the "read" register. The "read" value will once again follow the counter value when the freeze signal goes away. The "read" register is frozen about 490nS before it is read (1MHz timing).



The timing of the freeze line changes slightly with ADC type. Other Setup times for the 500Khz and 307Khz systems are listed below.

Max ADC speed	freeze line
1MHz	490nS (max)
500KHz	890nS (max)
307KHz	1890nS (max)

CONFIGURATION JUMPERS:

The following mode, configuration, and polarity jumpers need to be setup prior to operation.

****** MODE SELECTION JUMPERS ******

	"Squeeze" (Main chassis)	"Channel" (Main chassis)	"Channel" (Exp. chassis)	
W23	OUT	OUT	IN	Exp. enable
W25	IN	OUT	OUT	Squeeze enable
W37	OUT	IN	IN	Poll enable
W62	---	POLL 1	POLL 1	Poll 1 chan
W63	---	POLL 2	POLL 2	Poll 2 chan
W34	1 TALK	IN	IN	1 talk
W33	2 TALK	OUT	OUT	2 talks

****** CONFIGURATION JUMPERS ******

W26 IN=freezes Counter 0 when "block freeze" happens.
W27 IN=freezes Counter 1 when "block freeze" happens.

W30 IN=inhibits "block freeze" signal. -MUST CHOOSE ONE-
W31 IN=makes "block freeze" when Counter 0 is read.
W32 IN=makes "block freeze" when Counter 1 is read.

W35 IN=ID/DAT0 select. (If omitted allows 2 chan listen)
W36 IN=ID/DAT1 select. (If omitted with W21 allows 4 ch)

W38 Listen address 1 (out)
W39 Listen address 2 (out)
W40 Listen address 4 (out)
W41 Listen address 8 (out)
W42 Listen address 16 (out)
W43 Listen address 32 (out)
W44 Listen address 64 (Installed)
W45 Listen address 128 (out)

W46 Talk address 1 (out)
W47 Talk address 2 (out)
W48 Talk address 4 (out)
W49 Talk address 8 (out)
W50 Talk address 16 (out)
W51 Talk address 32 (out)
W52 Talk address 64 (Installed)
W53 Talk address 128 (out)

W61 block freeze to MISC 7. (Caution: make sure the line you)
W60 block freeze to MISC 6. (choose is not in use)
W59 block freeze to MISC 5. (by another device.)
W58 block freeze to MISC 4.
W57 block freeze to MISC 3.
W56 block freeze to MISC 2.

W55 block freeze to MISC 1.
W54 block freeze to MISC 0.

W64 Squeezes on COIN. -MUST CHOOSE ONE-
W65 Squeezes on CAM BIT 32k
W66 Squeezes on CAM BIT 16k
W67 Squeezes on CAM BIT 8k
W68 Squeezes on CAM BIT 4k

****** POLARITY JUMPERS ******

W2 IN=positive going edge start for Counter 0.
W3 IN=negative going edge start for Counter 0.

W4 IN=positive level clear for Counter 0.
W5 IN=negative level clear for Counter 0.

W13 IN=positive going edge start for Counter 1.
W14 IN=negative going edge start for Counter 1.

W15 IN=positive level clear for Counter 1.
W16 IN=negative level clear for Counter 1.

NUMERICAL LIST OF JUMPERS:

The following is a quick run down of all the jumpers used on the 16/32 Bit Counter Card. For a detailed explanation of the purpose of each jumper, refer to the "Jumper Discussion" section, just following this section.

JUMPER #	FUNCTION	
W1	Start source: Counter 0 (int) ADC run condition.	(*)
W2	Start source: Counter 0 (ext) positive edge.	(*)
W3	Start source: Counter 0 (ext) negative edge.	(*)
W4	Clear source: Counter 0 (ext) negative edge.	(*)
W5	Clear source: Counter 0 (ext) positive edge.	(*)
W6	Clear source: Counter 0 (int) RESET1*.	(*)
W7	Clear source: Counter 0 (int) RESET2*.	(*)
W8	Clear source: Counter 0 (int) RESET3*.	(*)
W9	IN=32 bit counter. (also install W11,W20)	
W10	IN=16 bit counters. (also install W21,W22)	
W11	IN=32 bit counter. (also install W9,W20)	
W12	Start source: Counter 1 (int) ADC run condition.	(*)
W13	Start source: Counter 1 (ext) positive edge.	(*)
W14	Start source: Counter 1 (ext) negative edge.	(*)
W15	Clear source: Counter 1 (ext) negative edge.	(*)
W16	Clear source: Counter 1 (ext) positive edge.	(*)
W17	Clear source: Counter 1 (int) RESET1*.	(*)
W18	Clear source: Counter 1 (int) RESET2*.	(*)
W19	Clear source: Counter 1 (int) RESET3*.	(*)
W20	IN=32 bit counter. (also install W9,W11)	
W21	IN=16 bit counters. (also install W10,W22)	
W22	IN=16 bit counters. (also install W10,W21)	
W23	Expansion chassis select.	
W24	Do Not Install	
W25	Squeeze mode select.	
W26	"block freeze" use signal to freeze Counter 0.	
W27	"block freeze" use signal to freeze Counter 1.	
W28	Spare	
W29	Spare	
W30	"block freeze" disable.	(*)
W31	"block freeze" source from Counter 0.	(*)
W32	"block freeze" source from Counter 1.	(*)

NOTES: (*) Must install one jumper out of the group.

NUMERICAL LIST OF JUMPERS: (Continued)

W33 Double talk (*)
W34 Single talk (*)

W35 ID/DAT 0 (fly listen)
W36 ID/DAT 1 (fly listen)

W37 Poll enable

W38 Listen address 1
W39 Listen address 2
W40 Listen address 4
W41 Listen address 8
W42 Listen address 16
W43 Listen address 32
W44 Listen address 64 (factory installed)
W45 Listen address 128

W46 Talk address 1
W47 Talk address 2
W48 Talk address 4
W49 Talk address 8
W50 Talk address 16
W51 Talk address 32
W52 Talk address 64 (factory installed)
W53 Talk address 128

W54 "block freeze" to Misc 7 (bus)
W55 "block freeze" to Misc 6 (bus)
W56 "block freeze" to Misc 5 (bus)
W57 "block freeze" to Misc 4 (bus)
W58 "block freeze" to Misc 3 (bus)
W59 "block freeze" to Misc 2 (bus)
W60 "block freeze" to Misc 1 (bus)
W61 "block freeze" to Misc 0 (bus)

W62 1 channel poll (*)
W63 2 channel poll (*)

W64 If squeeze mode, squeeze on COIN. (*)
W65 If squeeze mode, squeeze on CAM bit 4k. (*)
W66 If squeeze mode, squeeze on CAM bit 8k. (*)
W67 If squeeze mode, squeeze on CAM bit 16k. (*)
W68 If squeeze mode, squeeze on CAM bit 32k. (*)

NOTES: (*) Must install one jumper out of the group.

Jumper Discussion:

Below is an explanation of the different jumpers and their function. This information is provided to give the user a more thorough understanding of the 16/32 Bit Counter Card. Since it is impossible to describe how all of these jumpers will affect every system, please consult the factory before changing any of the jumpers on this or any card.

W1-W2-W3 Start source for Counter 0 (16 bit). Also the start source for the counter if it is configured as a 32 bit counter. The counter will ignore any clock signals until the start signal has been detected. This start signal is edge sensitive. Once started additional start signals will be ignored until the counter is stopped by a clear. Only one (1) jumper should be install at a time. W1 selects the RUN signal from the ADC, therefore installing this jumper will start the counter anytime the ADC is put into a run condition. W2-W3 selects external start. If pin 2 is connected to a positive going external start signal and pin 6 connected to its ground return, then installing W2 will start the counter when a positive true signal is seen, while W3 will start the counter when a negative true signal is seen.

W4-W5-W6-W7-W8 Clear sources for Counter 0 (16 bit). Also the clear for the counter if it is configured as a 32 bit counter. The counter will reset it's value to 0000h upon receiving a clear pulse. The counter is also stopped and requires a "start" signal to begin counting again. The clear signal is level sensitive, so holding the clear signal active will prevent the counter from starting. W4-W5 selects external clear. With pin 3 connected to a positive true signal and pin 8 connected to its ground return, installing W4 will cause a clear when a positive true signal is applied, while installing W5 will cause a clear when a negative true signal is applied. W6-W7-W8 are internal clears. W6 is RESET1*, which is asserted whenever the interface is reset. W7 is RESET2*, which is asserted whenever the system is reset with FFFFh or stopped. W8 is RESET3*, which is not normally implemented, but per user requirements would be asserted whenever a specific user need is met.

W10-W21-W22 are used to separate the counters to function as two (2) independent 16 bit counters. Omit W9-W11-W20.

W9-W11-W20 are used to connect the two 16 bit counters together to form as a single (1) 32 bit counter. Omit W10-W21-W22.

W12-W13-W14 Start select for Counter 1. (Same as W1-W2-W3) except this start is for Counter 1, and is NOT used when counter is setup as a (1) 32 bit counter.

W15-W16-W17-W18-W19 Clear select for Counter 1. (Same as W4-W5-W6-W7-W8) except this clear is for Counter 1, and is NOT used when setup as a (1) 32 bit counter.

W23 Expansion chassis select. When the counter card is used in an expansion chassis, this jumper must be installed to provide the proper timing to the expansion chassis.

W24 DO NOT INSTALL!!!

W25 Squeeze mode select. Install to select "squeeze mode" data transfer. Omit to select "channel mode" (normal) data transfer.

W26-W27 "Block freeze" use select. Whenever a group of counters is to be read, or even the (1) 32 bit counter, a means of freezing all counters to be read is necessary. In order to freeze a group of counter cards in a block, we first need a signal called "Block freeze" this signal would be generated (or sourced) by the first counter in the block only! All counters connected to (or using) the "Block freeze" signal would freeze their count values and wait to be read. After reading, a counter is (unfrozen and) allowed to update once again, until all counters have been read and the entire block is updating normally. Now that we have "Block freeze" we need a way to use it. That's where W26 and W27 come in. W26 tells Counter 0 to freeze when it gets the "Block freeze" signal. W27 tells Counter 1 to freeze when it gets the block freeze signal.

W28-W29 Spares.

W30-W31-W32 "Block freeze" Source Select.
(See W26-W27 for "using" the source) This selection chooses who will be the "source" of the "block freeze" signal. The "source" must be the first channel of the block that needs to be frozen together. One of the (3) jumpers must always be installed. If "block freeze" is not used, W30 must be installed. W31 selects Counter 0 as the "block freeze" source, and W32 selects Counter 1 as the "block freeze" source. If the card is being configured as (1) 32 bit counter, "block freeze" should come from Counter 0 and is used by Counter 1 to freeze the entire counter as a block. In this case the "block freeze" signal need not leave the card and drive a Miscellaneous (Misc) line on the backplane. However, if this counter is the first of many counters that need to be frozen as a block, driving a Misc line will be necessary. (Please see W54-W61 for driving the Misc lines). Normally, W30 is installed and no connection to "block freeze" is used. Freezing occurs on each counter individually as the counter is read.

W33-W34 Double/Single Talk Select. Selects how the talk protocol logic is to work on the card. W34 is used to provide a single talk for "channel mode" operation, where the ADC system is providing an address that selects Counter (0 or 1) as a channel. In "squeeze mode" operation, W34 selects Counter 0 (16 bits) to be read. W33 is used only in "squeeze mode" operation where both Counters, (0 and 1) are read together, either as (2) 16 bit counters, or (1) 32 bit counter.

W35-W36 ID/DAT0 and ID/DAT1 selection. These jumpers are very user specific, and are normally left off. For the sake of completeness of information on this card it will be discussed briefly here. W35 and W36 are used in systems where ADC data is being sent to multiple Fifo's. That is, where some or all ADC data is being sent to fifo #1 and other ADC data is being sent to fifo #2, on a channel-by-channel bases. This type of operation is referred to as "fly talking" where the talk address of the ADC section is modified "on the fly". Anyway, in order to "squeeze" a counter channel into a system of this type, a method to "fly listen" must be used, and that is what W35 and W36 allow us to do. When W35 and W36 are left off the counter card will "fly listen" to all (4) fly talk addresses. When W35 (ID/DAT0) is installed, the Counter card will "fly listen" to only (2) fly talk addresses. If W35 and W36 are installed, the Counter card will "fly listen to only (1) fly talk address. For info on "fly talking" read the description on the Opto Interface Card.

W37-W62-W63 Polling selection. Polling is used in "channel mode" to build a configuration table, on power up, that contains a contiguous block of addressable channels. Gaps left by removing cards from the system are removed automatically from the channel list so that an uninterrupted sequence of channels exists from first to last channel. W37 enables polling. W62 and W63 tells the system how many addressable channels exist on the card. W62 installed tells PreSys the card is a (1) channel card where installing W63 tells PreSys the card is a (2) channel card. Install W63 if the counter is setup as (1) 32 bit counter, the 16 LSBs will be channel 0 and the 16 MSBs channel 1.

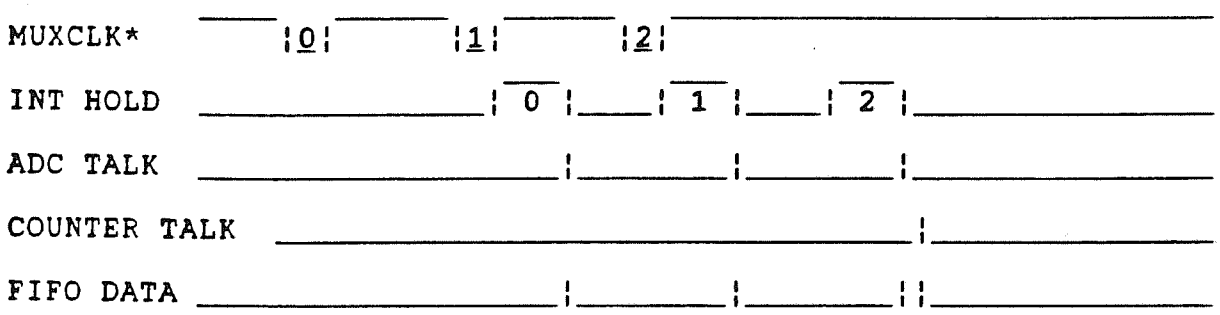
W38-W39-W40-W41-W42-W43-W44-W45 Listen address select jumpers. Allows the standard listen address of 64, to be changed. Increases system resources for special user needs. An alternate listen address would be needed if multiple or fly talking ADC's were being implemented.

W64-W47-W48-W49-W50-W51-W52-W53 Talk address select jumpers. Allows the standard talk address of 64 to be changed. Increases system resources, same as the ability to change the listen address, for special user requirements. An alternate talk address would be needed if multiple interface Fifo's were being used.

W54-W55-W56-W57-W58-W59-W60-W61 "Block freeze" drive lines. For maximum flexibility, the "Block freeze" signal may drive any of the 8 miscellaneous lines (0-7). Once the "Block freeze" signal is generated on a card, it can be routed and used by other cards via the miscellaneous lines. (See W30-W31-W32 for sourcing the "Block freeze" signal, and W26-W27 for using the "Block freeze" signal).

W64-W65-W66-W67-W68 Select squeeze channel location. "Squeeze mode" data will immediately follow data from a "channel mode" device. In order to tell the counter card when to squeeze its' data, a method of marking the specified channel is needed. W65 through W68 are CAM bit positions 4k-32k respectfully which may be used to mark the channel at which squeezing is to occur. (4) possible CAM bits are available so the likelihood of a CAM bit being used for another purpose is minimized. The 5th jumper (W64) is used to squeeze data on COIN (after last channel). If W65 through W68 are used, the CAM must be programmed, however if W64 is used (COIN), no CAM need be programmed. If more than (1) counter card is running in squeeze mode and using the same "squeeze channel location" then the order of the squeezed channels will be from left to right (as viewed from the back of the chassis) the left hand most card squeezing it's data first.

SQUEEZE MODE TIMING (squeeze using COIN).

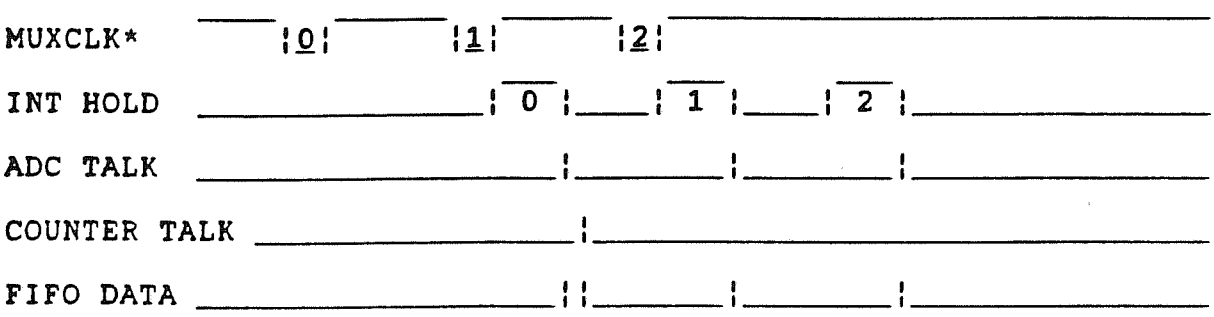


In this example data from the system is in the following order:
1) Channel #0 ADC data
2) Channel #1 ADC data
3) Channel #2 ADC data
4) Counter data

SQUEEZE MODE TIMING (Squeeze using a CAM bit).

"Squeeze mode" example #2: The first channel must, as part of its channel value, have a cam data bit set (say the 4k bit, where W65 is also installed on the counter card) for proper operation.

The CAM would contain the following data:
0 = 0 (0001 0000 0000 0000) *notice 4k bit set*
1 = 1 (0000 0000 0000 0001)
2 = 2 (0000 0000 0000 0010)



Data read out of the Fifo will be organized as follows:
1) Channel #0 ADC data
2) Counter data
3) Channel #1 ADC data
4) Channel #2 ADC data

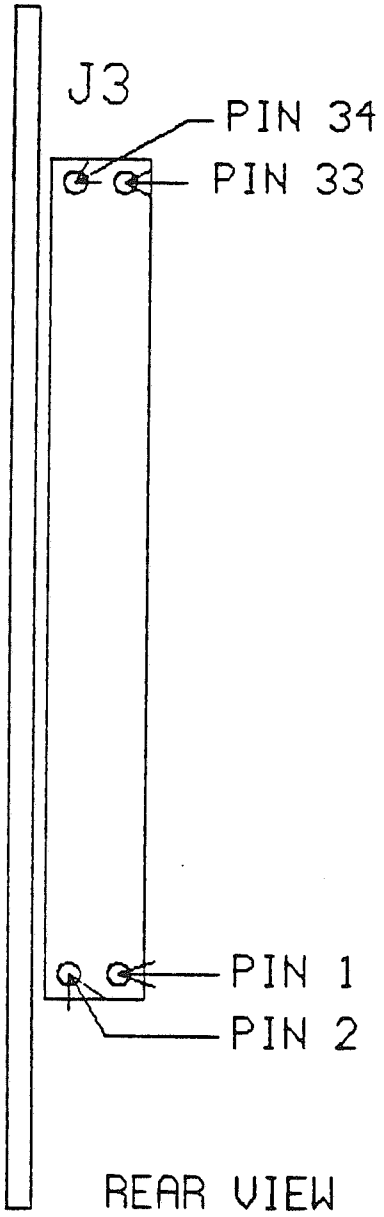
INPUT CONNECTOR:
The 16/32 bit counter card connector may be of two types. Unless otherwise specified (2) 9 pin "D" style connectors are used. A single (1) 37 pin "D" style connector maybe be used, in that case the pin assignments will need to be adjusted accordingly.

CONNECTOR PIN OUT:

J1 37 PIN D Counter 0-1		J1 9 PIN D Counter 0		J2 9 PIN D Counter 1	
PIN 01	CLOCK 1 HI	PIN 01	CLOCK 0 HI	PIN 01	CLOCK 1 HI
PIN 02	START 1 HI	PIN 02	START 0 HI	PIN 02	START 1 HI
PIN 03	CLEAR 1 HI	PIN 03	CLEAR 0 HI	PIN 03	CLEAR 1 HI
PIN 04	not used	PIN 04	not used	PIN 04	not used
PIN 05	not used	PIN 05	not used	PIN 05	not used
PIN 06	not used	PIN 06	CLOCK 0 LO	PIN 06	CLOCK 1 LO
PIN 07	not used	PIN 07	START 0 LO	PIN 07	START 1 LO
PIN 08	not used	PIN 08	CLEAR 0 LO	PIN 08	CLEAR 1 LO
PIN 09	not used	PIN 09	not used	PIN 09	not used
PIN 10	not used				
PIN 11	not used				
PIN 12	not used				
PIN 13	not used				
PIN 14	not used				
PIN 15	CLOCK 0 HI				
PIN 16	START 0 HI				
PIN 17	CLEAR 0 HI				
PIN 18	not used				
PIN 19	not used				
PIN 20	CLOCK 1 LO				
PIN 21	START 1 LO				
PIN 22	CLEAR 1 LO				
PIN 23	not used				
PIN 24	not used				
PIN 25	not used				
PIN 26	not used				
PIN 27	not used				
PIN 28	not used				
PIN 29	not used				
PIN 30	not used				
PIN 31	not used				
PIN 32	not used				
PIN 33	not used				
PIN 34	CLOCK 0 LO				
PIN 35	START 0 LO				
PIN 36	CLEAR 0 LO				
PIN 37	not used				

28V, ISOLATED DIGITAL INPUT, 32 CH.

PART NUMBER 201220-00



REAR VIEW

SIGNAL	PIN	SIGNAL	PIN
DL0	34	DL0	33
D16HI	32	D00HI	31
D17HI	30	D01HI	29
D18HI	28	D02HI	27
D19HI	26	D03HI	25
D20HI	24	D04HI	23
D21HI	22	D05HI	21
D22HI	20	D06HI	19
D23HI	18	D07HI	17
D24HI	16	D08HI	15
D25HI	14	D09HI	13
D26HI	12	D10HI	11
D27HI	10	D11HI	9
D28HI	8	D12HI	7
D29HI	6	D13HI	5
D30HI	4	D14HI	3
D31HI	2	D15HI	1

201220_BD

Table of Contents

Introduction:

The ISO 2 Channel Digital Input Card P/N 201220-T is a two channel, 16 bits per channel, isolated digital input card. The two channels together total 32 bits of digital input. Data bits 0-15 are on channel 0, and data bits 16-31 are on channel 1.

Input drive requirements:

All user supplied data inputs are optically isolated, and must be capable of driving the isolator's LED which is about 8.1mA at 28 volts. The inputs are also protected against reverse polarity damage. Do not exceed 40 volts maximum on any input!

The 28 volt input voltage will result in a logic "1" level stored in the PreSys Fifo. If the interface doesn't invert the data, then a logic high value will be read into the host computer. The logic transition point (from low-to-high) is around 13 volts using the Dash -00 resistor networks for 28 volt input.

If 5 volt logic voltages are needed, you will need to change the resistor networks RN1-RN4 to 330 ohm (Dash -01). RN1-RN4 are series current limit resistors for the isolator LED. In this case do not exceed 5.4 volts on any isolated input!.

Data insertion:

The three methods or MODES available to transfer data will be referred to as:

MODE 1 (SQUEEZE)

MODE 2 (ADDRESS)

MODE 3 (EXPANSION).

MODE 1: This method is the fastest. Data is squeezed in AFTER the ADC has transmitted its data word. This method does not use a channel time to transfer data. The data word is triggered to squeeze by either the COIN signal, or a CAM BIT. Choosing COIN places the DI data word after the last channel in the scan. Choosing a CAM BIT allows the squeezed channel to be placed in between any ADC channel within a scan.

NOTE: Squeeze mode only works in a main chassis. If more than one DI card is to squeeze, the squeeze order is fixed from lowest to highest slot number (that is, cards to the left will squeeze before cards to the right). Squeeze mode may also squeeze data on request, using the INSTROBE signal, this is useful for sending data to another card asynchronously. (Note: Squeeze on request is not available on the ISO 2 Channel Digital Input Card P/N 201220-T).

MODE 2: This method is slow, but can use all of the features the ADC uses. In this mode data is read from the Digital Input card by Addressing the channel. Data is then transmitted to the bus in place of ADC data. Each data read requires one mux clock.

MODE 3: This mode works like mode 2 except in an Expansion box. Data is addressed one channel for each mux clock.

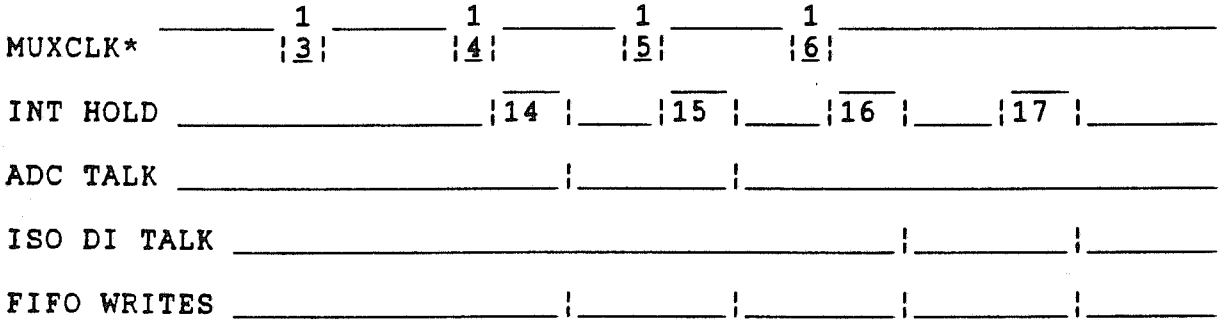
Data insertion timing information:

The two read modes, used to transfer input data to the PreSys Fifo, are better known as "CHANNEL MODE" (Mode 2&3) AND "SQUEEZE MODE" (Mode 1).

CHANNEL MODE: (Mode 2&3)
In Channel Mode the card transmits its data when the system addresses a channel on the card. Like an ADC analog channel, this method uses up one channel time per channel.

"Channel Mode" example: 2 ADC channels, and 2 ISO DI channels. The entire scan takes 4 channel times.

CHANNEL MODE TIMING:



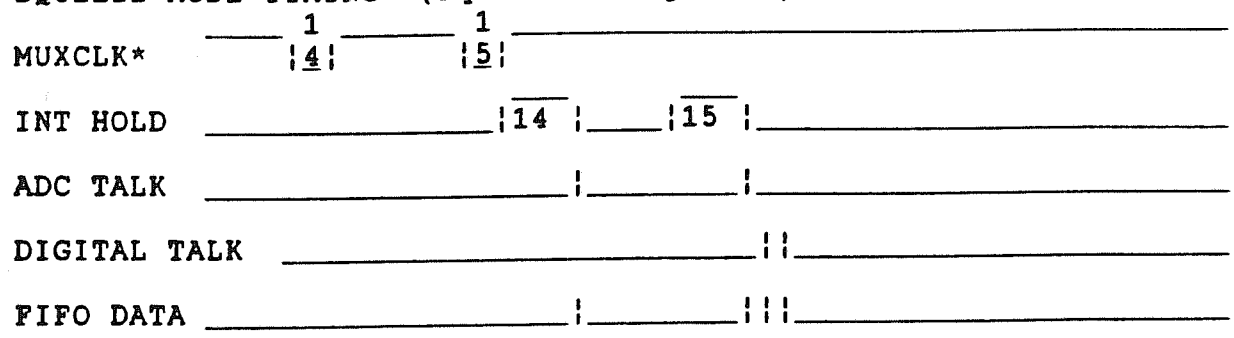
In this example data from the system is in the following order:

1) Channel #14 ADC data
2) Channel #15 ADC data
3) Channel #16 Iso digital input data
4) Channel #17 Iso digital input data

SQUEEZE MODE: (Mode 1)
In Squeeze Mode the card transmits its data AFTER a "Channel Mode" device has transmitted its data word. Unlike a "Channel Mode" device, this method does not use up a channel time. The user chooses "when" the card is to squeeze its data into the data stream by using either the COIN signal, or a CAM bit (32k, 16k, 8k, 4k). Choosing COIN will place the ISO data channel after the last addressed channel in a scan. Using a CAM bit allows you to place the ISO digital channel anywhere in a scan. NOTE: Squeeze mode will not work in an expansion chassis.

"Squeeze mode" example: 2 ADC channels, and 2 ISO DI channels. The entire scan now only takes 2 channel times.

SQUEEZE MODE TIMING (Squeeze using COIN).



In this example data from the system is in the following order:

1) Channel #14 ADC data
2) Channel #15 ADC data
3) ISO digital input data
4) ISO digital input data

CONFIGURATION JUMPERS:

The following mode, configuration, and polarity jumpers need to be setup prior to operation.

****** MODE SELECTION JUMPERS ******

	MODE 1 "Squeeze" (Main chassis)	MODE 2 "Channel" (Main chassis)	MODE 3 "Channel" (Exp. chassis)	
W3	OUT	OUT	IN	Exp. enable
W5	IN	OUT	OUT	Squeeze enable
W31	OUT	IN	IN	Poll enable
W32	---	POLL 1	POLL 1	Poll 1 chan
W33	---	POLL 2	POLL 2	Poll 2 chan
W16	1 TALK	IN	IN	1 talk
W15	2 TALK	OUT	OUT	2 talks

****** CONFIGURATION JUMPERS ******

For (MODE 1):

SQUEEZE DATA AFTER ADC	SQUEEZE DATA ON COMMAND
W4=OUT	W4=IN (n/a)
W19=OUT	W19=IN (n/a)
W20=IN	W20=OUT (n/a)

W6	IN=freezes channel 0 when "block freeze" happens.		(out)
W7	IN=freezes channel 1 when "block freeze" happens.		(out)
W12	IN=inhibits "block freeze" signal.	(*)	(in)
W13	IN=makes "block freeze" when channel 0 is read.	(*)	(out)
W14	IN=makes "block freeze" when channel 1 is read.	(*)	(out)
W21	IN=ID/DAT0 select. (If omitted allows 2 chan listen)		(out)
W22	IN=ID/DAT1 select. (If omitted with W21 allows 4 ch)		(out)

W23	Listen address 1	(out)
W24	Listen address 2	(out)
W25	Listen address 4	(out)
W26	Listen address 8	(out)
W27	Listen address 16	(out)
W28	Listen address 32	(out)
W29	Listen address 64	(Installed)
W30	Listen address 128	(out)

(*)=MUST CHOOSE ONE! (out of the group)
(n/a)=Not applicable, has no function but may require tie off.
(out/in)=defaults

```
W47  Talk address 1      (out)
W48  Talk address 2      (out)
W49  Talk address 4      (out)
W50  Talk address 8      (out)
W51  Talk address 16     (out)
W52  Talk address 32     (out)
W53  Talk address 64     (Installed)
W54  Talk address 128    (out)

W34  block freeze to MISC 7.  ( Caution: make sure the line you )
W35  block freeze to MISC 6.  (          choose is not in use   )
W36  block freeze to MISC 5.  (          by another device.     )
W37  block freeze to MISC 4.
W38  block freeze to MISC 3.
W39  block freeze to MISC 2.
W40  block freeze to MISC 1.
W41  block freeze to MISC 0.

W42  Squeezes on COIN.           (*)                      (in)
W43  Squeezes on CAM BIT 32k     (*)                      (out)
W44  Squeezes on CAM BIT 16k     (*)                      (out)
W45  Squeezes on CAM BIT 8k      (*)                      (out)
W46  Squeezes on CAM BIT 4k      (*)                      (out)


****** POLARITY JUMPERS ******

W1   (IN=POS, OUT=NEG) INSTRB FOR CHANNEL 0.              (n/a "out")
W2   (IN=POS, OUT=NEG) INSTRB FOR CHANNEL 1.              (n/a "out")

W17  IN=positive CH0 ACK* pulse.  (pin 19)  (*)           (n/a "out")
W18  IN=negative CH0 ACK* pulse.  (pin 19)  (*)           (n/a  "in")

W10  (IN=POS, OUT=NEG) FREEZE CHANNEL 0.                  (n/a "out")
W11  (IN=POS, OUT=NEG) FREEZE CHANNEL 1.                  (n/a "out")

(*)=MUST CHOOSE ONE! (out of the group)
(n/a)=Not applicable, has no function but may require tie off.
(out/in)=defaults
```

NUMERICAL LIST OF JUMPERS:

The following is a quick run down of all the jumpers used on the ISO 2 Channel Digital Input Card. For a detailed explanation of the purpose of each jumper, refer to the "Jumper Discussion" section, just following this section.

W1	STROBE0 polarity. (IN=POS, OUT=NEG)		(n/a)
W2	STROBE1 polarity. (IN=POS, OUT=NEG)		(n/a)
W3	Chassis type select. (IN=EXPANSION, OUT=MAIN)		
W4	Disable coin bit. (use for squeeze on strobe)		(out)
W5	SQUEEZE mode.		
W6	Sets FREEZE0 line when "block freeze" happens.		(n/a)
W7	Sets FREEZE1 line when "block freeze" happens.		(n/a)
W8	Channel 1 rank select. (IN=DUAL, OUT=SINGLE)	(n/a)	(out)
W9	Channel 0 rank select. (IN=DUAL, OUT=SINGLE)	(n/a)	(out)
W10	FREEZE0 output polarity. (IN=POS, OUT=NEG)		(n/a)
W11	FREEZE1 output polarity. (IN=POS, OUT=NEG)		(n/a)
W12	Install to inhibit FREEZE ALL signal.		(*)
W13	Install to generate FREEZE ALL with FREEZE0 signal.		(*)
W14	Install to generate FREEZE ALL with FREEZE1 signal.		(*)
W15	double talk. (squeeze both channels)		(*)
W16	single talk. (squeeze only channel 0) and (channel mode)		(*)
W17	Positive going CH0 ACK* pulse. (pin 19)	(n/a)	(*)
W18	Negative going CH0 ACK* pulse. (pin 19)	(n/a)	(*)
W19	If squeeze mode, squeeze on STROBE0.	(n/a)	(*)
W20	If squeeze mode, squeeze on LCLK.	(n/a)	(*)
W21	ID/DAT 0 (fly listen)		
W22	ID/DAT 1 (fly listen)		
W23	Listen address 1		
W24	Listen address 2		
W25	Listen address 4		
W26	Listen address 8		
W27	Listen address 16		
W28	Listen address 32		
W29	Listen address 64 (factory installed)		
W30	Listen address 128		

(*)=MUST CHOOSE ONE! (out of the group)
(n/a)=Not applicable, has no function but may require tie off.
(out/in)=defaults

W31 Install to Enable Polling.
W32 Install for 1 channel poll. (*)
W33 Install for 2 channel poll. (*)

W34 Block Freeze to MISC 7.
W35 Block Freeze to MISC 6.
W36 Block Freeze to MISC 5.
W37 Block Freeze to MISC 4.
W38 Block Freeze to MISC 3.
W39 Block Freeze to MISC 2.
W40 Block Freeze to MISC 1.
W41 Block Freeze to MISC 0.

W42 If squeeze mode, squeeze on COIN. (*)
W43 If squeeze mode, squeeze on CAM BIT 32k (*)
W44 If squeeze mode, squeeze on CAM BIT 16k (*)
W45 If squeeze mode, squeeze on CAM BIT 8k (*)
W46 If squeeze mode, squeeze on CAM BIT 4k (*)

W47 Talk address 1
W48 Talk address 2
W49 Talk address 4
W50 Talk address 8
W51 Talk address 16
W52 Talk address 32
W53 Talk address 64 (factory installed)
W54 Talk address 128

(*)=MUST CHOOSE ONE! (out of the group)
(n/a)=Not applicable, has no function but may require tie off.
(out/in)=defaults

Jumper Discussion:

Below is an explanation of the different jumpers and their function. This information is provided to give the user a more thorough understanding of the ISO 2 Channel Digital Input Card. Since it is impossible to describe how all of these jumpers will affect every system, please consult the factory before changing any of the jumpers on this or any card.

W1-W2 Input Strobe polarity select. When the digital input card is configured to squeeze data on command, these two jumpers are used to change which edge the data transfer occurs on. W1 determines the polarity of channel 0 and W2 for channel 1. Not used with ISO digital cards.

W3 Expansion chassis select. When the digital input card is used in an expansion chassis, this jumper must be installed to provide the proper timing to the expansion chassis.

W4 "Coin Bit Disable". Is used to disable the COIN/CAM squeeze mechanism so the squeeze-on-request function will work properly.

W5 Squeeze mode select. Selects between the "squeeze mode" data transfer timing and the "channel mode" (normal) data transfer timing.

W6-W7 "Block freeze" use select. Whenever a group of digital input cards is to be read, a means of freezing all channels to be read is necessary. In order to freeze a group together, we use a signal called "Block freeze" this signal would be generated (or sourced) by the first channel in the block only! All channels connected to (or using) the "Block freeze" signal would freeze their value and wait to be read.

After reading, a channel is (unfrozen and) allowed to update once again, until all channels have been read and the entire block is updating normally. Now that we have "Block freeze" we need a way to use it. That's where W6 and W7 come in. W6 tells Channel 0 to freeze when it gets the "Block freeze" signal. W7 tells Channel 1 to freeze when it gets the block freeze signal.

W8-W9 "Rank" select. Selects the operating mode of the digital input card. In Single Rank Mode, any data on the input of the connector is read in when the channel is read by the system. In Dual Rank Mode, data is strobed into the first rank by the user. (single rank mode only for ISO digital input cards)

W10-W11 "Freeze" output polarity. The "freeze" signal is used by the user to know when to stop moving the input data (in single rank mode). W10 determines the output drive polarity of this signal, when asserted, for channel 0. W11 determines the polarity of channel 1. (No output available on ISO digital input cards)

W12-W13-W14 "Block freeze" Source Select. (See W13-W14 for "using" the source) This selection chooses who will be the

"source" of the "block freeze" signal. The "source" must be the first channel of the block that needs to be frozen together. One of the (3) jumpers must always be installed. If "block freeze" is not used, W12 must be installed. W13 selects Channel 0 as the "block freeze" source, and W14 selects Channel 1 as the "block freeze" source.

If the card is being configured as (1) 32 bit digital word, "block freeze" should come from Channel 0 and is used by Channel 1 to freeze the entire card as a block. In this case the "block freeze" signal need not leave the card and drive a Miscellaneous (Misc) line on the backplane. However, if this card is the first of many digital cards that need to be frozen as a block, driving a Misc line will be necessary. (Please see W34-W41 for driving the Misc lines). Normally, W12 is installed and no connection to "block freeze" is used. Freezing occurs on each channel individually as the card is read.

W15-W16 Double/Single Talk Select. Selects how the talk protocol logic is to work on the card. W16 is used to provide a single talk for "channel mode" operation, where the ADC system is providing an address that selects Channel (0 or 1). In "squeeze mode" operation, W16 selects Channel 0 only to be read. W15 is used only in "squeeze mode" operation where both Channels, (0 and 1) are read together.

W21-W22 ID/DAT0 and ID/DAT1 selection. These jumpers are very user specific, and are normally left off. For the sake of completeness of information on this card it will be discussed briefly here. W21 and W22 are used in systems where ADC data is being sent to multiple Fifo's. That is, where some or all ADC data is being sent to fifo #1 and other ADC data is being sent to fifo #2, on a channel-by-channel bases. This type of operation is referred to as "fly talking" where the talk address of the ADC section is modified "on the fly".

Anyway, in order to "squeeze" a digital channel into a system of this type, a method to "fly listen" must be used, and that is what W21 and W22 allow us to do. When W21 and W22 are left off, the card will "fly listen" to all (4) fly talk addresses. When W21 (ID/DAT0) is installed, the card will "fly listen" to only (2) fly talk addresses. If W21 and W22 are installed, the card will "fly listen to only (1) fly talk address. For info on "fly talking" read the description on the Opto Interface Card.

W31-W32-W33 Polling selection. Polling is used in "channel mode" to build a configuration table, on power up, that contains a contiguous block of addressable channels. Gaps left by removing cards from the system are removed automatically from the channel list so that an uninterrupted sequence of channels exists from first to last channel. W31 enables polling. W32 and W33 tells the system how many addressable channels exist on the card. W32 installed tells PreSys the card is a (1) channel card where installing W33 tells PreSys the card is a (2) channel card.

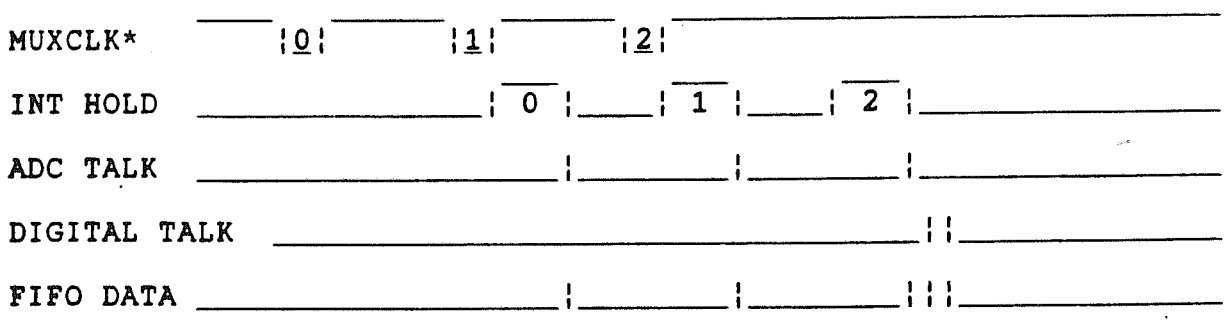
W23-W24-W25-W26-W27-W28-W29-W30 Listen address select jumpers. Allows the standard listen address of 64, to be changed. Increases system resources for special user needs. An alternate listen address would be needed if multiple or fly talking ADC's were being implemented.

W47-W48-W49-W50-W51-W52-W53-W54 Talk address select jumpers. Allows the standard talk address of 64 to be changed. Increases system resources, same as the ability to change the listen address, for special user requirements. An alternate talk address would be needed if multiple interface Fifo's were being used.

W41-W40-W39-W38-W37-W36-W35-W34 "Block freeze" drive lines. For maximum flexibility, the "Block freeze" signal may drive any of the 8 miscellaneous lines (0-7). Once the "Block freeze" signal is generated on a card, it can be routed and used by other cards via the miscellaneous lines. (See W12-W13-W14 for sourcing the "Block freeze" signal, and W6-W7 for using the "Block freeze" signal).

W42-W43-W44-W45-W46 Select squeeze channel location. "Squeeze mode" data will immediately follow data from a "channel mode" device. In order to tell the digital card when to squeeze its' data, a method of marking the specified channel is needed. W46 through W43 are CAM bit positions 4k-32k respectfully which may be used to mark the channel at which squeezing is to occur. (4) possible CAM bits are available so the likelihood of a CAM bit being used for another purpose is minimized.
The 5th jumper (W42) is used to squeeze data on COIN (after last channel). If W43 through W46 are used, the CAM must be programmed, however if W42 is used (COIN), no CAM need be programmed. If more than (1) digital card is running in squeeze mode and using the same "squeeze channel location" then the order of the squeezed channels will be from left to right (as viewed from the back of the chassis) the left hand most card squeezing it's data first.

SQUEEZE MODE TIMING (squeeze using COIN).

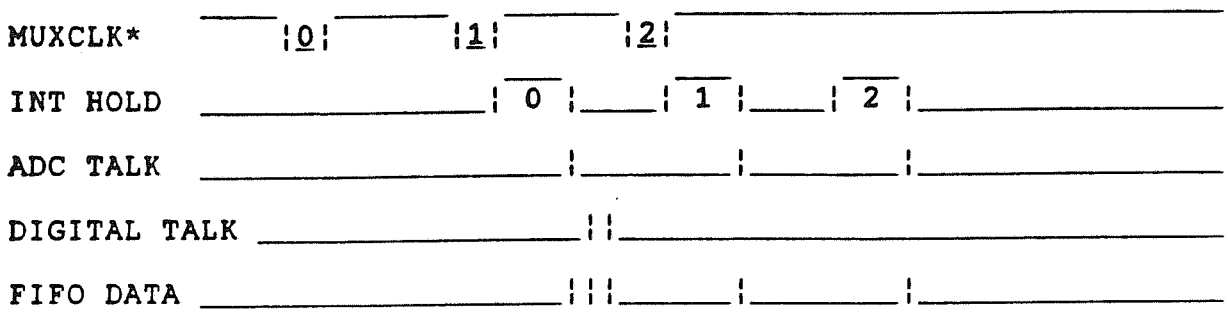


In this example, data from the system is in the following order:
1) Channel #0 ADC data
2) Channel #1 ADC data
3) Channel #2 ADC data
4) Digital data word 0
5) Digital data word 1

SQUEEZE MODE TIMING (Squeeze using a CAM bit).

"Squeeze mode" example #2: The first channel must, as part of its channel value, have a cam data bit set (say the 4k bit, where W46 is also installed on the digital card) for proper operation.

The CAM would contain the following data:
0 = 0 (0001 0000 0000 0000) *notice 4k bit set*
1 = 1 (0000 0000 0000 0001)
2 = 2 (0000 0000 0000 0010)



Data read out of the Fifo will be organized as follows:
1) Channel #0 ADC data
2) Digital data word 0
3) Digital data word 1
3) Channel #1 ADC data
4) Channel #2 ADC data

INPUT CONNECTOR:

The ISO 2 Channel Digital Input Card connector is a 34 pin header type connector whose signal pin assignments are as follows:

CONNECTOR PIN OUT:

J3 34 PIN
Digital Input

PIN 01	D15 HI
PIN 02	D31 HI
PIN 03	D14 HI
PIN 04	D30 HI
PIN 05	D13 HI
PIN 06	D29 HI
PIN 07	D12 HI
PIN 08	D28 HI
PIN 09	D11 HI
PIN 10	D27 HI
PIN 11	D10 HI
PIN 12	D26 HI
PIN 13	D09 HI
PIN 14	D25 HI
PIN 15	D08 HI
PIN 16	D24 HI
PIN 17	D07 HI
PIN 18	D23 HI
PIN 19	D06 HI
PIN 20	D22 HI
PIN 21	D05 HI
PIN 22	D21 HI
PIN 23	D04 HI
PIN 24	D20 HI
PIN 25	D03 HI
PIN 26	D19 HI
PIN 27	D02 HI
PIN 28	D18 HI
PIN 29	D01 HI
PIN 30	D17 HI
PIN 31	D00 HI
PIN 32	D16 HI
PIN 33	DLO
PIN 34	DLO

DYNAMIC INPUT CHARACTERISTICS OF ANALOG MULTIPLEXERS USED IN ANALOG TO DIGITAL CONVERSION SYSTEMS

Early in the 1960's, the introduction of the transistor to data acquisition systems permitted an increase in signal acquisition speed. Since that time, the dynamic input characteristics of analog multiplexers have been a potential source of error in those systems.

It is easy to describe the static input characteristics of a multiplexer and to analyze the errors contributed by those characteristics. Typically the specifications will describe the input resistance and pump-out current for the on-state and for the off-state of the multiplexer switch. Knowing the DC impedance characteristics of the source then permits the applications engineer, or user, to calculate the resulting error.

To analyze the dynamic situation is far more complex. It is first necessary to characterize a multiplexer during the time that it is switching from one channel to another. Then it is necessary to characterize the signal source and to determine its response to the switching of the multiplexer. This interaction will be further influenced by the length, capacity and resistance of the interconnection.

DYNAMIC CHARACTERISTICS OF THE MULTIPLEXER SWITCH

The first characteristic of the multiplexer switch to consider is the capacity to signal common of the output bus of the switch (see Figure 1).

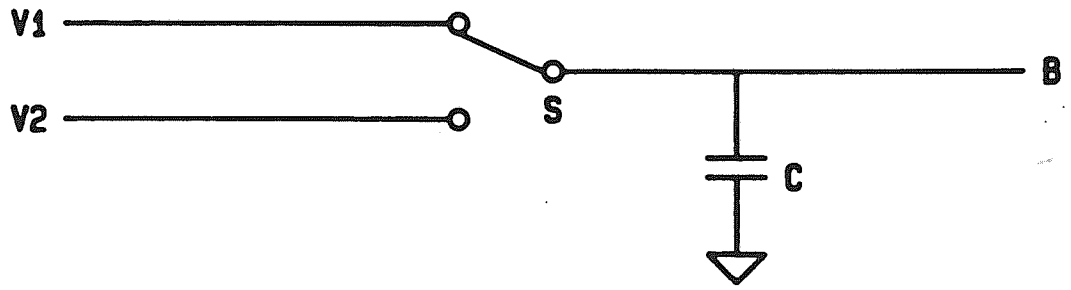


Figure 1

If we assume that the multiplexer switch S has connected output bus B to signal V1 then capacitor C will have charged to the voltage of V1. When switch S disconnects from V1 and connects to signal V2 then capacitor C must charge from the voltage of V1 to the voltage of V2. This charge must come from the source V2. The following formula will calculate this charge:

$$QB = C * (V2 - V1)$$

In a typical circuit where V2 is at 10 volts, V1 is at -10 volts, and C is 50 picofarads, then when S switches from V1 to V2, the charge QB that must be supplied by V2 is 1000 picocoulombs. Note that if V1 and V2 can each vary over the range of +10 volts to -10 volts, then the value of QB will vary from -1000 to +1000 picocoulombs. If V2 has a source with some series impedance, switch S has near zero on resistance, and there is near zero capacitance on the input lead, then when the switch closes onto V2 the voltage on V2 will instantaneously become equal to V1 then charge to the voltage of V2 as the impedance of V2 permits.

The second characteristic of the multiplexer switch to consider is whether the switch can operate in a make-before-break mode. In most designs, great care is taken to avoid operating this way. If, however, this operation should occur, then the charge transferred from one source to the other will be a function of the sum of the source impedance of the two sources, the time the switch is bridging the sources, and the difference in their voltage.

The third characteristic of the multiplexer switch is the effect of the switching mechanism. In every solid state switch, whether it is a transistor, JFET, or CMOS, the switching function requires that the control terminal move several volts. The interelectrode capacitance of the device will couple this control signal into the sources (see Figure 2).

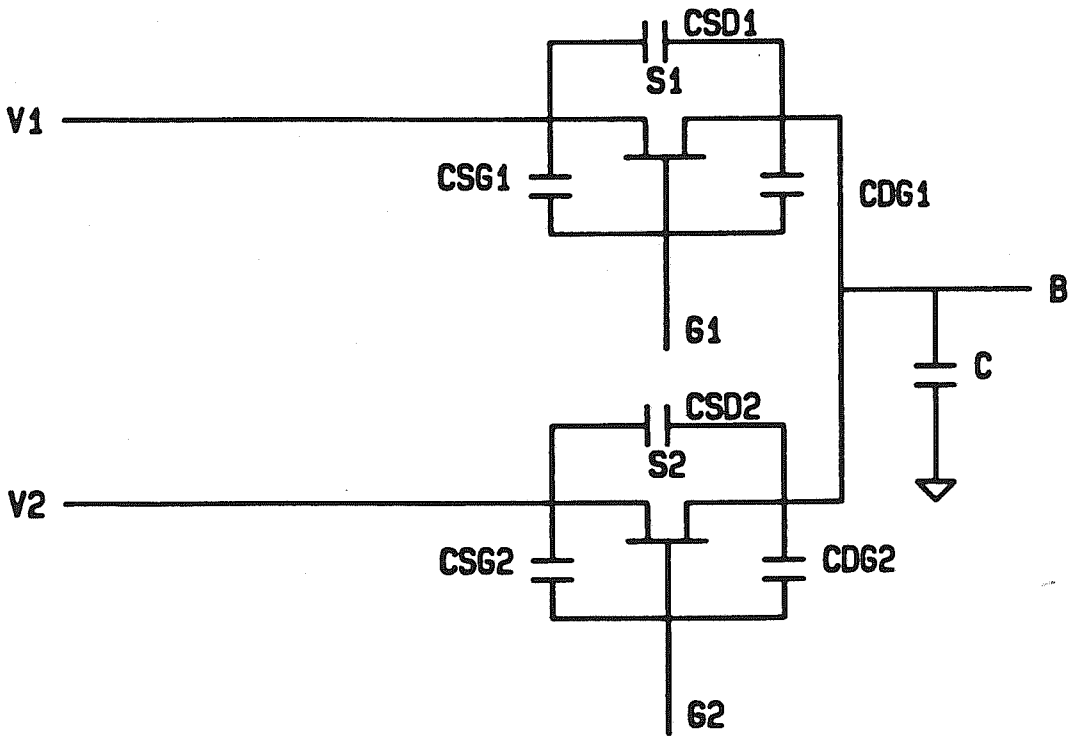


Figure 2.

When the switch S1 is turned off with a voltage step VG1 on control terminal G1, then a charge will be removed from capacitor C equal to VG1 * CDG1. When switch S2 is then turned on with a voltage step VG2 on control terminal G2, a charge will be placed on capacitor C equal to VG2 * CDG2. In some circuits these two charges will cancel and in other circuits the effective step will be equal to the voltage

difference between V1 and V2. Also when switch S2 turns on, a charge will be transferred to V2 from capacitor CSG2 equal to VG2 * CSG2. In some circuits the effective voltage step may be modified by the V2 voltage. A typical circuit may have capacitor values of 4 picofarads and a voltage step of 25 volts which would result in a charge transfer on the order of 100 picocoulombs.

DYNAMIC CHARACTERISTICS OF THE INTERCONNECTION

The interconnection between the multiplexer switch and the source must first be considered as a transmission line. Since one of the standard specifications for a multiplexer is that it must have high input impedance, the transmission line will have one end open. If the interconnection is not driven by a source having an output impedance equal to the lines characteristic impedance, the potential for resonance or ringing of the line will occur. The longer the line is, the lower the frequency of the ring will be, and the lower the losses, the longer the ringing will last - possibly well into the measurement period. The frequency of the ring can be expected to be approximately equal to 400 megahertz divided by the length of the line in feet, assuming that the line is driven by a zero ohm source.

If the interconnection is driven by a relatively high impedance source, then of particular importance is the capacity of the line. When the multiplexer switches and the previously discussed charge is transferred to the source, a portion of that charge may be stored on the capacity of the interconnection. This charge will be removed by the source through its output impedance if the capacity is low enough to have its voltage changed significantly by the multiplexer charge and the output impedance of the source is high enough to have a long recharge time constant, then the error could still be significant during the measurement period. If the capacity of the interconnection is so large that it does not change significantly due to the multiplexer charge transfer, errors can still arise if the channel is read frequently enough so that the charges can be integrated on the interconnection capacity.

DYNAMIC CHARACTERISTICS OF THE SOURCE

The most significant source of error resulting from the dynamic switching characteristics of a multiplexer can be caused by the poor transient response of an amplifier to a load on its output. Its response can be very slow, particularly if it is the active element of a filter or has its bandwidth modified by feedback elements. In some designs the source may have marginal stability which results in excessive ringing.

Amplifiers cannot be specified in a manner that will insure satisfactory operation in all multiplexing applications. he time for the source to settle from the disturbance must be compared with the allowed settling time of the multiplexer switch. The individual responsible for the system design must test the proposed sources to determine their response to dynamic loading. This test must then be evaluated based on a thorough understanding of the multiplexer timing requirements.

A relatively simple test can be performed on a source to perform an initial screening. The test consists of connecting the output of

the source through a 50 picofarad capacitor to the output of a square wave source with a fast rise 20 volt peak to peak capability. A generator with a 50 ohm output is satisfactory. A sensitive oscilloscope is used to observe the settling of the transient at the junction of the 50 picofarad capacitor and the source output. If the transient settles to an amplitude less than the allowed error, within the time allowed for the multiplexer, then the source is probably satisfactory. An additional test that could be performed at this time would be to connect a sample of the actual interconnect cable, of the actual length, between the capacitor and the source. The oscilloscope should observe the transient at the junction of the capacitor and the cable. As a test, a resistor with a resistance equal to the characteristic cable impedance can be inserted between the source and the cable.

CONCLUSION

As Analog to Digital Conversion Systems are used at higher and higher speeds and at high resolutions the effect of source characteristics on overall system performance becomes more and more important. At the highest speeds and resolutions the only acceptable solution may be to install special buffer amplifiers in series with every multiplexer switch -- a solution which may require additional rack space and additional expense.

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