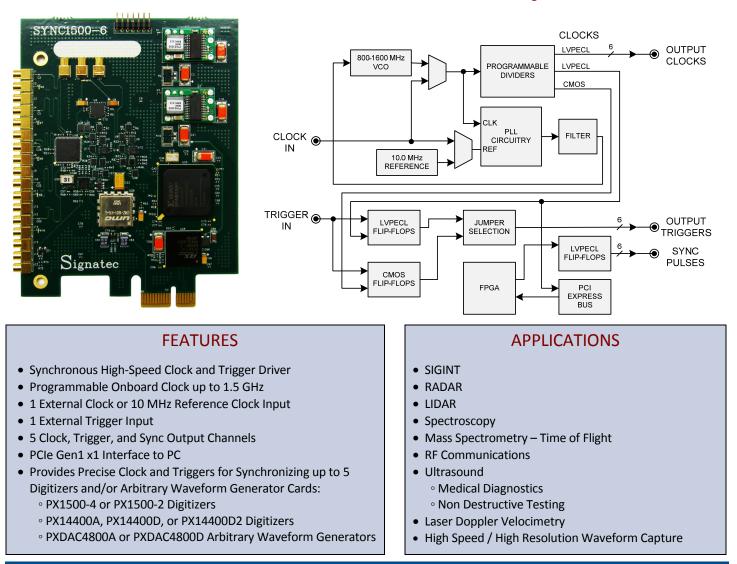


SYNC1500

Product Information Sheet **SYNC1500** Synchronized 1.5 GHz Clock/Trigger Driver

Functional Block Diagram



OVERVIEW

The SYNC1500 was created to allow for both high board (or channel) count synchronized A/D and D/A systems as well as increased system scalability. With the SYNC1500 card module, synchronized channel record or playback systems are no longer bound to single chassis configurations and can span multiple chassis, which allows for significantly greater I/O and processing resources versus a single chassis system.

The SYNC1500 provides clock and trigger distribution for up to 5 data acquisition and arbitrary waveform generator boards. When utilized in conjunction with the Signatec PX1500-4 for example, a system can be mechanized incorporating up to 20 channels of fully synchronized, very high-speed data acquisition.

The SYNC1500 board is designed for PC systems and utilizes a single lane PCI Express bus (PCIe) Gen1 interface. This PCIe Gen1 x1 interface is plug-in compatible with all PCIe lane configurations (x1, x4, x8 and x16).

An onboard frequency synthesized clock allows the output clock rate to be set to any value from 25 MHz to 1500 MHz, offering maximum flexibility for clock rate selection. The synthesized clock is locked to an onboard 10 MHz reference clock and is used in conjunction with the phase lock loop (PLL) to maintain the desired internal clock rate. An externally provided 10 MHz reference and/or an external clock input can also be selected.

SYNC1500 SPECIFICATIONS AND ORDERING INFORMATION

Input Signal Connections	
Trigger	: MMCX (miniature RF)
Clock	: MMCX
<u></u>	
Output Signal Connections	
Clocks (5)	: MMCX

Triggers (5)	: MMCX	
Svnc Pulses (5)	: MMCX	

Trigger Input Signal Type Impedance Active Edge

: Digital, TTL Level : 200 ohms

ge	: Positive

Clock Input	
Signal Type	: Analog or Digital
Coupling	: AC
Impedance	: 50 ohms
Frequency	: 10 MHz to 1500 MHz
Amplitude	: 800 mV p-p (-200/+700)

Internal Synthesized Clock

Frequency range	: 25.0 -
Resolution	: bette
Accuracy	: bette

25.0 - 1500 MHz better than 62.5 PPM better than 5 PPM

Reference Clock

Internal	: 10.0 MHz, ± 5 PPM
External	: 10.0 MHz, ± 50 PPM (required for lock)

Output Clocks	
Coupling	: AC
Required Termination	: 50 ohms
Amplitude	: 800 mV p-p (typical)

Output Triggers

Signal Type

: LVPECL (+3.3V); for use with PX1500/PXDAC4800 LVTTL (+3.3V); for use with PX14400

Required Termination : 50 ohms to +1.3V (LVPECL only)

Output Sync PulsesSignal Type: LVPECL (+3.3V)

Required Termination : 50 ohms to +1.3V

Absolute Maximum Ratings Trigger Input :-0.2V to +3.5V

Clock Input : 3V p-p Ambient Temperature : 0 to 50 °C

Part Numbers

SYNC1500-P

: LVPECL Output Triggers (for use with PX1500/PXDAC4800)

SYNC1500-T : LVTTL Output Triggers (for use with PX14400)

Cables

The SYNC1500 is supplied with the following cables:

One 4-foot length (48 inches / 1219.2 mm) 50Ω RG-316 MMCX straight male plug to BNC straight male plug cable for use in connecting an external trigger source to the SYNC1500.

Multiple 3-foot length (36 inches / 914.4 mm) 50 Ω RG-316 MMCX straight male plug to SMA straight male cables in sufficient quantity to connect each digitizer/arbitrary waveform generator unit ordered with the SYNC1500.

Documentation & Accessories

The SYNC1500 is supplied with a comprehensive operator's manual, which thoroughly describes the operation of both the hardware and the software. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to examples.

Product Warranty

All Signatec products carry a standard full 2-year warranty. During the warranty period, DynamicSignals will repair or replace any defective product at no cost to the customer. Warranties do not cover customer misuse or abuse of the products.

Notes:

Signatec is a product brand of DynamicSignals LLC, an ISO 9001:2008 Certified Company

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