Model V110-Ax11

4 to 128 Megabyte Memory

INSTRUCTION MANUAL

March, 1996

CONTENTS

TABLES

4 to 128 Megabyte Memory

A versatile read-write RAM memory

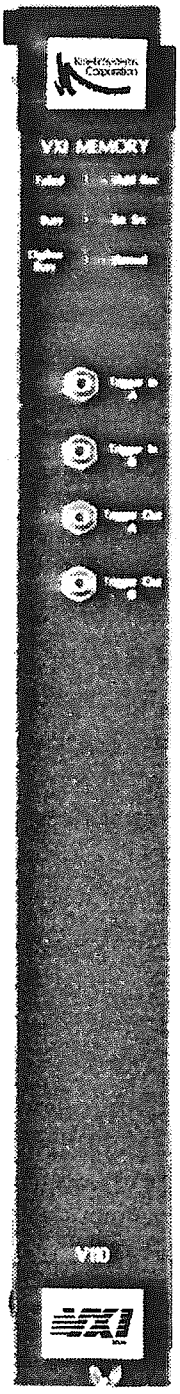
V110

Features

- **Available either as a general-purpose, read/write memory, as a data source for output modules, or as data storage for input modules**
- **Compatible with I/O modules that use the Digi-bus™ protocol**
- **Memory size options are available from 4 Mbyte to 128 Mbyte**
- **Can be used as a circular buffer for transient recorder applications with programmable pre- and post-trigger sample sizes**
- **Built-in self-test**

Typical Applications

- **Acoustic/vibration measurements**
- **Sonar (hydro-acoustics)**
- **Automotive safety testing**
- **Transient recording**
- **Local storage of data**



General Description *(Product specifications and descriptions subject to change without notice.)*

The V110 is a single-width, register-based, C-size, VXI module that can be used as a general-purpose, read/write memory on VXIbus or can interface with the family of I/O modules from KineticSystems that uses the Digi-bus™ protocol. Options of the V110 are available which provide a memory-based data source for output modules such as the V285 Arbitrary Waveform Generator or the V387 Discrete I/O modules (with output options installed); data storage for input modules such as the V207 ADC Subsystem with its family of signal conditioning modules; or VXIbus only operation (no Digi-bus interface). The physical path for the Digi-bus communications is the VXI Local Bus on the backplane P2 connector. Data can be read or written over Digi-bus from the V110 at a peak rate of 10 Mbyte/s. The actual average transfer rate may be limited by the associated I/O modules and their clock rate settings.

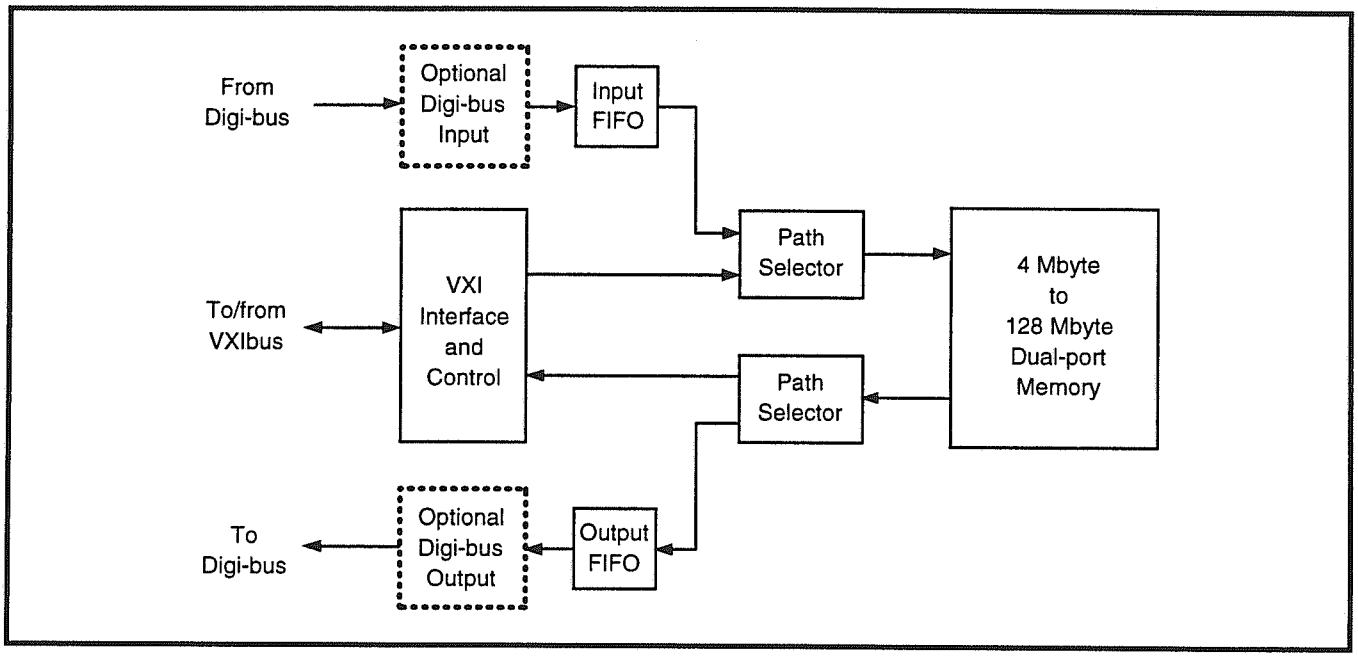
The memory on the V110 VXIbus memory module is dual-ported:

- When a Digi-bus OUT module option is used, one buffer on the V110 can be written from VXIbus while a second buffer is supplying data over Digi-bus to a V285 Arbitrary Waveform Generator, for example. When that second buffer is empty, the module begins reading data from the first buffer, allowing the second buffer to be filled from VXIbus.
- When a Digi-bus IN module option is used, one buffer on the V110 can be read from VXIbus while a second buffer is receiving data over Digi-bus from a V207 ADC Subsystem, for example. When that second buffer is full, Digi-bus begins writing data to the first buffer, allowing the second buffer to be read from VXIbus.
- With all options of the V110, it can be used as a general-purpose, read/write memory via VXIbus.

The Digi-bus input option of the V110 can also be used as a transient data recorder memory. When this feature is programmed, the memory is configured as a circular buffer. The logical size of the memory can be programmed to be the entire physical memory or a portion of it. In operation, data from an ADC module begins to be stored in the V110 prior to an "event." The logical memory size can be divided into pre-trigger and post-trigger samples. When an event trigger is received, the memory will continue recording until all post-trigger samples have been received.

The V110 supports both static and dynamic configuration capabilities. It may be accessed using A32/A16, D32/D16 data transfers. A built-in self-test is provided which performs a full memory test at power up.

Memory Data Paths



Item	Specification
Power Requirements	
+5 V	6.9 A, maximum
Environmental and Mechanical	
Temperature range	
Operational	0°C to 50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing, to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V110-wx11

w: Digi-bus options

A = no Digi-bus option
B = Digi-bus input (The V110 can read data from Digi-bus)
C = Digi-bus output (The V110 can write data to Digi-bus)

x: Memory size

A = 4 Mbyte memory
B = 8 Mbyte memory
C = 16 Mbyte memory
D = 32 Mbyte memory
E = 64 Mbyte memory
F = 128 Mbyte memory

Related Products

Model V165	Digital Signal Processor
Model V207	16-bit, 500,000 Sample/second ADC Subsystem
Model V208	16-bit, 200,000 Sample/second ADC Subsystem
Model V285	8 or 16-channel, 16-bit, 500 kHz DAC/Waveform Generator
Model V387	128-channel Discrete Input/Output
Model 5919-Z1A	Connector—SMB Cable-type

VXI CONFIGURATION REGISTER DESCRIPTIONS

VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, the V110 implements those required for extended register-based devices. The V110 also contains a set of operational registers to monitor and control operational aspects of the device.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V110 are offset from the base address. **Note: the V110 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the VMEbus cycle.** Table 1 shows the applicable Configuration Registers present in the V110, their offset from the base (Logical) address, and their Read/Write capabilities.

Table 1. Configuration Registers Configuration (A16) Space

A16 Offset	Write/Read	Register Name
00_{16}	Write/Read	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Write/Read	Status/Control Register
06_{16}	Write/Read	Offset Register
08_{16}	Read Only	Attribute Register
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved Registers
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Write/Read	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	N/A	Reserved

ID/Logical Address Register

The ID/Logical Address Register, which is located at offset 0 from the logical base address, serves two functions, depending on the direction of the VME transfer. When executing a read operation to this register, the data returned indicates the Device Class, the Address Space requirements outside of A16 space, and the Manufacturer's Identification. A write operation to this register is only executed during a dynamic configuration sequence. During the configuration sequence, the Resource Manager assigns a logical address to the V110 by writing the logical address into the lower 8-bits of this register. The format and bit assignments for this ID/Logical Address register are shown in the following diagram. Since this register has write-only and read-only bits, two bit patterns are shown.

On Read transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1

Bit(s)	Mnemonic	Meaning
15,14	Device Class	These bits determine the Device Class of a VXI device. These bits are set by the V110 to indicate an Extended Register Based device
13,12	Address Space	These two bits reflect the address requirements for operational registers of a VXI device. These bits are set by the V110 to indicate use of A32 address space.
11-0	Manufacturer's ID	These twelve bits are used to indicate the manufacturer of a VXI device. The Manufacturer Identification for KineticSystems is 3881 ($F29_{16}$).

On Write transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Not Used								LA 128	LA 64	LA 32	LA 16	LA 08	LA 04	LA 02	LA 01

For Write transfers to offset 0 of the V110, bits 15 through 08 are not used. A write to these bits has no effect on the V110. In Dynamically Configured Systems (i.e., the Logical Address switches were set to a value of 255), bits 07 through 00 are written with the new Logical Address value. This write operation is typically executed by a Resource Manager.

Model V110-Ax11

Device Type Register

The Device Type Register is a read-only register located at an offset of 2 from the logical base address. This register contains the Model Code of the V110 as well as the required A32 address space for the operational registers. The resource manager uses this field to allocate physical addresses for the V110 operational registers.

The following diagram shows the bit pattern of the Device Type Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RM 3	RM 2	RM 1	RM 0	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-12	Required Memory	These bits reflect the amount of A32 address space required by the V110. This field varies depending on the option of the V110. The following chart shows various required memory combinations based on the V110 option.

V110 Option	DRAM Size	A32 Addressing Requirement	Memory Requirement Field
V110-AA11	4 Megabyte	8 Megabyte	1000
V110-AB11	8 Megabyte	16 Megabyte	0111
V110-AC11	16 Megabyte	32 Megabyte	0110
V110-AD11	32 Megabyte	64 Megabyte	0100
V110-AE11	64 Megabyte	128 Megabyte	0011
V110-AF11	128 Megabyte	256 Megabyte	0010

11-6	Model Code	These twelve bits reflect the Model Code of a VXI device. This field is set to 272 (110_{16}) by the V110.

Status/Control Register

The Status/Control Register, which is located at an offset of 4 from the logical base address, contains write-only, read-only, and write/read bits. The following describes the bits for write and read operations.

This bit pattern shows the register layout for read accesses to the Status/Control Register.

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A32 Act	MODID*	1	1	1	1	1	1	1	1	1	1	Ready	Pass	SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15	A32 Active	This bit is read as a one when the V110 is enabled for access in A32 space.
14	MODID*	This bit is set to a one if the module is not selected with the MODID line on the VXI P2 connector. A zero indicates that the device is selected by a high state on the P2 MODID line.
13-4	Not Used	These bits are not used and read as ones.
3	Ready	READY is a read-only bit which is set to a one indicating successful completion of register initialization.
2	Pass	Pass is a read-only bit that is set to a one after the V110 has completed its power-on self-test without any errors. If errors occur, this bit is set to a zero and the SYSFAIL signal is asserted by the V110.
1	SYS INB	Reading this bit as a one indicates that the V110 is disabled from driving the SYSFAIL* line.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

This bit pattern shows the register layout for write accesses to the Status/Control Register.

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15-2	Not Used	These bits are not used for write operations.

1	SYS INB	SYSFAIL INHIBIT is a write-only bit that is set to a one to inhibit the V110 from asserting the VXI SYSFAIL* signal.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

Offset Register

The Offset register, which is located at offset 6 from the logical base address, is used for specifying the base address of the V110 operational registers in A32 space. Since different options of the V110 require varying amounts of A32 address space, the number of address bits in the Offset Register is based on the V110 DRAM size. The V110 can occupy from 8 Megabytes to 256 Megabytes of address space. This register is a 16-bit write/read register with the following bit assignments:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A31	A30	A29	A28	A27	A26	A25	A24	A23	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-07	A31 - A23	These write/read bits are used for defining the base address of the V110 Operational Registers. The number of address bits used depends on the V110 option. The following chart shows the number of address bits used based on the V110 option.

V110 Option	DRAM Size	A32 Addressing Requirement	Offset Address Bits Used
V110-AA11	4 Megabyte	8 Megabyte	A31 through A23
V110-AB11	8 Megabyte	16 Megabyte	A31 through A24
V110-AC11	16 Megabyte	32 Megabyte	A31 through A25
V110-AD11	32 Megabyte	64 Megabyte	A31 through A26
V110-AE11	64 Megabyte	128 Megabyte	A31 through A27
V110-AF11	128 Megabyte	256 Megabyte	A31 through A28

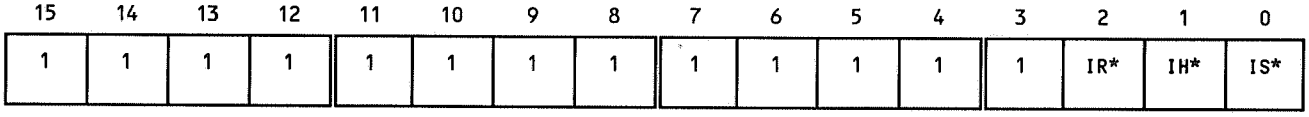
06-00	Not Used	These bits are not used but should be written as zeros.

After SYSRESET*, and prior to self-test, all bits are set to zero. Writing to this register is executed by the Resource Manager during the configuration process. The user may then examine this register to determine the base address of the V110 Operational Registers. The physical address in A32 address space can be calculated by reading this register and shifting the data 16 places to the left. The resultant data is the base address of the Operational Registers of the V110. After this register is written with the desired base address, the A32 ENABLE bit in the Status/Control register must be set to a one before the V110 Operational Registers may be accessed.

Attribute Register

The Attribute Register is located at an offset of 8 from the logical base address. This register defines the interrupting capability of the V110. The V110 is an interrupter with interrupt status functionality, but does not implement an interrupt handler.

The format of the Attribute Register is shown in the following diagram:

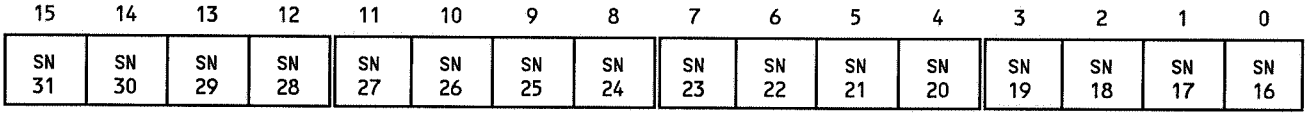


Bit(s)	Mnemonic	Meaning
15-3	Not Used	These bits are not used and read as ones.
2	IR*	The V110 has interrupter control capabilities and returns this bit set to zero.
1	IH*	The V110 does not have interrupt handling capabilities and returns this bit set to one.
0	IS*	The V110 has interrupt status capabilities and returns this bit set to zero.

Serial Number High Register

The Serial Number High Register, which is located at an offset of $0A_{16}$ from the logical base address, is used in combination with the Serial Number Low Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number High Register is shown in the following diagram:



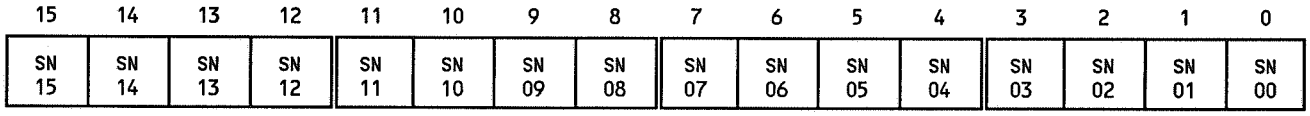
Bit(s)	Mnemonic	Meaning
15-0	SN31-16	SERIAL NUMBER 31 through 16 are read-only bits which represent the upper 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN15-SN00 in the Serial Number Low register.

Serial Number Low Register

The Serial Number Low Register, which is located at an offset of $0C_{16}$ from the logical base address, is used in combination with the Serial Number High Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

Model V110-Ax11

The format of the Serial Number Low Register is shown in the following diagram:

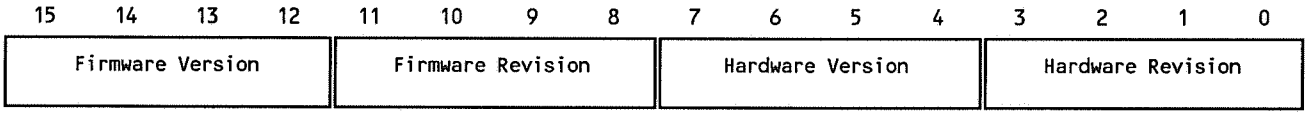


Bit(s)	Mnemonic	Meaning
15-0	SN15-0	SERIAL NUMBER 15 through 0 are read-only bits which represent the lower 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN31-SN16 in the Serial Number High register.

Version Number Register

The Version Number Register, which is located at an offset of $0E_{16}$ from the logical base address, is a read-only register that reflects the current revision level of the hardware and firmware residing on the V110. All write operations to this register are ignored.

The following shows the bit layout of the Version Number Register.



Bit(s)	Mnemonic	Meaning
15-12	Firmware Version	These bits reflect the module's firmware main version level.
11-8	Firmware Revision	These bits reflect the module's firmware revision number.
7-4	Hardware Version	These bits reflect the module's firmware main version number.
3-0	Hardware Revision	These bits reflect the module's firmware revision number.

Interrupt Status Register

The Interrupt Status Register is a 16-bit read-only register located at an offset of $1A_{16}$ from the logical base address. The contents of this register are enabled onto the VMEbus during interrupt acknowledge cycles. The register contains the logical address of the V110 in the lower 8-bits of the register and the upper 8-bits indicate the cause/status of the interrupt. The lower 8-bits of this register return the Logical Address of the V110 only for interrupt acknowledge cycles. An I/O read of this register returns the lower 8-bits set to ones. The V110 has only one source for generating an interrupt. The interrupt source is generated by the on-board DSP when it requires service. The DSP Request Interrupt Source is generated when the DSP writes to the DSP Communication I/O Register.

The interrupt acknowledge cycle executed on the VME bus reads a 16-bit value from the V110. The lower 8-bits of this data reflect the Logical Address of the V110. The upper 8-bits of the data field indicates the cause of the interrupt within the V110. Of the 8 bit locations, only one of them is used.

Once an interrupt acknowledge cycle occurs, the interrupt source bit that was set when the interrupt vector was read is reset to zero. This bit is also cleared when the Interrupt Status Register is read by programmed I/O.

The format of the Interrupt Status Register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DSP REQ	0	0	0	0	0	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1
Interrupt Cause/Status								Device Logical Address							

Bit(s)	Mnemonic	Meaning
15-14	Not Used.	These bits are not used and read as zeros.
13	DSP REQ	DSP REQUEST is a read-and-clear bit that is set when the DSP writes to the DSP Communication I/O Register.
12-8	Not Used	These bits are not used and read as zeros.
7-0	LA128-LA1	These bits return the current logical address of the V110 during interrupt acknowledge cycles. An I/O read of these bits returns all ones.

Interrupt Control Register

The Interrupt Control Register, which is located at offset $1C_{16}$ from the logical base address, is a write/read register used to configure the V110 for interrupt generation. The Interrupt Request Level and Interrupt Enable bit are located in this register.

The format and description of the bits in the Interrupt Control Register are shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	DSP REQ	1	1	1	1	1	IREN*	1	IRQ S3	IRQ S2	IRQ S1	1	1	1

Bit(s)	Mnemonic	Meaning
15-14	Not Used	These bits are not used and read as ones.
13	DSPREQ*	DSP REQUEST is a write/read bit used to enable/disable the V110 from generating an interrupt when the DSP requires service. The interrupt is enabled by setting this bit to a zero and disabled with a one.

12-8	Not Used	These bits are not used and read as ones.
7	IREN*	INTERRUPT REQUEST ENABLE is a write/read bit used to enable/disable the generation of an interrupt by the V110. Setting this bit to a zero enables the V110 to interrupt and a one disables all interrupts.
6	Not Used	This bit is not used and read as a one.
5-3	IRQS3-IRQS1	INTERRUPT REQUEST SELECT 3 through 1 are write/read bits used to select the desired Interrupt Request Level that the V110 asserts when an interrupt is sourced. The following shows the Interrupt Request Level selections.

IRQS3	IRQS2	IRQS1	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

2-0 Not Used — These bits are not used and read as ones.

Subclass Register

The Subclass Register, which is located at an offset of $1E_{16}$ from the logical base address, is a read-only register that indicates the subclass of the V110. The V110 is an Extended Register Based Device as the following pattern indicates.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Meaning
15	This bit is set to a one indicating that this is a VXIbus extended device.
14-0	These bits are set of $7FFE_{16}$ which indicates that the V110 is an Extended Register Based Device.

Model V110-Ax11

Suffix High Register

The Suffix High register, which is located at an offset of 20_{16} from the logical base address, is a read-only register used in combination with the Suffix Low Register to determine the module model number suffix. The Suffix High Register contains the first two ASCII characters of the suffix and the Suffix Low Register contains the second two characters. The suffix shown is for the V110-BA11 module.

The format and bit assignments for the Suffix High Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1

This read only register contains the first two ACSII characters of the module's suffix ("AA"=4141_{16}). The following chart shows the values returned for the various V110 options.

V110 Option	ASCII Suffix Data	Suffix High Data
V110-AA11	"AA"	4141_{16}
V110-AB11	"AB"	4142_{16}
V110-AC11	"AC"	4143_{16}
V110-AD11	"AD"	4144_{16}
V110-AE11	"AE"	4145_{16}
V110-AF11	"AF"	4146_{16}

Suffix Low Register

The Suffix Low register, which is located at an offset of 22_{16} from the logical base address, is a read-only register used in combination with the Suffix High Register to determine the module model number suffix. The Suffix Low Register contains the last two ASCII characters of the suffix and the Suffix High Register contains the first two characters.

The format and bit assignments for the Suffix Low Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1

This read only register contains the last two ACSII characters of the module's suffix ("11" = 4141_{16}).

V110 Register Operational Register Layout

Address Offset	Register	Mnemonic
0_{16}	Control/Status Register	CSR
4_{16} - 20_{16}	Reserved	
24_{16}	DSP Communication I/O	DSP

After the Operational Registers in A32 address space is the DRAM Memory. The following chart shows the address range of the RAM address as an offset from the A32 base address.

0400000 - 07FFFFF	DRAM Range for 4 Megabyte Option
0800000 - 0FFFFFF	DRAM Range for 8 Megabyte Option
1000000 - 1FFFFFF	DRAM Range for 16 Megabyte Option
2000000 - 3FFFFFF	DRAM Range for 32 Megabyte Option
4000000 - 7FFFFFF	DRAM Range for 64 Megabyte Option
8000000 - FFFFFFF	DRAM Range for 128 Megabyte Option

All of these registers and the DRAM may be accessed as longwords (32-bits) or shortwords (16-bits). When accessing a register using shortwords, the upper 16-bits of a register is accessed with VME address bit A1 is equal to 0. The lower 16-bits of a 32-bit register is accessed when VME address bit A1 is equal to 1. For example, to access the upper 16-bits of the Buffer Total Frame Count Register an offset of 08_{16} is used. To access the lower 16-bits of this registers an offset of $0A_{16}$ is used.

Control/Status Register

The Control/Status Register (CSR) is a write/read register located at an offset of 0 from the base of the Operational Registers. This register is used to assist in communicating tothe DSP.

The following diagram shows the bit pattern for the Control/Status Register.

Offset: 00_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 02_{16}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	DSP REQ	0	0	0	0	0	0

<31:7> These bits are not used and read as zeros.

<6> DSP REQUEST is a read-only bit that is set when the DSP writes to the DSP Communication Register. When this bit is set, it indicates to the host that the DSP has information available in the I/O register. The bit is cleared after the host reads the DSP Communication Register.

<5:0> These bits are not used and read as zeros.

DSP Communication I/O Register

The DSP Communication I/O Register is a write/read register located at an offset of 24 hex from the base of the operational registers. This 16-bit register provides a bidirectional communication path to the on-board DSP. The data passed to/from the DSP depends on the how the DSP is to interact with the DRAM buffer data. The use of this register is currently reserved but is shown here for completeness.

The following diagram shows the bit layout for the DSP Communication I/O Register:

Offset: 24_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 26_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSP 15	DSP 14	DSP 13	DSP 12	DSP 11	DSP 10	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0

<31:16> These bits are not used and read as zeros.

<15:0> DSP15 through 0 are general purpose bits used to establish a bidirectional communication path to the DSP.

Front Panel LEDs and Connectors

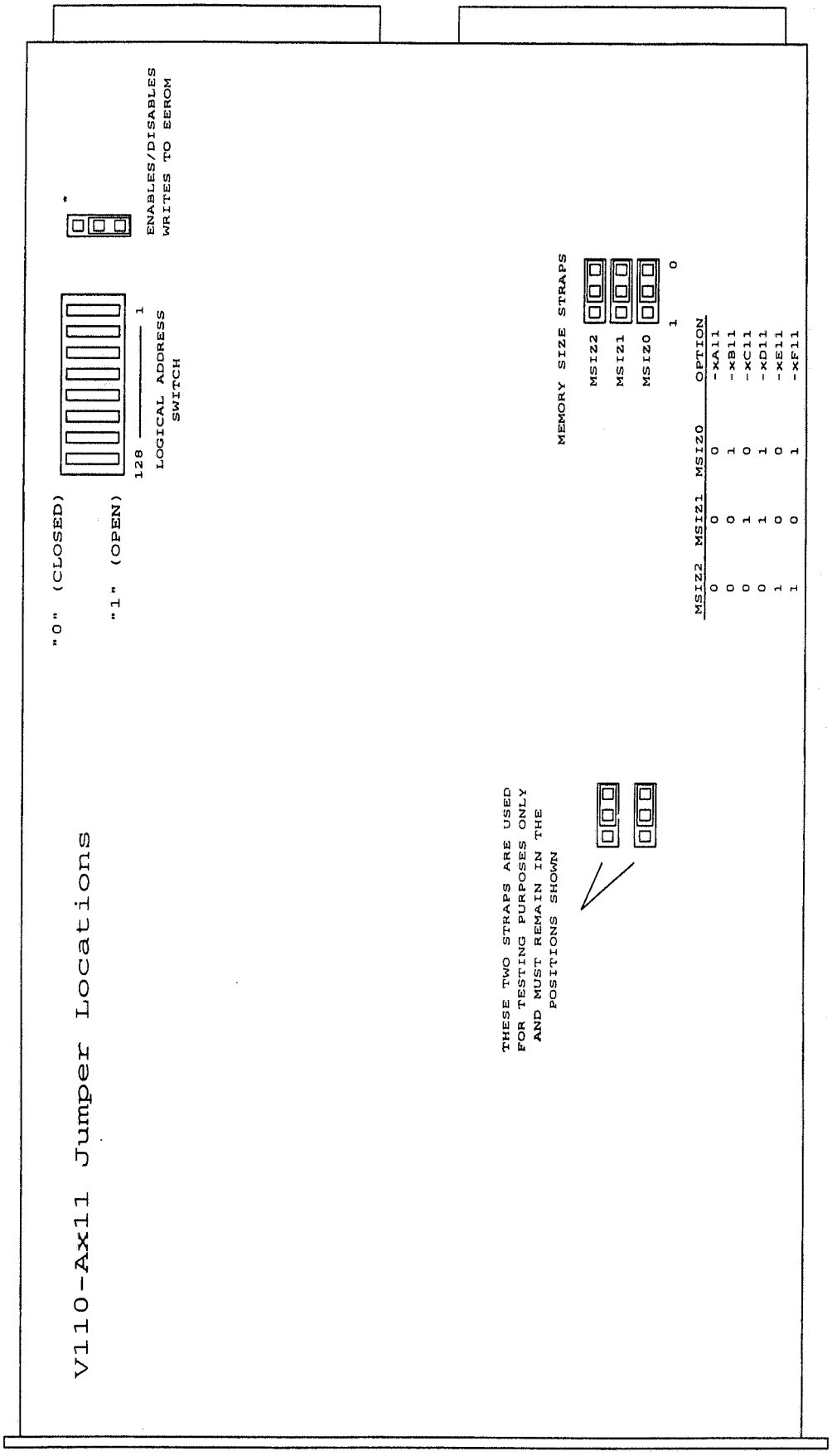
The front-panel of the V110 contains 3 LEDs that reflect various status signals of the V110.

The SYSFAIL LED is illuminated while the V110 is executing its power-on self-test and will remain illuminated if the power-on self-test fails. While this LED is on, the V110 is asserting the VMEbus signal SYSFAIL (as long as the SYSFAIL INHIBIT bit in the Status/Control Register is configuration space is false). If this LED is on for more than 5 seconds, the V110 has failed the self-test and must be returned for repair.

The ADDRESS RECEIVED LED is a one-shot extended LED that is illuminated when the V110 is addressed in either A16 and A32 address space.

The INTERRUPT SOURCE LED is illuminated as long as the V110 has an interrupt request pending.

V110-Ax11 Jumper Locations



WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

The product warranty may vary outside the United States and does not include shipping, customs clearance, or any other charges. Consult your local authorized representative or reseller for more information regarding specific warranty coverage and shipping details.

PRODUCT SPECIFICATIONS AND DESCRIPTIONS IN THIS DOCUMENT SUBJECT TO CHANGE WITHOUT NOTICE.

KINETICSYSTEMS SPECIFICALLY MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR ANY OTHER WARRANTY EITHER EXPRESSED OR IMPLIED, EXCEPT AS IS EXPRESSLY SET FORTH HEREIN. PRODUCT FAILURES CREATED BY UNAUTHORIZED MODIFICATIONS, PRODUCT MISUSE, OR IMPROPER INSTALLATION ARE NOT COVERED BY THIS WARRANTY.

THE WARRANTIES PROVIIDED HEREIN ARE THE PURCHASER'S SOLE AND EXCLUSIVE REMEDIES ON ANY CLAIM OF ANY KIND FOR ANY LOSS OR DAMAGE ARISING OUT OF, CONNECTED WITH, OR RESULTING FROM THE USE, PERFORMANCE OR BREACH THEREOF, OR FROM THE DESIGN, MANUFACTURE, SALE, DELIVERY, RESALE, OR REPAIR OR USE OF ANY PRODUCTS COVERED OR FURNISHED BY KINETICSYSTEMS INCLUDING BUT NOT LIMITED TO ANY CLAIM OF NEGLIGENCE OR OTHER TORTIOUS BREACH, SHALL BE THE REPAIR OR REPLACEMENT, FOB FACTORY, AS KINETICSYSTEMS MAY ELECT, OF THE PRODUCT OR PART THEREOF GIVING RISE TO SUCH CLAIM, EXCEPT THAT KINETICSYSTEMS' LIABILITY FOR SUCH REPAIR OR REPLACEMENT SHALL IN NO EVENT EXCEED THE CONTRACT PRICE ALLOCABLE TO THE PRODUCTS OR PART THEROF WHICH GIVES RISE TO THE CLAIM. IN NO EVENT SHALL KINETICSYSTEMS BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, INCLUDING LOSS OF PROFITS.

Products will not be accepted for credit or exchange without the prior written approval of KineticSystems. If it is necessary to return a product for repair, replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center prior to shipping the product to KineticSystems. The following steps should be taken before returning any product:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com