Model V110-Bx11

4 to 128 Megabyte Memory

INSTRUCTION MANUAL

January, 1998

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4 to 128 Megabyte Memory

A versatile read-write RAM memory

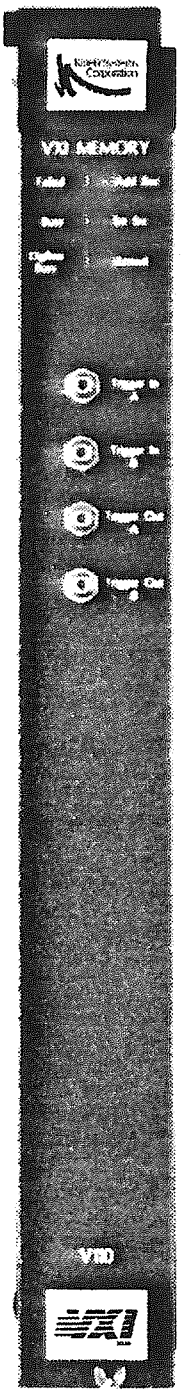
V110

Features

- **Available either as a general-purpose, read/write memory, as a data source for output modules, or as data storage for input modules**
- **Compatible with I/O modules that use the Digi-bus™ protocol**
- **Memory size options are available from 4 Mbyte to 128 Mbyte**
- **Can be used as a circular buffer for transient recorder applications with programmable pre- and post-trigger sample sizes**
- **Built-in self-test**

Typical Applications

- **Acoustic/vibration measurements**
- **Sonar (hydro-acoustics)**
- **Automotive safety testing**
- **Transient recording**
- **Local storage of data**



General Description *(Product specifications and descriptions subject to change without notice.)*

The V110 is a single-width, register-based, C-size, VXI module that can be used as a general-purpose, read/write memory on VXIbus or can interface with the family of I/O modules from KineticSystems that uses the Digi-bus™ protocol. Options of the V110 are available which provide a memory-based data source for output modules such as the V285 Arbitrary Waveform Generator or the V387 Discrete I/O modules (with output options installed); data storage for input modules such as the V207 ADC Subsystem with its family of signal conditioning modules; or VXIbus only operation (no Digi-bus interface). The physical path for the Digi-bus communications is the VXI Local Bus on the backplane P2 connector. Data can be read or written over Digi-bus from the V110 at a peak rate of 10 Mbyte/s. The actual average transfer rate may be limited by the associated I/O modules and their clock rate settings.

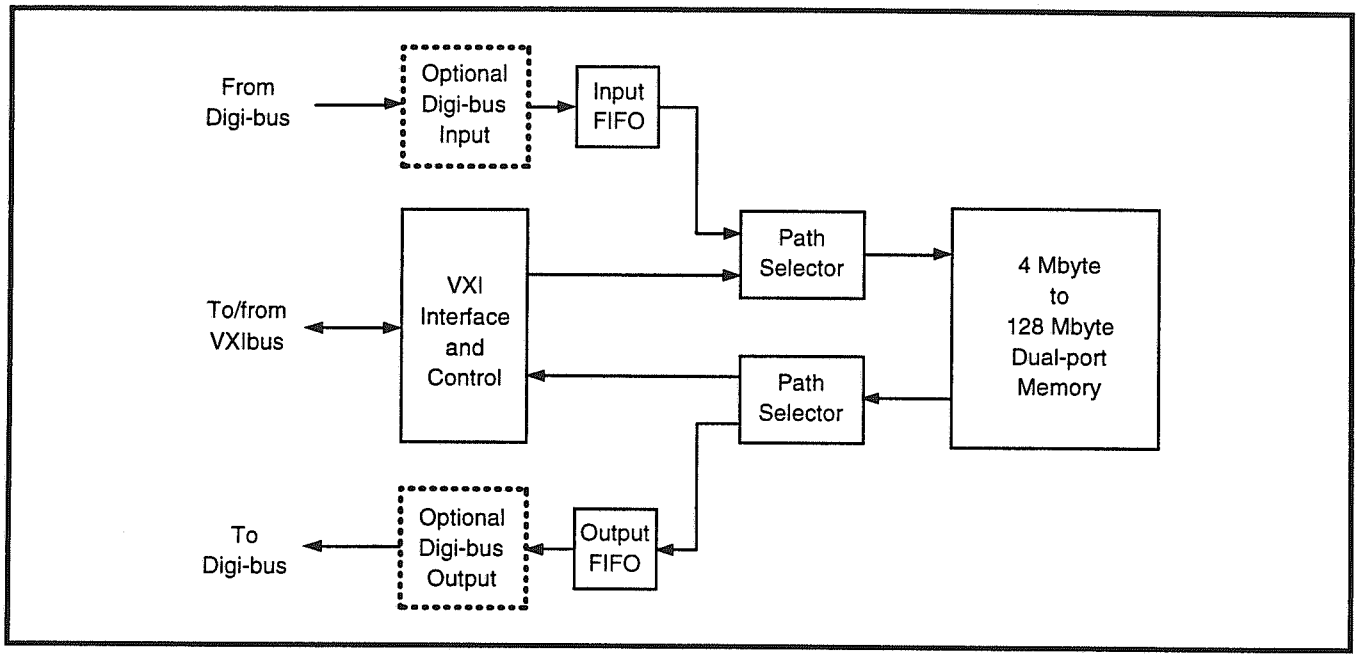
The memory on the V110 VXIbus memory module is dual-ported:

- When a Digi-bus OUT module option is used, one buffer on the V110 can be written from VXIbus while a second buffer is supplying data over Digi-bus to a V285 Arbitrary Waveform Generator, for example. When that second buffer is empty, the module begins reading data from the first buffer, allowing the second buffer to be filled from VXIbus.
- When a Digi-bus IN module option is used, one buffer on the V110 can be read from VXIbus while a second buffer is receiving data over Digi-bus from a V207 ADC Subsystem, for example. When that second buffer is full, Digi-bus begins writing data to the first buffer, allowing the second buffer to be read from VXIbus.
- With all options of the V110, it can be used as a general-purpose, read/write memory via VXIbus.

The Digi-bus input option of the V110 can also be used as a transient data recorder memory. When this feature is programmed, the memory is configured as a circular buffer. The logical size of the memory can be programmed to be the entire physical memory or a portion of it. In operation, data from an ADC module begins to be stored in the V110 prior to an "event." The logical memory size can be divided into pre-trigger and post-trigger samples. When an event trigger is received, the memory will continue recording until all post-trigger samples have been received.

The V110 supports both static and dynamic configuration capabilities. It may be accessed using A32/A16, D32/D16 data transfers. A built-in self-test is provided which performs a full memory test at power up.

Memory Data Paths



Item	Specification
Power Requirements	
+5 V	6.9 A, maximum
Environmental and Mechanical	
Temperature range	
Operational	0°C to 50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing, to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V110-wx11

w: Digi-bus options

A = no Digi-bus option
B = Digi-bus input (The V110 can read data from Digi-bus)
C = Digi-bus output (The V110 can write data to Digi-bus)

x: Memory size

A = 4 Mbyte memory
B = 8 Mbyte memory
C = 16 Mbyte memory
D = 32 Mbyte memory
E = 64 Mbyte memory
F = 128 Mbyte memory

Related Products

Model V165	Digital Signal Processor
Model V207	16-bit, 500,000 Sample/second ADC Subsystem
Model V208	16-bit, 200,000 Sample/second ADC Subsystem
Model V285	8 or 16-channel, 16-bit, 500 kHz DAC/Waveform Generator
Model V387	128-channel Discrete Input/Output
Model 5919-Z1A	Connector—SMB Cable-type

VXI Configuration Register Descriptions

VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, the V110 implements those required for extended register-based devices. The V110 also contains a set of operational registers to monitor and control operational aspects of the device.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V110 are offset from the base address. **Note: the V110 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the VMEbus cycle.** Table 1 shows the applicable Configuration Registers present in the V110, their offset from the base (Logical) address, and their Read/Write capabilities.

Table 1. Configuration Registers Configuration (A16) Space

A16 Offset	Write/Read	Register Name
00_{16}	Write/Read	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Write/Read	Status/Control Register
06_{16}	Write/Read	Offset Register
08_{16}	Read Only	Attribute Register
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved Registers
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Write/Read	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	N/A	Reserved

ID/Logical Address Register

The ID/Logical Address Register, which is located at offset 0 from the logical base address, serves two functions, depending on the direction of the VME transfer. When executing a read operation to this register, the data returned indicates the Device Class, the Address Space requirements outside of A16 space, and the Manufacturer's Identification. A write operation to this register is only executed during a dynamic configuration sequence. During the configuration sequence, the Resource Manager assigns a logical address to the V110 by writing the logical address into the lower 8-bits of this register. The format and bit assignments for this ID/Logical Address register are shown in the following diagram. Since this register has write-only and read-only bits, two bit patterns are shown.

On Read transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1

Bit(s)	Mnemonic	Meaning
15,14	Device Class	These bits determine the Device Class of a VXI device. These bits are set by the V110 to indicate an Extended Register Based device
13,12	Address Space	These two bits reflect the address requirements for operational registers of a VXI device. These bits are set by the V110 to indicate use of A32 address space.
11-0	Manufacturer's ID	These twelve bits are used to indicate the manufacturer of a VXI device. The Manufacturer Identification for KineticSystems is 3881 ($F29_{16}$).

On Write transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Not Used								LA 128	LA 64	LA 32	LA 16	LA 08	LA 04	LA 02	LA 01

For Write transfers to offset 0 of the V110, bits 15 through 08 are not used. A write to these bits has no effect on the V110. In Dynamically Configured Systems (i.e., the Logical Address switches were set to a value of 255), bits 07 through 00 are written with the new Logical Address value. This write operation is typically executed by a Resource Manager.

Device Type Register

The Device Type Register is a read-only register located at an offset of 2 from the logical base address. This register contains the Model Code of the V110 as well as the required A32 address space for the operational registers. The resource manager uses this field to allocate physical addresses for the V110 operational registers.

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The following diagram shows the bit pattern of the Device Type Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RM 3	RM 2	RM 1	RM 0	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-12	Required Memory	These bits reflect the amount of A32 address space required by the V110. This field varies depending on the option of the V110. The following chart shows various required memory combinations based on the V110 option.

V110 Option	DRAM Size	A32 Addressing Requirement	Memory Requirement Field
V110-BA11	4 Megabyte	8 Megabyte	1000
V110-BB11	8 Megabyte	16 Megabyte	0111
V110-BC11	16 Megabyte	32 Megabyte	0110
V110-BD11	32 Megabyte	64 Megabyte	0101
V110-BE11	64 Megabyte	128 Megabyte	0100
V110-BF11	128 Megabyte	256 Megabyte	0011

11-6	Model Code	These twelve bits reflect the Model Code of a VXI device. This field is set to 272 (110_{16}) by the V110.

Status/Control Register

The Status/Control Register, which is located at an offset of 4 from the logical base address, contains write-only, read-only, and write/read bits. The following describes the bits for write and read operations.

This bit pattern shows the register layout for read accesses to the Status/Control Register.

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A32 Act	MODID*	1	1	1	1	1	1	1	1	1	1	Ready	Pass	SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15	A32 Active	This bit is read as a one when the V110 is enabled for access in A32 space.
14	MODID*	This bit is set to a one if the module is <u>not</u> selected with the MODID line on the VXI P2 connector. A zero indicates that the device is selected by a high state on the P2 MODID line.

13-4	Not Used	These bits are not used and read as ones.
3	Ready	READY is a read-only bit which is set to a one indicating successful completion of register initialization.
2	Pass	Pass is a read-only bit that is set to a one after the V110 has completed its power-on self-test without any errors. If errors occur, this bit is set to a zero and the SYSFAIL signal is asserted by the V110.
1	SYS INB	Reading this bit as a one indicates that the V110 is disabled from driving the SYSFAIL* line.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

This bit pattern shows the register layout for write accesses to the Status/Control Register.

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15-2	Not Used	These bits are not used for write operations.
1	SYS INB	SYSFAIL INHIBIT is a write-only bit that is set to a one to inhibit the V110 from asserting the VXI SYSFAIL* signal.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

Offset Register

The Offset register, which is located at offset 6 from the logical base address, is used for specifying the base address of the V110 operational registers in A32 space. Since different options of the V110 require varying amounts of A32 address space, the number of address bits in the Offset Register is based on the V110 DRAM size. The V110 can occupy from 8 Megabytes to 256 Megabytes of address space. This register is a 16-bit write/read register with the following bit assignments:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A31	A30	A29	A28	A27	A26	A25	A24	A23	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-07	A31 - A23	These write/read bits are used for defining the base address of the V110 Operational Registers. The number of address bits used depends on the V110 option. The following chart shows the number of address bits used based on the V110 option.

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V110 Option	DRAM Size	A32 Addressing Requirement	Offset Address Bits Used
V110-BA11	4 Megabyte	8 Megabyte	A31 through A23
V110-BB11	8 Megabyte	16 Megabyte	A31 through A24
V110-BC11	16 Megabyte	32 Megabyte	A31 through A25
V110-BD11	32 Megabyte	64 Megabyte	A31 through A26
V110-BE11	64 Megabyte	128 Megabyte	A31 through A27
V110-BF11	128 Megabyte	256 Megabyte	A31 through A28

06-00 Not Used These bits are not used but should be written as zeros.

After SYSRESET*, and prior to self-test, all bits are set to zero. Writing to this register is executed by the Resource Manager during the configuration process. The user may then examine this register to determine the base address of the V110 Operational Registers. The physical address in A32 address space can be calculated by reading this register and shifting the data 16 places to the left. The resultant data is the base address of the Operational Registers of the V110. After this register is written with the desired base address, the A32 ENABLE bit in the Status/Control register must be set to a one before the V110 Operational Registers may be accessed.

Attribute Register

The Attribute Register is located at an offset of 8 from the logical base address. This register defines the interrupting capability of the V110. The V110 is an interrupter with interrupt status functionality, but does not implement an interrupt handler.

The format of the Attribute Register is shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	IR*	IH*	IS*

Bit(s)	Mnemonic	Meaning
15-3	Not Used	These bits are not used and read as ones.
2	IR*	The V110 has interrupter control capabilities and returns this bit set to zero.
1	IH*	The V110 does not have interrupt handling capabilities and returns this bit set to one.
0	IS*	The V110 has interrupt status capabilities and returns this bit set to zero.

Serial Number High Register

The Serial Number High Register, which is located at an offset of $0A_{16}$ from the logical base address, is used in combination with the Serial Number Low Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number High Register is shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 31	SN 30	SN 29	SN 28	SN 27	SN 26	SN 25	SN 24	SN 23	SN 22	SN 21	SN 20	SN 19	SN 18	SN 17	SN 16

Bit(s)	Mnemonic	Meaning
15-0	SN31-16	SERIAL NUMBER 31 through 16 are read-only bits which represent the upper 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN15-SN00 in the Serial Number Low register.

Serial Number Low Register

The Serial Number Low Register, which is located at an offset of $0C_{16}$ from the logical base address, is used in combination with the Serial Number High Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number Low Register is shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 09	SN 08	SN 07	SN 06	SN 05	SN 04	SN 03	SN 02	SN 01	SN 00

Bit(s)	Mnemonic	Meaning
15-0	SN15-0	SERIAL NUMBER 15 through 0 are read-only bits which represent the lower 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN31-SN16 in the Serial Number High register.

Version Number Register

The Version Number Register, which is located at an offset of $0E_{16}$ from the logical base address, is a read-only register that reflects the current revision level of the hardware and firmware residing on the V110. All write operations to this register are ignored.

The following shows the bit layout of the Version Number Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Firmware Version				Firmware Revision				Hardware Version				Hardware Revision			

Bit(s)	Mnemonic	Meaning
15-12	Firmware Version	These bits reflect the module's firmware main version level.
11-8	Firmware Revision	These bits reflect the module's firmware revision number.
7-4	Hardware Version	These bits reflect the module's firmware main version number.
3-0	Hardware Revision	These bits reflect the module's firmware revision number.

Interrupt Status Register

The Interrupt Status Register is a 16-bit read-only register located at an offset of $1A_{16}$ from the logical base address. The contents of this register are enabled onto the VMEbus during interrupt acknowledge cycles. The register contains the logical address of the V110 in the lower 8-bits of the register and the upper 8-bits indicate the cause/status of the interrupt. The lower 8-bits of this register return the Logical Address of the V110 only for interrupt acknowledge cycles. An I/O read of this register returns the lower 8-bits set to ones. The V110 has 6 sources for generating an interrupt. The interrupt sources are as follows:

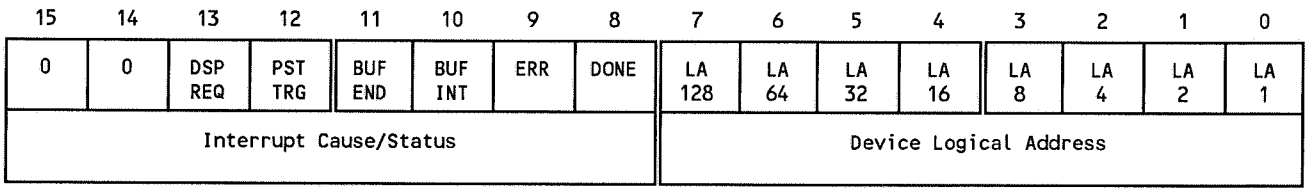
1.) DSP Request
2.) Post Trigger Counter Expiration
3.) Buffer Total Frame Count Reached
4.) Buffer Frame Interval Reached
5.) Error
6.) Done

The DSP Request Interrupt Source is generated when the DSP writes to the DSP Communication I/O Register. The Post Trigger Interrupt is sourced when the Post Trigger Frame Counter is decremented to zero. The Buffer Total Frame Count Interrupt source is asserted once the Buffer Total Frame Count has decremented to zero. The Buffer Frame Interval Interrupt is sourced when the Buffer Frame Interval count has decremented to zero. The ERROR interrupt is generated when the DIGIBUS input FIFO overflows due to the host computer accessing the DRAM buffer, preventing the DIGIBUS receive data from being stored at the selected DIGIBUS rate. The DONE interrupt source is set once a requested mode of operation has completed.

The interrupt acknowledge cycle executed on the VME bus reads a 16-bit value from the V110. The lower 8-bits of this data reflect the Logical Address of the V110. The upper 8-bits of the data field indicates the cause of the interrupt within the V110. Of the 8 bit locations, only 6 of them are used.

Once an interrupt acknowledge cycle occurs, the interrupt source bits that were set when the interrupt vector was read are reset to zero. Also, when the Interrupt Status Register is read, all interrupt source bits that were read as set are reset to zero.

The format of the Interrupt Status Register is as follows:



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Bit(s)	Mnemonic	Meaning
15-14	Not Used.	These bits are not used and read as zeros.
13	DSP REQ	DSP REQUEST is a read-and-clear bit that is set when the DSP writes to the DSP Communication I/O Register.
12	PST TRG	POST TRIGGER interrupt source is a read-and-clear bit that is set when the Post Trigger Frame Counter decrements to zero.
11	BUF END	BUFFER END interrupt source is a read-and-clear bit that is set when the Buffer Total Frame Counter is decremented to zero.
10	BUF INT	BUFFER INTERVAL interrupt source is a read-and-clear bit that is set when the Buffer Frame Interval counter decrements to zero.
9	ERR	ERROR interrupt source is a read-and-clear bit that is set when an error occurs due to the host computer accessing the DRAM buffer preventing the DIGIBUS receive data from being stored at the selected rate.
8	DONE	DONE interrupt source is a read-and-clear bit that is set once a requested operation is complete.
7-0	LA128-LA1	These bits return the current logical address of the V110 during interrupt acknowledge cycles. An I/O read of these bits returns all ones.

Interrupt Control Register

The Interrupt Control Register, which is located at offset $1C_{16}$ from the logical base address, is a write/read register used to configure the V110 for interrupt generation. The Interrupt Request Level and Interrupt Enable bit are located in this register.

The format and description of the bits in the Interrupt Control Register are shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	DSP REQ	PST TRG	BUF END	BUF INT	ERR	DONE	IREN*	1	IRQ S3	IRQ S2	IRQ S1	1	1	1

Bit(s)	Mnemonic	Meaning
15-14	Not Used	These bits are not used and read as ones.
13	DSPREQ*	DSP REQUEST is a write/read bit used to enable/disable the V110 from generating an interrupt when the DSP requires service. The interrupt is enabled by setting this bit to a zero and disabled with a one.
12	PST TRG*	POST TRIGGER is a write/read bit used to enable/disable the V110 from generating an interrupt when the Post Trigger Counter expires. The interrupt is enabled by setting this bit to a zero and disabled with a one.

11	BUF END*	BUFFER END is a write/read bit used to enable/disable the V110 from generating an interrupt when the Buffer Total Frame counter decrements to zero. The interrupt is enabled by setting this bit to a zero and disabled with a one.
10	BUF INT*	BUFFER INTERVAL is a write/read bit used to enable/disable the V110 from generating an interrupt when the Buffer Frame Interval Counter decrements to zero. The interrupt is enabled by setting this bit to a zero and disabled with a one.
9	ERR*	ERROR is a write/read bit used to enable/disable the V110 from generating an interrupt when an error occurs from a DIGIBUS input operation. The interrupt is enabled by setting this bit to a zero and disabled with a one.
8	DONE*	DONE is a write/read bit used to enable/disable the V110 from generating an interrupt when a selected operating mode has completed. The interrupt is enabled by setting this bit to a zero and disabled with a one.
7	IREN*	INTERRUPT REQUEST ENABLE is a write/read bit used to enable/disable the generation of an interrupt by the V110. Setting this bit to a zero enables the V110 to interrupt and a one disables all interrupts.
6	Not Used	This bit is not used and read as a one.
5-3	IRQS3-IRQS1	INTERRUPT REQUEST SELECT 3 through 1 are write/read bits used to select the desired Interrupt Request Level that the V110 asserts when an interrupt is sourced. The following shows the Interrupt Request Level selections.

IRQS3	IRQS2	IRQS1	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

2-0	Not Used	These bits are not used and read as ones.

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Subclass Register

The Subclass Register, which is located at an offset of $1E_{16}$ from the logical base address, is a read-only register that indicates the subclass of the V110. The V110 is an Extended Register Based Device as the following pattern indicates.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Meaning
15	This bit is set to a one indicating that this is a VXIbus extended device.
14-0	These bits are set of $7FFE_{16}$ which indicates that the V110 is an Extended Register Based Device.

Suffix High Register

The Suffix High register, which is located at an offset of 20_{16} from the logical base address, is a read-only register used in combination with the Suffix Low Register to determine the module model number suffix. The Suffix High Register contains the first two ASCII characters of the suffix and the Suffix Low Register contains the second two characters. The suffix shown is for the V110-BA11 module.

The format and bit assignments for the Suffix High Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1

This read only register contains the first two ACSII characters of the module's suffix ("BA"=4241_{16}). The following chart shows the values returned for the various V110 options.

V110 Option	ASCII Suffix Data	Suffix High Data
V110-BA11	"BA"	4241_{16}
V110-BB11	"BB"	4242_{16}
V110-BC11	"BC"	4243_{16}
V110-BD11	"BD"	4244_{16}
V110-BE11	"BE"	4245_{16}
V110-BF11	"BF"	4246_{16}

Suffix Low Register

The Suffix Low register, which is located at an offset of 22_{16} from the logical base address, is a read-only register used in combination with the Suffix High Register to determine the module model number suffix. The Suffix Low Register contains the last two ASCII characters of the suffix and the Suffix High Register contains the first two characters.

The format and bit assignments for the Suffix Low Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1

This read only register contains the last two ACSII characters of the module's suffix ("11" = 4141_{16}).

V110 Register Operational Register Layout

Address Offset	Register	Mnemonic
0_{16}	Control/Status Register	CSR
4_{16}	MultiBuffer Flag Register	FLAG
8_{16}	Buffer Total Frame Count	BTFC
C_{16}	Buffer Frame Interval Counter/Buffer End Address	BFIC / BEA
10_{16}	Post Trigger Frame Count	PTFC
14_{16}	Trigger Select Register	TSR
18_{16}	Frame Skip Counter	FSC
$1C_{16}$	Arm Capture	ARM
20_{16}	Trigger Capture	TC
24_{16}	DSP Communication I/O	DSP
28_{16}	Total Samples per Frame	TSPF
$2C_{16}$	Reserved	
30_{16}	Reserved	
34_{16}	Reserved	
200_{16} $3FF_{16}$	Sample Selection Memory	SSM

After the Operational Registers in A32 address space is the DRAM Memory. The following chart shows the address range of the RAM address as an offset from the A32 base address.

0400000 - 07FFFFF	DRAM Range for 4 Megabyte Option
0800000 - 0FFFFFF	DRAM Range for 8 Megabyte Option
1000000 - 1FFFFFF	DRAM Range for 16 Megabyte Option
2000000 - 3FFFFFF	DRAM Range for 32 Megabyte Option
4000000 - 7FFFFFF	DRAM Range for 64 Megabyte Option
8000000 - FFFFFFF	DRAM Range for 128 Megabyte Option

All of these registers and the DRAM may be accessed as longwords (32-bits) or shortwords (16-bits). When accessing a register using shortwords, the upper 16-bits of a register is accessed when VME address bit A1 is equal to 0. The lower 16-bits of a 32-bit register is accessed when VME address bit A1 is equal to 1. For example, to access the upper 16-bits of the Buffer Total Frame Count Register an offset of 08_{16} is used. To access the lower 16-bits of this registers an offset of $0A_{16}$ is used.

Control/Status Register

The Control/Status Register (CSR) is a write/read register located at an offset of 0 from the base of the Operational Registers. This register is used to control and monitor the V110. The operating mode of the V110 along with an error indication and a operation complete bit are also contained in this register.

The following diagram shows the bit pattern for the Control/Status Register.

Offset: 00_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 02_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	0	0	0	0	0	0	0	DONE	DSP REQ	ARM	1	0	MDSL 2	MDSL 1	MDSL 0

<31:16> These bits are not used and read as zeros.

<15> ERROR is a read/write-to-clear bit that is set when an error occurs during a DIGIBUS capture operation. The ERROR bit is set if the V110 is not able to store DIGIBUS data fast enough to keep the DIGIBUS input FIFO from overflowing. This is causes by the host computer accessing the DRAM buffer too frequently preventing the received DIGIBUS data from being stored in the buffer. To eliminate this problem, either slow down the DIGIBUS transmit rate of the sourcing module, use the skip counter and accept every other frame of data, or reduce the number of samples the V110 receives through the Sample Selection Memory.

The ERROR bit may also be set during Multibuffer operations when a segment of the DIGIBUS buffer contains valid data and the V110 is requested to store additional data in those locations before it is read. The ERROR bit is cleared when the V110 is placed in the idle mode or by writing a one to this bit location.

<14:8> These bits are not used and read as zeros.

<7> The DONE bit is set to a one whenever a requested operation is complete. For example, when multi-hit mode is selected, this bit is set to a zero until the Buffer Total Frame Counter is decremented to zero indicating that the DIGIBUS data has been transmitted.

<6> DSP REQUEST is a read-only bit that is set when the DSP writes to the DSP Communication Register. When this bit is set, it indicates to the host that the DSP has information available in the I/O register. The bit is cleared after the host reads the DSP Communication Register.

<5> ARM is a read-only bit that is set once the DSP is armed to capture DIGIBUS data. Once a hardware or software trigger is received to initiate data capture, this bit is cleared to a zero.

<4:3> These bits are not used and read as zero.

<2:0> MODE SELECT 2 through 0 are write/read bits used select the operating mode of the V110. The binary combination of these bits determine the operating mode. The following chart shows the various modes obtained with these three bits.

MDSL2	MDSL1	MDSL0	Selected Mode
0	0	0	Idle
0	0	1	DIGIBUS In - Single-Hit
0	1	0	DIGIBUS In - Multi-Hit
0	1	1	DIGIBUS In - Multibuffer
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

For a complete discussion of the V110 operating modes, please refer to the V110 Operating Modes section of this manual for additional details.

Multibuffer Flag Register

The Multibuffer Flag Register (FLAG) is a write/read register located at an offset of 4 from the base of the operational registers. This register is used to monitor/control the status of the eight buffer flags used during multibuffer operating modes. The flags are used to indicate when a particular buffer of data has filled, indicating that the buffer is ready for readout.

During the Multibuffer operation, DIGIBUS frames are continually received and stored in the DRAM buffer. As each frame of data is received, the Buffer Total Frame Counter and the Buffer Frame Interval Counter are decremented. When the Buffer Frame Interval Counter is decremented to zero, the next successive flag bit is set to a one indicating the buffer segment is full and ready for readout. After the Buffer Frame Interval Counter expires the first time, the FULL0 flag is set. This indicates that the first segment of the data buffer is available for readout. The number of reads the host can execute is defined as follows:

Buffer Frame Interval Counter * Number of Samples-per-Frame received

The FULL flag bits are incrementally set until the Buffer Total Frame Counter is decremented to zero, at which time the DIGIBUS buffer storage pointer is reset to zero and storage continues. The number of FULL flags bits used depends on the division of the DRAM buffer. If the Buffer Total Frame Counter divided by the Buffer Frame Interval Counter equals four, only the first four FULL flags will be used. After the fourth FULL flag is set, the DIGIBUS storage pointer is reset and the next FULL flag to be set is FULL0.

Once a segment FULL flag has been set, the host computer must read the received data and reset the FLAG to zero before the buffer segment is again accessed by DIGIBUS data storage. Failure to reset the FLAG bits before the buffer segment is again accessed will result in an ERROR being reported in the Control/Status Register.

The following diagram shows the bit layout for the Multibuffer Flag Register.

Offset: 04_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 06_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	OVER RUN	FULL 7	FULL 6	FULL 5	FULL 4	FULL 3	FULL 2	FULL 1	FULL 0

<31:9> These bits are not used and read as zeros.

<8:0> OVERRUN is a read/write-to-clear bit that is set whenever a multibuffer segment is about to be filled and the host computer has not read out the next segment to be loaded and cleared the corresponding FLAG bit.

<7:0> FULL FLAG 7 through 0 are read/write-to-clear bits that are used during multibuffer DIGIBUS IN operations. These flag bits are incrementally set to a one by the V110 when a segment of data has been stored in the DRAM buffer.

Buffer Total Frame Count Register

The Buffer Total Frame Counter (BTFC) is a write/read register located at an offset of 8 from the base of the operational registers. This register is used for specifying the number of frames that the entire RAM buffer can hold. This effectively sets the size of the circular buffer for receiving DIGIBUS data.

The data loaded into this register must not exceed the total size of the buffer. The Buffer Frame Interval multiplied by the number of samples-per-frame must not exceed the size of the DRAM buffer. The Buffer Total Frame Count Register is also used for multi-hit DIGIBUS reception for specifying the maximum number of frames to receive before the operation is complete and the DONE bit set.

The data loaded into this register is one less that the desired frame count. The following diagram shows the bit pattern of the Buffer Total Frame Count Register.

Offset: 08_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	BTFC 24	BTFC 23	BTFC 22	BTFC 21	BTFC 20	BTFC 19	BTFC 18	BTFC 17	BTFC 16

Offset: $0A_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BTFC 15	BTFC 14	BTFC 13	BTFC 12	BTFC 11	BTFC 10	BTFC 9	BTFC 8	BTFC 7	BTFC 6	BTFC 5	BTFC 4	BTFC 3	BTFC 2	BTFC 1	BTFC 0

<31:25> These bits are not used and read as zeros.

<24:0> BUFFER TOTAL FRAME COUNT 24 through 0 are write/read bits that are used to specify the number of frames that the entire DRAM can hold.

Buffer Frame Interval Counter/Buffer End Address

The Buffer Frame Interval Counter/Buffer End Address is a write/read register located at an offset of 0C hex from the base of the operational registers. This register serves two purposes and its operation varies depending on the operating mode selected. For Multibuffer modes of operation this register is used to specify the number of frames that are stored in the DRAM buffer before an FULL FLAG is set. The second function of this register is to provide a buffer end address for the Single-Hit capture operating mode.

For Multibuffer Operations:

The Buffer Frame Interval Counter must be set to a number that is result of dividing the Buffer Total Frame Count by either 1, 2, 3, 4, 5, 6, 7 or 8. The divisor determines the number of segments contained in the DRAM buffer and also indicates the number of flag bits that are used during multibuffer operations. The actual value written to this register is actually one less than the desired interval.

If desired, an interrupt may be generated when the Buffer Frame Interval Counter is decremented to zero. Refer to the Interrupt Control Register description in Configuration Space for additional information on enabling the interrupt.

For Single-Hit Operations:

When using the V110 for the Single-Hit mode of operation, the V110 is enabled and armed which causes the V110 to store all DIGIBUS data received in the DRAM buffer. For these operations, the Buffer End Address Register must be loaded with the last longword accessed before the DIGIBUS buffer pointer rolls over to zero. The combination of this register and the Buffer Total Frame Count Register determine the size of the circular buffer used for the Single-Hit mode. The value loaded into this register is calculated as follows:

((Total Number of Frames for DRAM Buffer to hold x Number of Samples-Per-Frame)/2) -1

The following diagram shows the bit layout of the Buffer Interval Counter / Buffer End Address.

Offset: $0C_{16}$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	BFIC 24	BFIC 23	BFIC 22	BFIC 21	BFIC 20	BFIC 19	BFIC 18	BFIC 17	BFIC 16

Offset: $0E_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BFIC 15	BFIC 14	BFIC 13	BFIC 12	BFIC 11	BFIC 10	BFIC 9	BFIC 8	BFIC 7	BFIC 6	BFIC 5	BFIC 4	BFIC 3	BFIC 2	BFIC 1	BFIC 0

<31:25> These bits are not used and read as zeros.

<24:0> BUFFER FRAME INTERVAL COUNTER 24 through 0 are write/read bits used to specify the number of frames of DIGIBUS data are stored into the DRAM buffer before a FULL flag bit is set during Multibuffer operations. These bits are also used for Single-Hit operations to specify the last DRAM address accessed before the circular buffer rolls over to zero.

Post Trigger Frame Count Register

The Post Trigger Frame Count Register (PTFC) is a write/read register located an offset of 10 hex from the base of the operational registers. This register is used only for the Multi-hit mode and the Single-hit mode.

When using the V110 in the Multi-hit and Single-hit modes, the Post Trigger Frame Counter is used to specify the number of frames to be stored in the DRAM buffer for every instance of a trigger. After a Multi-Hit operation is complete, indicated by the Buffer Total Frame Counter decrementing to zero, the DONE bit in the Control/Status Register is set. In Single-hit mode, this register is used to specify the number of frames to be stored after a trigger is encountered. After the Post Trigger Frame Counter is exhausted for Single-Hit operations, the DONE bit in the CSR is set and the operation is complete.

The data loaded in this register is actually one less that the desired frame count. The following diagram shows the bit pattern of the Post Trigger Frame Count Register:

Offset: 10_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	PTRG 24	PTRG 23	PTRG 22	PTRG 21	PTRG 20	PTRG 19	PTRG 18	PTRG 17	PTRG 16

Offset: 12_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PTRG 15	PTRG 14	PTRG 13	PTRG 12	PTRG 11	PTRG 10	PTRG 9	PTRG 8	PTRG 7	PTRG 6	PTRG 5	PTRG 4	PTRG 3	PTRG 2	PTRG 1	PTRG 0

<31:25> These bits are not used and read as zeros.

<24:0> POST TRIGGER COUNT 24 through 0 are write/read bits used to specify the number of frames to be stored into the DRAM buffer after a trigger occurs.

Trigger Select Register

The Trigger Select Register is a write/read register located at an offset of 14 hex from the operational registers base address. This register is used to select the source of triggering that initiates DIGIBUS data storage and enables the post trigger countdown. This register is also provides a mechanism to source a trigger from the V110 when the post trigger counter expires, allowing additional V110s to be triggered.

The trigger sources include two front panel SMB connectors, the 8 VXI TTL trigger lines and a software command. The trigger mechanism allows any or all of the sources to be enabled. Each bit that is set to a one enables the corresponding function. If all the TRIGGER INPUT SELECT bits are set to ones, the V110 may be triggered by any of the sources. Note that the software trigger mechanism is always enabled and does not require an enable bit.

After the post-trigger count expires, the V110 may output a pulse on any or all the VXI TTL Trigger lines as well as two front-panel mounted SMB connectors. The trigger output select bits determine the output trigger path. Any bit set to a one causes the corresponding signal to be asserted when the counter expires.

The following diagram shows the bit pattern for the Trigger Select Register.

Offset: 14_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	FP TOB	FP TOA	TTL TGO7	TTL TGO6	TTL TGO5	TTL TGO4	TTL TGO3	TTL TGO2	TTL TGO1	TTL TGO

Offset: 16_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FP TINB	FP TINA	TTL TGI7	TTL TGI6	TTL TGI5	TTL TGI4	TTL TGI3	TTL TGI2	TTL TGI1	TTL TGI0

<31:26> These bits are not used and read as zeros.

<25> FRONT PANEL TRIGGER OUTPUT B is a write/read bit used to enable the V110 to assert a trigger out pulse on the Trigger Output B SMB when the Post Trigger Frame Counter is decremented to zero.

<24> FRONT PANEL TRIGGER OUTPUT A is a write/read bit used to enable the V110 to assert a trigger out pulse on the Trigger Output A SMB when the Post Trigger Frame Counter is decremented to zero.

<23:16> VXI TTL TRIGGER OUTPUT 7 through 0 are write/read bits used to enable the VXI TTL Triggers to be pulsed by the V110 when the Post Trigger Frame Counter is decremented to zero.

<15:10> These bits are not used and read as zeros.

<9> FRONT PANEL TRIGGER IN ENABLE B is a write/read bit used to enable the V110 to accept a trigger input from the front panel Trigger Input B. This signal is used to initiate post trigger countdown for Multi-hit and Single-Hit operations.

<8> FRONT PANEL TRIGGER IN ENABLE A is a write/read bit used to enable the V110 to accept a trigger input from the front panel Trigger Input A. This signal is used to initiate post trigger countdown for Multi-Hit and Single-Hit operations.

<7:0> VXI TTL TRIGGER INPUT 7 through 0 are write/read bits used to select the source of triggering for transient capture modes. These signals are used to initiate post-trigger countdown for Multi-Hit and Single-Hit operations. Any bit set to a one enables the V110 to be triggered when the corresponding signal is asserted.

Frame Skip Counter

The Frame Skip Counter is a write/read register located at an offset of 18 hex from the operational registers base address. This register is used to specify the interval at which DIGIBUS frames are accepted by the V110. This register can be used to prevent the V110 from accepting all DIGIBUS frames.

The data loaded into this register is decremented as DIGIBUS frames are seen by the V110. When the counter reaches zero, the next DIGIBUS frame is stored by the V110 and the counter is reloaded. This provides a mechanism to lower the amount of data the V110 stores into the DRAM buffer. To enable the V110 to store all frames of data, load this register with a zero. To accept every other frame, load this counter with a 1. The maximum value for this register is 255 (FF_{16}), allowing the V110 to accept every 256th frame of data.

The following diagram shows the bit layout of the Frame Skip Counter.

Offset: 18_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: $1A_{16}$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	FSK 7	FSK 6	FSK 5	FSK 4	FSK 3	FSK 2	FSK 1	FSK 0

<31:8> These bits are not used and read as zeros.

<7:0> FRAME SKIP7 through 0 are write/read bits used to specify the frame capture interval.

ARM Capture

The ARM Capture address is a write-only address located at an offset of 1C hex from the base of the operational registers. This register address is used to 'arm' (enable) the capture mechanism of the V110 after all the setup registers have been loaded. Once the V110 has been setup for a capture operation, a write to the ARM Capture address with any data pattern enables the trigger mechanism.

Before Single-Hit, Multi-Hit, and Multi-Buffer operations are triggered, they must be armed. The arming of the V110 is the last event required before a trigger initiates post-trigger countdown. Once the V110 is armed, the ARMED bit in the Control/Status Register is set to a one until a trigger is received, at which time it is reset to zero. After the V110 is armed for a Single-Hit mode, DIGIBUS data is continually stored in the DRAM buffer until a trigger is found. When the trigger is received, the DIGIBUS storage address is latched by the V110 and DIGIBUS data storage continues until the post-trigger counter decrements to zero. After the port-trigger counter decrements to zero, the DONE bit in the Control/Status Register is set and the operation is complete. For Multi-Hit operations, the V110 does not store any DIGIBUS data until a trigger is received. Once the trigger is received, the V110 stores data into the DRAM buffer until the post-trigger counter decrements to zero. This continues for each trigger until the total frame counter is decremented to zero. After this counter reaches zero, the DONE bit in the Control/Status Register is set to a one and the operation is complete.

Trigger Capture

The Trigger Capture address is a write-only addressed located at an offset of 20 hex from the base of the operational registers. This register is used as a software trigger to start a DIGIBUS Multi-Hit or Single-Hit operations.. This trigger source may be used instead of the hardware trigger selections. When writing to this register, any data pattern may be used. For shortword addressing, address offset 22 hex must be used.

DSP Communication I/O Register

The DSP Communication I/O Register is a write/read register located at an offset of 24 hex from the base of the operational registers. This 16-bit register provides a bidirectional communication path to the on-board DSP. The data passed to/from the DSP depends on the how the DSP is to interact with the DRAM buffer data. The use of this register is currently reserved but is shown here for completeness.

The following diagram shows the bit layout for the DSP Communication I/O Register:

Offset: 24_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 26_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSP 15	DSP 14	DSP 13	DSP 12	DSP 11	DSP 10	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0

<31:16> These bits are not used and read as zeros.

<15:0> DSP15 through 0 are general purpose bits used to establish a bidirectional communication path to the DSP.

Total Samples Per Frame Register

The Total Samples Per Frame Register (TSPF) is a write/read register located at an offset of 28 hex from the base of the operational registers. This register is used to specify the number of 16-bit samples to allocate within each DIGIBUS frame of data. A DIGIBUS frame may contain from 1 to 2048 samples, which corresponds to data of 0 and 2047. Since the V110 memory is organized as 32-bits, only even number frame counts may be specified. If the actual desired number of total samples per frame is odd, the number must be rounded up to the next even location.

The following diagram shows the bit layout of the Total Samples Per Frame Register.

Offset: 28_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: $2A_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	TSPF 10	TSPF 9	TSPF 8	TSPF 7	TSPF 6	TSPF 5	TSPF 4	TSPF 3	TSPF 2	TSPF 1	TSPF 0

<31:11> These bits are not used and read as zeros.

<10:0> TOTAL SAMPLES PER FRAME 10 through 0 are write/read bits used to specify the total number of DIGIBUS samples that are contained in each frame of data. The value loaded in this register is actually one less than the desired sample count.

Sample Selection Memory

The Sample Selection Memory (SSM) is a 16-bit write/read memory that occupies offset 200_{16} to $3FF_{16}$ from the base of the operational registers. This memory, which is 2048 bits in length, is used to specify the samples within a frame that the V110 is to accept. Each bit position in the memory corresponds to a 16-bit sample within a frame.

Before a DIGIBUS is enabled, the Sample Selection Memory must be loaded with the samples of interest from a DIGIBUS frame. The V110 may accept all samples in a frame or a subset. To enable the V110 to accept a sample, set the corresponding bit in the Sample Selection Memory to a one. Setting any bit location to a zero causes the V110 to ignore the sample.

The following diagram shows the bit layout of the Sample Selection Memory. Since this memory is only 16-bits wide, the upper 16-bits of a 32-bit word are ignored.

Short Offset	Long Offset	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
202	200	SMP 15	SMP 14	SMP 13	SMP 12	SMP 11	SMP 10	SMP 9	SMP 8	SMP 7	SMP 6	SMP 5	SMP 4	SMP 3	SMP 2	SMP 1	SMP 0
206	204	SMP 31	SMP 30	SMP 29	SMP 28	SMP 27	SMP 26	SMP 25	SMP 24	SMP 23	SMP 22	SMP 21	SMP 20	SMP 19	SMP 18	SMP 17	SMP 16
20A	208	SMP 47	SMP 46	SMP 45	SMP 44	SMP 43	SMP 42	SMP 41	SMP 40	SMP 39	SMP 38	SMP 37	SMP 36	SMP 35	SMP 34	SMP 33	SMP 32
3FA	3F8	SMP 2031	SMP 2030	SMP 2029	SMP 2028	SMP 2027	SMP 2026	SMP 2025	SMP 2024	SMP 2023	SMP 2022	SMP 2021	SMP 2020	SMP 2019	SMP 2018	SMP 2017	SMP 2016
3FE	3FC	SMP 2047	SMP 2046	SMP 2045	SMP 2044	SMP 2043	SMP 2042	SMP 2041	SMP 2040	SMP 2039	SMP 2038	SMP 2037	SMP 2036	SMP 2035	SMP 2034	SMP 2033	SMP 2032

The following equations may be useful for determining the address offset and the data to enable a particular sample. Note that the samples within a frame are counted from 0 through 2047 and all operations are integer arithmetic.

Offset = 200_{16} + (4 * (Sample# / 16))

Data = 2 ^ ((Sample# / 16) * 16)

DIGIBUS Operation

DIGIBUS is a 10 Megabyte-per-second local bus connection between two adjacent VXI modules. The left-most side of a DIGIBUS source module's P2 connector is connected on the VXI backplane to the right-most side of a DIGIBUS sink module's P2 connector. This provides a dedicated private bus to transfer data without impeding VXIbus operations.

The DIGIBUS local connections consist of 8 data bits and three control signals. The three control signals are FRAME, BYTE CELL and SAMPLE CLOCK. The FRAME signal is used to indicate the beginning and end of a frame of DIGIBUS data. The length of a frame can be from 1 to 2048 samples. Samples consist of two 8-bit data words that are strobed using the BYTE CELL signal. The rising edge of the BYTE CELL signal strobes the first 8 data bits and the falling edge strobes the remaining 8 bits.

The V110 can pass through the DIGIBUS by strapping the V110 appropriately. Please refer to the Strap Selection Options section of this manual for addition information. The V110 may need to pass through the local bus signals in cases where multiple DIGIBUS sources reside on a single segment. In applications requiring multiple sources, one device must be designated the 'master' DIGIBUS device. The 'master' device must be enabled to generate the DIGIBUS control signals. The V110 is enabled to source the timing signals by an enable bit in the Control/Status Register in Operational Register space.

When configuring DIGIBUS source modules' registers for DIGIBUS operation, care should be taken to allocate samples within a frame correctly. Each DIGIBUS source module contains a pair of registers for allocating data during a DIGIBUS frame. These registers are used for specifying the initial sample location within a frame to deposit data along with a number of samples to source.

DIGIBUS Operating Modes

The V110 provides three operating modes to receive DIGIBUS data. These three modes are the Multibuffer Mode, the Multi-Hit Mode and the Single-Hit Mode. Once any mode is configured and enabled, DIGIBUS data reception may be started by a software trigger or by several sources of hardware triggers. The software trigger is sourced by writing to the Trigger Capture address location in Operation Register address space. The hardware trigger modes include the assertion of one of the VXI TTL trigger lines or by one of the two front panel trigger input signals. These selections are made through the Trigger Select Register.

Before a DIGIBUS capture operation, several registers must be set up prior to enabling any operating mode. The first set of registers to be programmed are used to control various aspects of the DIGIBUS.

1.) The Total Samples Per Frame Register is loaded with the number of samples per frame the DIGIBUS transfers during each frame. The data for this register ranges from 0 to 2047. These values correspond to samples-per-frame of 1 and 2048 respectively. Note that the total samples per frame must be an even number.

2.) The Sample Selection Memory must be loaded to reflect the samples of interest within a DIGIBUS frame. Each bit location in the memory corresponds to a 16-bit sample location in the frame. Any bit position in the memory set to a one enables the data to be stored in the DRAM buffer and a zero causes the V110 to ignore the sample.

The second set of registers configured prior to a DIGIBUS operation concerns the memory in which the DIGIBUS data is stored. The size of the entire memory buffer must be specified as well as the individual segment size used for multibuffer operations. These registers are loaded with data values in terms of DIGIBUS frames and not by physical addresses. The Buffer Total Frame Count Register must be loaded regardless of the operating mode selected. The Buffer Total Frame Count Register (BTFC) is loaded with a value representing the number of frames the entire memory can hold. The actual value loaded in this register is one less than the calculated value. For example, if the V110 is to hold 2048 frames of DIGIBUS data which each contain 1024 samples per frame, the BTFC is loaded with the value of 1FFFFF hex.

Depending on the desired operating mode, either the Buffer Frame Interval Count Register / Buffer End Address (BFIC/BEA) is loaded or the Post Trigger Frame Count Register (PTFC) is loaded. The BFIC/BEA register is loaded for Multibuffer operations and Single-Hit operations. The PTFC register is loaded for Single-Hit and Multi-Hit operations. The following sections further describe the DIGIBUS operating modes.

Single-Hit Operation

The V110 can be configured to store a predetermined number of DIGIBUS frames on the occurrence of a single trigger event. The number of frames stored after the receipt of a trigger is controlled through the Post Trigger Frame Counter. The trigger event can be sourced by software or by a hardware source. To enable this mode, the Mode Selection bits in the Control/Status Register of the operational registers must be set to the Single-Hit mode. The amount of memory used for this mode is controlled through the Buffer Total Frame Count. The Buffer Frame Interval/Buffer End Address Register must also be loaded with data corresponding to the last longword used for DIGIBUS storage before the buffer pointer rolls over to zero.

The amount of post-trigger data is set by using the Post Trigger Frame Counter. This controls the number of frames stored in the DRAM buffer once a trigger condition is found. The amount of pre-trigger data is then the difference between the Buffer Total Frame Count and the Post Trigger Frame Count.

Before a Single-Hit operation may occur, the V110 must be armed . The V110 is armed by writing to the Arm Capture address in operational register space. Once the V110 is armed, DIGIBUS data is continually stored into the DRAM buffer. When the Buffer Total Frame Counter expires, the DIGIBUS storage pointer address is reset and filling continues. This creates a circular data buffer for the incoming DIGIBUS data.

When the V110 receives a trigger, the DRAM buffer pointer is latched for later use during the readout process and enables the Post Trigger Frame Counter. As DIGIBUS frames are stored in the DRAM buffer, this counter is decremented until it reaches zero. When all post-trigger samples have been stored in the DRAM buffer, the DONE bit in the Control/Status Register is set and the operations is complete.

During readout of the acquired data, the DRAM pointer is controlled through a counter that is loaded with the DRAM address at the time the trigger was encountered. This counter is incremented as samples are read from the DRAM buffer. When this readout is occurring, the V110 does not pay any attention to the DRAM offset present on the VXI address lines. The results of a Single-Hit capture can actually be read though a single VXI address. This relative addressing allows the post-trigger and pre-trigger data to be read out without regard to the offsets if data within the DRAM buffer.

The first section of data read from the V110 after a Single-Hit capture ends is the post-trigger data. The data read remains post-trigger data until the number of samples read from the DRAM buffer is equal to the number of samples-per-frame times the post-trigger frame count. After this data is read, the pre-trigger data is read. Readout of the pre-trigger data can continue until all the samples have been read. The V110 must then be placed in the IDLE state to reset all the Single-Hit circuitry and to allow the DRAM buffer to be read through VXI without relative addressing.

Multi-Hit Operation

Multi-Hit operations allow the V110 to store a predetermined number of DIGIBUS frames when a trigger event is encountered. The trigger event can be generated by a front-panel trigger, a VXI TTL trigger or by a software command. Once the Multi-Hit operation is setup and enabled, the trigger event causes DIGIBUS data to be stored in the DRAM buffer until the Post Trigger Frame Counter is decremented to zero. After the counter decrements to zero, it is automatically reloaded and the V110 awaits subsequent trigger events. This continues until the Buffer Total Frame Counter is decremented to zero. When the Buffer Total Frame Counter is decremented to zero, the DONE bit in the Control/Status Register is set and the operation is complete.

Unlike the Single-Hit mode, this Multi-Hit mode does not provide for any pre-trigger data. All data entered into the DRAM buffer is the result of a trigger event, which results in all post-trigger data. If pre-trigger data is required, the Single-Hit capture mode should be used.

To use this mode, the Post Trigger Frame Counter is loaded with the number of DIGIBUS frames to be stored in the DRAM buffer after a trigger occurs. The Buffer Total Frame Counter is loaded with the number of DIGIBUS frames the entire buffer is to contain. This number can be calculated by multiplying the number of frames to enter the DRAM buffer for each trigger event times the number of trigger events to store. After these registers are loaded, the V110 may then be armed. The V110 is armed by writing to the Arm Capture address with any data pattern. At this stage, the V110 is enabled and ready to accept a trigger event.

Multibuffer Operation

The V110 Multibuffer Mode of operation is used to continually store DIGIBUS data. After setup is complete, the V110 stores DIGIBUS data as long as it is enabled and an error does not occur. An error occurs when the host computer cannot maintain the DIGIBUS data rate by reading the received data from the DRAM buffer before it is overwritten.

Prior to enabling the Multibuffer Mode, the Buffer Frame Interval Count Register (BFIC) must be loaded. This register is used to divide the buffer memory into segments of 1 to 8. The value loaded into this register represents the number of frames that are to be received from the DIGIBUS before a multibuffer flag is then set. After a DRAM buffer segment has been received, a FLAG is set indicating to the host that the buffer segment is full and is ready for readout.

After all registers have been loaded, the V110 continually loads DIGIBUS data into the DRAM buffer. The size of the DRAM buffer is controlled through the Buffer Total Frame Count Register. This sets the size of the circular buffer. The Buffer Interval Counter is decremented for each DIGIBUS frame loaded into the DRAM buffer. When this counter decrements to zero, a FLAG bit is set in the Multibuffer Flag Register and the Buffer Interval Counter is automatically reloaded. Optionally, a VXI interrupt may be generated when a FLAG is set. Once the host has been informed of the FLAG being set, either through an interrupt or through polling, the host may then read the segment of the DRAM buffer just filled. When the host has read a buffer segment, it must access the Multibuffer Flag Register to reset the corresponding FLAG bit to a zero. This sequence is used to guard against an overflow condition where a buffer segment is overwritten. The V110 examines the next sequential FLAG bit before filling the corresponding buffer segment. If the FLAG bit is set, an error is generated indicating that an overrun condition occurred.

The FLAG bits are incrementally set until the Buffer Total Frame Counter expires, which causes the DRAM buffer to be filled from the base of the buffer. The number of FLAG's used is the result of dividing the Buffer Total Frame Count by the Buffer Frame Interval Count. The V110 can be configured to use from 1 to 8 FLAG's. The Multibuffer operation continues until the V110 is placed in the IDLE mode or until an error occurs. When an error occurs, the V110 does not stop storing DIGIBUS data. This must be done manually be placing the V110 in the IDLE mode. The overflow condition is indicated by the ERROR bit in the Control/Status Register. The error condition can be found by polling the Control/Status Register or optionally, generating an interrupt.

Single-Hit DIGIBUS Receive Example

As an example, assume it is desired to setup a Single-Hit capture that is to contain a total of 3 frames of DIGIBUS data for post-trigger information and 7 frames of DIGIBUS data for pre-trigger information. The trigger mechanism is VXI trigger line 3. The DIGIBUS frames accepted have 4 samples-per-frame and the V110 is to be configured to accept all frames and all samples within the frame.

For this example, the size of the circular buffer is determined by adding the number of pre-trigger frames to the number of post-trigger frames. This yields a total buffer size of 10 frames.

The following procedure can be followed to execute this operation.

1.) Load the Buffer Total Frame Counter with the total number of DIGIBUS frames it contains minus 1. The value for this examples is 10 - 1 (9).

2.) Load the Post Trigger Frame Counter with the number of DIGIBUS frames -1. The value for this example is 3 - 1 (2).

3.) Load the Buffer Frame Interval / Buffer End Address Register with the last address accessed before a buffer rollover occurs for DIGIBUS data storage. This value is ((number of samples-per-frame times (pre-trigger frame count plus post-trigger frame count) divided by 2) minus 1. For this example, the result is 19 (13_{16}).

4.) Load the Trigger Select Register with 8 to indicate that the DIGIBUS transmission should start when TTL Trigger Line 3 is asserted.

5.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 4 - 1 (3).

6.) Load the Frame Skip Register with data of zero indicating that the V110 should accept all DIGIBUS frames.

7.) Load the first entry of the Sample Selection Memory with data that corresponds with accepting DIGIBUS samples 1, 2, 3 and 4. The data for this example is 15 (F_{16}).

8.) Write to the Control/Status Register with data set to 1 to enable the V110 for Single-Hit Mode.

9.) Execute a write operation with any data pattern to the Arm Capture address to enable the V110 to be triggered.

10.) At this point, the V110 is continually storing DIGIBUS data as each frame is received. When a trigger occurs, the V110 will enable the Post Trigger Frame Counter and decrement it as each frame is written into the DRAM buffer. After the counter decrements to zero, the DONE bit in the Control/Status Register (CSR) is set to a one. Therefore, this step is to wait for the DONE bit in the CSR to be asserted. This can be accomplished by either polling or waiting for the DONE interrupt to be asserted. The DONE interrupt must have been previously enabled in the Interrupt Control/Status Register.

11.) After DONE has been set, the host can now readout the received DIGIBUS data. First, execute enough read commands to obtain the pre-trigger data. The number of longwords to read for this example is 6. This is calculated as ((number of sample-per-frame times number of post trigger frames) divided by 2).

12.) The next data read from the V110 is the post-trigger data. The number of longwords read for this example is 14. This is calculated as ((number of sample-per-frame times number of pre-trigger frames) divided by 2).

13.) Now that all the data has been read, the V110 must be placed in the IDLE mode by writing a zero to the Control/Status Register.

Multi-Hit DIGIBUS Receive Example

As an example, assume it is desired to receive 10 DIGIBUS frames of data when TTL trigger line 2 is asserted. This operation is executed each time the trigger is seen until after the 500th occurrence at which time is should cease. This operation is executed as a Multi-Hit operation and each DIGIBUS frame contains 1024 samples. The following procedure can be followed to execute this operation.

1.) Load the Buffer Total Frame Counter with the total number of frames to receive before the operation is complete -1. The value for this example is ((10 frames * 500 occurrences) - 1) = 4999.

2.) Load the Post Trigger Frame Counter with the number of DIGIBUS frames to be received for each trigger occurrence -1. The value for this example is 10 - 1 (9).

3.) Load the Trigger Select Register with 4 to indicate that the DIGIBUS reception should start when TTL Trigger Line 2 is asserted.

4.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 1024 - 1 (1023).

5.) Load the Frame Skip Register with zero to indicate the V110 is to accept all DIGIBUS frames.

6.) Load the first 64 locations of the Sample Selection Memory with $FFFF_{16}$ to enable all DIGIBUS samples within a frame to be stored.

7.) Load the Control/Status Register with 2 to select the Multi-Hit Mode.

8.) Execute a write operation with any data pattern to the Arm Capture address to enable the V110 to be triggered.

9.) At this point, the V110 is ready to accept DIGIBUS data once a trigger event occurs on TTL Trigger Line 2. Each occurrence of the trigger line causes the V110 to store 10 frames of DIGIBUS data. This continues until 500 triggers have occurred. The user program can either wait for the DONE bit in the Control/Status Register to be asserted or use the interrupt scheme with the DONE interrupt enabled to inform the host computer that the operation is complete.

10.) Once the DONE bit has been set, the DRAM buffer can be read to retrieve the data stored from the DIGIBUS.

Multi-Buffer DIGIBUS Receive Example

As an example, assume it is desired to continually receive DIGIBUS data and inform the host computer when a predetermined number of frames have been received. This operation is executed as a Multibuffer operation and each DIGIBUS frame contains 1024 samples. The number of buffers the V110 is to use is four. The example assumes a 1000 frame buffer and is divided (segmented) into fourths, which will use four of the eight flag bits in the Multibuffer Flag Register. This results in a FLAG bit being set for every 250 frames.

The following procedure can be followed to execute this operation.

1.) Load the Buffer Total Frame Counter with the total number of frames to receive before the buffer address should rollover back to zero, minus one. The value for this example is 1000 - 1 (999).

2.) Load the Buffer Frame Interval / Buffer End Address Register with the number of frames to be received before a FLAG bit is set, minus 1. For this example, the value is 250 - 1 (249).

3.) Load the Trigger Select Register with 0 to prevent any unnecessary trigger inputs.

4.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 1024 - 1 (1023).

5.) Load the Frame Skip Register with zero to indicate the V110 is to accept all DIGIBUS frames.

6.) Load the first 64 locations of the Sample Selection Memory with $FFFF_{16}$ to enable 1024 DIGIBUS samples within a frame to be stored.

7.) Load the Control/Status Register with 3 to select the Multi-Buffer Mode.

8.) At this point, the V110 is ready to accept DIGIBUS data and store it into the DRAM buffer. After the V110 has stored 250 frames of data, the first flag bit is set to a one indicating that the first segment of data can be read. The host can be notified of the FLAG bit by either polling the Multibuffer Flag Register or by enabling the V110 to generate an interrupt when any FLAG bit is set.

9.) Read the first segment of the DRAM buffer. The initial address for the readout is at the base of the memory. The number of longwords to read is ((number of samples-per-frame times frames-per-segment) divided by 2). For this example, the result is ((1024 x 250) /2) = 128000.

10.) After the first segment is read, execute a write operation to the Multibuffer Flag Register with data set to a one to reset the first FLAG to zero.

11.) Return to polling/interrupt scheme to look for the occurrence of second flag bit. Once the flag bit has been set, read out the second segment of the memory. The initial address for this readout should start where the last segment readout stopped. For this example, the longword

offset into the memory is 512000 ($7D000_{16}$). 128000 longwords should be read for this segment. After the segment is read, a write to the Multibuffer Flag Register is executed with data set to 2 to reset the second flag bit.

12.) Return to polling/interrupt scheme to look for the occurrence of third flag bit. Once the flag bit has been set, read out the third segment of the memory. The initial address for this readout should start where the last segment readout stopped. For this example, the longword offset into the memory is 1024000 ($FA000_{16}$). 128000 longwords should be read for this segment. After the segment is read, a write to the Multibuffer Flag Register is executed with data set to 4 to reset the third flag bit.

13.) Return to polling/interrupt scheme to look for the occurrence of fourth flag bit. Once the flag bit has been set, read out the fourth segment of the memory. The initial address for this readout should start where the last segment readout stopped. For this example, the longword offset into the memory is 1536000 (177000_{16}). 128000 longwords should be read for this segment. After the segment is read, a write to the Multibuffer Flag Register is executed with data set to 8 to reset the fourth flag bit.

14.) This concludes the readout of one pass through the buffer memory. To continue, repeat steps 8 through 13. When the entire operation is to cease, write a zero into the Control/Status Register.

Front Panel LEDs and Connectors

The front-panel of the V110 contains six LEDs and four SMB connectors. The LEDs reflect various status signals of the V110. Two of the SMBs are used to trigger the V110 to start transmitting data. The other two SMBs are outputs of the V110 and are sourced when the Post Trigger Counter expires.

The SYSFAIL LED is illuminated while the V110 is executing its power-on self-test and will remain illuminated if the power-on self-test fails. While this LED is on, the V110 is asserting the VMEbus signal SYSFAIL (as long as the SYSFAIL INHIBIT bit in the Status/Control Register is configuration space is false). If this LED is on for more than 5 seconds, the V110 has failed the self-test and must be returned for repair.

The ADDRESS RECEIVED LED is a one-shot extended LED that is illuminated when the V110 is addressed in either A16 and A32 address space.

The INTERRUPT SOURCE LED is illuminated as long as the V110 has an interrupt request pending.

The DIGIBUS BUSY LED is illuminated whenever DIGIBUS activity is occurring. When the LED is off, the DIGIBUS is idle.

The BUSY LED is illuminated after the V110 has been armed and the DONE bit in the Control/Status Register of the operational register set is cleared.

The ARMED LED is illuminated when the V110 has been armed to transmit DIGIBUS data but has not received a trigger.

The V110 contains four SMB type connectors used to pass TTL level signals to/from the V110. The TRIGGER IN B and TRIGGER IN A SMB's are used as a hardware trigger mechanisms to initiate DIGIBUS data transmission. These two signals are independently enable through the Trigger Select Register. These two input signals are low true and must have a minimum pulse duration of 500 nanoseconds. These inputs are received by an 74LS14 gate and are terminated with a 180 ohm resistor to +5 volts and a 390 ohm resistor to ground.

The remaining two SMB connections are used as trigger out's from the V110. These two connections have a 200 nanosecond low true TTL level pulse applied to them when the Post Trigger Frame Counter is decremented to zero. The outputs are driven by an 74F38 open-collector driver and have a 4700 ohm pullup to +5 volts. These two signals are independently enabled through the Trigger Select Register.

DRAM Buffer Memory

The DRAM Buffer Memory is located at different offsets from the base address of the operational register depending on the amount of DRAM the V110 contains. The following shows the offset from the base address for the various options.

0400000 - 07FFFFF	DRAM Range for 4 Megabyte Option
0800000 - 0FFFFFF	DRAM Range for 8 Megabyte Option
1000000 - 1FFFFFF	DRAM Range for 16 Megabyte Option
2000000 - 3FFFFFF	DRAM Range for 32 Megabyte Option
4000000 - 7FFFFFF	DRAM Range for 64 Megabyte Option
8000000 - FFFFFFF	DRAM Range for 128 Megabyte Option

The DRAM is used to hold data obtained from receiving DIGIBUS frames. This memory can be accessed as longwords (32-bits) or shortwords (16-bits). The DIGIBUS sample storage in memory is shown in the following diagram using a 32-bit format. Notice that the first sample received below is located in the lower 16-bits of the memory and has VME address bit A1 set to 1. The sample storage shown is the default configuration for the V110. A set of straps located on the V110 can be moved to change the storage of the DIGIBUS data. The default storage is referred to as Low-Word first. The second set of tables shows the DRAM data storage for High-Word first.

Low-Word First Storage:

Memory Offset	High 16 Data Bits	Low 16 Data Bits
0_{16}	Frame #1 Sample #2	Frame #1 Sample #1
4_{16}	Frame #1 Sample #4	Frame #1 Sample #3
8_{16}	Frame #1 Sample #6	Frame #1 Sample #5
C_{16}	Frame #2 Sample #2	Frame #2 Sample #1
10_{16}	Frame #2 Sample #4	Frame #2 Sample #3
14_{16}	Frame #2 Sample #6	Frame #2 Sample #5

Model V110-Bx11

The following diagram shows the same memory buffer except it is shown in a 16-bit format.

Memory Offset	Shortword Data
0_{16}	Frame #1 Sample #2
2_{16}	Frame #1 Sample #1
4_{16}	Frame #1 Sample #4
6_{16}	Frame #1 Sample #3
8_{16}	Frame #1 Sample #6
A_{16}	Frame #1 Sample #5
C_{16}	Frame #2 Sample #2
E_{16}	Frame #2 Sample #1
10_{16}	Frame #2 Sample #4
12_{16}	Frame #2 Sample #3
14_{16}	Frame #2 Sample #6
16_{16}	Frame #2 Sample #5

High-Word First Storage:

Memory Offset	High 16 Data Bits	Low 16 Data Bits
0_{16}	Frame #1 Sample #1	Frame #1 Sample #2
4_{16}	Frame #1 Sample #3	Frame #1 Sample #4
8_{16}	Frame #1 Sample #5	Frame #1 Sample #6
C_{16}	Frame #2 Sample #1	Frame #2 Sample #2
10_{16}	Frame #2 Sample #3	Frame #2 Sample #4
14_{16}	Frame #2 Sample #5	Frame #2 Sample #6

Model V110-Bx11

The following diagram shows the same memory buffer except it is shown in a 16-bit format.

Memory Offset	Shortword Data
0_{16}	Frame #1 Sample #1
2_{16}	Frame #1 Sample #2
4_{16}	Frame #1 Sample #3
6_{16}	Frame #1 Sample #4
8_{16}	Frame #1 Sample #5
A_{16}	Frame #1 Sample #6
C_{16}	Frame #2 Sample #1
E_{16}	Frame #2 Sample #2
10_{16}	Frame #2 Sample #3
12_{16}	Frame #2 Sample #4
14_{16}	Frame #2 Sample #5
16_{16}	Frame #2 Sample #6

Strap Selection Options

Two dual inline jumper packs are used to route the DIGIBUS IN to the DIGIBUS OUT on the VXI P2 connector. Since the V110 is a DIGIBUS sink device, data is received by the V110 enters on the right side of the chassis. If a DIGIBUS data sink is to reside on the same segment as the V110 and is located to the left hand side of the V110, the jumper packs are left installed. If there are no other DIGIBUS sinks on the left hand side of the V110, the two jumper packs should be removed to prevent inadvertently inserting a module next to the V110 that uses the local bus signals. These two strap jumper packs are labeled STP7 and STP8. The location of these jumper packs can be found in the diagram following this section.

The DIGIBUS is terminated on both ends of a segment by a termination network. This network consists of a 180 ohm resistor to +5 volts and a 390 ohm resistor to ground. The first and last DIGIBUS module of a segment contain this termination. The V110 has a socketed 16 pin dual inline package that holds the resistor terminator. If no other DIGIBUS modules reside on the DIGIBUS segment to the left side of the V110, the resistor terminator must be left installed. The resistor network is removed if additional DIGIBUS sink modules reside to the left of the V110 on the same segment. The location of this resistor terminator is shown in the diagram following this section.

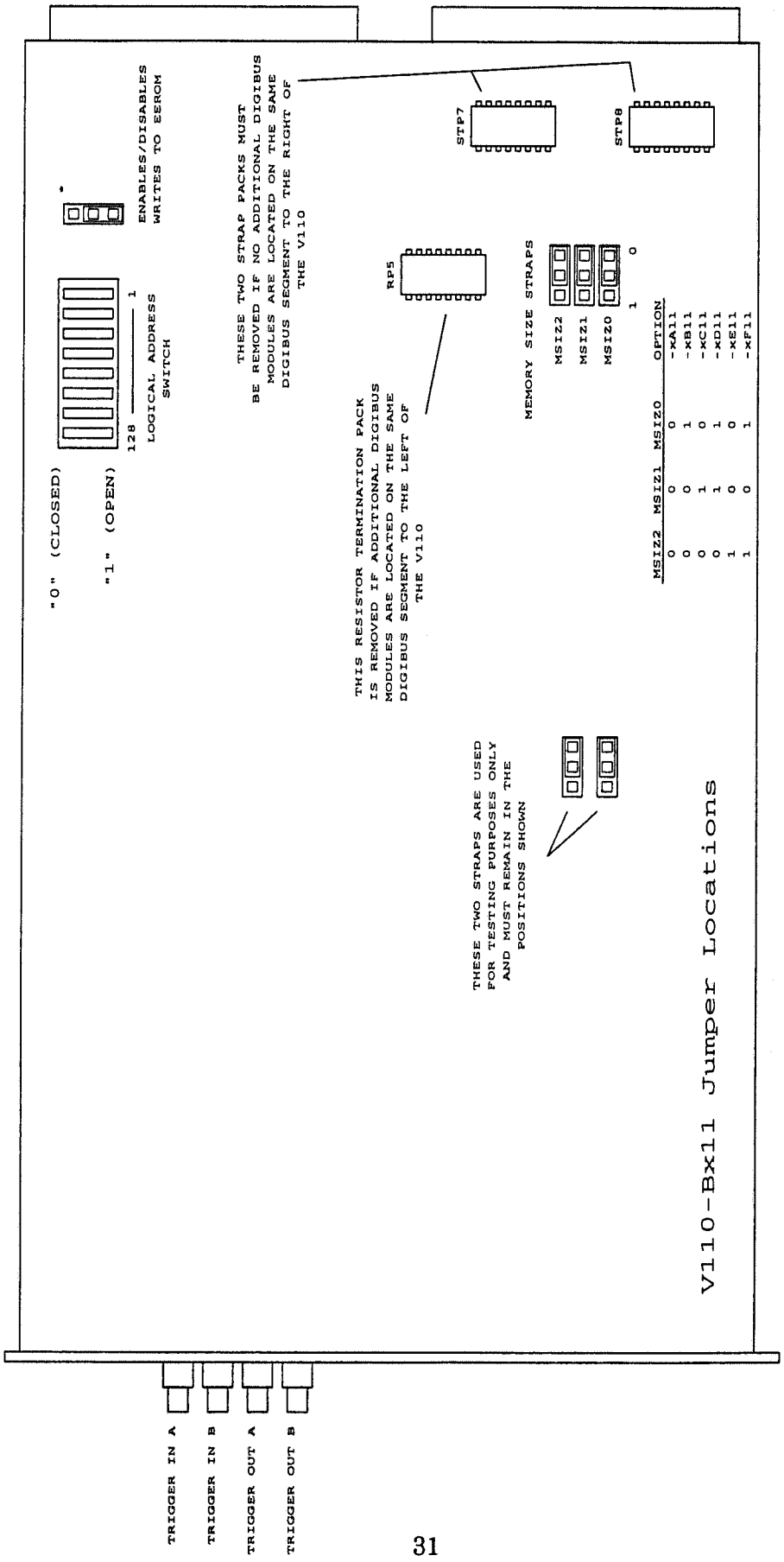
Two straps are used for configuring the order in which DIGIBUS data samples are stored in the DRAM buffer. Each DIGIBUS sample is 16-bits wide. Two 16-bit samples are contained in each 32-bit longword of the DRAM buffer. These strap selections allow the first sample of a DIGIBUS frame to be placed in either the Low-Word of the DRAM memory of the High-Word. Please refer to the DRAM Buffer Memory section of this manual for additional information on data storage.

The V110 is strapped from the factory as Low-Word first. To change the V110 configuration to be High-Word first, reverse the positions of the STP9 and STP10 straps. For Low-Word first, STP9 is loaded to jumper the

right-most two posts and STP10 is loaded to jumper the left-most two posts. For High-Word first, STP9 is loaded to jumper the left-most two posts and STP10 is loaded to jumper the right-most two posts.

Several other strap selections can be found on the V110. These straps are used during testing of the V110 and should not be altered from their factory configuration. The following diagram shows all the strap and jumpers on the V110 along with an indication of their default positions.

V110-Bx11 Jumper Locations



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4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com