Model V110-Cx11

4 to 128 Megabyte Memory

INSTRUCTION MANUAL

January, 1997

CONTENTS

TABLES

FIGURES

4 to 128 Megabyte Memory

A versatile read-write RAM memory

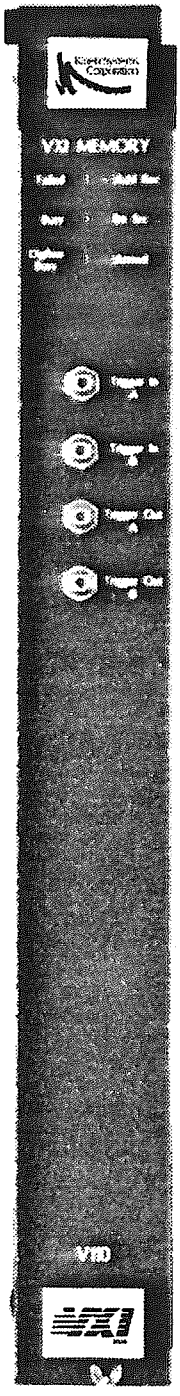
V110

Features

- **Available either as a general-purpose, read/write memory, as a data source for output modules, or as data storage for input modules**
- **Compatible with I/O modules that use the Digi-bus™ protocol**
- **Memory size options are available from 4 Mbyte to 128 Mbyte**
- **Can be used as a circular buffer for transient recorder applications with programmable pre- and post-trigger sample sizes**
- **Built-in self-test**

Typical Applications

- **Acoustic/vibration measurements**
- **Sonar (hydro-acoustics)**
- **Automotive safety testing**
- **Transient recording**
- **Local storage of data**



General Description *(Product specifications and descriptions subject to change without notice.)*

The V110 is a single-width, register-based, C-size, VXI module that can be used as a general-purpose, read/write memory on VXIbus or can interface with the family of I/O modules from KineticSystems that uses the Digi-bus™ protocol. Options of the V110 are available which provide a memory-based data source for output modules such as the V285 Arbitrary Waveform Generator or the V387 Discrete I/O modules (with output options installed); data storage for input modules such as the V207 ADC Subsystem with its family of signal conditioning modules; or VXIbus only operation (no Digi-bus interface). The physical path for the Digi-bus communications is the VXI Local Bus on the backplane P2 connector. Data can be read or written over Digi-bus from the V110 at a peak rate of 10 Mbyte/s. The actual average transfer rate may be limited by the associated I/O modules and their clock rate settings.

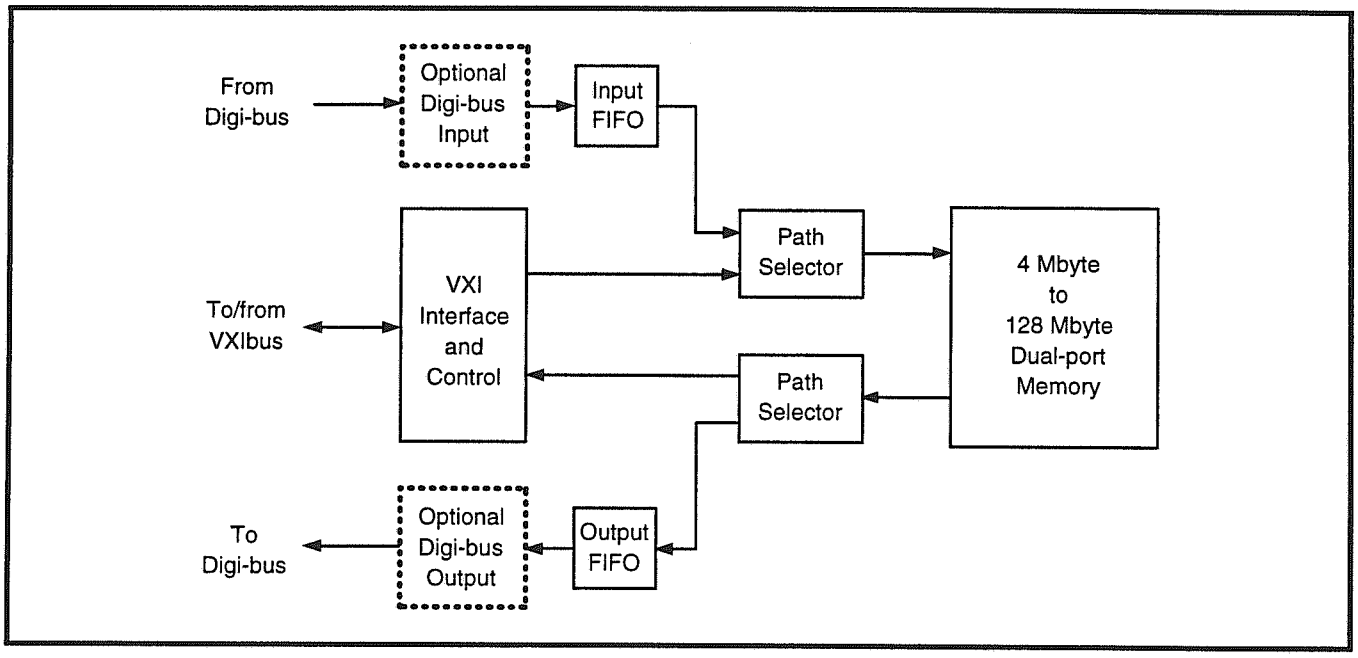
The memory on the V110 VXIbus memory module is dual-ported:

- When a Digi-bus OUT module option is used, one buffer on the V110 can be written from VXIbus while a second buffer is supplying data over Digi-bus to a V285 Arbitrary Waveform Generator, for example. When that second buffer is empty, the module begins reading data from the first buffer, allowing the second buffer to be filled from VXIbus.
- When a Digi-bus IN module option is used, one buffer on the V110 can be read from VXIbus while a second buffer is receiving data over Digi-bus from a V207 ADC Subsystem, for example. When that second buffer is full, Digi-bus begins writing data to the first buffer, allowing the second buffer to be read from VXIbus.
- With all options of the V110, it can be used as a general-purpose, read/write memory via VXIbus.

The Digi-bus input option of the V110 can also be used as a transient data recorder memory. When this feature is programmed, the memory is configured as a circular buffer. The logical size of the memory can be programmed to be the entire physical memory or a portion of it. In operation, data from an ADC module begins to be stored in the V110 prior to an "event." The logical memory size can be divided into pre-trigger and post-trigger samples. When an event trigger is received, the memory will continue recording until all post-trigger samples have been received.

The V110 supports both static and dynamic configuration capabilities. It may be accessed using A32/A16, D32/D16 data transfers. A built-in self-test is provided which performs a full memory test at power up.

Memory Data Paths



Item	Specification
Power Requirements	
+5 V	6.9 A, maximum
Environmental and Mechanical	
Temperature range	
Operational	0°C to 50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing, to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V110-wx11

w: Digi-bus options

A = no Digi-bus option
B = Digi-bus input (The V110 can read data from Digi-bus)
C = Digi-bus output (The V110 can write data to Digi-bus)

x: Memory size

A = 4 Mbyte memory
B = 8 Mbyte memory
C = 16 Mbyte memory
D = 32 Mbyte memory
E = 64 Mbyte memory
F = 128 Mbyte memory

Related Products

Model V165	Digital Signal Processor
Model V207	16-bit, 500,000 Sample/second ADC Subsystem
Model V208	16-bit, 200,000 Sample/second ADC Subsystem
Model V285	8 or 16-channel, 16-bit, 500 kHz DAC/Waveform Generator
Model V387	128-channel Discrete Input/Output
Model 5919-Z1A	Connector—SMB Cable-type

VXI CONFIGURATION REGISTER DESCRIPTIONS

VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, the V110 implements those required for extended register-based devices. The V110 also contains a set of operational registers to monitor and control operational aspects of the device.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V110 are offset from the base address. **Note: the V110 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the VMEbus cycle.** Table 1 shows the applicable Configuration Registers present in the V110, their offset from the base (Logical) address, and their Read/Write capabilities.

Table 1. Configuration Registers Configuration (A16) Space

A16 Offset	Write/Read	Register Name
00_{16}	Write/Read	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Write/Read	Status/Control Register
06_{16}	Write/Read	Offset Register
08_{16}	Read Only	Attribute Register
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved Registers
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Write/Read	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	N/A	Reserved

ID/Logical Address Register

The ID/Logical Address Register, which is located at offset 0 from the logical base address, serves two functions, depending on the direction of the VME transfer. When executing a read operation to this register, the data returned indicates the Device Class, the Address Space requirements outside of A16 space, and the Manufacturer's Identification. A write operation to this register is only executed during a dynamic configuration sequence. During the configuration sequence, the Resource Manager assigns a logical address to the V110 by writing the logical address into the lower 8-bits of this register. The format and bit assignments for this ID/Logical Address register are shown in the following diagram. Since this register has write-only and read-only bits, two bit patterns are shown.

On Read transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1

Model V110-Cx11

Bit(s)	Mnemonic	Meaning
15,14	Device Class	These bits determine the Device Class of a VXI device. These bits are set by the V110 to indicate an Extended Register Based device
13,12	Address Space	These two bits reflect the address requirements for operational registers of a VXI device. These bits are set by the V110 to indicate use of A32 address space.
11-0	Manufacturer's ID	These twelve bits are used to indicate the manufacturer of a VXI device. The Manufacturer Identification for KineticSystems is 3881 ($F29_{16}$).

On Write transactions:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Not Used								A128	LA64	LA32	LA16	LA08	LA04	LA02	LA01

For Write transfers to offset 0 of the V110, bits 15 through 08 are not used. A write to these bits has no effect on the V110. In Dynamically Configured Systems (i.e., the Logical Address switches were set to a value of 255), bits 07 through 00 are written with the new Logical Address value. This write operation is typically executed by a Resource Manager.

Model V110-Cx11

Device Type Register

The Device Type Register is a read-only register located at an offset of 2 from the logical base address. This register contains the Model Code of the V110 as well as the required A32 address space for the operational registers. The resource manager uses this field to allocate physical addresses for the V110 operational registers.

The following diagram shows the bit pattern of the Device Type Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RM 3	RM 2	RM 1	RM 0	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-12	Required Memory	These bits reflect the amount of A32 address space required by the V110. This field varies depending on the option of the V110. The following chart shows various required memory combinations based on the V110 option.

V110 Option	DRAM Size	A32 Addressing Requirement	Memory Requirement Field
V110-CA11	4 Megabyte	8 Megabyte	1000
V110-CB11	8 Megabyte	16 Megabyte	0111
V110-CC11	16 Megabyte	32 Megabyte	0110
V110-CD11	32 Megabyte	64 Megabyte	0100
V110-CE11	64 Megabyte	128 Megabyte	0011
V110-CF11	128 Megabyte	256 Megabyte	0010

11-6	Model Code	These twelve bits reflect the Model Code of a VXI device. This field is set to 272 (110_{16}) by the V110.

Status/Control Register

The Status/Control Register, which is located at an offset of 4 from the logical base address, contains write-only, read-only, and write/read bits. The following describes the bits for write and read operations.

This bit pattern shows the register layout for read accesses to the Status/Control Register.

On Read transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A32 Act	MODID*	1	1	1	1	1	1	1	1	1	1	Ready	Pass	SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15	A32 Active	This bit is read as a one when the V110 is enabled for access in A32 space.
14	MODID*	This bit is set to a one if the module is not selected with the MODID line on the VXI P2 connector. A zero indicates that the device is selected by a high state on the P2 MODID line.
13-4	Not Used	These bits are not used and read as ones.
3	Ready	READY is a read-only bit which is set to a one indicating successful completion of register initialization.
2	Pass	Pass is a read-only bit that is set to a one after the V110 has completed its power-on self-test without any errors. If errors occur, this bit is set to a zero and the SYSFAIL signal is asserted by the V110.
1	SYS INB	Reading this bit as a one indicates that the V110 is disabled from driving the SYSFAIL* line.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

This bit pattern shows the register layout for write accesses to the Status/Control Register.

On Write transactions:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not Used														SYS INB	Soft Reset

Bit(s)	Mnemonic	Meaning
15-2	Not Used	These bits are not used for write operations.

1	SYS INB	SYSFAIL INHIBIT is a write-only bit that is set to a one to inhibit the V110 from asserting the VXI SYSFAIL* signal.
0	Soft Reset	This write/read bit used to reset the V110. Reading this bit as a one indicates that the V110 is currently in the RESET state. Setting this bit to a zero removes the V110 from the RESET state.

Offset Register

The Offset register, which is located at offset 6 from the logical base address, is used for specifying the base address of the V110 operational registers in A32 space. Since different options of the V110 require varying amounts of A32 address space, the number of address bits in the Offset Register is based on the V110 DRAM size. The V110 can occupy from 8 Megabytes to 256 Megabytes of address space. This register is a 16-bit write/read register with the following bit assignments:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A31	A30	A29	A28	A27	A26	A25	A24	A23	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Meaning
15-07	A31 - A23	These write/read bits are used for defining the base address of the V110 Operational Registers. The number of address bits used depends on the V110 option. The following chart shows the number of address bits used based on the V110 option.

V110 Option	DRAM Size	A32 Addressing Requirement	Offset Address Bits Used
V110-CA11	4 Megabyte	8 Megabyte	A31 through A23
V110-CB11	8 Megabyte	16 Megabyte	A31 through A24
V110-CC11	16 Megabyte	32 Megabyte	A31 through A25
V110-CD11	32 Megabyte	64 Megabyte	A31 through A26
V110-CE11	64 Megabyte	128 Megabyte	A31 through A27
V110-CF11	128 Megabyte	256 Megabyte	A31 through A28

06-00	Not Used	These bits are not used but should be written as zeros.

After SYSRESET*, and prior to self-test, all bits are set to zero. Writing to this register is executed by the Resource Manager during the configuration process. The user may then examine this register to determine the base address of the V110 Operational Registers. The physical address in A32 address space can be calculated by reading this register and shifting the data 16 places to the left. The resultant data is the base address of the Operational Registers of the V110. After this register is written with the desired base address, the A32 ENABLE bit in the Status/Control register must be set to a one before the V110 Operational Registers may be accessed.

Attribute Register

The Attribute Register is located at an offset of 8 from the logical base address. This register defines the interrupting capability of the V110. The V110 is an interrupter with interrupt status functionality, but does not implement an interrupt handler.

The format of the Attribute Register is shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	IR*	IH*	IS*

Bit(s)	Mnemonic	Meaning
15-3	Not Used	These bits are not used and read as ones.
2	IR*	The V110 has interrupter control capabilities and returns this bit set to zero.
1	IH*	The V110 does not have interrupt handling capabilities and returns this bit set to one.
0	IS*	The V110 has interrupt status capabilities and returns this bit set to zero.

Serial Number High Register

The Serial Number High Register, which is located at an offset of $0A_{16}$ from the logical base address, is used in combination with the Serial Number Low Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number High Register is shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 31	SN 30	SN 29	SN 28	SN 27	SN 26	SN 25	SN 24	SN 23	SN 22	SN 21	SN 20	SN 19	SN 18	SN 17	SN 16

Bit(s)	Mnemonic	Meaning
15-0	SN31-16	SERIAL NUMBER 31 through 16 are read-only bits which represent the upper 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN15-SN00 in the Serial Number Low register.

Serial Number Low Register

The Serial Number Low Register, which is located at an offset of $0C_{16}$ from the logical base address, is used in combination with the Serial Number High Register to define the serial number of the V110 module. These registers are read-only and a write operation to these registers have no effect.

The format of the Serial Number Low Register is shown in the following diagram:

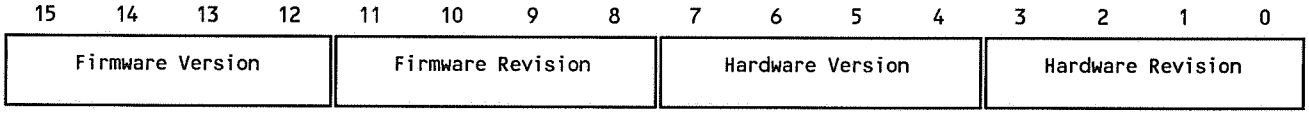
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 09	SN 08	SN 07	SN 06	SN 05	SN 04	SN 03	SN 02	SN 01	SN 00

Bit(s)	Mnemonic	Meaning
15-0	SN15-0	SERIAL NUMBER 15 through 0 are read-only bits which represent the lower 16-bits of the 32-bit module serial number. These bits are used in conjunction with the bits SN31-SN16 in the Serial Number High register.

Version Number Register

The Version Number Register, which is located at an offset of $0E_{16}$ from the logical base address, is a read-only register that reflects the current revision level of the hardware and firmware residing on the V110. All write operations to this register are ignored.

The following shows the bit layout of the Version Number Register.



Bit(s)	Mnemonic	Meaning
15-12	Firmware Version	These bits reflect the module's firmware main version level.
11-8	Firmware Revision	These bits reflect the module's firmware revision number.
7-4	Hardware Version	These bits reflect the module's firmware main version number.
3-0	Hardware Revision	These bits reflect the module's firmware revision number.

Interrupt Status Register

The Interrupt Status Register is a 16-bit read-only register located at an offset of $1A_{16}$ from the logical base address. The contents of this register are enabled onto the VMEbus during interrupt acknowledge cycles. The register contains the logical address of the V110 in the lower 8-bits of the register and the upper 8-bits indicate the cause/status of the interrupt. The lower 8-bits of this register return the Logical Address of the V110 only for interrupt acknowledge cycles. An I/O read of this register returns the lower 8-bits set to ones. The V110 has 6 sources for generating an interrupt. The interrupt sources are as follows:

1.) DSP Request
2.) Post Trigger Counter Expiration
3.) Buffer Total Frame Count Reached
4.) Buffer Frame Interval Reached
5.) Error
6.) Done

The DSP Request Interrupt Source is generated when the DSP writes to the DSP Communication I/O Register. The Post Trigger Interrupt is sourced when the Post Trigger Frame Counter is decremented to zero. The Buffer Total Frame Count Interrupt source is asserted once the Buffer Total Frame Count has decremented to zero. The Buffer Frame Interval Interrupt is sourced when the Buffer Frame Interval count has decremented to zero. The ERROR interrupt is generated when a multibuffer mode of operation terminates due to the failure of the host computer to supply the necessary data for DIGIBUS transmission for the selected rate. The DONE interrupt source is set once a requested mode of operation has completed.

The interrupt acknowledge cycle executed on the VME bus reads a 16-bit value from the V110. The lower 8-bits of this data reflect the Logical Address of the V110. The upper 8-bits of the data field indicates the cause of the interrupt within the V110. Of the 8 bit locations, only 6 of them are used.

Once an interrupt acknowledge cycle occurs, the interrupt source bits that were set when the interrupt vector was read are reset to zero. Also, when the Interrupt Status Register is read, all interrupt source bits that were read as set are reset to zero.

The format of the Interrupt Status Register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DSP REQ	PST TRG	BUF END	BUF INT	ERR	DONE	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1
Interrupt Cause/Status								Device Logical Address							

Bit(s)	Mnemonic	Meaning
15-14	Not Used.	These bits are not used and read as zeros.
13	DSP REQ	DSP REQUEST is a read-and-clear bit that is set when the DSP writes to the DSP Communication I/O Register.
12	PST TRG	POST TRIGGER interrupt source is a read-and-clear bit that is set when the Post Trigger Frame Counter decrements to zero.
11	BUF END	BUFFER END interrupt source is a read-and-clear bit that is set when the Buffer Total Frame Counter is decremented to zero.
10	BUF INT	BUFFER INTERVAL interrupt source is a read-and-clear bit that is set when the Buffer Frame Interval counter decrements to zero.
9	ERR	ERROR interrupt source is a read-and-clear bit that is set when an error occurs due to the host computer not supplying data to maintain the selected DIGIBUS transmission rate.
8	DONE	DONE interrupt source is a read-and-clear bit that is set once a requested operation is complete.
7-0	LA128-LA1	These bits return the current logical address of the V110 during interrupt acknowledge cycles. An I/O read of these bits returns all ones.

Interrupt Control Register

The Interrupt Control Register, which is located at offset $1C_{16}$ from the logical base address, is a write/read register used to configure the V110 for interrupt generation. The Interrupt Request Level and Interrupt Enable bit are located in this register.

The format and description of the bits in the Interrupt Control Register are shown in the following diagram:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	DSP REQ	PST TRG	BUF END	BUF INT	ERR	DONE	IREN*	1	IRQ S3	IRQ S2	IRQ S1	1	1	1

Bit(s)	Mnemonic	Meaning
15-14	Not Used	These bits are not used and read as ones.
13	DSPREQ*	DSP REQUEST is a write/read bit used to enable/disable the V110 from generating an interrupt when the DSP requires service. The interrupt is enabled by setting this bit to a zero and disabled with a one.
12	PST TRG*	POST TRIGGER is a write/read bit used to enable/disable the V110 from generating an interrupt when the Post Trigger Counter expires. The interrupt is enabled by setting this bit to a zero and disabled with a one.
11	BUF END*	BUFFER END is a write/read bit used to enable/disable the V110 from generating an interrupt when the Buffer Total Frame counter decrements to zero. The interrupt is enabled by setting this bit to a zero and disabled with a one.
10	BUF INT*	BUFFER INTERVAL is a write/read bit used to enable/disable the V110 from generating an interrupt when the Buffer Frame Interval Counter decrements to zero. The interrupt is enabled by setting this bit to a zero and disabled with a one.
9	ERR*	ERROR is a write/read bit used to enable/disable the V110 from generating an interrupt when an error occurs during multibuffer modes of operation. The interrupt is enabled by setting this bit to a zero and disabled with a one.
8	DONE*	DONE is a write/read bit used to enable/disable the V110 from generating an interrupt when a selected operating mode has completed. The interrupt is enabled by setting this bit to a zero and disabled with a one.
7	IREN*	INTERRUPT REQUEST ENABLE is a write/read bit used to enable/disable the generation of an interrupt by the V110. Setting this bit to a zero enables the V110 to interrupt and a one disables all interrupts.
6	Not Used	This bit is not used and read as a one.
5-3	IRQS3-IRQS1	INTERRUPT REQUEST SELECT 3 through 1 are write/read bits used to select the desired Interrupt Request Level that the V110 asserts when an interrupt is sourced. The following shows the Interrupt Request Level selections.

IRQS3	IRQS2	IRQS1	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

2-0 Not Used — These bits are not used and read as ones.

Subclass Register

The Subclass Register, which is located at an offset of $1E_{16}$ from the logical base address, is a read-only register that indicates the subclass of the V110. The V110 is an Extended Register Based Device as the following pattern indicates.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Bit(s)	Meaning
15	This bit is set to a one indicating that this is a VXIbus extended device.
14-0	These bits are set of $7FFE_{16}$ which indicates that the V110 is an Extended Register Based Device.

Suffix High Register

The Suffix High register, which is located at an offset of 20_{16} from the logical base address, is a read-only register used in combination with the Suffix Low Register to determine the module model number suffix. The Suffix High Register contains the first two ASCII characters of the suffix and the Suffix Low Register contains the second two characters. The suffix shown is for the V110-CA11 module.

The format and bit assignments for the Suffix High Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	1

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This read only register contains the first two ACSII characters of the module's suffix ("CA"=4341_{16}). The following chart shows the values returned for the various V110 options.

V110 Option	ASCII Suffix Data	Suffix High Data
V110-CA11	"CA"	4341_{16}
V110-CB11	"CB"	4342_{16}
V110-CC11	"CC"	4343_{16}
V110-CD11	"CD"	4344_{16}
V110-CE11	"CE"	4345_{16}
V110-CF11	"CF"	4346_{16}

Suffix Low Register

The Suffix Low register, which is located at an offset of 22_{16} from the logical base address, is a read-only register used in combination with the Suffix High Register to determine the module model number suffix. The Suffix Low Register contains the last two ASCII characters of the suffix and the Suffix High Register contains the first two characters.

The format and bit assignments for the Suffix Low Register are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1

This read only register contains the last two ACSII characters of the module's suffix ("11" = 4141_{16}).

V110 Register Operational Register Layout

Address Offset	Register	Mnemonic
0	Control/Status Register	CSR
4	MultiBuffer Flag Register	FLAG
8	Buffer Total Frame Count	BTFC
C	Buffer Frame Interval Counter	BFIC
10	Post Trigger Frame Count	PTFC
14	Trigger Select Register	TSR
18	Reserved	
1C	Arm Transmission	ARM
20	Trigger Transmission	TT
24	DSP Communication I/O	DSP
28	Total Samples per Frame	TSPF
2C	Output Samples per Frame	OSPF
30	Sample Starting Address	SSA
34	Clock Select Register	CSEL

After the Operational Registers in A32 address space is the DRAM Memory. The following chart shows the address range of the RAM address as an offset from the A32 base address.

0400000 - 07FFFFF	DRAM Range for 4 Megabyte Option
0800000 - 0FFFFFF	DRAM Range for 8 Megabyte Option
1000000 - 1FFFFFF	DRAM Range for 16 Megabyte Option
2000000 - 3FFFFFF	DRAM Range for 32 Megabyte Option
4000000 - 7FFFFFF	DRAM Range for 64 Megabyte Option
8000000 - FFFFFFF	DRAM Range for 128 Megabyte Option

All of these registers and the DRAM may be accessed as longwords (32-bits) or shortwords (16-bits). When accessing a register using shortwords, the upper 16-bits of a register is accessed with VME address bit A1 is equal to 0. The lower 16-bits of a 32-bit register is accessed when VME address bit A1 is equal to 1. For example, to access the upper 16-bits of the Buffer Total Frame Count Register an offset of 08_{16} is used. To access the lower 16-bits of this registers an offset of $0A_{16}$ is used.

Control/Status Register

The Control/Status Register (CSR) is a write/read register located at an offset of 0 from the base of the Operational Registers. This register is used to control and monitor the V110. The operating mode of the V110 along with an error indication and a operation complete bit are also contained in this register.

The following diagram shows the bit pattern for the Control/Status Register.

Offset: 00_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 02_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ERR	0	0	0	0	0	0	0	DONE	DSP REQ	ARM	OUT ENA	0	MDSL 2	MDSL 1	MDSL 0

<31:16> These bits are not used and read as zeros.

<15> ERROR is a read/write-to-clear bit that is set when an error occurs during DIGIBUS transmission. The ERROR bit is set if the V110 is requested to output DIGIBUS data and no transmit data is available. This is caused in multibuffer mode when the V110 crosses a segment boundary and the next segment does not contain any valid write data. This error is typically caused by slow VXI accesses which prevents the DIGIBUS from operating at the selected speed. The ERROR bit may also be set when a DIGIBUS out operation in executed and data is not available due to another device sourcing the DIGIBUS timing signals. The ERROR bit is cleared when the V110 is placed in the idle mode or by writing a one to this bit location.

<14:8> These bits are not used and read as zeros.

<7> The DONE bit is set to a one whenever a requested operation is complete. For example, when multi-hit mode is selected, this bit is set to a zero until the Buffer Total Frame Counter is decremented to zero indicating that the DIGIBUS data has been transmitted.

<6> DSP REQUEST is a read-only bit that is set when the DSP writes to the DSP Communication Register. When this bit is set, it indicates to the host that the DSP has information available in the I/O register. The bit is cleared after the host reads the DSP Communication Register.

<5> ARM is a read-only bit that is set once the DSP is armed to transmit DIGIBUS data. Once a hardware or software trigger is received to initiate data sourcing, this bit is cleared to a zero.

<4> OUTPUT ENABLE is a write/read bit used to enable/disable the V110 from sourcing the DIGIBUS timing signals. Setting this bit to a zero disables the timing signals and a one enables the strobes.

<3> This bits are not used and read as zero.

<2:0> MODE SELECT 2 through 0 are write/read bits used select the operating mode of the V110. The binary combination of these bits determine the operating mode. The following chart shows the various modes obtained with these three bits.

MDSL2	MDSL1	MDSL0	Selected Mode
0	0	0	Idle
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	DIGIBUS Out - Multibuffer
1	1	0	DIGIBUS Out - Multi-Hit
1	1	1	DIGIBUS Out - Single-Hit

For a complete discussion of the V110 operating modes, please refer to the V110 Operating Modes section of this manual for additional details.

Multibuffer Flag Register

The Multibuffer Flag Register (FLAG) is a write/read register located at an offset of 4 from the base of the operational registers. This register is used to monitor/control the status of the eight buffer flags used during multibuffer operating modes. The flags are used to indicate when a particular buffer of data has been transmitted onto DIGIBUS.

After multibuffer operation is initiated, these flags are all set to one indicating there is no data available for DIGIBUS transmission. It is then up to the host computer to supply the DIGIBUS transmit data by loading the DRAM buffer and clearing the corresponding EMPTY flag. After the Buffer Frame Interval Counter expires for the first time, the EMPTY FLAG0 bit is set. This indicates that the first segment of the data buffer has been transmitted. The flag bits are incrementally set until the Buffer Total Frame Count is decremented to zero; at which time the DRAM address is reset and buffer readout continues. The number of flag bits that are used depends on the division of the buffer. If the Buffer Total Frame Count divided by the Buffer Frame Interval Count equals 4, only the first four flag bits are used. After a segment of data has been written, a write operation is executed to the corresponding flag bit to reset it to zero.

An error bit is provided to indicate when a request is made during multibuffer operations to transmit DIGIBUS data and the buffer segments' flag bit is not set; indicating data is not available for transmission. This error is referred is to as an underrun condition. The following diagram shows the bit layout for the Multibuffer Flag Register.

Offset: 04_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 06_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	UNDR RUN	MT 7	MT 6	MT 5	MT 4	MT 3	MT 2	MT 1	MT 0

<31:9> These bits are not used and read as zeros.

<8> The UNDERRUN bit is a read/write-to-clear bit that is set when the V110 is used in the multibuffer mode and the V110 is requested to transmit DIGIBUS data from a segment of the DRAM buffer and the buffer is empty. This error is generated when VXI is not able to sustain the data rate required by the DIGIBUS transmit rate. The assertion of this bit also sets the ERROR bit in the Control/Status Register. This bit is cleared when the V110 is placed in the idle mode or a write to this bit location with data set to one.

<7:0> EMPTY FLAG 7 through 0 are read/write-to-clear bits that are used during multibuffer DIGIBUS OUT operations. These flag bits are set to zero by the V110 when a segment of data has been transmitted and must be set to a one by the host computer as DIGIBUS data frame segments are loaded into the RAM.

Buffer Total Frame Count Register

The Buffer Total Frame Counter (BTFC) is a write/read register located at an offset of 8 from the base of the operational registers. This register is used for specifying the number of frames that the entire RAM buffer can hold. This effectively sets the size of the circular buffer for sourcing DIGIBUS data.

The data loaded into this register must not exceed the total size of the buffer. The Buffer Frame Interval multiplied by the number of samples-per-frame must not exceed the size of the DRAM buffer. The Buffer Total Frame Count Register is also used for multi-hit DIGIBUS transmission for specifying the maximum number of frames to source before the operation is complete and the DONE bit set.

The data loaded into this register is one less that the desired frame count. The following diagram shows the bit pattern of the Buffer Total Frame Count Register.

Offset: 08_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	BTFC 24	BTFC 23	BTFC 22	BTFC 21	BTFC 20	BTFC 19	BTFC 18	BTFC 17	BTFC 16

Offset: $0A_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BTFC 15	BTFC 14	BTFC 13	BTFC 12	BTFC 11	BTFC 10	BTFC 9	BTFC 8	BTFC 7	BTFC 6	BTFC 5	BTFC 4	BTFC 3	BTFC 2	BTFC 1	BTFC 0

<31:25> These bits are not used and read as zeros.

<24:0> BUFFER TOTAL FRAME COUNT 24 through 0 are write/read bits that are used to specify the number of frames that the entire DRAM can hold.

Buffer Frame Interval Counter

The Buffer Frame Interval Counter is a write/read register located at an offset of 0C hex from the base of the operational registers. This register is used to specify the number of frames that are sent from the DRAM buffer before an EMPTY FLAG is set during multibuffer operations.

The Buffer Frame Interval Counter must be set to a number that is result of dividing the Buffer Total Frame Count by either 1, 2, 3, 4, 5, 6, 7 or 8. The divisor determines the number of segments contained in the DRAM buffer and also indicates the number of flag bits that are used during multibuffer operations. The actual value written to this register is actually one less than the desired interval.

If desired, an interrupt may be generated when the Buffer Frame Interval Counter is decremented to zero. Refer to the Interrupt Control Register description in Configuration Space for additional information on enabling the interrupt.

The following diagram shows the bit layout of the Buffer Interval Counter:

Offset: $0C_{16}$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	BFIC 24	BFIC 23	BFIC 22	BFIC 21	BFIC 20	BFIC 19	BFIC 18	BFIC 17	BFIC 16

Offset: $0E_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BFIC 15	BIC 14	BFIC 13	BFIC 12	BFIC 11	BFIC 10	BFIC 9	BFIC 8	BFIC 7	BFIC 6	BFIC 5	BFIC 4	BFIC 3	BFIC 2	BFIC 1	BFIC 0

<31:25> These bits are not used and read as zeros.

<24:0> BUFFER FRAME INTERVAL COUNTER 24 through 0 are write/read bits used to specify the number of frames of DIGIBUS data are transmitted from the DRAM buffer before an EMPTY flag bit is set.

Post Trigger Frame Count Register

The Post Trigger Frame Count Register (PTFC) is a write/read register located an offset of 10 hex from the base of the operational registers. This register is used only for the multi-hit mode and the single-hit mode.

When using the V110 in the multi-hit and single-hit transmission modes, the Post Trigger Frame Counter is used to specify the number of frames to be sent from the DRAM buffer for every instance of a trigger. After the transmission is complete, indicated by the Buffer Total Frame Counter decrementing to zero, the DONE bit in the Control/Status Register is set. In single-hit mode, this register is used to specify the number of frames to be sent after a trigger is encountered. After the Post Trigger Frame Counter is exhausted, the DONE bit in the CSR is set and the operation is complete.

The data loaded in this register is actually one less that the desired frame count. The following diagram shows the bit pattern of the Post Trigger Frame Count Register:

Offset: 10_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	PTRG 24	PTRG 23	PTRG 22	PTRG 21	PTRG 20	PTRG 19	PTRG 18	PTRG 17	PTRG 16

Offset: 12_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PTRG 15	PTRG 14	PTRG 13	PTRG 12	PTRG 11	PTRG 10	PTRG 9	PTRG 8	PTRG 7	PTRG 6	PTRG 5	PTRG 4	PTRG 3	PTRG 2	PTRG 1	PTRG 0

<31:25> These bits are not used and read as zeros.

<24:0> POST TRIGGER COUNT 24 through 0 are write/read bits used to specify the number of frames to be sent from the DRAM buffer after a trigger occurs.

Trigger Select Register

The Trigger Select Register is a write/read register located at an offset of 14 hex from the operational registers base address. This register is used to select the source of triggering that initiates DIGIBUS transmission and enables the post trigger countdown. This register is also provides a mechanism to source a trigger from the V110 when the post trigger counter expires, allowing additional V110s to be triggered.

The trigger sources include two front panel SMB connectors, the 8 VXI TTL trigger lines and a software command. The trigger mechanism allows any or all of the sources to be enabled. Each bit that is set to a one enables the corresponding function. If all the TRIGGER INPUT SELECT bits are set to ones, the V110 may

be triggered by any of the sources. Note that the software trigger mechanism is always enabled and does not require an enable bit.

After the post-trigger count expires, the V110 may output a pulse on any or all the VXI TTL Trigger lines as well as two front-panel mounted SMB connectors. The trigger output select bits determine the output trigger path. Any bit set to a one causes the corresponding signal to be asserted when the counter expires.

The following diagram shows the bit pattern for the Trigger Select Register.

Offset: 14_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	FP TOB	FP TOA	TTL TGO7	TTL TGO6	TTL TGO5	TTL TGO4	TTL TGO3	TTL TGO2	TTL TGO1	TTL TGO

Offset: 16_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FP TINB	FP TINA	TTL TGI7	TTL TGI6	TTL TGI5	TTL TGI4	TTL TGI3	TTL TGI2	TTL TGI1	TTL TGI0

<31:26> These bits are not used and read as zeros.

<25> FRONT PANEL TRIGGER OUTPUT B is a write/read bit used to enable the V110 to assert a trigger out pulse on the Trigger Output B SMB when the Post Trigger Frame Counter is decremented to zero.

<24> FRONT PANEL TRIGGER OUTPUT A is a write/read bit used to enable the V110 to assert a trigger out pulse on the Trigger Output A SMB when the Post Trigger Frame Counter is decremented to zero.

<23:16> VXI TTL TRIGGER OUTPUT 7 through 0 are write/read bits used to enable the VXI TTL Triggers to be pulsed by the V110 when the Post Trigger Frame Counter is decremented to zero.

<15:10> These bits are not used and read as zeros.

<9> FRONT PANEL TRIGGER IN ENABLE B is a write/read bit used to enable the V110 to accept a trigger input from the front panel Trigger Input B. This signal is used to initiate post trigger countdown for multi-hit transmission.

<8> FRONT PANEL TRIGGER IN ENABLE A is a write/read bit used to enable the V110 to accept a trigger input from the front panel Trigger Input A. This signal is used to initiate post trigger for multi-hit transmission.

<7:0> VXI TTL TRIGGER INPUT 7 through 0 are write/read bits used to select the source of triggering for transient capture modes. Any bit set to a one enables the V110 to be triggered when the corresponding signal is asserted.

Trigger Transmission

The Trigger Transmission address is a write-only addressed located at an offset of 20 hex from the base of the operational registers. This register is used as a software trigger to start a DIGIBUS multi-hit or single-hit transmission. This trigger source may be used instead of the hardware trigger selections. When writing to this register, any data pattern may be used. For shortword addressing, address offset 22 hex must be used.

DSP Communication I/O Register

The DSP Communication I/O Register is a write/read register located at an offset of 24 hex from the base of the operational registers. This 16-bit register provides a bidirectional communication path to the on-board DSP. The data passed to/from the DSP depends on the how the DSP is to interact with the DRAM buffer data. The use of this register is currently reserved but is shown here for completeness.

The following diagram shows the bit layout for the DSP Communication I/O Register:

Offset: 24_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 26_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DSP 15	DSP 14	DSP 13	DSP 12	DSP 11	DSP 10	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0

<31:16> These bits are not used and read as zeros.

<15:0> DSP15 through 0 are general purpose bits used to establish a bidirectional communication path to the DSP.

Total Samples Per Frame Register

The Total Samples Per Frame Register (TSPF) is a write/read register located at an offset of 28 hex from the base of the operational registers. This register is used to specify the number of 16-bit samples to allocate within each DIGIBUS frame of data. A DIGIBUS frame may contain from 1 to 2048 samples, which corresponds to data of 0 and 2047. Since the V110 memory is organized as 32-bits, only even number frame counts may be specified. If the actual desired number of total samples per frame is odd, the number must be rounded up to the next even location. This does not cause any problems with the device receiving the DIGIBUS data since it can be instructed to ignore the sample.

The following diagram shows the bit layout of the Total Samples Per Frame Register.

Offset: 28_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: $2A_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	TSPF 10	TSPF 9	TSPF 8	TSPF 7	TSPF 6	TSPF 5	TSPF 4	TSPF 3	TSPF 2	TSPF 1	TSPF 0

<31:11> These bits are not used and read as zeros.

<10:0> TOTAL SAMPLES PER FRAME 10 through 0 are write/read bits used to specify the total number of DIGIBUS OUTPUT samples that are contained in each frame of data. The value loaded in this register is actually one less than the desired sample count.

Output Samples Per Frame Register

The Output Samples Per Frame Register (OSPF) is a write/read register located at an offset of 2C hex from the base of the operational registers. This register is used to specify the number of 16-bit samples that the V110 is to output for each DIGIBUS frame of data. The frame may contain from 1 to 2048 samples. This corresponds to data of 0 and 2047 respectively. Since the V110 memory is organized as 32-bits, only even number frame counts may be specified. If the actual desired number of total samples per frame is odd, the number must be rounded up to the next even location. This does not cause any problems with the device receiving the DIGIBUS data since it can be instructed to ignore the sample. Note that the value in this register must be less than or equal to the data in the Total Samples Per Frame Register.

The following diagram shows the bit layout of the Total Samples Per Frame Register.

Offset: $2C_{16}$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: $2E_{16}$

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	OSPF 10	OSPF 9	OSPF 8	OSPF 7	OSPF 6	OSPF 5	OSPF 4	OSPF 3	OSPF 2	OSPF 1	OSPF 0

<31:11> These bits are not used and read as zeros.

<10:0> OUTPUT SAMPLES PER FRAME10 through 0 are write/read bits used to specify the number of DIGIBUS OUTPUT samples that the V110 outputs for each frame of data. The value loaded in this register is actually one less than the desired sample count.

Sample Starting Address Register

The Sample Starting Address Register is a write/read register located at an offset of 30 hex from the base of the operational registers. This register is used to specify the initial address within a frame which the V110 starts transmitting output samples. This value can range from 0 to 2047 and corresponds to sample locations 1 through 2048 of a DIGIBUS frame. This allows other DIGIBUS source devices located on a DIGIBUS segment to output samples in other locations within a frame.

The following diagram shows the bit pattern for the Sample Starting Address Register.

Offset: 30_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Offset: 32_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	SSA 10	SSA 9	SSA 8	SSA 7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0

<31:11> These bits are not used and read as zeros.

<10:0> STARTING SAMPLE ADDRESS10 through 0 are write/read bits that specify the initial location sample location within a frame at which the V110 starts outputting DIGIBUS data.

Clock Select Register

The Clock Select Register is a write/read register located at an offset of 34 hex from the base of the operational registers. This register is used to select the data rate at which the V110 runs the DIGIBUS. The rate at which samples are transmitted during a frame and the rate at which frames are transmitted are selected through this register. This data rates range from 50 Kilobytes per second to 10 Megabytes per second for the rate of sample transmission within a frame. The frame output rate ranges from 5 Megahertz to 76 hertz in 200 nanosecond increments.

Three bits are provided for selecting the rate at which samples are output within a frame. The rate at which frames are transmitted is controlled through a 16-bit modulo-N counter. This counter is loaded with the number of 200 nanosecond increments between the start of DIGIBUS frames. For example, to transmit a DIGIBUS frame at a 10 Kilohertz (100 millisecond period) the Frame Rate Counter bits should be loaded with 500. The calculation f or determining the data for this register is:

Sample Rate divided by 200 nanoseconds

(100 millisecond/200 nanoseconds = 500)

The following diagram shows the bit pattern for the Clock Select Register.

Offset: 34_{16}

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	0	0	0	0	0	0	0	SPRT 2	SPRT 1	SPRT 0

Offset: 36_{16}

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
FRT 15	FRT 14	FRT 13	FRT 12	FRT 11	FRT 10	FRT 9	FRT 8	FRT 7	FRT 6	FRT 5	FRT 4	FRT 3	FRT 2	FRT 1	FRT 0

<31:19> These bits are not used and read as zeros.

<18:16> CLOCK SELECT2 through 0 are write/read bits used to specify the rate at which the samples are transmitted during the frame. The following chart shows the various data rates obtained by the binary combination of these three bits.

CKSL2	CKSL1	CKSL0	DIGIBUS Sample Data Rate
0	0	0	10 Megabytes Per Second
0	0	1	5 Megabytes Per Second
0	1	0	2.5 Megabytes Per Second
0	1	1	1 Megabyte Per Second
1	0	0	500 Kilobytes Per Second
1	0	1	250 Kilobytes Per Second
1	1	0	100 Kilobytes Per Second
1	1	1	50 Kilobytes Per Second

<15:0> FRAME RATE 15 through 0 are write/read bits used to specify the rate at which DIGIBUS frames are transmitted. This register is loaded with the number of 200 nanosecond increments between DIGIBUS frames. The FRAME CLOCK ENABLE must be set to a one to enable the clock rate.

DIGIBUS Operation

DIGIBUS is a 10 Megabyte-per-second local bus connection between two adjacent VXI modules. The left-most side of a DIGIBUS source module's P2 connector is connected on the VXI backplane to the right-most side of a DIGIBUS sink module's P2 connector. This provides a dedicated private bus to transfer data without impeding VXIbus operations.

The DIGIBUS local connections consist of 8 data bits and three control signals. The three control signals are FRAME, BYTE CELL and SAMPLE CLOCK. The FRAME signal is used to indicate the beginning and end of a frame of DIGIBUS data. The length of a frame can be from 1 to 2048 samples. Samples consist of two 8-bit data words that are strobed using the BYTE CELL signal. The rising edge of the BYTE CELL signal strobes the first 8 data bits and the falling edge strobes the remaining 8 bits.

The V110 can pass through the DIGIBUS by strapping the V110 appropriately. Please refer to the Strap Selection Options section of this manual for addition information. The V110 may need to pass through the local bus signals in cases where multiple DIGIBUS sources reside on a single segment. In applications requiring multiple sources, one device must be designated the 'master' DIGIBUS device. The 'master' device must be enabled to generate the DIGIBUS control signals. The V110 is enabled to source the timing signals by an enable bit in the Control/Status Register in Operational Register space.

When configuring DIGIBUS source modules' registers for DIGIBUS operation, care should be taken to allocate samples within a frame correctly. Each DIGIBUS source module contains a pair of registers for allocating data during a DIGIBUS frame. These registers are used for specifying the initial sample location within a frame to deposit data along with a number of samples to source.

DIGIBUS Operating Modes

The V110 provides three operating modes to source DIGIBUS data. These three modes are the Multibuffer Mode, the Multi-Hit Mode and the Single-Hit Mode. Once any mode is configured and enabled, DIGIBUS transmission may be started by a software trigger or by several sources of hardware triggers. The software trigger is sourced by writing to the Trigger Transmission address location in Operation Register address space. The hardware trigger modes include the assertion of one of the VXI TTL trigger lines or by one of the two front panel trigger input signals. These selections are made through the Trigger Select Register.

Before DIGIBUS transmission, several registers must be set up prior to enabling any operating mode. The first set of registers to be programmed are used to control various aspects of the DIGIBUS. These parameters concern the timing of the DIGIBUS and the sample information within a frame. The following registers are loaded with data to configure DIGIBUS parameters:

1.) The Total Samples Per Frame Register is loaded with the number of samples per frame the DIGIBUS transfers during each frame. The data for this register ranges from 0 to 2047. These values correspond to samples-per-frame of 1 and 2048 respectively. Note that the total samples per frame must be an even number.

2.) The Output Samples Per Frame Register is loaded with the number of samples-per-frame that the V110 is to place onto the DIGIBUS once its initial storage slot is reached. Note that the total samples per frame must be an even number.

3.) The Sample Starting Address Register is loaded with the initial sample location within a DIGIBUS frame where the V110 is to place data. This data ranges from 0 to 2047 and corresponds to sample locations 1 and 2048 respectively.

4.) The Clock Select Register is loaded with the rate at which DIGIBUS frames are output onto the local bus and the rate at which the samples are generated inside each frame. These should normally be set to the fastest settings unless the DIGIBUS data receiver cannot handle the data rate.

The second set of register configured prior to DIGIBUS transmission concerns the memory in which the DIGIBUS data is stored. The size of the entire memory buffer must be specified as well as the individual segment size used for multibuffer operations. These registers are loaded with data values in terms of DIGIBUS frames and not by physical addresses. The Buffer Total Frame Count Register must be loaded regardless of the operating mode selected. The Buffer Total Frame Count Register (BTFC) is loaded with a value representing the number of frames the entire memory can hold. The actual value loaded in this register is one less than the calculated value. For example, if the V110 is to hold 2048 frames of DIGIBUS data which each contain 1024 samples per frame, the BTFC is loaded with the value of 1FFFFF hex.

Depending on the desired operating mode, either the Buffer Frame Interval Count Register (BFIC) is loaded or the Post Trigger Frame Count Register (PTFC) is loaded. The BFIC register is loaded for multibuffer operations and the PTFC register is loaded for multihit operations. The following sections further describe the DIGIBUS source operating modes.

Multibuffer Operation

The V110 Multibuffer Mode of operation is used to continually source DIGIBUS data. After setup is complete, the V110 sources DIGIBUS data as long as it is enabled and an error does not occur. An error occurs when the host computer cannot maintain the DIGIBUS data rate by supplying the data as it is needed.

Prior to enabling the Multibuffer Mode, the Buffer Frame Interval Count Register (BFIC) must be loaded. This register is used to divide the buffer memory into segments of 1 to 8. The value loaded into this register represents the number of frames that are to be transmitted onto the DIGIBUS before a multibuffer flag is then set. After a buffer segment has been transmitted the segment may then be refilled by the host computer.

After all registers have been loaded, the V110 memory may then be loaded with the data to be transmitted. Starting at the base of the memory, the DIGIBUS data is written until at least one segment of data has been loaded. When the initial memory (buffer) segment is loaded, the first multibuffer flag must then be set to a one indicating that the first segment of the memory contains legitimate DIGIBUS data. The segment size has already been determined by the setting in the Buffer Frame Interval Counter. As additional segments of the buffer are filled with DIGIBUS data, the corresponding flags are set as required.

The V110 is now ready to be armed. The arming of the V110 is accomplished by writing any data pattern to the Arm Transmission address in operational register space. Once armed, the V110 can be trigger to start the data transmission by either software or a preselected hardware trigger source. After the trigger is received, the V110 start transferring DIGIBUS data as configured in the Clock Select Register.

The V110 will transfer data as long as data is available. The host computer must fill buffer segments emptied by transmitting DIGIBUS data and must also set the appropriate flags. The transfer of data continues until the V110 is placed in the idle mode or the host computer fails to sustain the data rate required to transfer the data.

Multi-Hit Operation

The V110 can be configured to output a predetermined number of DIGIBUS frames on the multiple occurrences of a trigger event. The trigger event can be sourced by software or by a hardware mechanism. To enable this mode, the Mode Selection bits in the Control/Status Register of the operational registers must be set to the Multi-Hit mode.

Before multi-hit operations may occur, the V110 memory must be preloaded with the data to send. After the data is loaded, the V110 may then be armed and triggered. The V110 is armed by writing to the Arm

Transmission address in operational register space. The V110 can be triggered by writing to the Trigger Transmission address or by a preselected hardware source. The trigger selection is made through the Trigger Select Register.

Once a trigger occurs, the V110 outputs frames of DIGIBUS data until the Post Trigger Counter is exhausted and then waits for subsequent triggers. Transmission of data continues for each trigger event until the Buffer Total Frame Count is exhausted. When the Buffer Total Frame Counter is exhausted, the DONE bit of the Control/Status register of the operational registers is set to one and the operation is complete.

Single-Hit Operation

The V110 can be configured to output a predetermined number of DIGIBUS frames on the a single trigger occurrence of a trigger event. The trigger event can be sourced by software or by a hardware source. To enable this mode, the Mode Selection bits in the Control/Status Register of the operational registers must be set to the Single-Hit mode.

Before a single-hit operations may occur, the V110 memory must be preloaded with the data to send. After the data is loaded, the V110 may then be armed and triggered. The V110 is armed by writing to the Arm Transmission address in operational register space. The V110 can be triggered by writing to the Trigger Transmission or by a preselected hardware mechanism. The trigger selection is made through the Trigger Select Register.

Once a trigger occurs, the V110 outputs frames of DIGIBUS data until the Post Trigger Counter is exhausted at which time the DONE bit of the Control/Status register of the operational registers is set to one and the operation is complete. For additional transmission, the V110 must be re-armed and re-triggered.

Single-Hit DIGIBUS Transmit Example

As an example, assume it is desired to transmit 100 DIGIBUS frames of data when TTL trigger line 3 is asserted. This operation is executed as a single-hit operation and each DIGIBUS frame contains 512 samples. The following procedure can be followed to execute this operation.

1.) Load the 100 DIGIBUS frames worth of data into the DRAM starting at the base of the DRAM. The total number of 16-bit samples the V110 will transmit is 51200 (100 * 512). This amount of data requires 25600 longwords in the memory buffer.

2.) Load the Buffer Total Frame Counter with -1 ($FFFFFFFF_{16}$) to ensure that the counter does not expire during the DIGIBUS transmission.

3.) Load the Post Trigger Frame Counter with the number of DIGIBUS frames -1. The value for this example is 100 - 1 (99).

4.) Load the Trigger Select Register with 8 to indicate that the DIGIBUS transmission should start when TTL Trigger Line 3 is asserted.

5.) Load the Clock Select Register with zero to use the fastest DIGIBUS rate.

6.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 512 - 1 (511).

7.) Load the Output Samples Per Frame with the number of samples the V110 is to place in each frame of DIGIBUS data. For this example, the number is the same as for the Total Samples Per Frame, which is 512 - 1 (511).

8.) Load the Sample Starting Address with the first location that the V110 is to place data. Since the V110 is the only device asserting DIGIBUS data, this data should be set to zero.

9.) Load the Control/Status Register with 23 (17_{16}) to select the Single-Hit Mode and enable the DIGIBUS output strobes.

10.) Execute a write operation with any data pattern to the Arm Transmission address to enable the V110 to be triggered.

11.) At this point, the V110 is ready to start transmitting DIGIBUS data as soon as the TTL Trigger Line 3 is asserted. The V110 will output 100 frames of data and then stop. The user program can either wait for the DONE bit in the Control/Status Register to be asserted or use the interrupt scheme with the DONE interrupt enabled to inform the host computer that the operation is complete.

Multi-Hit DIGIBUS Transmit Example

As an example, assume it is desired to transmit 10 DIGIBUS frames of data when TTL trigger line 2 is asserted. This operation is executed each time the trigger is seen until after the 500th occurrence at which time is should cease. This operation is executed as a multi-hit operation and each DIGIBUS frame contains 1024 samples. The following procedure can be followed to execute this operation.

1.) Load the 5000 DIGIBUS frames (10 frames * 500 occurrences) worth of data into the DRAM starting at the base of the DRAM. The total number of 16-bit samples the V110 will transmit is 5120000 (5000 * 1024). This amount of data requires 2560000 longwords in the memory buffer.

2.) Load the Buffer Total Frame Counter with the total number of frames to transmit before the operation is complete -1. The value for this example is ((10 frames * 500 occurrences) - 1) = 4999.

3.) Load the Post Trigger Frame Counter with the number of DIGIBUS frames to be transmitted for each trigger occurrence -1. The value for this example is 10 - 1 (9).

4.) Load the Trigger Select Register with 4 to indicate that the DIGIBUS transmission should start when TTL Trigger Line 2 is asserted.

5.) Load the Clock Select Register with zero to use the fastest DIGIBUS rate.

6.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 1024 - 1 (1023).

7.) Load the Output Samples Per Frame with the number of samples the V110 is to place in each frame of DIGIBUS data. For this example, the number is the same as for the Total Samples Per Frame, which is 1024 - 1 (1023).

8.) Load the Sample Starting Address with the first location that the V110 is to place data. Since the V110 is the only device asserting DIGIBUS data, this data should be set to zero.

9.) Load the Control/Status Register with 22 (16_{16}) to select the Multi-Hit Mode and enable the DIGIBUS output strobes.

10.) Execute a write operation with any data pattern to the Arm Transmission address to enable the V110 to be triggered.

11.) At this point, the V110 is ready to start transmitting DIGIBUS data as soon as the TTL Trigger Line 2 is asserted. The V110 will output 10 frames of data and then wait for a subsequent trigger. This continues until 500 triggers have occurred. The user program can either wait for the DONE bit in the Control/Status Register to be asserted or use the interrupt scheme with the DONE interrupt enabled to inform the host computer that the operation is complete.

Multi-Buffer DIGIBUS Transmit Example

As an example, assume it is desired to continually transmit DIGIBUS data at a rate of about 1Khz. This operation is executed as a multi-buffer operation and each DIGIBUS frame contains 1024 samples. The number of buffers the V110 is to use is four. The example assumes a 1000 frame buffer and is divided (segmented) into fourths, which will use four of the eight flag bits in the Multibuffer Flag Register. The following procedure can be followed to execute this operation.

1.) Load the segment of DIGIBUS data to be transmitted once the operation is initiated. The entire 4 segments may be loaded at this time but is not required. This example will assume that the entire buffer (4 segments) is loaded prior to enabling multibuffer operation. The number of DIGIBUS samples loaded for the entire buffer is 1000 frames * 1024 samples per frame yields 1024000 ($FA000_{16}$) samples.. This requires 512000 ($7D000_{16}$) longwords. The first longword loaded is at the base of the DRAM and subsequent longwords are written to incremental locations.

2.) Load the Buffer Total Frame Counter with the total number of frames to transmit before the buffer address should rollover back to zero minus one. The value for this example is 1000 - 1 (999).

3.) Load the Trigger Select Register with 0 to prevent any unnecessary trigger inputs.

4.) Load the Clock Select Register with 5000 (1388_{16}) to select a frame rate of about 1 Khz.

5.) Load the Total Samples Per Frame Register with the total samples per frame -1. The value for this example is 1024 - 1 (1023).

6.) Load the Output Samples Per Frame with the number of samples the V110 is to place in each frame of DIGIBUS data. For this example, the number is the same as for the Total Samples Per Frame, which is 1024 - 1 (1023).

7.) Load the Sample Starting Address with the first location that the V110 is to place data. Since the V110 is the only device asserting DIGIBUS data, this data should be set to zero.

8.) Load the Control/Status Register with 21 (15_{16}) to select the Multi-Buffer Mode and enable the DIGIBUS output strobes.

9.) Execute a write operation to the Multibuffer Flag Register to clear FLAGS 1 through 4 indicating that these segments contain valid DIGIBUS transmit data.

10.) To start DIGIBUS transmission, the V110 can be triggered by writing t the Trigger Transmission address with any data pattern. The V110 does not need to be armed for multibuffer modes. The V110 is automatically armed when the mode is selected.

11.) At this point, the V110 is transmitting DIGIBUS data. The host computer must now supply additional write data to the DRAM buffer for DIGIBUS transmission. The host computer can use either the Frame Interval interrupt or poll the Multibuffer Flag Register to determine when additional write data is required. For this example, assume the polling technique is used.

First, poll the Multibuffer Flag Register (FLAG) until the first flag is read back as a zero. The V110 sets this bit to a one once the first segment of data has been transmitted onto DIGIBUS. Once this flag is read as one, the host computer must reload the first segment with additional transmit data. For this example, the host must load 250 frames of additional data. This corresponds to 256000 ($3E800_{16}$) samples, or 128000 ($1F400_{16}$) longwords. Once the data has been stored in the buffer, a write operation must be executed to the Multibuffer Flag Register to clear the first flag to indicate not empty. The host may then return to polling the FLAG register until the second flag is read as empty. This sequence continues until the fourth flag is serviced and then flag 1 is again polled. The operation is stopped by writing a zero into the Control/Status Register which sets the V110 back to the idle state.

Front Panel LEDs and Connectors

The front-panel of the V110 contains six LEDs and four SMB connectors. The LEDs reflect various status signals of the V110. Two of the SMBs are used to trigger the V110 to start transmitting data. The other two SMBs are outputs of the V110 and are sourced when the Post Trigger Counter expires.

The SYSFAIL LED is illuminated while the V110 is executing its power-on self-test and will remain illuminated if the power-on self-test fails. While this LED is on, the V110 is asserting the VMEbus signal SYSFAIL (as long as the SYSFAIL INHIBIT bit in the Status/Control Register is configuration space is false). If this LED is on for more than 5 seconds, the V110 has failed the self-test and must be returned for repair.

The ADDRESS RECEIVED LED is a one-shot extended LED that is illuminated when the V110 is addressed in either A16 and A32 address space.

The INTERRUPT SOURCE LED is illuminated as long as the V110 has an interrupt request pending.

The DIGIBUS BUSY LED is illuminated whenever DIGIBUS activity is occurring. When the LED is off, the DIGIBUS is idle.

The BUSY LED is illuminated after the V110 has been armed and the DONE bit in the Control/Status Register of the operational register set is cleared.

The ARMED LED is illuminated when the V110 has been armed to transmit DIGIBUS data but has not received a trigger.

The V110 contains four SMB type connectors used to pass TTL level signals to/from the V110. The TRIGGER IN B and TRIGGER IN A SMB's are used as a hardware trigger mechanisms to initiate DIGIBUS data transmission. These two signals are independently enable through the Trigger Select Register. These two input signals are low true and must have a minimum pulse duration of 500 nanoseconds. These inputs are received by an 74LS14 gate and are terminated with a 180 ohm resistor to +5 volts and a 390 ohm resistor to ground.

The remaining two SMB connections are used as trigger out's from the V110. These two connections have a 200 nanosecond low true TTL level pulse applied to them when the Post Trigger Frame Counter is decremented to zero. The outputs are driven by an 74F38 open-collector driver and have a 4700 ohm pullup to +5 volts. These two signals are independently enabled through the Trigger Select Register.

DRAM Buffer Memory

The DRAM Buffer Memory is located at different offsets from the base address of the operational register depending on the amount of DRAM the V110 contains. The following shows the offset from the base address for the various options.

0400000 - 07FFFFF	DRAM Range for 4 Megabyte Option
0800000 - 0FFFFFF	DRAM Range for 8 Megabyte Option
1000000 - 1FFFFFF	DRAM Range for 16 Megabyte Option
2000000 - 3FFFFFF	DRAM Range for 32 Megabyte Option
4000000 - 7FFFFFF	DRAM Range for 64 Megabyte Option
8000000 - FFFFFFF	DRAM Range for 128 Megabyte Option

The DRAM is used to hold data prior to DIGIBUS transmission. This memory can be accessed as longwords (32-bits) or shortwords (16-bits). The DIGIBUS sample storage in memory is shown in the following diagram using a 32-bit format. Notice that the first sample transmitted below is located in the lower 16-bits of the memory and has VME address bit A1 set to 1.

Memory Offset	High 16 Data Bits	Low 16 Data Bits
0_{16}	Frame #1 Sample #2	Frame #1 Sample #1
4_{16}	Frame #1 Sample #4	Frame #1 Sample #3
8_{16}	Frame #1 Sample #6	Frame #1 Sample #5
C_{16}	Frame #2 Sample #2	Frame #2 Sample #1
10_{16}	Frame #2 Sample #4	Frame #2 Sample #3
14_{16}	Frame #2 Sample #6	Frame #2 Sample #5

The following diagram shows the same memory buffer except it is shown in a 16-bit format.

Memory Offset	Shortword Data
0_{16}	Frame #1 Sample #2
2_{16}	Frame #1 Sample #1
4_{16}	Frame #1 Sample #4
6_{16}	Frame #1 Sample #3
8_{16}	Frame #1 Sample #6
A_{16}	Frame #1 Sample #5
C_{16}	Frame #2 Sample #2
E_{16}	Frame #2 Sample #1
10_{16}	Frame #2 Sample #4
12_{16}	Frame #2 Sample #3
14_{16}	Frame #2 Sample #6
16_{16}	Frame #2 Sample #5

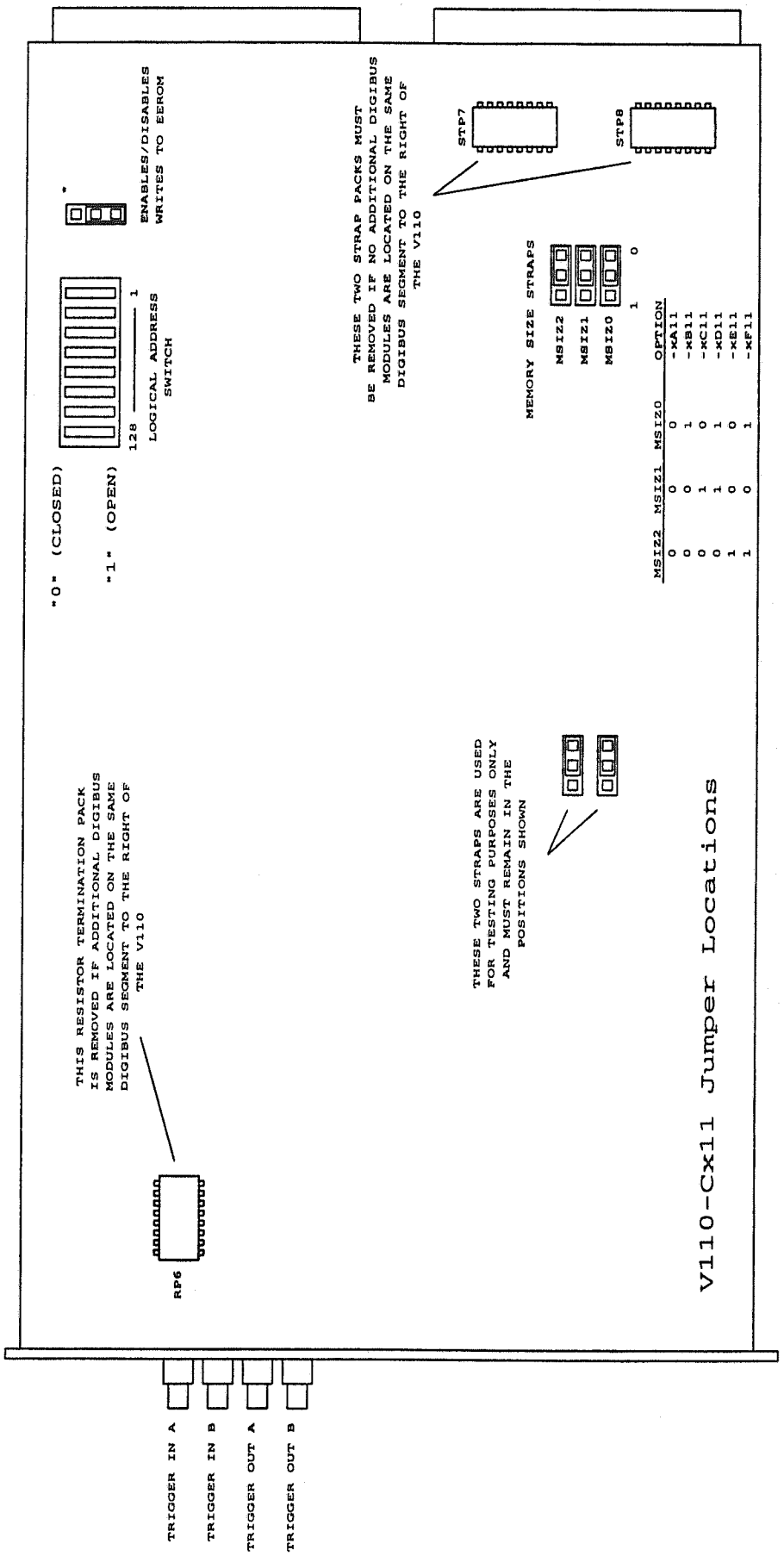
Strap Selection Options

The only strap selections made on the V110 concerns the configuration of the DIGIBUS. Two dual inline jumper packs are used to route the DIGIBUS IN to the DIGIBUS OUT on the VXI P2 connector. Since the V110 is a DIGIBUS source device, data is transmitted from the V110 towards the left side of the chassis. If a DIGIBUS data source is to reside on the same segment as the V110 and is located to the right hand side of the V110, the jumper packs are left installed. If there are no other DIGIBUS sources on the right hand side of the V110, the two jumper packs should be removed to prevent inadvertently inserting a module next to the V110 that uses the local bus signals. These two strap jumper packs are labeled STP7 and STP8. The location of these jumper packs can be found in the diagram following this section.

The DIGIBUS is terminated on both ends of a segment by a termination network. This network consists of a 180 ohm resistor to +5 volts and a 390 ohm resistor to ground. The first and last DIGIBUS module of a segment contain this termination. The V110 has a socketed 16 pin dual inline package that holds the resistor terminator. If no other DIGIBUS modules reside on the DIGIBUS segment to the right side of the V110, the resistor terminator must be left installed. The resistor network is removed of the V110 additional DIGIBUS source modules reside to the right of the V110 on the same segment. The location of this resistor terminator is shown in the diagram following this section.

Several other strap selections can be found on the V110. These straps are used during testing of the V110 and should not be altered from their factory configuration. The following diagram shows all the strap and jumpers on the V110 along with an indication of their default positions.

Figure 1 - V110-Cx11 Jumper Locations



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5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com