Installation and Setup

The Model V15X-AA11 is shipped in an anti-static bag with a styrofoam packing container. Carefully remove the module from its anti-static bag and prepare to set the various options to conform to the operating environment. Make sure that all anti-static precautions are taken to avoid damaging the module.

For an initial test the V15X-AA11 and the VME Single Board Computer (SBC) may be plugged together without any modification needed.

The following chart shows the strap/switch selections along with their default configurations. If any of the user requirements vary from the default configuration, consult the following sections for changing the parameter. Please refer to Appendix A of this manual for the location of the straps and switches on the V15X-AA11.

Selectable Parameter	**Default Value**
Slot0/Non-Slot0 Configuration	Slot 0 Configuration
Logical Address	0
System Controller	Enabled

Slot0 Configuration

The V15X-AA11 may be configured as a Slot0 controller or as a non-Slot0 controller. The V15X-AA11 is shipped from the factory as a Slot0 controller. Several strap and switch setting must be set to enable the V15X-AA11 Slot0 functionality. Refer to the SBC manual for enabling the System Controller.

The V15X-AA11 must first be setup as system controller to assume the responsibilities of a Slot0 controller. A switch setting on the V15X-AA11 must be set. The switch on the V15X-AA11 is labeled SW2 and the switch location of interest is position 1. This switch must be placed in the OPEN (1) position to allow the V15X-AA11 to function as a Slot0 controller. This switch controls the direction of the VXI*bus* signals SYSCLK and BCLR. If the V15X-AA11 adapter is configured as a system controller, the must also be configured the same way.

The next selection to be made concerns the VXI*bus* MODID (Module ID) signal and an internal signal on the V15X-AA11 indicating Slot0 operation. These selections are made via three of the switch positions of switch SW2. Position 2 controls the internal indication for Slot0 operation. This switch must be set to the OPEN (1) position for Slot0 operation. Position 3 of switch SW2 controls the MODID signal 825 ohm pulldown resistor. When the V15X-AA11 is in a Slot0 position, this switch must be set to the OPEN (1) position to disconnect the resistor from the MODID signal since this resistor is provided on the VXI chassis backplane for the Slot0 position.

Position 4 of switch SW2 controls the connection of the 16.8Kohm pullup resistor to the MODID signal. When the V15X-AA11 is configured as a Slot0 device, this switch position must be CLOSED (0) to allow the MODID signal to be terminated with the pull-up resistor

The remaining setup of the V15X-AA11 adapter concerns the VXI*bus* signal CLK10. The CLK10 signal is a 10 Megahertz timing clock generated by the Slot0 controller. A differential ECL driver drives this signal onto the VXIbus. A set of straps on the V15X-AA11 adapter controls whether this signal is sourced onto VXI by the internal clock of the V15X-AA11 or not sourced by the V15X-AA11. To alter the selection, two straps must be moved. The V15X-AA11 is configured at the factory to source the CLK10 signal from the internal clock. This is enabled by placing the two CLK10 straps into the INTERNAL position. You need to enable this for Slot0 operation.

This concludes the configuration of the V15X-AA11 adapter for Slot0 operation. The SBC must also be configured to operate as a system controller. Please refer to the SBC manual for strap/switch locations along with a description of changing operating parameters.

Non-Slot0 Configuration

To setup the V15X-AA11 as a non-Slot0 device, the module must first be disabled from being the system controller. The system controller function is usually an operation provided by a Slot0 controller. A switch setting on the V15X-AA11 must be set. The switch on the V15X-AA11 is labeled SW2 and the switch location of interest is position 1. This switch must be placed in the CLOSED (0) position to allow the V15X-AA11 to function as a non-Slot0 device. This switch controls the direction of the VXI*bus* signals SYSCLK and BCLR. Setting this switch to the CLOSED (0) position enables the V15X-AA11 to receive the SYSCLK and BCLR signals for non-Slot0 applications. If the V15X-AA11 adapter is not configured as a system controller, the SBC must also be configured the same way.

The next selections to be made concerns the VXI*bus* MODID (Module ID) signal and an internal signal on the V15X-AA11 indicating Slot0 operation. These selections are made via three of the switch positions of switch SW2. Position 2 controls the internal indication for Slot0 operation. This switch must be set to the CLOSED (0) position for non-Slot0 operation. Position 3 of switch SW2 controls the MODID signal 825 ohm pulldown resistor. If the V15X-AA11 is to operate in a non-Slot0 configuration, this switch must be set to the CLOSED (0) position allowing the pulldown resistor to connect to the MODID signal.

Position 4 of switch SW2 controls the connection of the 16.8Kohm pull-up resistor to the MODID signal. When the V15X-AA11 is to be used in a non-Slot0 configuration, this switch position must be set to the OPEN (1) position to disconnect the pull-up resistor from the MODID signal.

The remaining setup of the V15X-AA11 adapter concerns the VXI*bus* signal CLK10. The CLK10 signal is a 10 Megahertz timing clock generated by the Slot0 controller. A set of straps on the V15X-AA11 adapter controls whether this signal is sourced onto VXI by the internal clock of the V15X-AA11 or not sourced by the V15X-AA11. To alter the selection, two straps must be moved. The V15X-AA11 is configured at the factory to source the CLK10 signal from the internal clock. To disable driving CLK10, place the two CLK10 straps into the NC position. This concludes the configuration of the V15X-AA11 adapter for non-Slot0 operation. The SBC

must also be configured to disable the system controller portion of the SBC. Please refer to the SBC manual for strap/switch locations along with a description of changing operating parameters.

Logical Address

The V15X-AA11 may be configured to operate as either a Slot0 controller or a non-Slot0 controller. When the V15X-AA11 is the Slot0 controller, it must be located in the left-most slot (Slot0) and be set for Logical Address 0. If the V15X-AA11 is not the Slot0 controller, it may be located in any other slot in the chassis and set for Logical Address 1 through 255. To statically assign a Logical Address to the V15X-AA11, simply set the 8-position DIP switch to the desired Logical Address in the range of 1 through 254. This sets the Logical Address of the V15X-AA11 and may only be altered by changing the setting on the DIP switch.

The V15X-AA11 may also be Dynamically Configured. A device that is Dynamically Configured must have its Logical Address set to 255 (FF_{16}). A device that is Dynamically Configured has its Logical Address set by the Resource Manager when the Logical Address Register of the V15X-AA11 is written. Dynamic Configuration is used to avoid conflicts in setting up a devices' Logical Addresses. The Resource Manager makes use of the feature of the VXI*bus* to address the various devices set at Logical Addresses of 255. This is accomplished by using the MODID (Module Identification) signal, which provides a geographic addressing mechanism to each individual slot location. A normal A16 address space transfer cycle is executed to a device with its MODID signal asserted. This differentiates one device at Logical Address 255 from another. After the device is addressed geographically, it is written with a new Logical Address number assigned by the Resource Manager. Dynamic Configuration eliminates the need to preassign Logical Addresses in a VXI chassis, as long as they are all set to 255 and allocated by the Resource Manager.

The V15X-AA11 contains a set of 8 DIP switches used to set the Logical Address. These switches represent a binary combination of numbers in the range of 0 to 255. The switch settings are made by depressing each Logical Address switch to the desired location. A switch that is in the OPEN position yields a bit set to a one. A switch that is in the CLOSED position yields a bit set to a zero. The left-most switch corresponds to Logical Address bit 128 and the right-most switch corresponds to Logical Address bit 1. Please refer to Appendix A for the location and setting of the Logical Address switches. The following diagram shows the bit pattern for the A16 Logical Base Address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0

Bits 15 and 14 are set to one (VXI defined).
Bits 13 through 6 are user selectable using the Logical Address switches LA128 - LA1.
Bits 5 though 0 are set to 0 to indicate the beginning of a 64 byte block.

For statically configured devices, the setting of the Logical Address switches locks the devices' Configuration Registers in A16 address space. Each device has an allocated configuration

address space of 64 bytes. The Logical Base Address of a device in A16 address space may then be calculated using the following equation:

A16 Base Address = 0xC000 + (Logical Address shifted left 6 places)

For example, the A16 Base Address of a device set for Logical Address 2 is 0xC080. For a device set to Logical Address 2, the following bit pattern is established for the base address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

CLK10 Signal Generation

The VXI*bus* CLK10 signal is a 10 Megahertz differential ECL clock driven onto the bus by the Slot0 controller. If the V15X-AA11 is used as a Slot0 controller, it must be configured to drive this VXI*bus* signal. The signal source may be generated internally by the V15X-AA11.

A set of six straps, located near the P1/P2 connector for VXI, is used to configure the source of the CLK10 signal. This set of straps actually controls the 2 CLK10 signals, +CLK10 and -CLK10. When the straps are installed in the INT (INTERNAL) position, the CLK10 signals are driven by a clock source on the V15X-AA11. If the V15X-AA11 is to be located in a non-Slot0 position in the chassis, the CLK10 signals must be disabled from driving CLK10 by placing the 2 sets of straps into the NC (NO CONNECTION) position.

Installation

After all the user selectable configuration parameters have been setup, the module may then be inserted into the VXI chassis. If the V15X-AA11 is configured for Slot0 operation, insert the V15X-AA11 into the left-most slot (Slot0) of the VXI chassis. For a non-Slot0 configuration, insert the V15X-AA11 into any slot in the range of 1 through 13.

CAUTION:	**TURN OFF MAINFRAME POWER BEFORE INSERTING OR REMOVING A VXI*bus* MODULE.**

WARNING:	**REMEMBER TO REMOVE THE INTERRUPT ACKNOWLEDGE AND BUS GRANT DAISY CHAIN JUMPERS BEFORE INSERTING A VXI MODULE**

The VXI*bus* backplane must be properly configured before inserting a VXI module and applying power. The Interrupt Acknowledge jumper must be removed from the slot in which the VXI module is to be inserted. The Bus Grant jumpers must also be removed from the slot in which the VXI module is to be inserted. All unoccupied slot locations must have the Interrupt Acknowledge and Bus Grant jumpers installed so that the interrupt and grant continuity is not disrupted by any open slots. When using backplanes that auto-configure, these steps are not

necessary since the installation of a VXI module in the chassis makes the required configuration occur.

VXI*bus* Configuration Registers and Operational Registers

The following table shows the various registers located in A16 space for the V15X-AA11 Slot 0 Controller.

A16 Offset	Write Access	Read Access
00_{16}	Logical Address Register	Identification
02_{16}	Reserved	Device Type Register
04_{16}	Status/Control Register	Status/Control Register
06_{16}	Reserved	Reserved
08_{16}	Write Signal Register	Protocol Register
$0A_{16}$	Reserved	Response Register
$0C_{16}$	Reserved	Reserved
$0E_{16}$	Data Low Register	Data Low Register
10_{16}	Reserved	Reserved
12_{16}	Reserved	Reserved
14_{16}	Reserved	Reserved
16_{16}	Reserved	Reserved
18_{16}	Reserved	Reserved
$1A_{16}$	Reserved	Reserved
$1C_{16}$	Reserved	Reserved
$1E_{16}$	Reserved	Reserved
20_{16}	Reserved	Suffix High Register
22_{16}	Reserved	Suffix Low Register
24_{16}	Reserved	Serial Number High Register
26_{16}	Reserved	Serial Number Low Register
28_{16}	Module ID Register	Module ID Register
$2A_{16}$	Reserved	Interrupt Status Register
$2C_{16}$	Interrupt Control Register	Interrupt Control Register
$2E_{16}$	Trigger Interrupt Mask	Trigger Interrupt Source
30_{16}	Trigger Interrupt Source Clear	Reserved
32_{16}	Trigger Source Register	Reserved
34_{16}	Trigger Timer Configuration Register	Reserved
36_{16}	Reserved	Reserved
38_{16}	SBC Slave Mode Configuration	Reserved
$3A_{16}$	Location Monitor Interrupt Control Register	Interrupt Status ID Register
$3C_{16}$	Miscellaneous Control Register	Read Signal Register
$3E_{16}$	Reserved	Version Number Register

ID/Logical Address Register

The ID/Logical Address Register is a write/read register located at an offset of 00_{16} from the A16 Logical Base Address. A read operation to this register returns the Device Class, the addressing modes of the devices' operational registers and the Manufacturers' Identification. A

write operation to this register address is typically executed by the Resource Manager during a Dynamic Configuration allocation sequence. During the sequence, the Resource Manager allocates a Logical Address to the V15X-AA11 by writing a logical address value to the least significant eight bits of this register. The format and bit assignments of this register are shown in the following diagram. Since this register has write-only and read-only bits, two bit patterns are shown.

On read transactions: **00h**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	0	1	1	1	1	1	1	0	0	1	0	1	0	0	1
	Class = Extended		**Addressing Mode = A16**		**KineticSystems' Manufacturer ID = $F29_{16}$ (3881)**											

Bit(s) Mnemonic **Meaning**

15:14 Device Class — These bits are set to reflect the Device Class of the V15X-AA11. This bit combination indicates that the V15X-AA11 is a Message Based Device.

13:12 Address Space — These bits are set to reflect the addressing mode(s) of the V15X-AA11's operational registers. Since all the communication registers of the V15X-AA11 appear in A16 address space, the bits in this field are both set to one.

11:0 Manufacturer — This field reflects the manufacturer of a VXI device. This value is 3881($F29_{16}$) for KineticSystems.

On write transactions: **00h**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	**Not Used**								**Logical Address**							

Bit(s) **Mnemonic** **Meaning**

15:8 Not Used — These 8 bits are not used. A write operation to these bits has no effect on the V15X-AA11.

7:0 128-LA1 — Logical Address 128 through 1 are write-only bits used to set the V15X-AA11's Logical Address during a Dynamic Configuration cycle executed by the Resource Manager. A Dynamic Configuration sequence is performed on a VXI module when its logical address has been set to 255 (FF_{16}).

Device Type Register

The Device Type Register is a read-only register located at an offset of 02_{16} from the A16 Logical Base Address of the V15X-AA11. This register contains the Model Code of the V15X-AA11. Since the V15X-AA11 is an A16-only device, the entire 16-bits of this field is used for the Model Code.

Model Codes for VXI Slot0 devices must be in the range of 00_{16} to FF_{16}. Model Codes for non-Slot0 devices must be in the range of 100_{16} to $FFFF_{16}$. When the V15X-AA11 is configured for non-Slot0 operation, the Model Code returned in this register is 152_{16}. When the V15X-AA11 is configured for Slot0 operation, the 100_{16} bit is set to zero, yielding a Model Code of 52_{16}.

V15X-AA11 Model Codes:

152_{16} for non-Slot0 configurations
52_{16} for Slot0 configurations

The following diagram shows the bit pattern for the Device Type Register for both Slot0 and non-Slot0 configurations.

For Slot0 Configurations:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**

For non-Slot0 Configurations:

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**

Status/Control Register

The Status/Control Register is a write/read register located at an offset of 04_{16} from the A16 Logical Base Address of the V15X-AA11. This register contains write-only, read-only and write/read bits. This register is used to monitor the Module ID VXI signal, control the assertion of SYSFAIL, control Soft Reset, and check the status of the Power-On Self Test. The following two diagrams show the Status/Control Register, one for read accesses and one for write.

For read operations executed to the Status/Control Register:

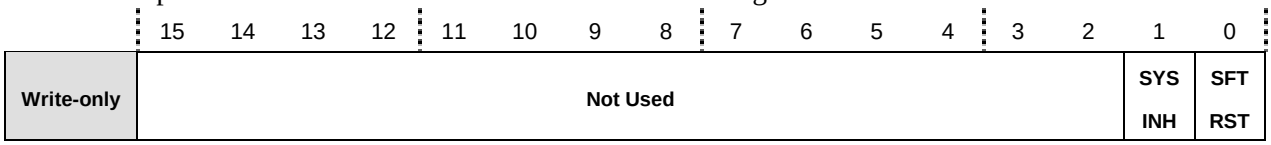
04h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Write	**0**	**MOD ID***	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**RDY**	**PASS**	**SYS INH**	**SFT RST**

Bit(s)	Mnemonic	Meaning
15	Not Used	This bit is not used and read as a zero.
14	MODID*	This bit is set to a one if the module is <u>not</u> selected with the MODID line on the VXI P2 connector. A zero indicates that the module is selected by the MODID signal.

Bit(s)	Mnemonic	Meaning
13:4	Not Used	These bits are not used and read as zeros.
3	READY	Ready is a read-only bit that is set to a one indicating successful completion of register initialization.
2	PASS	Pass is a read-only bit that is set to a one when the V15X-AA11 has completed its power-on self-test without any errors. If an error occurs, this bit is set to a zero and the SYSFAIL signal is asserted by the V15X-AA11.
1	SYS INH	SYSFAIL INHIBIT. Reading this bit as a one indicates that the V15X-AA11 is prevented from driving the backplane SYSFAIL line.
0	SFT RST	SFT RST This bit is read as a one when the V15X-AA11 has been placed into the Soft Reset state. Writing this register with this bit set to a zero removes the V15X-AA11 from the soft reset state.

For write operations executed to the Status/Control Register: **04h**



Bit(s)	Mnemonic	Meaning
15:2	Not Used	These bits are not used for write operations.
1	SYS INH	SYSFAIL INHIBIT is a write/read bit used to inhibit the V15X-AA11 from asserting the backplane signal SYSFAIL. Setting this bit to a one disables the assertion of SYSFAIL and a zero enables the signal.
0	SFT RST	SOFT RESET is a write/read bit used to reset the V15X-AA11. Setting this bit to a one places the V15X-AA11 in the soft reset state and writing the bit to a zero removes the V15X-AA11 from the reset state.

Protocol Register

The Protocol Register is a read-only register located at an offset of 08_{16} from the A16 Logical Base Address of the V15X-AA11. The Protocol Register is accessed by executing a read to this address location and the Signal Register is accessed by writing to this location. The Protocol Register is used to define the communication capabilities of the Message Based Device. The following diagram shows the bit layout of the Protocol Register of the V15X-AA11.

08h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	CMDR*	SGNL REG*	MSTR*	INTR	FHS*	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Meaning
15	CMDR*	COMMANDER is a read-only bit that is set to a one for a device that only capable of Message Based Servant functions. A zero in this bit location indicates that the device is capable of both Commander and Servant Message Based functions. The V15X-AA11 sets this bit to a zero indicating it has both Commander and Servant capability.
14	SGNL-REG*	SIGNAL REGISTER is a read-only bit that is set to a one for a device that does not contain a Signal Register. Devices that contain a Signal Register set this bit to a zero. Since the V15X-AA11 contains a functional Signal Register, this bit is set to a zero
13	MSTR*	MASTER is a read-only bit that is set to a one for devices that do not have VME*bus* mastering capability. A zero for this bit location indicates the device has the ability to become a VME*bus* master. The V15X-AA11 has VME*bus* mastering capability and sets this bit to a zero.
12	INTR	INTERRUPTER is a read-only bit that indicates whether the device can generate interrupts. A zero in this bit location indicates no interrupting ability and a one indicates that the device can generate interrupts. The V15X-AA11 can generate interrupts and sets this bit to a one.
11	FHS*FAST	HANDSHAKE is a read-only bit used to indicate whether a Message based devices' data register supports the Fast Handshake Mode. This bit is set to a one if Fast Handshake is not supported and a zero if Fast Handshake is supported. The V15X-AA11 does not support the Fast Handshake transfer mode and sets this bit to a one.
10	SHR MEM*	SHARED MEMORY is a read-only bit used to indicate if a device implements shared memory. A zero in this bit location indicates that shared memory is supported and a one indicates that it is not. The V15X-AA11 does contain some amount of shared memory, but it does not comply with the VXI specification for Shared Memory. Therefore, the V15X-AA11 sets this bit to a one.
9:0	Not Used	These bits are not used by the V15X-AA11 and returned as ones.

Write Signal Register

The Write Signal Register is a write-only register located at an offset of 08_{16} from the A16 Logical Base Address of the V15X-AA11. A write operation to this register address accesses the

Signal Register. This register is used for device to device signaling. This register can be read at offset $3C_{16}$ in A16 address space. A signal received from a device contains the devices' Logical Address along with a field for device specific information. There are two different formats for the Signal Register, depending on the value of the most significant bit (bit 15). The following two diagrams show the various formats.

08h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	**0**	**Response**							**Logical Address**							

08h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	**0**	**Event**							**Logical Address**							

The fields shown for the two Signal Register patterns are as follows:

Response: This field reflects bits 14 through 8 of the device's Response Register.
Event: This field reflects the event associated with the signal.
Logical Address: This field reflects the Logical Address of the device generating the signal.

Response Register

The Response Register is a read-only register located at an offset of $0A_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used to return the status of a device's communication registers and their associated functions. The following diagram shows the bit layout for the Response Register on the V15X-AA11.

0Ah

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	**0**	**1**	**0**	**0**	**ERR***	**READ RDY**	**WRT RDY**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Bit(s)	**Mnemonic**	**Meaning**
15	Not Used	This bit is not used and read as a zero.
14	Not Used	This bit is not used and read as a one.
13:12	Not Used	These two bits are not used by the V15X-AA11 and returned as zeros.
11	ERR	ERROR is a read-only bit used to signify when an error occurs in one of the serial protocols and has not yet been reported. This bit is set and cleared by using the Miscellaneous Control Register located at offset $3C_{16}$.

Bit(s)	Mnemonic	Meaning
10	READ RDY	READ READY is a read-only bit that is set to a one indicating that the device's Data Register(s) contain data to be read. This bit is set to a one by executing a write operation to the Miscellaneous Control Register with the SET READ READY bit set to a one. After the READ READY bit has been set, it is cleared when the Data Low Register is read.
9	WRT RDY	WRITE READY is a read-only bit that is set to a one indicating that the device is ready for data transfers to its Data Register(s). This bit is set to a one by executing a write to the Miscellaneous Control Register with the SET WRITE READY bit set to a one. After the Data Low Register is written, the WRITE READY bit is cleared.
8:0	Not Used	These bits are not used by the V15X-AA11 and read as ones.

Data Low Register

The Data Low Register is a write/read register located at an offset of $0E_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used communicate data between two Message Based Devices. Accessing this register causes the appropriate flags to be set/cleared in the Response Register. Please refer to the Response Register for additional information.

The following diagram shows the bit pattern for the Data Low Register.

0Eh

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Write	**0**	**MOD ID***	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**RDY**	**PASS**	**SYS INH**	**SFT RST**

Bit(s)	Mnemonic	Meaning
15:0	W/R15:0	WRITE/READ DATA 15 through 0 are write/read bits used to communicate data between two Message Based Devices.

Suffix High Register

The Suffix High Register is a read-only register located at an offset of 20_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used in combination with the Suffix Low Register to determine the module model number suffix. The Suffix High Register contains the first two ASCII characters of the suffix and the Suffix Low Register contains the last two characters. The suffix shown is for the V15X-AA11-AA11 module.

The bit pattern for the Suffix High Register is as follows:

20h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**

Suffix Low Register

The Module Suffix Low Register is a read-only register located at an offset of 22_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used in combination with the Suffix High Register to determine the module model number suffix. The Suffix Low Register contains the last two ASCII characters of the suffix and the Suffix High Register contains the first two characters. The suffix shown is for the V15X-AA11-AA11 module.

The bit pattern for the Suffix Low Register is as follows:

22h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**

Serial Number High Register

The Serial Number High Register is a read-only register located at an offset of 24_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used in conjunction with the Serial Number Low Register to define the serial number of the V15X-AA11. The following diagram shows the bit pattern of the Serial Number High Register.

24h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	**SN 31**	**SN 30**	**SN 29**	**SN 28**	**SN 27**	**SN 26**	**SN 25**	**SN 24**	**SN 23**	**SN 22**	**SN 21**	**SN 20**	**SN 19**	**SN 18**	**SN 17**	**SN 16**

Serial Number Low Register

The Serial Number Low Register is a read-only register located at an offset of 26_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used in conjunction with the Serial Number High Register to define the serial number of the V15X-AA11. The following diagram shows the bit pattern of the Serial Number Low Register.

26h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	**SN 15**	**SN 14**	**SN 13**	**SN 12**	**SN 11**	**SN 10**	**SN 9**	**SN 8**	**SN 7**	**SN 6**	**SN 5**	**SN 4**	**SN 3**	**SN 2**	**SN 1**	**SN 0**

Module ID Register

The Module ID Register is a write/read register located at an offset of 28_{16} from the A16 Logical Base Address of the V15X-AA11. This register is only available when the V15X-AA11 is configured as a Slot0 device. The Module ID Register is used to control the MODID geographic addressing lines on the VXI P2 connector. Each of the 13 slots of a VXI chassis has an

individual line that can be asserted and monitored through the Module ID Register. Before any of the MODID lines can be asserted by the V15X-AA11, the Output Enable bit (bit 13) of this register must be set to a one. When the outputs are enabled, setting a MODID bit location to a one asserts the corresponding MODID signal.

The data read from this register does not necessarily reflect the data written. Instead, a read of this register returns the actual state of the MODID signals on the VXI backplane.

The following diagram shows the bit pattern for the Module ID Register.

28h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Write	**0**	**0**	**MID ENA**	**MID 12**	**MID 11**	**MID 10**	**MID 9**	**MID 8**	**MID 7**	**MID 6**	**MID 5**	**MID 4**	**MID 3**	**MID 2**	**MID 1**	**MID 0**

Bit(s)	**Mnemonic**	**Meaning**
15:14	Not Used	These bits are not used and read as ones.
13	MID ENA	MODID OUTPUT ENABLE is a write/read bit used to enable/disable the V15X-AA11 from driving the MODID signals. Setting this bit to a one enables the drivers and a zero disables them.
12:0	MID12:0	MODULE ID 12 through 0 is write/read bits used to assert and monitor the 13 MODID signals. Writing a bit to a one asserts the corresponding module's MODID signal.

Interrupt Status Register

The Interrupt Status Register is a read-only register located at an offset of $2A_{16}$ from the A16 Logical Base Address of the V15X-AA11. The contents of this register are enabled onto the VME*bus* during an interrupt acknowledge cycle. This register contains the Logical Address of the V15X-AA11 in the lower 8-bits of the register and the upper 8-bits contains the cause/status of the interrupt. The lower 8-bits of this register return the Logical Address of the V15X-AA11 only for interrupt acknowledges cycles. An I/O read of this field returns all 8-bits set to ones.

The V15X-AA11 has two interrupt sources. One of the sources is from a preselected VXI Trigger input and the other source is from Location Monitors. The VXI interrupt sources are enabled through the Trigger Interrupt Mask Register located at offset $2E_{16}$. The Location Monitor interrupt sources are enabled through the Location Monitor Interrupt Control Register located at an offset of $3A_{16}$. These two registers must be appropriately enabled before the V15X-AA11 can generate an interrupt source. The interrupt source(s) may then generate a VXI interrupt request when interrupts are enabled in the Interrupt Control Register located at an offset of $2C_{16}$.

The interrupt acknowledges cycle executed by the Interrupt Handler reads a 16-bit value from the V15X-AA11. The lower 8-bits of this data reflects the Logical Address of the device generating the interrupt. The upper 8-bits reflects the cause of the interrupt. Of the upper 8-bits, only 2 of them are used by the V15X-AA11. Once an interrupt acknowledges cycle occurs, the interrupt source bits that were set in this register when the interrupt vector was read are reset to zero. This will also occur when the Interrupt Status Register is read.

The format of the Interrupt Status Register is as follows:

2Ah

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	**0**	**0**	**0**	**0**	**0**	**0**	**LOC MON**	**TRG IN**	**LA 128**	**LA 64**	**LA 32**	**LA 16**	**LA 8**	**LA 4**	**LA 2**	**LA 1**

Bit(s)	**Mnemonic**	**Meaning**
15:10	Not Used	These bits are not used and read as zeros.
9	LOC MON	LOCATION MONITOR INTERRUPT SOURCE is a read-and-clear bit that is set when an interrupt source is generated by one of the Location Monitor Interrupts enabled in the Location Monitor Interrupt Control Register. To find out the actual cause of the location monitor interrupt, the Location Monitor Interrupt Control Register must be consulted.
8	TRG IN	TRIGGER IN INTERRUPT SOURCE is a read-and-clear bit that is set when an interrupt source is generated by one of the enabled trigger input interrupt sources in the Trigger Interrupt Mask Register. To find out the actual cause of the trigger input interrupt, the Trigger Interrupt Source Register must be consulted.
7:0	LA128:1	LOGICAL ADDRESS 128 through 1 return the Logical Address of the V15X-AA11 during an interrupt acknowledge cycle to the V15X-AA11. An I/O read of these bits return all ones.

Interrupt Control Register

The Interrupt Control Register is a write/read register located at an offset $2C_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used to configure the V15X-AA11 for interrupt sourcing. The Interrupt Request Level, Interrupt Enable, and Interrupt Source Mask are contained in this register.

The format and description of the Interrupt Control Register are shown in the following diagram.

2Ch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Read-Write	1	1	1	1	1	1	LOC MON*	TRG IN*	IR ENA*	1	IRQ S3	ORQ S2	IRQ S1	1	1	1

Bit(s)	Mnemonic	Meaning
5:10	Not Used	These bits are not used and read as ones.
9	LOC MON*	LOCATION MONITOR INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of a VXI interrupt when one of the Location Monitor interrupt sources are enabled in the Location Monitor Interrupt Control Register. Setting this bit to a one disables the Location Monitor interrupts and a zero enables the interrupt.
8	TRG IN*	TRIGGER IN INTERRUPT ENABLE is a write/read bit used to enable and disable the generation of a VXI interrupt when one of the enabled interrupt sources in the Trigger Interrupt Mask is generated. Setting this bit to a one disables the interrupts and a zero enables the interrupt.
7	IR ENA*	INTERRUPT REQUEST ENABLE is a write/read bit used to enable/disable the V15X-AA11 from generating an interrupt request to the VME*bus*. Setting this bit to a one disables the V15X-AA11 from generating an interrupt request and a zero enables the interrupt request.
6	Not Used	This bit is not used and read as a one.
5:3	IRQS3:1	INTERRUPT REQUEST SELECT 3 through 1 are write/read bits used to select the desired interrupt request level that the V15X-AA11 asserts when an interrupt is sourced.

The following chart shows the interrupt request level selections.

IRQ S3	IRQ S2	IRQ S1	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

2:0	Not Used	These bits are not used and read as ones.

Trigger Interrupt Mask/Trigger Interrupt Source Register

The Trigger Interrupt Mask/Trigger Interrupt Source Register is located at an offset of $2E_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register serves two purposes, depending on the direction of the transfer. A write operation to this register address accesses the Trigger Interrupt Mask Register. This register is used to enable and disable interrupts to the VXI bus on the occurrence of a trigger condition. Trigger conditions include the 8 VXI TTL Trigger lines, the two ECL VXI Trigger lines. A mask bit is set to a one to enable the interrupt source and set to a zero to disable the source.

The second register at this address is the Trigger Interrupt Source Register. This read-only register is used to determine which trigger event caused the interrupt source. Each bit read as a one was involved in generating the trigger interrupt source. After an interrupt has been generated and acknowledged, the Trigger Interrupt Source Clear Register must be written with data to clear the individual interrupt source.

The following two diagrams show the two registers.

Trigger Interrupt Mask Register (Write-Only):

2Eh

	15	14	13	12	9	8	7	6	5	4	3	2	1	0
Write-Only	**Not Used**				**ECL TG1**	**ECL TG0**	**TTL TG7**	**TTL TG6**	**TTL TG5**	**TTL TG4**	**TTL TG3**	**TTL TG2**	**TTL TG1**	**TTL TG0**

Bit(s)	**Mnemonic**	**Meaning**
15:12	Not Used	These bits are not used and setting them to ones does not have any effect on the V15X-AA11.
9:8	ECL TG1:0	ECL TRIGGER 1 and 0 are write-only bits used to enable the generation of a VXI interrupt when the corresponding VXI ECL Trigger line is asserted. A bit set to a one enables the interrupt source and a zero disables the interrupt source.
7:0	TTL TG1:0	TTL TRIGGER 7 and 0 are write-only bits used to enable the generation of a VXI interrupt when the corresponding VXI TTL Trigger line is asserted. A bit set to a one enables the interrupt source and a zero disables the interrupt source.

Trigger Interrupt Source Register (read-only):

2Eh

	15	14	13	12	9	8	7	6	5	4	3	2	1	0
Read-Only	**0**	**0**	**0**	**0**	**ECL TG1**	**ECL TG0**	**TTL TG7**	**TTL TG6**	**TTL TG5**	**TTL TG4**	**TTL TG3**	**TTL TG2**	**TTL TG1**	**TTL TG0**

Bit(s)	**Mnemonic**	**Meaning**
15:12	Not Used	These bits are not used and read as zeros.
9:8	ECL TG1:0	ECL TRIGGER INTERRUPT 1 and 0 are read-only bits that

Bit(s)	Mnemonic	Meaning
		are read as a one when the V15X-AA11 has received the assertion of the corresponding VXI ECL Trigger line and the Interrupt Mask bit was enabled. Reading this bit as a zero indicates that the ECL Trigger line is not generating an interrupt source.
9:8	TTL TG7:0	TTL TRIGGER INTERRUPT 7 through 0 are read-only bits that are read as a one when the V15X-AA11 has received the assertion of the corresponding VXI TTL Trigger line and the Interrupt Mask bit was enabled. Reading this bit as a zero indicates that the TTL Trigger line is not generating an interrupt source.

Trigger Interrupt Source Clear Register

The Trigger Interrupt Source Cleat Register is a write-only register located at an offset of 30_{16} from the A16 Logical base Address of the V15X-AA11. This register is used to clear the Interrupt Source bits in the Trigger Interrupt Source Register once they have been set by the receipt of a preselected trigger input. Any bit location set to a one when writing to this register clears the corresponding Interrupt Source bit. Any bit set to a zero has not effect on the Interrupt Source. The following diagram shows the bit layout for the Trigger Interrupt Source Clear Register.

30h

	15	14	13	12	10	9	8	7	6	5	4	3	2	1	0
Write-Only	Not Used				Not Used	ECL TG1	ECL TG0	TTL TG7	TTL TG6	TTL TG5	TTL TG4	TTL TG3	TTL TG2	TTL TG1	TTL TG0

Bit(s)	Mnemonic	Meaning
15:12	Not Used	These bits are not used. Any write to these bit locations have no effect on the V15X-AA11.
9:8	ECL TG1:0	CLEAR ECL TRIGGER INTERRUPT SOURCE 1 and 0 are write-only bits used to clear the corresponding ECL trigger interrupt source once set by the assertion of the signal.
7:0	TTL TG7:0	CLEAR TTL TRIGGER INTERRUPT SOURCE 7 through 0 are write-only bits used to clear the corresponding TTL trigger interrupt source once set by the assertion of the signal.

Trigger Source Register

The Trigger Source Register is a write-only register located at an offset of 32_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used to source the VXI ECL, VXI TTL. This register allows the trigger signals to be either asserted, negated or pulsed. The binary combination of bits 15 and 14 of this register determine what action is to be taken on

the selected trigger signals. The following chart shows the binary combination of the control bits and the effect they have on the selected trigger signals.

CNTL1	CNTL0	Effect On Trigger Signal
0	0	Assertion
0	1	Negation
1	0	Pulse
1	1	Reserved

When a trigger is asserted through the Trigger Source Register, it remains asserted until either a reset condition occurs or the Trigger Source Register is written to negate the trigger signal. A pulsed output lasts for approximately 1.5 microseconds.

The following diagram shows the bit pattern for the Trigger Source Register.

32h

	15	14	13	12	9	8	7	6	5	4	3	2	1	0
Write-Only	CNTL 1		Not Used		ECL TG1	ECL TG0	TTL TG7	TTL TG6	TTL TG5	TTL TG4	TTL TG3	TTL TG2	TTL TG1	TTL TG0

Bit(s)	Mnemonic	Meaning
15:14	CNTL1:0	CONTROL 1 and 0 are write-only bits used to define the operation to be performed on the requested trigger signal. The binary combination of these bits determine what action to take on the selected trigger signals. The previous chart shows the required binary combinations to set, clear and pulse the trigger signals.
13:12	Not Used	These bits are not used and may be written with any data pattern.
9:8	ECL TG1:0	ECL TRIGGER 1 and 0 are set to a one when writing to this register to allow the selected operation specified by the control bits to occur to the VXI ECL Trigger lines. Any trigger bit set to a zero when writing to this register has no effect on the trigger signal itself.
7:0	TTL TG7:0	TTL TRIGGER 7 through 0 are set to a one when writing to this register to allow the selected operation specified by the control bits to occur to the VXI TTL Trigger lines. Any trigger bit set to a zero when writing to this register has no effect on the trigger signal itself.

Trigger Timer Configuration Register

The Trigger Timer Configuration Register is a write-only register located at an offset of 34_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used to configure the timer interval and specify the trigger signals to assert once the Trigger Timer expires. The Trigger Timer, which is a 32-bit modulo-n type counter, can be tied to any or all of the trigger

signals. At a predetermined interval, the enabled trigger signals are pulsed for a period of approximately 1.5 microseconds.

The actual register accessed through this A16 address offset is determined by the four most significant bits of the Miscellaneous Control Register at offset $3C_{16}$. The binary combination of these four bits specify the register to be accessed as shown in the following table.

RSEL3	RSEL2	RSEL1	RSEL0	Register Accessed
0	0	0	0	Trigger Timer Low
0	0	0	1	Trigger Timer High
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Trigger Timer Control
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

A Trigger Timer is configured by first loading the Trigger Timer High Register and Trigger Timer Low Register. The Trigger Timer Low Register is used in conjunction with the Trigger Timer High Register for establishing the timer interval. This 32-bit counter is programmable from 2 microseconds to 429 seconds in 100 nanosecond increments. The data value loaded into the combination of the Trigger Timer Low and High Registers is the number of 100 nanosecond increments between trigger assertions. For example, to obtain an interval of 1 millisecond, the 32-bit timer must be loaded with data set to 10000 (2710_{16}). Therefore, the Trigger Timer High Register is loaded with 0 and the Trigger Timer Low Register is loaded with 10000 (2710_{16}).

The following diagram shows the bit pattern for the Trigger Timer High Register.

34h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-Only	TMR 31	TMR 30	TMR 29	TMR 28	TMR 27	TMR 26	TMR 25	TMR 24	TMR 23	TMR 22	TMR 21	TMR 20	TMR 19	TMR 18	TMR 17	TMR 16

Bit(s) Mnemonic Meaning

15:0 TMR31:16 TIMER DATA 31 through 16 are write-only bits used to establish the interval at which trigger signals are asserted. This register is used in combination with the Trigger Timer Low Register to determine the number of 100 nanosecond increments between trigger assertion.

The following diagram shows the bit pattern for the Trigger Timer Low Register.

34h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-Only	TMR 15	TMR 14	TMR 13	TMR 12	TMR 11	TMR 10	TMR 9	TMR 8	TMR 7	TMR 6	TMR 5	TMR 4	TMR 3	TMR 2	TMR 1	TMR 0

Bit(s) Mnemonic Meaning

15:0 TMR15:0 TIMER DATA 15 through 0 are write-only bits used to establish the interval at which trigger signals are asserted. This register is used in combination with the Trigger Timer High Register to determine the number of 100 nanoseconds increments between trigger assertion.

The Trigger Timer Control Register contains an enable bit that allows the timer to operate. This register also contains the 10 trigger source bits which determine the trigger signals to assert once the timer expires. Any trigger signal bit set to a one in this register is asserted once the timer expires. The following diagram shows the bit layout for the Trigger Timer Register.

34h

	15	14	13	12	9	8	7	6	5	4	3	2	1	0
Write-Only	TMR ENA	Not Used			ECL TG1	ECL TG0	TTL TG7	TTL TG6	TTL TG5	TTL TG4	TTL TG3	TTL TG2	TTL TG1	TTL TG0

Bit(s) Mnemonic Meaning

15 TMR ENA TIMER ENABLE is a write-only bit used to enable and disable the timer from operating. Setting this bit to a one enables the timer and a zero disables the timer.

14:12 Not Used These bits are not used and may be written with any data pattern.

9:8 ECL TG1:0 VXI ECL TRIGGER1 and 0 are write-only bits used to enable the assertion of the corresponding VXI ECL Trigger signal once the timer expires. A zero in a bit location prevents the signal from being asserted once the timer expires.

7:0 TTL TG7:0 VXI TTL TRIGGER7 through 0 are write-only bits used to enable the assertion of the corresponding VXI TTL Trigger signal once the timer expires. A zero in a bit location prevents the signal from being asserted once the timer expires.

SBC Slave Mode Enable Register

The SBC (Single Board Computer) Slave Mode Enable Register is a write-only register located at an offset of 38_{16} from the A16 Logical Base Address of the V15X-AA11. This register is used to enable accesses to the SBC slave mode functions.

Please refer to the SBC manual for additional information on enabling these accesses on the SBC.

This register provides access to setup and enable the VXI*bus* transfers to the SBC as a slave. There are three individual address specifications and enables to control the three address spaces. The binary combination of the most significant two bits of this register are used to select which address configuration is written. The following chart shows the address configuration selection.

CNTL1	CNTL0	Address Configuration Register
0	0	A32 Address
0	1	A24 Address
1	0	A16 Address
1	1	Reserved

The following diagrams show the bit patterns for the three Address Configuration Registers. The two most significant bits must be set as shown in the bit patterns to access the indicated register. The ENABLE bit in each of the registers is used to enable or disable the specified slave address space. Setting the bit to a one enables the address space and disabled by setting this bit to a zero. The address bit specifications for each register represent the VME address bits that are used during the compare to determine the address match for the selected address space.

The following diagram shows the bit pattern for the A32 Address Configuration Register.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-Only	**0**	**0**	**Not Used**					**ENA**	**A31**	**A30**	**A29**	**A28**	**A27**	**A26**	**A25**	**A24**

Location Monitor Interrupt Control Register

The Location Monitor Interrupt Control Register is a write/read register located at an offset of $3A_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used to enable/disable the generation of an interrupt to VXI when an access is made to the Message Based communication registers. This includes a write to the Signal Register, a write to the Data Register, a read from the Data Register, or a Message Based Device ERROR is encountered. This register contains an interrupt enable bit for each of the four sources along with four bits used to clear the interrupt source.

The following diagram shows the bit layout of the Location Monitor Interrupt Control Register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Read/Write	0	0	0	0	0	0	0	0	ERR	WRT DATA	RD DATA	WRT SGNL	ERR IE	WDAT IE	RDAT IE	WSGL IE

Bit(s)	Mnemonic	Meaning
15:8	Not Used	These bits are not used and read as zeros.
7	ERR	ERROR INTERRUPT SOURCE is a write/read bit which is used to read and to clear the interrupt source generated from an ERROR interrupt. Reading this bit as a one indicates an interrupt source is pending from this ERROR source. A write operation with this bit set to a one clears the interrupt source.
6	WRT DATA	WRITE DATA INTERRUPT SOURCE is a write/read bit used to read and to clear the interrupt source generated from writing to the Data Register during a Message Based device transaction. Reading this bit as a one indicates an interrupt source is pending from the Write Data Register source. A write operation with this bit set to a one clears the interrupt source.
5	RD DATA	READ DATA INTERRUPT SOURCE is a write/read bit used to read and to clear the interrupt source generated from reading the Data Register during a Message Based Device transaction. Reading this bit as a one indicates an interrupt source is pending from a Read Data Register source. A write operation with this bit set to a one clears the interrupt source.
4	WRT SGNL	SIGNAL INTERRUPT SOURCE is a write/read bit used to read and to clear the interrupt source generated from writing the Signal Register during a Message Based Device transaction. Reading this bit as a one indicates that an interrupt source is pending from a write to the Signal Register. A write operation with this bit set to a one causes the interrupt source to be cleared.
3	ERR IE	ERR INTERRUPT ENABLE is a write-only bit used to enable and disable the generation of an interrupt source when an error is encountered during a Message Based Device transaction. Setting this bit to a one enables the interrupt source and a zero disables the source.
2	WDAT IE	WRITE DATA INTERRUPT ENABLE is a write-only bit used to enable/disable the generation of an interrupt source when the Data Register is written during a Messaged Based Device transaction. Setting this bit to a one enables the interrupt source and a zero disables the source.
1	RDAT IE	READ DATA INTERRUPT ENABLE is a write-only bit used to enable/disable the generation of an interrupt source when the Data Register is read during a Message Based Device transaction. Setting this bit to a one enables the interrupt source and a zero disables the source.

0 SGNL IE WRITE SIGNAL INTERRUPT ENABLE is a write-only bit used to enable/disable the generation of an interrupt source when the Signal Register is written during a Message Based Device transaction. Setting this bit to a one enables the interrupt source and a zero disables the source.

Interrupt Status ID Register

The Interrupt Status ID Register is a read-only register located at an offset of $3A_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used to read the 16-bits of data received from the V15X-AA11 during an interrupt acknowledge cycle on the VXI*bus*. Since the SBC only supports an 8-bit interrupt vector, an external mechanism has been provided to latch the entire 16-bit of interrupt vector information. The following diagram shows the bit pattern for the Interrupt Status ID Register.

3Ah

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	**ISRC 7**	**ISRC 6**	**ISRC 5**	**ISRC 4**	**ISRC 3**	**ISRC 2**	**ISRC 1**	**ISRC 0**	**LA 128**	**LA 64**	**LA 32**	**LA 16**	**LS 8**	**LA 4**	**LA 2**	**LA 1**

Bit(s) Mnemonic Meaning

15:8 ISRC7:0 INTERRUPT SOURCE 7 through 0 are read-only bits which reflect the interrupt source bits set by then interrupting VXI module during the interrupt acknowledge cycle.

7:0 LA128:1 LOGICAL ADDRESS 128 through 1 is read-only bits used to determine the Logical Address of the interrupting VXI module.

Miscellaneous Control Register

The Miscellaneous Control Register is a write-only register located at an offset of $3C_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is used to set and clear the ERR bit in the Response Register of the V15X-AA11, to set the WRITE READY and READ READY bits in the Response Register, and to control which buried register is accessed through the Trigger Timer Configuration Register address. The following diagram shows the bit pattern for the Miscellaneous Control Register.

3Ah

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-Only	**RESL 3**	**RESL 2**	**RESL 1**	**RESL 0**	**MFG BIT**	**Not Used**							**SET WRDY**	**SET RRDY**	**SET ERR**	**CLR ERR**

Bit(s) Mnemonic Meaning

15:12. RSEL3:0 REGISTER SELECT3 through 0 are write-only bits used to specify which buried register is to be accessed when writing to the Trigger Timer Configuration Register as shown in the following table.

RSEL3	RSEL2	RSEL1	RSEL0	Register Accessed
0	0	0	0	Trigger Timer Low
0	0	0	1	Trigger Timer High
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Trigger Timer Control
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

11 MFG BIT MANUFACTURING BIT is write-only bit used to test the V15X-AA11 during the manufacturing process. This bit must be set to a zero when writing to this register.

10:4 Not Used These bits are not used and must be set to zeros.

3 SET WRDY SET WRITE READY is a write-only bit used to set the WRITE READY bit in the Response Register to a one.

2 SET RRDY SET READ READY is a write-only bit used to set the READ READY bit in the Response Register to a one.

1 SET ERR SET ERROR is a write-only bit used to set the ERROR bit in the Response Register to a one.

0 CLR ERR CLEAR ERROR is a write-only bit used to clear the ERROR bit in the Response Register to a zero.

Read Signal Register

The Read Signal Register is a read-only register located at an offset of $3C_{16}$ from the A16 Logical Base Address of the V15X-AA11. A write operation to the Signal Register is addressed to offset 08_{16}. This register is used for device to device signaling for message based devices. A signal received from a device contains the devices' Logical Address along with a field for device

specific information. There are two different formats for the Signal Register, depending on the value of the most significant bit (bit 15). The following two diagrams show the various formats.

3Ch

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	0	Response							Logical Address							

3Ch

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	0	Event							Logical Address							

The fields shown for the two Signal Register patterns are as follows:

Response: This field reflects bits 14 through 8 of the device's Response Register.

Event: This field reflects the event associated with the signal.

Logical Address: This field reflects the Logical Address of the device generating the signal.

Version Number Register

The Version Number Register is a read-only register located at an offset of $3E_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register is read to determine the revision number of the V15X-AA11's firmware and hardware. The initial revision of the V15X-AA11 has a firmware revision level of 1.0 and a hardware version of 1.0. The following two diagrams show the various fields of the Version Number Register along with a bit pattern for the initial version.

3Eh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Firmware Main Version Number				Firmware Minor Version Number				Hardware Major Version Number				Hardware Minor Version Number			

3Eh

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-Only	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Mnemonic	Meaning
15:12	Firmware Main Version	These bits reflect the main version number of the firmware.
11:8	Firmware Minor Version	These bits reflect the minor version number of the firmware.

7:4	Hardware Main Version	These bits reflect the main version number of the hardware.
3:0	Hardware Minor Version	These bits reflect the minor version number of the hardware.

VXI Transfers

This section of the manual provides basic information on executing VXI*bus* transfers using the Motorola PowerPC750 Single Board Computer (SBC), as an example. For a complete description of VXI*bus* transfers, please refer to the SBC manual.

VXI*bus* addresses are mapped directly into the Motorola processors address space. A transfer to a range of processor addresses causes a VXI*bus* transfer to be executed. The processor addresses that correspond to the various address spaces can be found in the following chart.

Processor Address Range	VXI/VME Address Range	Address Space
$FBff0000_{16}$ - $FBFFFFFF_{16}$	VME Short Address 0000_{16} - $FFFF_{16}$	A16
	VME Standard Address 000000_{16} - $FFFFFF_{16}$	A24
$FA000000_{16}$ - $FAFFFFFF_{16}$		
10000000_{16} - $17FFFFFF_{16}$	VME Extended Address $0800\ 0000_{16}$ - $FFFFFFF_{16}$	A32

The complete A16 and A24 addressing range are supported by the V15X-AA11. The A32 addressing range is limited due to the amount of memory that the SBC contains.

The following section of sample code shows one method of accessing a VXI address. This function is used for returning a 32-bit data value from a VXI module in A32 address space.

```
void long_a32_read (unsigned long address, unsigned long *data) {

    unsigned long lrdata;

    lrdata = *(volatile unsigned long * ) address;
    *data = lrdata;
    }
```

To access data as either 8-bit or 16-bit values instead of longwords (32-bits), the variable receiving the data and the pointer must be changed to the appropriate data word size.

Please refer to the VxWorks documentation for the Board Specific Routines for additional information on block transfers.

VXI Triggers

The V15X-AA11 supports the eight VXI TTL trigger lines as well as the two VXI ECL trigger lines. These signals operate in the same manner as the VXI trigger lines. The V15X-AA11 hardware supports the Stop/Start protocol and the Synchronous protocol for asserting the VXI trigger lines.

The Start/Stop protocol provides a mechanism to assert a trigger line under computer control and maintain the signal level until the trigger line is negated by programmed control. This can be useful for generating a trigger signal completed under computer control. The Synchronous protocol permits the V15X-AA11 to generate a pulse on a trigger line for a duration of approximately 1.5 microseconds. The computer merely writes to the Trigger Source Register with the trigger signals to be asserted.

Synchronous Trigger Example:

As an example, assume it is desired to apply a 1.5 microsecond pulse to VXI trigger line 2. The V15X-AA11 is set for Logical Address 0, which results in a A16 Logical Base Address of $C000_{16}$. This can be accomplished by writing to the Trigger Source Register, at an offset of 32_{16} from the A16 Logical Base Address of the V15X-AA11, with the data set to 8804_{16}.

Shown in pseudocode, the trigger may be sourced as follows:

```
short_a16_write (  0xC032, 0x8004);        /* 16-bit A16 write to address 0xc032
                                              with     data of 0x8004 */
```

Start/Stop Trigger Example:

As an example, assume it is desired to apply assert VXI trigger line 5 and the ECL trigger line 0, wait for a period of time, negate ECL trigger 0, wait for a period of time, and then negate VXI trigger line 5. The V15X-AA11 is set for Logical Address 0, which results in a A16 Logical Base Address of $C000_{16}$.

Shown in pseudocode, the trigger sequence can be sourced as follows:

```
short_a16_write ( 0xC032, 0x120);          /* 16-bit A16 write to address 0xc032 with
                                              data of 0x120 */

                                           /* to assert TTL trigger line 5 and ECL trigger
                                              line 0       */

taskDelay ( 1 );                           /* delay for a period of time */short_a16_write
                                           ( 0xc032, 0x4100);   /* 16-bit A16 write to
                                           address 0xc032 with data of 0x4100 */
                                           /* to negate ECL trigger line 0 */
```

```
taskDelay ( 1 );                    /* delay for a period of time */
                                    short_a16_write ( 0xc032, 0x4020); /*  16-bit
                                    A16 write to address 0xc032 with data of
                                    0x4020 */
                                    /* to negate TTL trigger line 5          */
```

The trigger lines may also be connected to a hardware timer to assert them at a predetermined interval. The interval counter (timer) is based off of the CLK10 10 megahertz VXI*bus* clock and contains 32 bits. When the timer expires, a 1.5 microsecond pulse is applied to the preselected trigger line(s). The 32-bit counter yields an interval from 2 microseconds to 429 seconds in 100 nanosecond increments. The 32-bit timer value is split into two 16-bit values that are loaded into the Trigger Timer High and Trigger Timer Low Registers. Please refer to the Trigger Timer Registers for additional information on timer operation.

As an example, assume it is desired to setup VXI TTL trigger line 4 to be pulsed every 1 millisecond. For this example, the Trigger Timer High Register must be loaded with 0, the Trigger Timer Low Register must be loaded with 2710_{16}, and the Trigger Timer Control is loaded with 8010_{16}. The V15X-AA11 is set for Logical Address 0, which results in a A16 Logical Base Address of $C000_{16}$.

Shown in pseudocode, the trigger sequence can be setup as follows:

```
short_a16_write ( 0xC03C, 0x00);    /* 16-bit A16 write to address 0xc03c with
                                    data 0f 0x00 */

                                    /* set the register select bits to zero in the
                                    misc. control register */

short_a16_write ( 0xC034, 0x2710);  /* 16-bit A16 write to address 0xc034 with
                                    data of 0x2710 */

                                    /* load the timer data into the timer data low
                                    register */

short_a16_write ( 0xC03C, 0x1000);  /* 16-bit A16 write to address 0xc03c with
                                    data of 0x1000 */

                                   /* set register select bits to point to timer data
                                    high register */

short_a16_write ( 0xC034, 0x00);    /* 16-bit A16 write to address 0xc034 with data
                                    of 0x00 */

                                    /* load the timer data into the timer data high
                                    */
```

```
short_a16_write ( 0xC03C, 0x8000);      /* 16-bit A16 write to address 0xc03c with data
                                           of 0x8000 */

                                        /* set register select bits to point to timer
                                           control register */

short_a16_write ( 0xC034, 0x8010);      /* 16-bit A16 write to address 0xc034 with data
                                           of 0x8010 */

                                        /* load enable timer and TTL trigger line 4 */
```

After the timer is setup and enabled, a 1.5 microsecond pulse is generated on VXI TTL trigger line 4 every 1 millisecond. To stop the timer, the Timer Enable bit in the Timer Control Register must be set to zero.

Along with the ability to assert VXI/Front Panel trigger lines, the V15X-AA11 can also respond to the assertion of these signals asserted by other devices. The V15X-AA11 can respond to these signals by either polling or by an interrupt. Once an enabled trigger source is received by the V15X-AA11, it is latched and 'held' until cleared by programmed control. To enable a specific trigger line source to be received by the V15X-AA11, it must first be enabled in the Trigger Interrupt Mask Register located at an offset of $2E_{16}$ from the A16 Logical Base Address of the V15X-AA11. This register contains individual bit positions for each of the 10 trigger sources. The trigger sources include the eight VXI TTL trigger lines, two VXI ECL trigger lines. Each bit set to a one enables the trigger source to be latched by the V15X-AA11. Once an enabled trigger source has been latched by the V15X-AA11, it may be read through the Trigger Interrupt Source Register, located at an offset of $2E_{16}$ from the A16 Logical Base Address. Any bit set to a one in this register may generate an interrupt request, if enabled. An interrupt source is any event that may generate an interrupt, if it is enabled in the Interrupt Control Register. The TRIGGER IN INTERRUPT ENABLE, the INTERRUPT REQUEST ENABLE and the INTERRUPT REQUEST SELECT bits must be set appropriately in order for an interrupt to be generated on the VXI*bus*. Please refer to the Interrupt Control Register section of this manual for additional information.

Once a trigger event has been latched and read through the Trigger Interrupt Source Register, it must be cleared before subsequent trigger events may be seen on that trigger line. The latched trigger source is cleared through the Trigger Interrupt Source Clear Register located at an offset of 30_{16} from the A16 Logical Base Address. Any bit set to a one when the register is written causes the corresponding trigger source to be reset to zero and ready for additional captures. This same routine must be followed regardless of the mechanism used to determine that a trigger event occurred.

As an example, assume it is desired to respond to the assertion of VXI trigger line 0 by asserting trigger line 1. This can be accomplished by setting up the V15X-AA11 to enable VXI trigger line 0 in the Trigger Interrupt Mask Register and waiting for the source to be set in the Trigger Interrupt Source Register. This routine is using the polling technique instead of an interrupt driven mechanism. For this example, the V15X-AA11 is set for Logical Address 0, which results in a A16 Logical Base Address of $C000_{16}$.

The pseudocode for this example is as follows:

```
short_a16_write ( 0xC02E, 0x01);        /* 16-bit A16 write to address 0xc02e with data
                                           of 0x01 */

                                        /* load interrupt mask register to enable VXI
                                           TTL trigger 0 */

data = 0;                               /* set a data variable to zero */
while( rdata == 0) {                    /* loop while rdata is equal to zero */

short_a16_read ( 0xC02E, &rdata );      /* 16-bit A16 read to address 0xc02e and
                                           return data in rdata */

                                        /* this is a read of the trigger interrupt source
                                           register */
                                        }

                                        /* the while loop is exited once the trigger is
                                           received */

short_a16_write ( 0xC030, 0x01);        /* 16-bit write to address 0xc030 with data of
                                           0x01 */

                                        /* write trigger interrupt source reg to clear
                                           TTL trigger 0 bit */

short_a16_write ( 0xC032, 0x8002);      /* 16-bit A16 write to address 0xc032 with data
                                           of 0x8002       */

                                        /* write trigger source register to pulse TTL
                                           trigger line 1 */
```

APPENDIX A

APPENDIX B

This Appendix shows the allocation of signals on the VXI*bus* P1 and P2 Connectors.

VXI P1 Connector Assignments:

Pin	Row A	Row B	Row C
1	D00	BBSY*	DO8
2	D01	No Connect	D09
3	D02	No Connect	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

VXI P2 Connector Assignments:

Pin	Row A	Row B	Row C
1	ECLTRG0	+5 V	CLK10+
2	-2 V	GND	CLK10-
3	ECLTRG1	RESERVED	GND
4	GND	A24	-5.2 V
5	MODID12	A25	LBUSC00
6	MODID11	A26	LBUSC01
7	-5.2 V	A27	GND
8	MODID10	A28	LBUSC02
9	MODID09	A29	LBUSC03
10	GND	A30	GND
11	MODID08	A31	LBUSC04
12	MODID07	GND	LBUSC05
13	-5.2 V	+5 V	-2 V
14	MODID06	D16	LBUSC06
15	MODID05	D17	LBUSC07
16	GND	D18	GND
17	MODID04	D19	LBUSC08
18	MODID03	D20	LBUSC09
19	-5.2 V	D21	-5.2 V
20	MODID02	D22	LBUSC10
21	MODID01	D23	LBUSC11
22	GND	GND	GND
23	TTLTRG0*	D24	TTLTRG1*
24	TTLTRG2*	D25	TTLTRG3*
25	+5 V	D26	GND
26	TTLTRG4*	D27	TTLTRG5*
27	TTLTRG6*	D28	TTLTRG7*
28	GND	D29	GND
29	RESERVED	D30	RESERVED
30	MODID00	D31	GND
31	GND	GND	+24 V
32	SUMBUS	+5 V	-24 V

CONTENTS