Model V200

16 or 32-Channel Sigma-Delta ADC

Instruction Manual

January 30, 2001

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This manual is organized into four chapters:

- The *Introduction* chapter describes the capabilities of the V200 and how it can be used in a wide variety of applications.
- The *Unpacking and Installation* chapter explains how to install the V200 into a VXI chassis. In addition, a procedure for installing field upgrades for the V200 is also provided.
- The *Programming Information* chapter explains how to access and control the V200. The first half of the section explains the use of the Configuration Registers. These general purpose registers are standard registers defined by the VXI standard which is used to identify the module and control interrupts. The second half of the section explains the use of the Operational Registers. The registers are specific for operation and control of the V200.
- The *Appendices* provide additional information that may be helpful in the use of the V200. Topics include register layout, module calibration procedures, grounding techniques when connecting field wiring, and programming examples.

Terminology

The following is a list of some of the terms used throughout this manual:

Term	Description
A16 Space	As described in the VXI specification, this mnemonic is used to describe the first 64 kBytes of address space. Every VXI module is automatically allocated a 64-byte block of this address space (also known as Configuration Registers). The exact location is determined by the logical address of the module.
A32 Space	As described in the VXI specification, this mnemonic is used to describe the 4 Giga-byte block of address space provided. Any module can request a block of this address space from information contained in its Configuration Registers. This memory block is also called the Operational Registers.
Configuration Registers	See A16 Space.

D16	As described in the VXI specification, this mnemonic is used to describe a single 16-bit data transfer.
D16 BLK	As described in the VXI specification, this mnemonic is used to describe a 16-bit block transfer.
D32	As described in the VXI specification, this mnemonic is used to describe a single 32-bit data transfer. This mode is not supported by all Slot-0 controllers. Check the owners manual for the Slot-0 before attempting this type of transfer.
D32 BLK	As described in the VXI specification, this mnemonic is used to describe a 32-bit block transfer. This is the fastest transfer type supported by the V200. This mode is most beneficial when retrieving data from the ADC (i.e., through Ping/Pong). However, this mode may not be supported by the Slot-0 controller. Check the owners manual for the Slot-0 before attempting this type of transfer.
Logical Address	Every VXI module is given a unique logical address. There are a total of 256 logical addresses with 0 reserved for the Slot-0 controller.
Operational Registers	See A32 Space.
Resource manager	Also referred to as Resman. This software is made available by the manufacturer of the Slot-0 controller and is used to set logical addresses and configure Operational Register addresses in a system.

Conventions

Hexadecimal numbers are represented by the prefix *0x*.
For example, 255_{10} = 0xFF.

The following icons are used in this manual:

NOTE: Information notes are used to call attention to important features or instructions.

CAUTION: Caution notices contain directions that must be followed to avoid immediate system damage or loss of data.

Chapter I: Introduction

General Description

The V200 module provides 16 channels of gain and analog to digital conversion in its base configuration. An architecture for the main card is shown in the accompanying block diagram. The discussion will be keyed to this diagram.

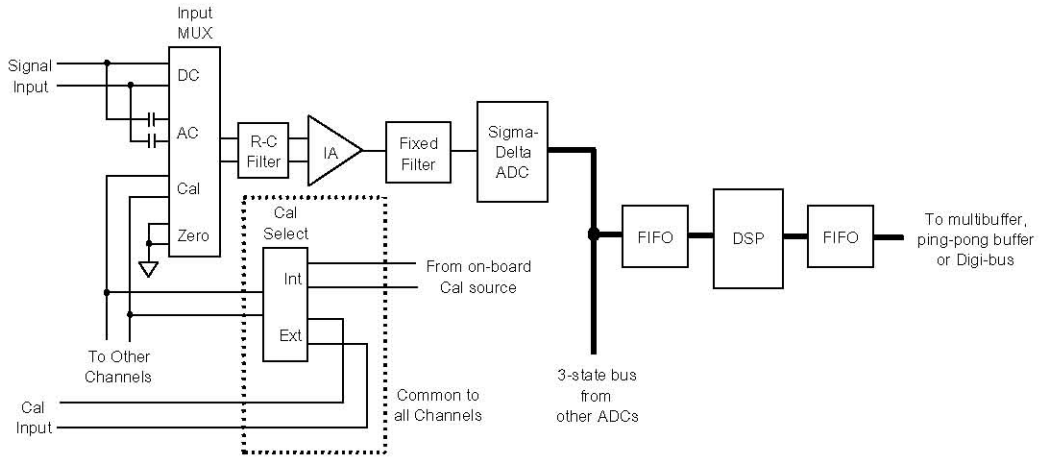


FIGURE 1 - V200 Main Card

The input channels are divided into two groups (A and B), each containing eight or sixteen channels. Data is acquired independently by each group.

Each of the groups consists of 8 or 16 input channels with a Sigma-Delta analog-to-digital converter (ADC), an input multiplexer, an instrumentation amplifier with programmable gain, a gain/attenuator stage (the ADC has an input span of +/-1 volt). Two-pole passive filtering is provided for each channel. The outputs of the ADCs are fed into the ADC FIFO. Up to sixteen channels may be synchronously loaded into this FIFO when the "Convert Complete" flag indicates that data is available.

The DSP is signaled by the FIFO control logic when the correct number of channels has been read into the FIFO. The DSP then reads up to sixteen data words, performs limit checking and writes the data to the output FIFO (also called Ping Pong FIFO).

When the appropriate number of datawords have been written to the output FIFO, its contents are transferred to Ping-Pong Buffer Memory, Multibuffer Memory, or the Digi-bus interfaces.

Channel Inputs

The input multiplexer allows one of four inputs to be routed into the channel. These are:

1. DC coupled signal input
2. AC coupled signal input
3. Calibration bus input
4. Zero (ground) reference.

An instrumentation amplifier with programmable gain follows the input MUX. This provides common mode rejection and gain. A combination of filtering, attenuation and gain stages follow the instrumentation amplifier, providing overall input spans from +/- 10 volts to +/- 10 millivolts in a 1, 2, 5, 10 sequence.

The Sigma Delta ADC used is an Analog Devices AD7722, running at a conversion rate of up to 200kSamples per second. The AD7722 provides extremely accurate 16-bit conversion.
The ADCs for each group are run at the same clock rate. All ADCs within a group are synchronized with each other. Additionally both groups may be run from the same sample clock and both groups may be synchronized.

Synchronization pulses may be applied by the DSPs, via the front panel Sync. Input or via one of the VXI Trigger Lines.

Clock Generator

The clock for the Sigma-Delta converters runs at 64 times the “sample rate”, the input being sampled twice per clock period. This provides an oversampling rate of 128. Thus to achieve a conversion rate of 200kSps a clock rate of 12.8MHz is needed. A Phase Lock Loop, which multiplies a preselected sample clock rate by 64, is provided for Group A. This clock source can be coupled to also run the Group B ADCs.

The input to the Phase Lock Loop (PLL) can be from the External Clock Input on the front panel, from the internal clock source or from the VXI Trigger lines. The internal clock source for the PLL selects a sampling rate in the range of 5 kHz to 200 kHz, in 100 nanosecond increments.

The A/D converter clock source can also be selected by using an on-board crystal controlled oscillator. For this mode, the PLL is bypassed and the crystal frequency is divided to provide the actual sampling rate. The A/D converter can accept clock frequencies in the range of 320KHz to 12.8MHz. This corresponds to sample clock frequencies of 5KHz to 200KHz.

Additionally, groups A and B can be locked together, in which case Group B becomes a slave of Group A.

DSP

Each group has a TMS320C50 running at 80MHz. Each DSP has 32k words of Flash RAM in program space and 64k words of static RAM in data space. The DSP program is downloaded into the flash RAM via the VXI bus. This is not user programmable.

The external static RAM is used for storing calibration data, etc.

Limit Checking

Limit checking is performed by the DSP, and is of the level/slope type or minimum/maximum type. An ADC value (level) and slope (positive or negative) or minimum and maximum is selected by the user before acquisition starts and may not be changed during acquisition. A limit violation can be programmed to cause a transient capture countdown to begin. It can also be routed to the VXI trigger lines or the front panel Trigger Out SMB connector.

Time Tagging

The contents of an on-board tick counter can be inserted into the data stream (to be written into Multibuffer Memory). This tick count can also be read through the ping pong interface. This tick count allows post-processing verification that no data samples were lost.

Ping Pong Memory

This is a dual-buffered memory, which allows synchronous reads to be made via the VXI bus. While one side of the memory is being filled by the Ping Pong FIFO the other half can be read out across the VXI bus.

After one set of data samples has been written to ping pong a clock pulse is generated which causes the ping pong memory to “flip” and present the last set of samples to the VXI bus. New data for each active channel is then written into the “inboard” side of the memory and so on. This “flip” clock corresponds to a delayed version of the sample clock and may be routed to the VXI trigger lines and used to synchronize data reads by the Slot 0 controller.

The set of registers accessible from the VXI bus are loaded synchronously with the start of a scan and are valid until the start of the next scan. This technique provides the full interval between scans for data access.

VXI Trigger Lines

Eight of the pins on the P2 connector of the VXI bus are defined as TTL trigger lines. These open collector lines provide a wired-OR function that is suited to their use in communicating event information between modules.

A practical concept in using these lines is that of event sources and event sinks. Events on a specific trigger line may be generated by any one of several modules. One or more modules may be programmed to respond to events, including the source module of the event.

Examples of event sources are sample rate, limit checking, and front-panel external trigger inputs. Examples of event sinks are transient capture triggers to initiate the capture and local storage of a data segment, and sample clocks to synchronize sampling of input signals or outputting of DAC or digital data.

Consider the case where several V200s are required to trigger simultaneously. The occurrence of a limit condition on any of the modules can cause a VXI trigger line to be asserted and a transient capture initiated across all modules. Meanwhile, another trigger line has been programmed as the source for the scan rate.

Trigger lines can be used to synchronize sampling across multiple modules.

Multibuffer Memory Option

Each group may have a Multibuffer Memory card. Each card provides 4 or 16 Mbytes of dynamic RAM.

The Multibuffer Memory option provides critical buffering between the Slot-0 processor and the ADC to prevent data loss due to processor latency when switching buffers and processing data. The Multibuffer Memory also can be configured to provide a transient capture function where a fixed block of data is captured in memory based on the occurrence of a trigger event. Possible trigger events might include an external trigger or one or more of some selected analog inputs exceeding a programmed threshold. The number of pre- and post-trigger samples may be selected by the user.

System Calibration/Diagnostics

In any system, particularly with larger data acquisition systems, verifying the proper functioning of the system and the calibration of analog I/O is essential. Generally, it is possible to check out some digital system components through exercising the hardware under software control.

To audit analog channels to any degree requires that a series of known analog signals be injected into each channel of the system. This can be accomplished either by operator intervention or by providing the capability to switch known calibration signals into the input

under software control. Switching of calibration signals by hand can be very time-consuming and is subject to errors.

For these reasons, KineticSystems has chosen an implementation with full end-to-end calibration features. To accomplish this goal with the architecture described, a known signal must be injected at the input to the signal conditioning. This is accomplished by a programmable active attenuator or an external user-supplied front-panel calibration signal.

The fixed-point DSP is used to provide calibration and self-test of each group on the V200.

AC calibration may be accomplished by injecting a precise sine wave into the external cal. Input and capturing a segment of the waveform for analysis.

System Configuration Validation

One of the issues, particularly in larger systems, is ensuring that the proper modules with the proper options are installed and configured in the system. This is especially important when you cannot accurately validate the current system configuration because of system size or physical access to areas in a distributed system. Verifying proper installation can be particularly frustrating when modules of the same type or model number can be configured with a number of internal options. Unfortunately, this is an increasingly common practice because of the high densities that can be achieved today and the relatively large card size of VXI. A related issue is the capability to identify and trace the history of specific modules within a larger system.

The VXI standard requires (or in some cases, suggests) that certain register conventions be followed. These register conventions partially address these issues. Standardized registers include the manufacturer ID assigned by the VXI Consortium, a device-type or model identifier, a serial number, and a version number or revision number for hardware and firmware.

An extension of this concept provides a module option identifier as well as some amount of user-writeable EEPROM (Electrically Erasable Programmable Read Only Memory). The EEPROM provides the capability to record in nonvolatile memory any option, calibration, or other module-specific information that may be important to system operation and/or maintenance.

Since these registers are accessible by software, it is possible to develop software to verify system configuration at startup, as well as track modules for maintenance purposes.

Self-Test

Upon reset or on command the V200 can perform a self-test function. When a self-test is initiated the DSP for each group switches through all possible gain settings for each of the channels. For each gain, precision voltages corresponding to plus and minus full scale and zero volts are applied to the channels. The resulting ADC value for each input voltage is compared to test limits. If any test fails, SYSFAIL remains asserted. The DSPs may be interrogated for details of the self-test results.

Channel Calibration

The DSP performs channel calibration on command. This consists of injecting the appropriate plus and minus full-scale voltages into the channel as well as zero volts. The DSP averages several readings and calculates the transfer function of the channel. The results of the calculation can be read back from the DSP.

Channels must be configured before initiating calibration.

Chapter II: Unpacking and Installation

At KineticSystems, static precautions are observed from production, test, and packaging of the module. This includes using static proof mats and wrist straps. Please observe these same precautions when unpacking and installing the module whenever possible.

CAUTION: To guard against electrostatic discharge if no wrist straps are available, touch the anti-static bag to a metal part of the VXI chassis before removing the V200.

The Model V200 is shipped in an anti-static bag within a Styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the logical address switches to the appropriate value.

Configuration

There is one set of user configurable switches on the V200, shown in figure 2. All eight switches, #1 (MSB) to #8 (LSB), are for the logical address. The logical address may be set from 1 to 254 as a statistically configured device. If the V200 is a statistically configured device, it is the user's responsibility to ensure that no two modules are set to the same logical address. Please refer to figure 3 for setting switches. If the module is set for logical address 255 (all switches open), then the V200 will be dynamically configured by the resource manager. A logical address of 0 is not valid since it is reserved for the Slot-0 controller. Logical address 255 is the factory default setting. Please refer to Appendix D for a composite drawing showing strap and switch locations on the V200.

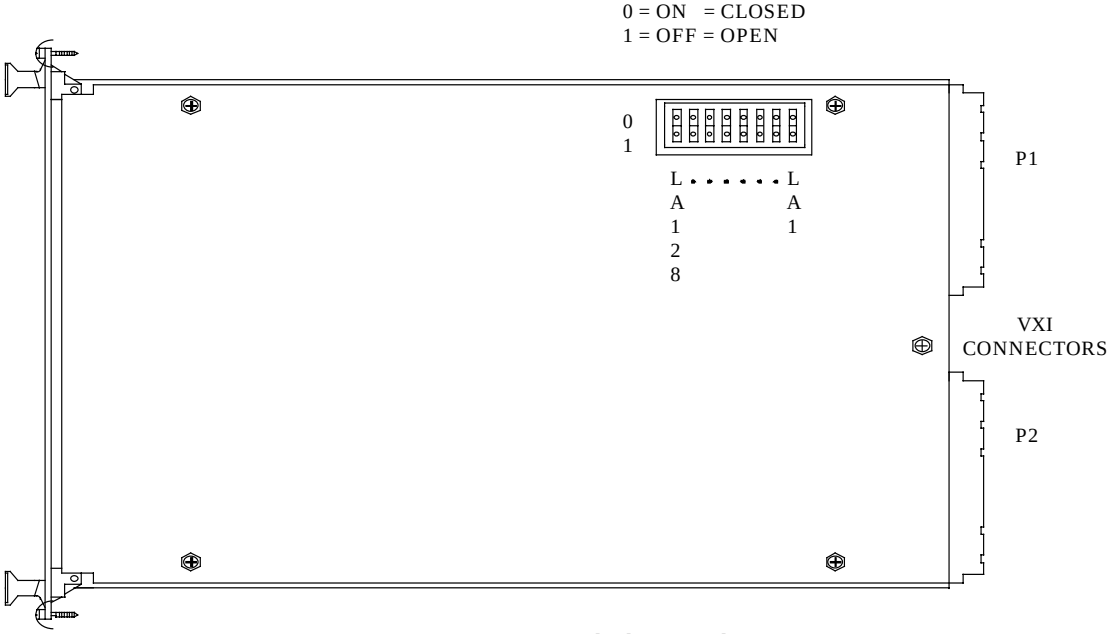


FIGURE 2 - V200 Switch Locations

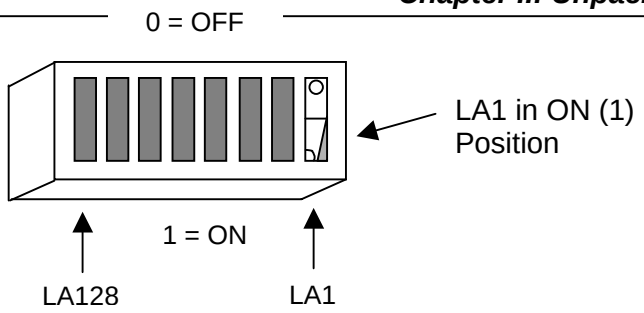


FIGURE 3 - Logical Address Switches

Front Panel Sync Signal Termination

The V200 can accept a Sync pule from an external source. Two SMB connections are available on the front panel to synchronize Group A and Group B ADCs. These inputs are terminated to +5 volts through a 1000 ohm resistor. If multiple V200s are tied together using the Sync signals, some of the termination resistors must be removed. Only the V200 that sources the Sync signal should have the termination resistor connected, all others should have them removed.

Two straps are provided on the V200 for enabling and disabling the connection of the 1000-ohm resistor. One resistor is for the Group A Sync signal and the other is for Group B. If the straps are installed, the termination resistors are connected to the Sync signal. Removal of the strap disconnects the Sync signal from the termination resistor. The following diagram, figure 4, shows the location of the two straps. Please refer to Appendix D for a composite drawing showing strap and switch locations on the V200.

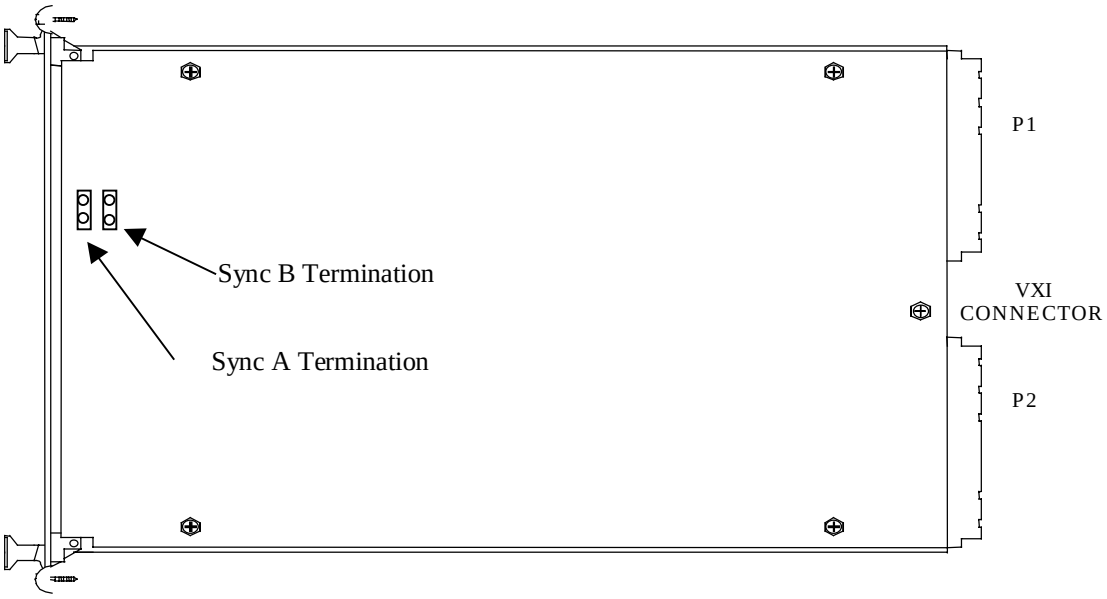


FIGURE 4 - V200 Strap Locations

+24 Volt Front Panel Connection

The V200 contains a strap option that allows a +24 volt supply signal to be connected to the P4 connector on the front panel. This signal is on contact 23 and is used to enable the 24-volt supply to power an ICP termination panel. This strap is factory configured to disable the 24-volt supply. If an ICP termination panel is used with the V200, this strap must be placed in the enable position. The following diagram shows the location of the +24 volt strap on the V200. Please refer to Appendix D for a composite drawing showing strap and switch locations on the V200.

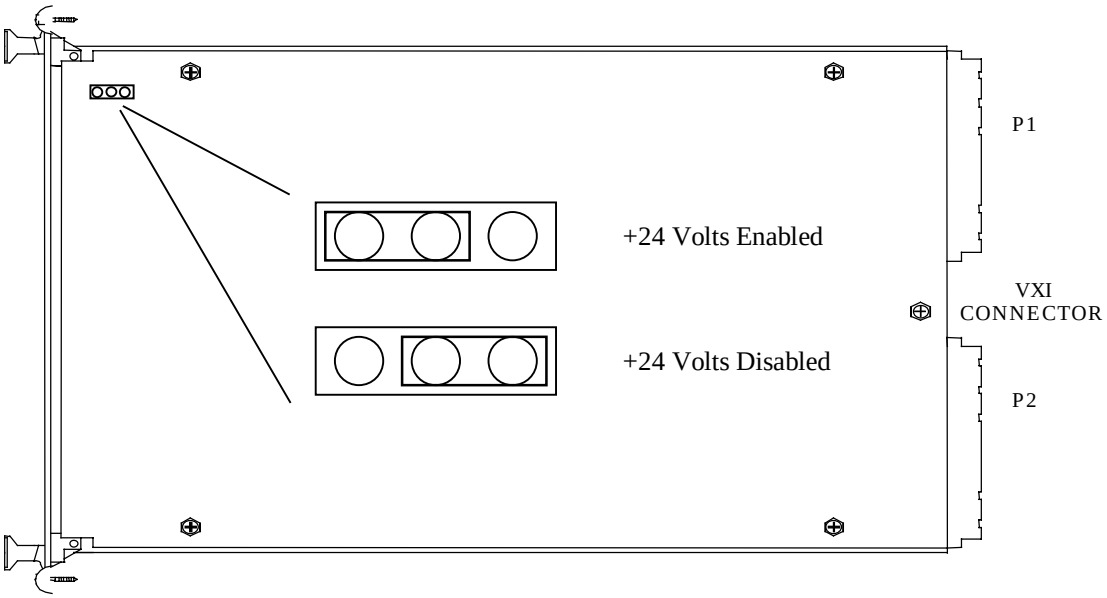


FIGURE 5 - V200 +24 Volt Strap Location

Motorola/Intel Data Format

The V200 is capable of transferring data in either the Motorola or Intel data format. For writing/reading longwords (32-bit values) to/from the V200, the format does not change. The change in format occurs when accessing shortwords (16-bit values) from 32-bit register locations. The following diagram shows a 32-bit longword.

High Shortword

Offset	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16

Low Shortword

Offset	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

An access to the long word address at offset 0 accesses bits 31 through 0 with one VXI transfer. Accesses to this register vary depending on the Data Format selected and the offset at which the register is accessed.

When the Motorola Data Format is selected, a shortword access to offset 0 of this register returns the high shortword, data bits D31 through D16. A shortword access to offset 2 of this register returns the low shortword, data bits D15 through D00.

When the Intel Data Format is selected, a shortword access to offset 0 of this register returns the low shortword, data bits D15 through D00. A shortword access to offset 2 of this register returns the high shortword, data bits D31 through D16.

The following diagram shows the location of the Motorola/Intel Data Format strap on the V200. Please refer to Appendix D for a composite drawing showing strap and switch locations on the V200.

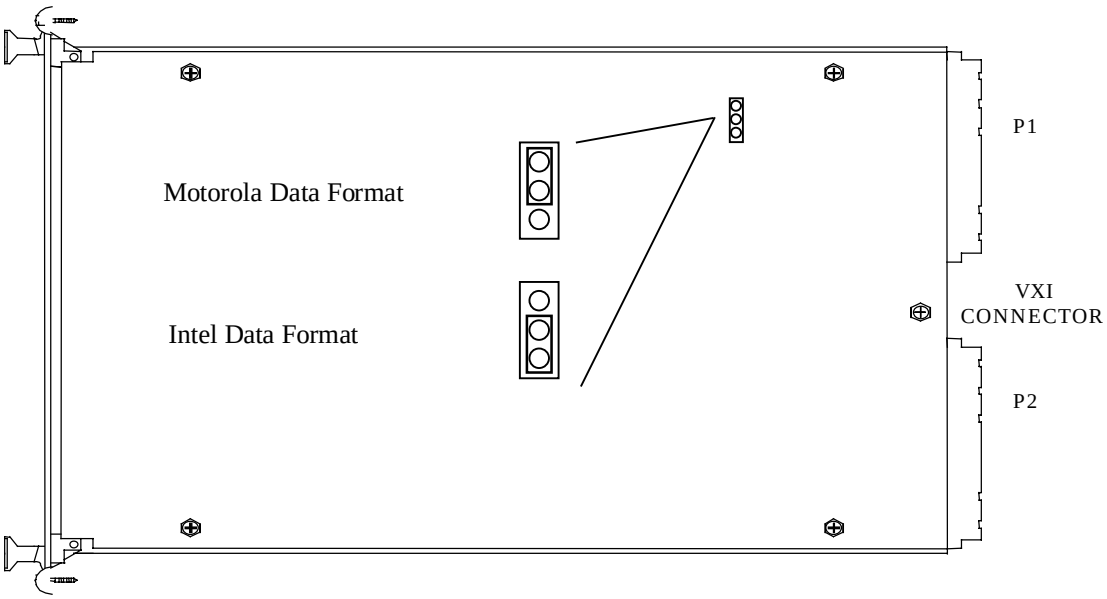


FIGURE 6 - V200 Motorola/Intel Data Format Strap Location

I/O Expansion Cards

The V200 has I/O expansion cards available to increase the number of channels or add additional functionality to the card. These options may be purchased as factory or field upgrades. In the case of factory upgrades, the I/O expansion card is tested and integrated with a base card of the V200. Usually, the base card of the V200 is ordered with the factory upgrade. However, the base card may also be returned to the factory for integration. In the case where the base card has already been purchased, this factory upgrade option is recommended. However, a field upgrade kit may also be purchased.

Refer to Figure 7 while installing the field upgrade of the I/O expansion card.

Place the I/O expansion card into the two inter-board connectors located on the main card. The inter-board connectors are shrouded and keyed to help prevent a misalignment of pins. Two screws are provided with the field upgrade kit to securely fit the card into place. Place the shield back over the card.

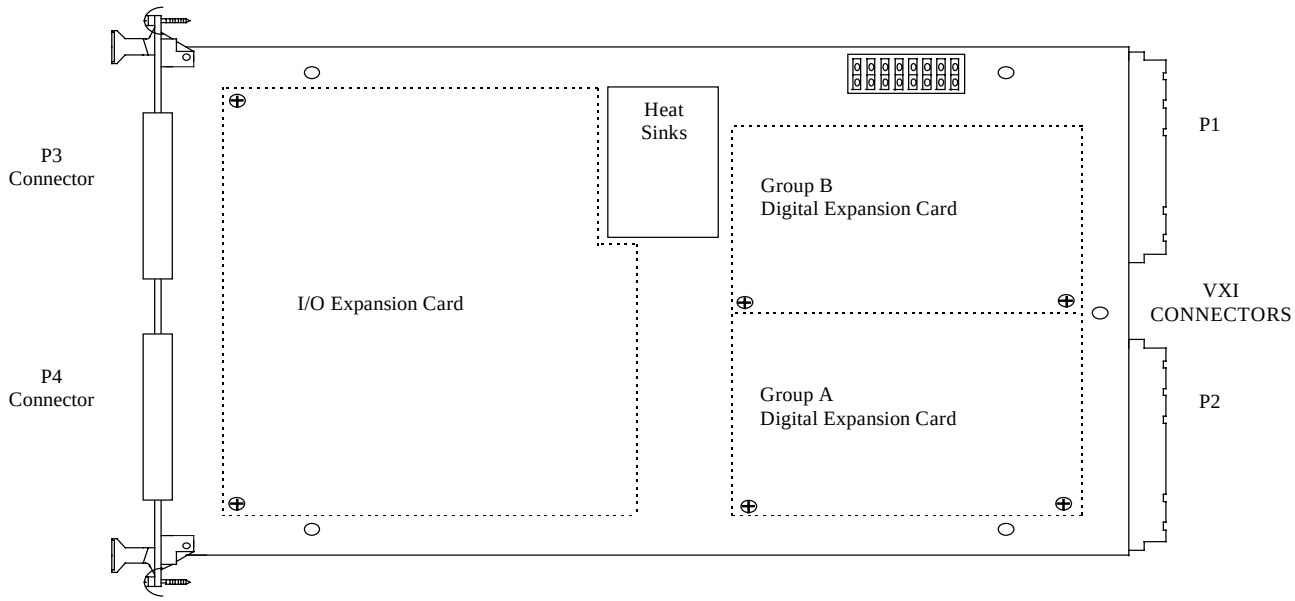


FIGURE 7 - V200 Upgrade Locations

Digital Expansion Cards

The V200 is capable of accepting digital expansion cards to add functionality to the card. These options may be purchased as a factory upgrade or as a field upgrade. The current upgrades consist of a 4 megabyte multibuffer and a 16-megabyte multibuffer. A multibuffer card is required for each group of ADC channels. If only the Group A channels need the multibuffer capability, only one multibuffer card is required.

Module Insertion

The V200 is a C-sized, single width, VXI*bus* module. Except for Slot-0, it can be mounted in any unoccupied slot in a C-size VXI*bus* mainframe.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE.

If the mainframe does not have an autoconfiguring backplane, special care is necessary when installing the V200. To insure proper interrupt acknowledge cycles from the V200 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V200 and the Slot-0 Controller.

NOTE: Remember to remove Interrupt Acknowledge daisy-chain jumpers prior to inserting this module in the backplane or use an autoconfiguring backplane.

Once the V200 is placed in the appropriate slot, make sure the screws located on the front panel are screwed into the mainframe. The shield of the high-density connectors are connected to the front panel and ground to provide additional protection from static electricity. To provide maximum protection, the front panel should be screwed into the chassis. Otherwise, the static electricity must discharge through the V200 potentially causing unexpected behavior.

Front Panel Description

Please refer to Figure 8 for the following section.

LEDs

After power up, the Failed LED will be on for at most five seconds while self-tests are being run. During this time, the ADC, DSP, and RUN LEDs may also turn on periodically. If the Failed LED stays on after five seconds, then the self-test failed. When self-tests are complete, all other LEDs will be off.

LED	Description
Failed	The LED will turn on whenever self-tests are run.
Add Rec.	Add Rec. (Address Received) LED lights to indicate the V200 is being accessed through VXI in either A16 or A32 address space.
Cal	The Cal LED will light while the V200 is executing a calibration sequence. This LED is illuminated for both the Group A and Group B calibration sequences.
Int. Src	The Int. Src LED will light while the V200 is requesting an interrupt.
Run A	The Run A LED is lit as long as the Group A ADCs are in the RUN mode transferring data to either the ping-pong memory or the multibuffer memory.
Run B	The Run B LED is lit as long as the Group B ADCs are in the RUN mode transferring data to either the ping-pong memory or the multibuffer memory.

Connectors

The V200 has two 50 pin, high-density connectors located on the front panel. The P4 connector has 16 differential inputs as well as a reference input. This connector, which contains connector pins, provides access to channels 1 through 16 of the V200. The connector labeled P3 on the V200 may be either a pin or socket connector. For a V200 with only 16 ADC channels, this connector is a socket connector and provides access to the buffered ADC signals after amplification/attenuation. For a V200 with 32 ADC channels, this connector is a pin connector and provides access to the 16 differential inputs for the additional 16 ADC channels. See Figure 8 on page 14, Figure 9 on page 97, and Tables 2-4 on pages 98-100 for the precise pinout descriptions.

A total of 10 SMB connectors are provided on the front panel of the V200. Six of the SMBs are located in a block for Group A and four are in a block for Group B. The following describes the function of each SMB located in the corresponding ADC group.

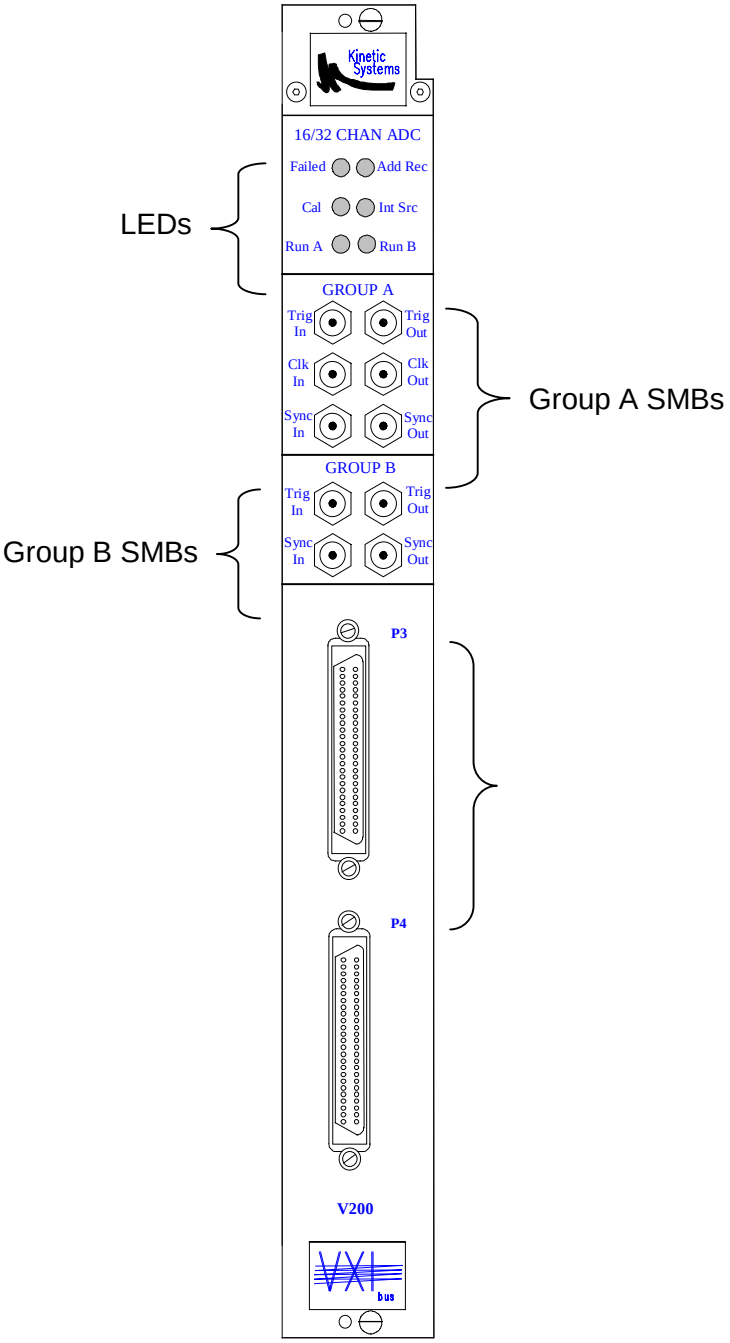


FIGURE 8 - V200 Front Panel

Group A SMBs

There are six SMBs for Group A. The Group A Trigger In and Group A Trigger Out SMBs are tied together and received by a 74F14 buffer. These inputs are tied to +5 volts through a 10KΩ resistor. This is a TTL level input with a minimum pulse width of 200 nanoseconds. The assertion of this signal is true when the input is low. This signal can be programmed to assert a VXI TTL trigger line. The assertion of this trigger line can then be used to start a run mode or trigger a transient capture. Please refer to the Group A Trigger Reception Register description on page 39 for additional information. The Trigger Out SMB can then be used to daisy chain the trigger signal to other V200s.

The **Group A Clock In** signal is received by a pair of 74F14 buffers. This clock input can be used to supply either the Sample Clock for the Group A/B ADCs or the high frequency oversampling clock to the ADCs. Although these signals are located in the Group A block, they can actually supply the clock for both Group A and Group B. For this mode, the Group A and Group B ADCs must be locked into one large group. The input is tied to +5 volts through a 10K resistor. This is a TTL level input that can be used to provide an external sample clock or the oversampling clock to the ADCs. The clock input frequency can range from 10KHz to 200 kHz when supplying the sample clock and should maintain a 40% to 60% duty cycle. If the clock input is to supply the high frequency oversampling clock, this input can range from 640 kHz to 12.8 MHz and should maintain a 40% to 60% duty cycle. When this input is used as a sample clock, a Phase Locked Loop (PLL) is used to multiply the input frequency by 64 to obtain the oversampling clock for the ADCs.

The **Group A Clock Out** SMB is internally connected to the ADC oversampling clock for Group A. This is a TTL level output and is driven by a 74F153 gate. When an external over sample clock is used, a selectively divided 12.8 MHz clock is switched out to this SMB.

The **Group A Sync** signal is received with a 74F04 buffer. This signal is configured at the factory with a 1KΩ pull-up resistor to +5 volts. Optionally, this signal may be unterminated by removing the strap to the pull-up resistor. When a V200 is the source of the Sync signal, the V200 drives the Sync signal with a 74F06 open-collector device. When used as an input to the V200, this signal is asserted when low and must have a minimum pulse width of 200 nanoseconds. When this pulse is received, all of the Group A ADCs are synchronized. After the sync pulse is applied, whether internally or externally generated, the ADCs within that group are synchronized to provide simultaneous sampling. The Group A Sync Out signal is internally connected to the synchronization signal on the Group A ADCs. This is a TTL level signal driven by a 74F04 gate.

The **Group A Trigger In** and **Trigger Out** SMBs are tied together on the V200 and provide a mechanism for triggering various V200 operations. These operations include starting ADC run mode and triggering a transient capture. In these instances, the V200 receives these signals to provide the indicated function. Also, these SMBs can be configured as outputs from the V200 and can be asserted when a Ping-Pong Flip occurs or an ADC limit violation occurs. Please refer to the Group A Trigger Reception Register and Group A Trigger Source Register descriptions for additional information regarding the capabilities of asserting/receiving the Front Panel trigger signals.

Group B SMBs

There are four SMBs for Group B. The Group B Trigger In and Group B Trigger Out SMBs are tied together and received by a 74F14 buffer. These inputs are tied to +5 volts through a 10KΩ resistor. This is a TTL level input with a minimum pulse width of 200 nanoseconds. The assertion of this signal is true when the input is low. This signal can be programmed to assert a VXI TTL trigger line. The assertion of this trigger line can then be used to start a run mode or trigger a transient capture. Please refer to the Group B Trigger Reception Register description for additional information. The Trigger Out SMB can then be used to daisy-chain the trigger signal to other V200s.

The **Group B Sync** signal is received with a 74F04 buffer. This signal is configured at the factory with a 1KΩ pull-up resistor to +5 volts. Optionally, this signal may be unterminated by removing the strap to the pull-up resistor. When a V200 is the source of the Sync signal, the V200 drives the Sync signal with a 74F06 open-collector device. When used as an input to the V200, this signal is asserted when low and must have a minimum pulse width of 200 nanoseconds. When this pulse is received, all of the Group B ADCs are synchronized. After the sync pulse is applied, whether internally or externally generated, the ADCs within that group are synchronized to provide simultaneous sampling. The Group B Sync Out signal is internally connected to the synchronization signal on the Group B ADCs. This is a TTL level signal driven by a 74F04 gate.

The **Group B Trigger In** and **Trigger Out** SMBs are tied together on the V200 and provide a mechanism for triggering various V200 operations. These operations include starting ADC run mode and triggering a transient capture. In these instances, the V200 receives these signals to provide the indicated function. Also, these SMBs can be configured as outputs from the V200 and can be asserted when a Ping-Pong Flip occurs or an ADC limit violation occurs. Please refer to the Group B Trigger Reception Register and Group B Trigger Source Register descriptions for additional information regarding the capabilities of asserting/receiving the Front Panel trigger signals.

Chapter III: Programming Information

VXI*bus* Addressing

The V200 is classified as an extended register-based device, which means it has registers that occupy A16 and A32 space. In accordance with the VXI specification, A16 space means that only 16 address bits are decoded by the V200. A32 space means that 32 address bits are decoded by the V200.

The configuration registers are located in A16 space and include the standard registers defined by VXI as well as additional general-purpose registers. From these registers information about the specific module can be read, the base address for the A32 registers can be controlled, and the interrupt level can be set. For example, by reading certain registers in A16 space, the following information about this module can be found just by knowing the module's logical address:

Manufacturer:	KineticSystems
Module Type:	V200
Base Card Option:	AA11
Serial Number:	20
Firmware Version:	1.0
Hardware Version:	1.0

In general, any configuration register can be accessed simply by knowing the module's logical address (set by the logical address switches) and the register's offset by using the following equation. A complete list of A16 register descriptions and their offsets is available on page 19. The following equation is used to determine the actual A16 address:

$$A16\_Address = 0xC000 + (Logical\_Address \cdot 0x40) + A16\_Register\_Offset$$

As defined by the VXI specification, these Configuration Registers will support D16 transfers only.

Manufacturer: can be found by looking at bits 11 through 0 at register offset 0x0. If the value is 0xF29, this indicates that the module was built by KineticSystems.

Module Type: can be found by looking at bits 11 through 0 at register offset 0x2. If the value is a binary coded decimal (BCD) number 200, this indicates that the module is a V200.

Base Card Option: can be found by reading the four-character string in registers located at offsets 0x20 and 0x22. If the string "AA" is found at offset 0x20 and "11" is found at offset 22, then the specific type of module is the V200-AA11 meaning this module is a V200 with 16 channels. The suffix registers are additional registers defined by KineticSystems to aid in identifying a module.

Serial Number: can be found reading the 32-bit, unsigned number stored in registers at offsets 0xA and 0xC. For example, if a the serial number was 20, the values in the Serial Number High Register would be 0x0 and the value in the Serial Number Low Register would be 0x14.

Firmware Version: can be found by reading the binary coded decimal (BCD) number stored in bits 15 through 8 of the Version Number Register at offset 0xE.

Hardware Version: can be found by reading the BCD number stored in bits 7 through 0 of the Version Number Register at offset 0xE.

In addition to the Suffix Registers, KineticSystems has left registers at offsets 0x24 through 0x3E open for user definition. These User Defined Registers can also be used to identify the module (i.e., with an internal identification number). These registers can only be written one at a time and only at 3ms intervals. However, once they have been written, the data is retained even after power has been removed.

The Operational Registers are located in A32 space and include the registers specific to V200 modules. This address space is configured by the resource manager. In general, any Operational Register can be accessed simply by knowing the value in the modules Offset Register (Configuration register in A16 space at offset 0x6) and using the following equation. A complete list of A32 register descriptions and their offsets is available starting on page 29.

$$A32\_Address = (Offset\_Register\_Value \cdot 0x10000) + A32\_Register\_Offset$$

All Operation Registers support D16, D32, D16 BLK and D32 BLK transfers.

The V200 can be configured to respond with either Intel addressing or Motorola addressing. The factory default is Motorola addressing. For Motorola addressing, a shortword address to a longword location is as follows:

V200 Configuration Registers, A16 Space

ID/Logical Address Register

0x00	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	(0)	(1)	(0)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	(1)	(0)	(1)	(0)	(0)	(1)

( ) Power Up Value

On READ transactions the V200 returns 0x5F29.

Bit(s)	Mnemonic	Meaning
15,14	Device Class	This is an Extended Register-Based Device.
13,12	Address Space	This module requires the use of A16/A32 address space.
11-00	Manufacturer's ID	3881 (0xF29) for KineticSystems.

0x00	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
W									LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0

( ) Power Up Value

For WRITE transactions, bits fifteen through eight are not used. These bits may be written with any data pattern. In Dynamically Configured systems (and the Logical Address switches were set to a value of 255), bits seven through zero are written with the Logical Address value. This register is used by the resource manager to dynamically set a module's logical address.

Device Type Register

0x02	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	(0)	(1)	(0)	(1)	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

This READ ONLY register returns 0x5200.

Bit(s)	Mnemonic	Meaning
15-12	Required Memory	The V200 requires 64 Mbytes of additional memory space.
11-00	Model Code	Identifies this device as a V200 (0x200).

Status/Control Register

04_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Mixed	A32 ENA (0)	Modid (0)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	Ready (0)	Pass (0)	Sys Inb. (0)	Soft Reset (0)

( ) Power Up Value

The bit assignments for the Status/Control register are defined as follows:

Bit(s)	Mnemonic	Meaning
15	A32 ENA	This bit is written with a "1" to enable A32 addressing and reset to "0" to disable these registers. Reads of this bit indicate its current state. This bit is reset to "0" by the assertion of SYSRESET*. This bit is set by the resource manager once the offset register has been written.
14	Modid*	This read only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" in this bit location indicates the device is selected via a high state on its P2 MODID line. This bit is used by the resource manager to dynamically configure the V200.
13-04	Not Used	These bits are not used and are read as "1s".
03	Ready	A "1" in this bit indicates the successful completion of register initialization.
02	Pass	A "0" indicates the V200 has failed or is currently executing its self-test. A "1" in this bit indicates the module's self-test has passed.
01	Sys. Inb.	(Sysfail Inhibit) Writing a "1" to this bit disables the V200 from driving the SYSFAIL* line. Reads of this bit indicate its current state.
00	Soft Reset	Writing a "1" to this bit forces the device into the Soft Reset State. While in this state, the module will only allow access to its Configuration Registers. Writing a "0" to this bit will the signal the V200 to begin executing its self-test

NOTE: The Soft Reset bit must be cleared along with the Pass and Ready bits set before any access to the Operational Registers is allowed.

NOTE: The A32 ENA bit must be set to allow access to the module's Operational Registers.

Offset Register

	A31	A30	A29	A28	A27	A26										
0x06	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	OFF 15 (0)	OFF 14 (0)	OFF 13 (0)	OFF 12 (0)	OFF 11 (0)	OFF 10 (0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

After SYSRESET* and prior to self-test all bits are reset to "0". Otherwise, a read or write defines the base address of the module's A32 registers. Bits 09-00 of this register are not used and should always be written with zeros. As shown above bits 15-10 map directly onto VXI address lines A31-A26. For example, if bits OFF15-0FF10 contain 010000 binary, the base address for the module's Operational Registers becomes 0x40000000.

Attribute Register

0x08	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	IR* (0)	IH* (1)	IC* (0)

( ) Power Up Value

This read only register returns 0xFFFA on READ transactions. Write transactions to this register have no effect and its usage is reserved for future definition.

Bit(s)	Mnemonic	Meaning
15-03	Reserved	These bits are read as "1s" and reserved for future definition.
02	IR*	This bit is read as a "0" to signify that the V200 is capable of generating interrupts.
01	IH*	This bit is read as a "1" and indicates the V200 is not capable of Interrupt Handler Control.
00	IS*	This bit is set to "0" to indicate the V200 has Interrupt Status Reporting capability.

Serial Number High

0x0A	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	SER 31 (?)	SER 30 (?)	SER 29 (?)	SER 28 (?)	SER 27 (?)	SER 26 (?)	SER 25 (?)	SER 24 (?)	SER 23 (?)	SER 22 (?)	SER 21 (?)	SER 20 (?)	SER 19 (?)	SER 18 (?)	SER 17 (?)	SER 16 (?)

( ) Power Up Value

Serial Number Low

0x0C	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	SER 15 (?)	SER 14 (?)	SER 13 (?)	SER 12 (?)	SER 11 (?)	SER 10 (?)	SER 9 (?)	SER 8 (?)	SER 7 (?)	SER 6 (?)	SER 5 (?)	SER 4 (?)	SER 3 (?)	SER 2 (?)	SER 1 (?)	SER 0 (?)

( ) Power Up Value

These READ ONLY registers indicate the serial number of the module. Each module is given a unique serial number. The serial number is represented by a 32-bit unsigned integer. The least significant bits (LSBs) reside in the Serial Number Low register while the most significant bits (MSBs) are in the Serial Number High register. Writing to these registers will have no effect and its use is reserved. For example, assume the module's serial number is 0x10064 (65636). A read of the Serial Number High register returns 0x0001 (1 ⇒ 1 * 65536); and the Serial Number Low register returns 0x0064 (100).

Version Number Register

0x0E	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	Firmware Version # (?)				Firmware Revision # (?)				Hardware Version # (?)				Hardware Revision # (?)			

( ) Power Up Value

This READ ONLY register indicates the hardware and firmware revision number of the module. A write to this register has no effect on its contents. The fields of this register are explained as follows:

Bits	Mnemonic	Meaning
15-12	Firmware Version #	Firmware Version Number
11-08	Firmware Revision #	Firmware Revision Number
07-04	Hardware Version #	Hardware Version Number
03-00	Hardware Revision #	Hardware Revision Number

The combination of Firmware Version Number and Firmware Revision Number indicate the module's firmware version level. These two fields contain two four-bit integers and are joined to form the level.

Interrupt Status Register

0x1A	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	GPB XSNT CMPL (0)	GPB BUF FULL (0)	GPB LMT ALM (0)	GPB BUF FLIP (0)	GPA XSNT CMPL (0)	GPA BUF FULL (0)	GPA LMT ALM (0)	GPA BUF FLIP (0)	Logical Address **(0xFF)**							

( ) Power Up Value

This READ ONLY register is defined as follows:

Bit(s)	Mnemonic	Meaning
15	GPB XSNT	Group B Transient Complete is a read-only bit set when a transient CMPL capture operation is completed by the post-trigger counter decrementing to zero after a transient event. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.
14	GPB BUF FULL	Group B Buffer Full is a read-only bit set when a multibuffer operation causes the setting of one of the segment full flags in the Group B Multibuffer Control Register. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.
13	GPB LMT ALM	Group B Limit Alarm is a read-only bit set when a limit violation is detected by the Group B DSP. This limit is programmed prior to enabling the ADCs. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.
12	GPB BUF FLIP	Group B Buffer Flip is a read-only bit set whenever a complete ADC scan has completed and the ping-pong buffer is flipped. This bit is cleared by an I/O read to this register or by an interrupt acknowledge cycle.
11	GPA XSNT CMPL	Group A Transient Complete is a read-only bit set when a transient capture operation is completed by the post-trigger counter decrementing to zero after a transient event. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.
10	GPA BUF FULL	Group A Buffer Full is a read-only bit set when a multibuffer operation causes the setting of one of the segment full flags in the Group A Multibuffer Control Register. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.

Bit(s)	Mnemonic	Meaning
9	GPA LMT ALM	Group A Limit Alarm is a read-only bit set when a limit violation is detected by the Group A DSP. This limit is programmed prior to enabling the ADCs. This bit is cleared by an I/O read of this register or by an interrupt acknowledge cycle.
8	GPA BUF FLIP	Group A Buffer Flip is a read-only bit set whenever a complete ADC scan has completed and the ping-pong buffer is flipped. This bit is cleared by an I/O read to this register or by an interrupt acknowledge cycle.
07-00	Logical Address	These bits contain the Logical Address of the V200 during an interrupt acknowledge cycle. These bits are read as all ones during a non-interrupt acknowledge cycle.

During an interrupt acknowledge cycle the V200 enables this register onto the D15-D00 data lines. As shown above, the data returned will indicate the current interrupt status as well as the V200s current logical address. Please note that since any enabled source can generate an interrupt, more than one status bit can be set during the acknowledge cycle.

Enabling interrupts, disabling the Interrupt Mask, and selecting an Interrupt Request Line are controlled by the Interrupt Control Register

The Interrupt Control Register will mask (prevent) or unmask (allow) the setting of bits 08-15 in the Interrupt Status Register accordingly.

Interrupt Control Register

0x1C	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	MSK GPB XCMP* (1)	MSK GPB BFUL* (1)	MSK GPB LMT* (1)	MSK GPB BFLP* (1)	MSK GPA XCMP* (1)	MSK GPA BFUL* (1)	MSK GPA LMT* (1)	MSK GPA BFLP* (1)	EN* (1)	(1)	IRQ2 (1)	IRQ1 (1)	IRL0 (1)	(1)	(1)	(1)

( ) Power Up Value

Using this register to control interrupts is defined as follows:

Bit(s)	Mnemonic	Meaning
15	MSK GPB XCMP*	A “1” in this bit masks (prevents) the Group B Transient Complete Interrupt Status bit from generating an interrupt request. This bit must be written with a "0" to allow the Group B Transient Complete Interrupt Source to generate an interrupt request.
14	MSK GPB BFUL*	A “1” in this bit masks (prevents) the Group B Buffer Full Interrupt Status bit from generating an interrupt request. This bit must be written with a "0" to allow the Group B Buffer Full to generate an interrupt request
13	MSK GPB LMT*	A “1” in this bit masks (prevents) the Group B Limit Alarm bit from generating an interrupt request. This bit must be written with a “0” to allow the Group B Limit Alarm to generate an interrupt request.
12	MSK GPB BFLP*	A “1” in this bit masks (prevents) the Group B Buffer Flip bit from generating an interrupt request. This bit must be written with a "0" to allow the Group B Buffer Flip to generate an interrupt request.
11	MSK GPA XCMP*	A “1” in this bit masks (prevents) the Group A Transient Complete Interrupt Status bit from generating an interrupt request. This bit must be written with a "0" to allow the Group A Transient Complete Interrupt Source to generate an interrupt request.
10	MSK GPA BFUL*	A “1” in this bit masks (prevents) the Group A Buffer Full Interrupt Status bit from generating an interrupt request. This bit must be written with a "0" to allow the Group A Buffer Full to generate an interrupt request.
9	MSK GPA LMT*	A “1” in this bit masks (prevents) the Group A Limit Alarm bit from generating an interrupt request. This bit must be written with a “0” to allow the Group A Limit Alarm to generate an interrupt request.
8	MSK GPA BFLP*	A “1” in this bit masks (prevents) the Group A Buffer Flip bit from generating an interrupt request. This bit must be written with a "0" to allow the Group A Buffer Flip to generate an interrupt request.

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td>7</td><td>EN*</td><td>A one in this bit is used to disable interrupt generation. This bit prevents any source from generating an interrupt. A zero in this field enables interrupt generation.</td></tr>
<tr><td>6</td><td>Not Used</td><td>This bit is reserved for use during interrupt handling. Since the V200 is not capable of interrupt handling, this bit should always be written with a "1".</td></tr>
<tr><td>5-3</td><td>IRL2*-
IRL0*</td><td>This 3-bit field selects the VXIbus interrupt line associated with the interrupt according to the following table:
<table>
<tr><th>IRL2*
(D05)</th><th>IRL1*
(D04)</th><th>IRL0*
(D03)</th><th>Interrupt Request Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>IRQ7</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IRQ6</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>IRQ5</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IRQ4</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>IRQ3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>IRQ2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>IRQ1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Disconnected</td></tr>
</table></td></tr>
<tr><td>2-0</td><td>Not Used</td><td>These bits are reserved for selecting an interrupt handler line. The V200 does not have interrupt handler capabilities, these bits should always be written with "1s".</td></tr>
</table>

All bits in this register are set to "1" on the assertion of SYSRESET* or if the SOFT RESET bit in the Status/Control register is written with a "1". If any condition is to generate an interrupt, the appropriate interrupt masks must be set to disable the mask, IREN* bits must be cleared, and IRL2*-IRL0* must be a binary code value other than 111. An interrupt request pending on any particular line is cleared by the assertion of SYSRESET*, putting the module into Soft Reset, changing IRL2*-IRL0*, or if the interrupt is properly acknowledged.

Subclass Register

0x1E	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(0)

( ) Power Up Value

Reads of this register return 0xFFFE. Writes to this register have no effect. The read contents are defined as follows:

Bit(s)	Meaning
15	This bit indicates that the V200 is a VXI*bus* defined Extended Device.
14-0	These bits indicate that this is an Extended Register Based Device.

Suffix High Register

0x20	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	Suffix High Register (?)															

( ) Power Up Value

Suffix Low Register

0x22	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	Suffix Low Register (?)															

( ) Power Up Value

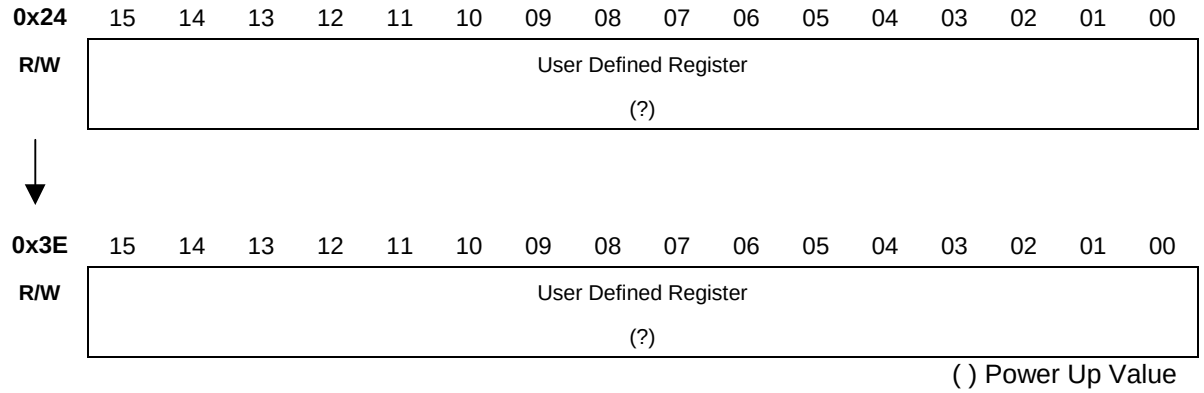
These two registers are KineticSystems defined and hold the module's suffix. The suffix determines the particular option of the module. This information can be used to remotely establish available channel count, multibuffer options, etc. of the module. For further information on each option, refer to the Ordering Information section of this manual.

The module's suffix is always composed of four ASCII characters. The Suffix High register contains the first two characters; while, the last two characters are in the Suffix Low register. For instance, assume the module is a model V200-AA11. The module's suffix is "AA11". Converting this to ASCII yields 0x41413131.

For “user upgrades” write access to the Suffix registers may be obtained by moving strap STP8 to the ENA position. Strap STP8 must be returned to the DIS position when writing is complete.

NOTE: Special care must be taken while writing information into these locations. Once a register has been written, a minimum of 3ms must pass before any User Defined Register may be read or written.

User Defined Registers



( ) Power Up Value

Offsets 0x24 through 0x3E are READ/WRITE registers and may be used to store user defined data. These registers are contained in non-volatile EEPROM.

NOTE: Special care must be taken while writing information into these locations. Once a register has been written, a minimum of 3ms must pass before any User Defined Register may be read or written.

V200 Operational Registers, A32 Space

Control/Status Register

The Control/Status Register is a write/read register located at an offset of 0x00 from the A32 base address of the V200 operational registers. This register is used to check various status indicators on the V200 and to enable or disable module functions. The following diagram shows the bit layout for the Control/Status Register.

0x00	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	(0)	GPB STG	GPB ARM	GPB TRE	GPB MBE	GPB DSF	GPB VXF	GPB RUN	(0)	GPA STG	GPA ARM	GPA TRE	GPA MBE	GPA DSF	GPA VXF	GPA RUN

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-15	Not Used	These bits are not used and read as zeros.
14	GPB STG	GROUP B SOFTWARE TRIGGER is a write-only bit used to trigger a transient capture mode of operation. After all the required registers are loaded prior to a transient capture, this bit may be set to a one, which causes the transient event to trigger. The digitized data is then stored until the Multibuffer Post Trigger counts down to zero, indicating the end of the event. This bit is not latched and read as a zero.
13	GPB ARM	GROUP B ARMED is a read-only bit used to indicate when the Group B channels are enabled and ready to receive a trigger, which starts ADC conversions and storing data.
12	GPB TRE	GROUP B TRANSIENT ENABLE is a write/read bit used to enable and disable the transient capture feature of the V200. A multibuffer memory must be installed onto the V200 in order for the transient capture feature to work properly. Transient captures are enabled by setting this bit to a one and disabled by clearing this bit to a zero. This bit is also cleared to a zero after a transient capture is complete, indicated by the post-trigger counter on the multibuffer memory expiring.

Bit(s)	Mnemonic	Meaning
11	GPB MBE	GROUP B MULTIBUFFER ENABLE is a write/read bit used to enable and disable the continuous multibuffer mode on the V200. In order for this feature to function properly, a multibuffer card must be installed on the V200. Continuous multibuffer operations are enabled by setting this bit to a one and disabled by setting this bit to a zero.
10	GPB DSF	GROUP B DSP BUFFER FULL is a read-only bit used to indicate when the Communication I/O Register for Group B has been written by a host computer. This bit is set to a one when a host computer writes to the Group B Communication I/O Register. When read as a one, this bit indicates that the host computer may not write to the Communication I/O Register until the Group B DSP reads the Communication I/O Register to receive the data sent to in by the host computer. After the Group B DSP reads the Communication I/O Register, this bit is reset to a zero. Once the host senses this bit as a zero, the Group B Communication I/O Register may then be written with additional data.
9	GPB VXF	GROUP B VXI BUFFER FULL is a read-only bit used to indicate when the Communication I/O Register for the Group B has been written by the DSP. This bit is set to a one when the Group B DSP writes to the Group B DSP Communication I/O Register. When read as a one, this bit indicates that the host computer may read the Group B DSP Communication I/O Register and retrieve the data sent by the DSP. This bit is cleared when the Communication I/O Register for Group B is read by VXI.
8	GPB RUN	GROUP B RUNNING is a read-only bit used to indicate whether the Group B channels are being digitized. Reading this bit as a zero indicates that the Group B ADCs are not storing data into the ping-pong memory. This bit is returned as a one as long as the ADCs are storing data into the ping-pong memory.
7	Not Used	This bit is not used and read as a zero.
6	GPA STG	GROUP A SOFTWARE TRIGGER is a write-only bit used to trigger a transient capture mode of operation. After all the required registers are loaded prior to a transient capture, this bit may be set to a one, which causes the transient event to trigger. The digitized data is then stored until the Multibuffer Post Trigger counts down to zero, indicating the end of the event. This bit is not latched and read as a zero.
5	GPA ARM	GROUP A ARMED is a read-only bit used to indicate when the Group A channels are enabled and ready to receive a trigger, which starts ADC conversions and storing data.

Bit(s)	Mnemonic	Meaning
4	GPA TRE	GROUP A TRANSIENT ENABLE is a write/read bit used to enable and disable the transient capture feature of the V200. A multibuffer memory must be installed onto the V200 in order for the transient capture feature to work properly. Transient captures are enabled by setting this bit to a one and disabled by clearing this bit to a zero. This bit is also cleared to a zero after a transient capture is complete, indicated by the post-trigger counter on the multibuffer memory expiring.
3	GPA MBE	GROUP A MULTIBUFFER ENABLE is a write/read bit used to enable and disable the continuous multibuffer mode on the V200. In order for this feature to function properly, a multibuffer card must be installed on the V200. Continuous multibuffer operations are enabled by setting this bit to a one and disabled by setting this bit to a zero.
2	GPA DSF	GROUP A DSP BUFFER FULL is a read-only bit used to indicate when the Communication I/O Register for Group A has been written by a host computer. This bit is set to a one when a host computer writes to the Group A Communication I/O Register. When read as a one, this bit indicates that the host computer may not write to the Communication I/O Register until the Group A DSP reads the Communication I/O Register to receive the data sent to in by the host computer. After the Group A DSP reads the Communication I/O Register, this bit is reset to a zero. Once the host senses this bit as a zero, the Group A Communication I/O Register may then be written with additional data.
1	GPA VXF	GROUP A VXI BUFFER FULL is a read-only bit used to indicate when the Communication I/O Register for the Group A has been written by the DSP. This bit is set to a one when the Group A DSP writes to the Group A DSP Communication I/O Register. When read as a one, this bit indicates that the host computer may read the Group A DSP Communication I/O Register and retrieve the data sent by the DSP. This bit is cleared when the Communication I/O Register for Group A is read by VXI.
0	GPA RUN	GROUP A RUNNING is a read-only bit used to indicate whether the Group A channels are being digitized. Reading this bit as a zero indicates that the Group A ADCs are not storing data into the ping-pong memory. This bit is returned as a one as long as the ADCs are storing data into the ping-pong memory.

Group A Trigger Source Register

The Group A Trigger Source Register is a write/read register located at an offset of 0x04 from the base address of the V200 Operational Registers. This register is used for configuring the TTL trigger lines that are asserted by the V200 for various events. The data in this register is used for allocating trigger lines for Group A. The trigger lines may be driven by any of the following sources:

1.) Start Simultaneous Sampling (Synchronous Run)
2.) Front Panel Trigger Input A
3.) Limit Violation in Group A Channels
4.) Synchronization Pulse to Group A Sigma-Delta ADCs
5.) Flip of Group A Ping-Pong Buffer
6.) Group A Sample Clock

Each source for generating a TTL trigger consists of an enable bit and a three bit binary pattern to determine which trigger line to assert. The following diagram shows the bit pattern for the Group A Trigger Source Register along with a description of each bit location.

0x04	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	SSP ENA	SSP 2	SSP 1	SSP 0	FTG ENA	FTG 2	FTG 1	FTG 0

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	LMT ENA	LMT 2	LMT 1	LMT 0	SYN ENA	SYN 2	SYN 1	SYN 0	PPF ENA	PPF 2	PPF 1	PPF 0	SCK ENA	SCK 2	SCK 1	SCK 0

Bit(s)	Mnemonic	Meaning
31-24	Not Used	These bits are not used and read as zeros.
23	SSP ENA	SIMULTANEOUS SAMPLING ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger to allow multiple V200s to enter run mode synchronously. This bit is set to a one on only one V200 (Master) to enable the Synchronous Run trigger source. All V200s Trigger Reception Registers "Arm Synchronous Run" (bits 19-16) need to be setup to receive this trigger.
22-20	SSP2-0	SIMULTANEOUS SAMPLING TRIGGER SELECTION 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted to synchronously start multiple V200s. The binary combination of these bits indicates the VXI TTL Trigger Line to generate according to the following table.
22-20	SSP2-0	

FTG2	FTG1	FTG0	VXI Trigger Line
0	0	0	0

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td>22-20
Cont'd</td><td>SSP2-0
Cont'd</td><td>
<table>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>19</td><td>FTG ENA</td><td>FRONT PANEL TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when the front panel trigger line is asserted. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>18-16</td><td>FTG2-0</td><td>FRONT PANEL TRIGGER SELECTION 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the front panel trigger line is received. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>FTG2</th><th>FTG1</th><th>FTG0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>15</td><td>LMT ENA</td><td>LIMIT TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when a limit violation is detected by the DSP. Setting this bit to a one enable the trigger source and a zero disables the source.</td></tr>
<tr><td>14-12

14-12</td><td>LMT2-0

LMT2-0</td><td>LIMIT TRIGGER SELECTION 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the DSP detects a limit violation. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>LMT2</th><th>LMT1</th><th>LMT0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>11</td><td>SYN ENA</td><td>SYNCHRONIZATION TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when a SYNC pulse is applied to the Sigma-Delta ADCs. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>10-8</td><td>SYN2-0</td><td>SYNCHRONIZATION TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI Trigger line is asserted when a SYNC pulse is applied to the Sigma-Delta ADCs. The binary combination of these bits indicates the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>SYN2</th><th>SYN1</th><th>SYN0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>7</td><td>PPF ENA</td><td>PING-PONG FLIP TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger line when the Ping-Pong Buffer switches from one section to the next. This signal is synchronous to the Sample Clock signal, but may not occur at exactly the same moment. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>6-4

6-4</td><td>PPF2-0

PPF2-0</td><td>PING-PONG FLIP TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the Ping-Pong Buffer switches from one section to the next. The binary combination of these bits indicates the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>PPF2</th><th>PPF1</th><th>PPF0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td>3</td><td>SCK ENA</td><td>SAMPLE CLOCK TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger line based on the Sample Clock. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>2-0</td><td>SCK2-0</td><td>SAMPLE CLOCK TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the Sample Clock cycles. The binary combination of these bits indicates VXI TTL Trigger Line to generate according to the
<table>
<tr><th>SCK2</th><th>SYN1</th><th>SYN0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
</table>

Group B Trigger Source Register

The Group B Trigger Source Register is a write/read register located at an offset of 0x08 from the base address of the V200 Operational Registers. This register is used for configuring the TTL trigger lines that are asserted by the V200 for various events. The data in this register is used for allocating trigger lines for Group A. The trigger lines may be driven by any of the following sources:

1.) Front Panel Trigger Input B
2.) Limit Violation in Group B Channels
3.) Synchronization Pulse to Group B Sigma-Delta ADCs
4.) Flip of Group B Ping-Pong Buffer
5.) Group B Sample Clock

Each source for generating a TTL trigger consists of an enable bit and a three bit binary pattern to determine which trigger line to assert. The following diagram shows the bit pattern for the Group B Trigger Source Register along with a description of each bit location.

0x08	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	FTG ENA	FTG 2	FTG 1	FTG 0

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	LMT ENA	LMT 2	LMT 1	LMT 0	SYN ENA	SYN 2	SYN 1	SYN 0	PPF ENA	PPF 2	PPF 1	PPF 0	SCK ENA	SCK 2	SCK 1	SCK 0

Bit(s)	Mnemonic	Meaning
31-20	Not Used	These bits are not used and read as zeros.
19	FTG ENA	FRONT PANEL TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when the front panel trigger line is asserted. Setting this bit to a one enables the trigger source and a zero disables the source.
18-16	FTG2-0	FRONT PANEL TRIGGER SELECTION 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the front panel trigger line is received. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.
18-16	FTG2-0	

FTG2	FTG1	FTG0	VXI Trigger Line
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>15</td><td>LMT ENA</td><td>LIMIT TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when a limit violation is detected by the DSP. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>14-12</td><td>LMT2-0</td><td>LIMIT TRIGGER SELECTION 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the DSP detects a limit violation. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>LMT2</th><th>LMT1</th><th>LMT0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>11</td><td>SYN ENA</td><td>SYNCHRONIZATION TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger when a SYNC pulse is applied to the Sigma-Delta ADCs. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>10-8

10-8</td><td>SYN2-0

SYN2-0</td><td>SYNCHRONIZATION TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI Trigger line is asserted when a SYNC pulse is applied to the Sigma-Delta ADCs. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.
<table>
<tr><th>SYN2</th><th>SYN1</th><th>SYN0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>7</td><td>PPF ENA</td><td>PING-PONG FLIP TRIGGER ENABLE is a write/read bit used to</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>enable the generation of a VXI TTL Trigger line when the Ping-Pong Buffer switches from one section to the next. This signal is synchronous to the Sample Clock signal, but may not occur at exactly the same moment. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>6-4</td><td>PPF2-0</td><td>PING-PONG FLIP TRIGGER SELECT2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the Ping-Pong Buffer switches from one section to the next. The binary combination of these bits indicate the VXI TTL Trigger Line to generate according to the following table.

<table>
<tr><th>PPF2</th><th>PPF1</th><th>PPF0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>SCK ENA</td><td>SAMPLE CLOCK TRIGGER ENABLE is a write/read bit used to enable the generation of a VXI TTL Trigger line based on the Sample Clock. Setting this bit to a one enables the trigger source and a zero disables the source.</td></tr>
<tr><td>2-0</td><td>SCK2-0</td><td>SAMPLE CLOCK TRIGGER SELECT2 through 0 are write/read bits used to specify which VXI TTL Trigger line is asserted when the Sample Clock cycles. The binary combination of these bits indicate VXI TTL Trigger Line to generate according to the following table.</td></tr>
<tr><td>2-0</td><td>SCK2-0</td><td>
<table>
<tr><th>SCK2</th><th>SCK1</th><th>SCK0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
</table>

Group A Trigger Reception Register

The Group A Trigger Reception Register is a write/read register located at an offset of 0x0C from the base address of the V200 Operational Registers. This register is used to specify the VXI TTL Trigger Lines that are used to trigger various functions within the V200 for Group A. The TTL Trigger lines may be used to generate any or all of the following:

1.) Drive the internal Sample Clock of the V200 for Group A
2.) Start a Transient Capture for Group A
3.) Start a Multibuffer Acquisition for Group A
4.) Stop a Multibuffer Acquisition for Group A
5.) Arm a Synchronous Run for Group A
6.) Synchronize Group A ADCs

Each trigger function is composed of an enable bit along with a three-bit pattern for specifying the VXI TTL Trigger line to be used to initiate the function. The following diagram shows the bit layout for Group A Trigger Reception Register.

0x0C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	SYN ENA	SYN 2	SYN 1	SYN 0	ASR ENA	ASR 2	ASR 1	ASR 0

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	SPM ENA	SPM 2	SPM 1	SPM 0	STM ENA	STM 2	STM1	STM 0	XST ENA	XST 2	XST 1	XST 0	RSK ENA	RSK 2	RSK 1	RSK 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-24	Not Used	These bits are not used and read as zeros.
23	SYN ENA	SYNCHRONIZE ENABLE is a write/read bit used to enable a preselected trigger line to synchronize the Group A ADCs. Once enabled, the assertion of the trigger line causes the ADCs in Group A to be synchronized that provides simultaneous sampling.
22-20	SYN2-0	SYNCHRONIZE TRIGGER 2 through 0 are write/read bits used to select which VXI TTL Trigger line is used to synchronize the Group A ADCs. The binary combination of these bits indicate which VXI TTL Trigger line to receive according to the following table.

SYN2	SYN1	SYN0	VXI Trigger Line
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td>19</td><td>ASR ENA</td><td>ARM SYNCHRONOUS RUN ENABLE is a write/read bit used to enable the arming of the RUN mode of the V200. Once armed, the V200 enters the RUN mode when the selected trigger occurs. The Trigger can be driven by the Start Simultaneous Sampling bits 23-20 in the Group A Trigger Source Register if simultaneous sampling is required. Setting this bit to a one enables the arming trigger and a zero disables the trigger.</td></tr>
<tr><td>18-16</td><td>ASR2-0</td><td>ARM SYNCHRONOUS RUN TRIGGER 2 through 0 are write/read bits used to select which VXI TTL Trigger line is used to place the V200 into RUN mode. The binary combination of these bits indicates VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>ASR2</th><th>ASR1</th><th>ASR0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>15</td><td>SPM ENA</td><td>STOP MULTIBUFFER MODE TRIGGER ENABLE is a write/read bit used to enable the VXI TTL Trigger lines from stopping a multibuffer mode of acquisition. Setting this bit to a one enables the trigger lines and a zero disables the trigger.</td></tr>
<tr><td>14-12</td><td>SPM2-0</td><td>STOP MULTIBUFFER MODE TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to stop a multibuffer mode of data acquisition. The binary combination of these bits indicates the VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>SPM2</th><th>SPM1</th><th>SPM0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>11</td><td>STM ENA</td><td>START MULTIBUFFER MODE TRIGGER ENABLE is a write/read bit used to enable the VXI TTL Trigger lines from starting a multibuffer mode of acquisition. Setting this bit to a one enables the</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>trigger lines and a zero disables the trigger.</td></tr>
<tr><td>10-8</td><td>STM2-0</td><td>START MULTIBUFFER MODE TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to start a multibuffer mode of data acquisition. The binary combination of these bits indicates which VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>STM2</th><th>STM1</th><th>STM0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>7</td><td>XST ENA</td><td>TRANSIENT MODE TRIGGER ENABLE is a write/read bit used to enable a transient capture into multibuffer memory on the occurrence of a VXI TTL Trigger. This bit is set to a one to enable the trigger line input and a zero to disable the trigger.</td></tr>
<tr><td>6-4</td><td>XST2-0</td><td>TRANSIENT MODE TRIGGER SELECT2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to start a transient capture. The binary combination of these bits indicates which VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>XST2</th><th>XST1</th><th>XST0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>3</td><td>RSK ENA</td><td>RECEIVE SAMPLE CLOCK TRIGGER ENABLE is a write/read bit used to enable a VXI TTL Trigger line to source the internal Sample Clock of the V200. This bit is set to a one to enable the trigger input and a zero to disable the trigger.</td></tr>
<tr><td>2-0</td><td>RSK2-0</td><td>RECEIVE SAMPLE CLOCK TRIGGER SELECT2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to source the internal sample clock. The binary combination of these</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>bits indicates which VXI TTL Trigger Line to receive according to the following table.</td></tr>
<tr><td></td><td></td><td>
<table>
<tr><th>RSK2</th><th>RSK1</th><th>RSK0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
</table>

Group B Trigger Reception Register

The Group B Trigger Reception Register is a write/read register located at an offset of 0x10 from the A32 base address of V200 Operational Registers. This register is used to specify the VXI TTL Trigger Lines that are used to trigger various functions within the V200 for Group B. The TTL Trigger lines may be used to generate any or all of the following:

1.) Drive the internal Sample Clock of the V200 for Group B
2.) Start a Transient Capture for Group B
3.) Start a Multibuffer Acquisition for Group B
4.) Stop a Multibuffer Acquisition for Group B
5.) Arm a Synchronous Run for Group B
6.) Synchronize Group B ADCs

Each trigger function is composed of an enable bit along with a three-bit pattern for specifying the VXI TTL Trigger line to be used to initiate the function. The following diagram shows the bit layout for Group A Trigger Reception Register.

0x10	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	SYN ENA	SYN 2	SYN 1	SYN 0	ASR ENA	ASR 2	ASR 1	ASR 0

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	SPM ENA	SPM 2	SPM 1	SPM 0	STM ENA	STM 2	STM1	STM 0	XST ENA	XST 2	XST 1	XST 0	RSK ENA	RSK 2	RSK 1	RSK 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-24	Not Used	These bits are not used and read as zeros.
23	SYN ENA	SYNCHRONIZE ENABLE is a write/read bit used to enable a preselected trigger line to synchronize the Group B ADCs. Once enabled, the assertion of the trigger line causes the ADCs in Group B to be synchronized that provides simultaneous sampling.
22-20	SYN2-0	SYNCHRONIZE TRIGGER 2 through 0 are write/read bits used to select which VXI TTL Trigger line is used to synchronize the Group B ADCs. The binary combination of these bits indicates which VXI TTL Trigger line to receive according to the following table.

SYN2	SYN1	SYN0	VXI Trigger Line
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td>19</td><td>ASR ENA</td><td>ARM SYNCHRONOUS RUN ENABLE is a write/read bit used to enable the arming of the RUN mode of the V200. Once armed, the V200 enters the RUN mode when the selected trigger occurs. The Trigger can be driven by the Start Simultaneous Sampling bits 23-20 in Group B Trigger Source Register if simultaneous sampling is required. Setting this bit to a one enables the arming trigger and a zero disables the trigger.</td></tr>
<tr><td>18-16</td><td>ASR2-0</td><td>ARM SYNCHRONOUS RUN TRIGGER 2 through 0 are write/read bits used to select which VXI TTL Trigger line is used to place the V200 into RUN mode. The binary combination of these bits indicates VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>ASR2</th><th>ASR1</th><th>ASR0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>15</td><td>SPM ENA</td><td>STOP MULTIBUFFER MODE TRIGGER ENABLE is a write/read bit used to enable the VXI TTL Trigger lines from stopping a multibuffer mode of acquisition. Setting this bit to a one enables the trigger lines and a zero disables the trigger.</td></tr>
<tr><td>14-12</td><td>SPM2-0</td><td>STOP MULTIBUFFER MODE TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to stop a multibuffer mode of data acquisition. The binary combination of these bits indicates VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>SPM2</th><th>SPM1</th><th>SPM0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>11</td><td>STM ENA</td><td>START MULTIBUFFER MODE TRIGGER ENABLE is a write/read bit used to enable the VXI TTL Trigger lines from starting a multibuffer mode of acquisition. Setting this bit to a one enables the</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>trigger lines and a zero disables the trigger.</td></tr>
<tr><td>10-8</td><td>STM2-0</td><td>START MULTIBUFFER MODE TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to start a multibuffer mode of data acquisition. The binary combination of these bits indicates which VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>STM2</th><th>STM1</th><th>STM0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>7</td><td>XST ENA</td><td>TRANSIENT MODE TRIGGER ENABLE is a write/read bit used to enable a transient capture into multibuffer memory on the occurrence of a VXI TTL Trigger. This bit is set to a one to enable the trigger line input and a zero to disable the trigger.</td></tr>
<tr><td>6-4</td><td>XST2-0</td><td>TRANSIENT MODE TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to start a transient capture. The binary combination of these bits indicates which VXI TTL Trigger Line to receive according to the following table.
<table>
<tr><th>XST2</th><th>XST1</th><th>XST0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table></td></tr>
<tr><td>3</td><td>RSK ENA</td><td>RECEIVE SAMPLE CLOCK TRIGGER ENABLE is a write/read bit used to enable a VXI TTL Trigger line to source the internal Sample Clock of the V200. This bit is set to a one to enable the trigger input and a zero to disable the trigger.</td></tr>
<tr><td>2-0</td><td>RSK2-0</td><td>RECEIVE SAMPLE CLOCK TRIGGER SELECT 2 through 0 are write/read bits used to specify which VXI TTL Trigger line is used to source the internal sample clock. The binary combination of these</td></tr>
</table>

<table>
<tr><th>Bit(s)</th><th>Mnemonic</th><th>Meaning</th></tr>
<tr><td></td><td></td><td>bits indicate which VXI TTL Trigger Line to receive according to the following table.</td></tr>
<tr><td></td><td></td><td>
<table>
<tr><th>RSK2</th><th>RSK1</th><th>RSK0</th><th>VXI Trigger Line</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>7</td></tr>
</table>
</td></tr>
</table>

Group A DSP Communication I/O Register

The Group A DSP Communication I/O Register is a write/read register located at an offset of 0x14 from the A32 base address of the V200 Operational Registers. This register is used to communicate data to and from the Group A DSP. To communicate with the Group A DSP, a write operation is executed to this register with the data set to a valid DSP operational code (opcode). This opcode defines specific instructions for the DSP to execute. Please refer to the DSP Opcodes section on page 70 for a list of valid DSP instructions.

When this register is written, the GROUP A DSP BUFFER FULL (GPA DSF) bit in the Control/Status Register is set to a one. The DSP senses the assertion of this bit and reads the Group A DSP Communication I/O Register. Once this register is read by the DSP, the GROUP A DSP BUFFER FULL bit in the Control/Status Register is reset to a zero. Once the DSP reads the register, it performs the requested operation and returns a status value in the Group A DSP Communication I/O Register. When the DSP writes to the Group A DSP Communication I/O Register, the GPA VXI BUFFER FULL bit in the Control/Status Register is set to a one. The host computer must then sense the assertion of this bit prior to reading the data in the Group A DSP Communication I/O Register. Once the data in the Group A DSP Communication I/O Register is read, the GROUP A VXI BUFFER FULL bit is reset to zero.

Note that a read of this register does not return the last value written. The data read from this register is the last value written to this register by the DSP.

The following diagram shows the bit pattern for the Group A DSP Communication I/O Register.

0x14	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	GPA C15	GPA C14	GPA C13	GPA C12	GPA C11	GPA C10	GPA C9	GPA C8	GPA C7	GPA C6	GPA C5	GPA C4	GPA C3	GPA C2	GPA C1	GPA C0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-16	Not Used	These bits are not used and read as zeros.
15-0	GPA C15-C0	GROUP A DSP COMMUNICATION I/O 15 through 0 are write/read bits used to transfer information between a VXI host computer and the Group A DSP of the V200.

Group B DSP Communication I/O Register

The Group B DSP Communication I/O Register is a write/read register located at an offset of 0x18 from the A32 base address of the V200 Operational Registers. This register is used to communicate data to and from the Group B DSP. To communicate with the Group B DSP, a write operation is executed to this register with the data set to a valid DSP operational code (opcode). This opcode defines specific instructions for the DSP to execute. Please refer to the DSP Opcodes section on page 70 for a list of valid DSP instructions.

When this register is written, the GROUP B DSP BUFFER FULL (GPB DSF) bit in the Control/Status Register is set to a one. The DSP senses the assertion of this bit and reads the Group B DSP Communication I/O Register. Once this register is read by the DSP, the GROUP B DSP BUFFER FULL bit in the Control/Status Register is reset to a zero. Once the DSP reads the register, is performs the requested operation and returns a status value in the Group B DSP Communication I/O Register. When the DSP writes to the Group B DSP Communication I/O Register, the GPB VXI BUFFER FULL bit in the Control/Status Register is set to a one. The host computer must then sense the assertion of this bit prior to reading the data in the Group B DSP Communication I/O Register. Once the data in the Group B DSP Communication I/O Register is read, the GROUP B VXI BUFFER FULL bit is reset to zero.

Note that a read of this register does not return the last value written. The data read from this register is the last value written to this register by the DSP.

The following diagram shows the bit pattern for the Group B DSP Communication I/O Register.

0x18	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	GPB C15	GPB C14	GPB C13	GPB C12	GPB C11	GPB C10	GPB C9	GPB C8	GPB C7	GPB C6	GPB C5	GPB C4	GPB C3	GPB C2	GPB C1	GPB C0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-16	Not Used	These bits are not used and read as zeros.
15-0	GPB C15-C0	GROUP B DSP COMMUNICATION I/O 15 through 0 are write/read bits used to transfer information between a VXI host computer and the Group B DSP of the V200.

Group A Multibuffer End Address Register

The Group A Multibuffer End Address is a write/read register located at an offset of 0x20 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. The register is used to specify the entire length of the multibuffer memory. This effectively sets the size of the circular buffer for storing digitized data.

The data loaded into this register must not exceed the physical size of the buffer. The data for the Multibuffer Interval Counter multiplied by the number of buffer segments must not be greater than the size of the DRAM array. The following chart shows the maximum values loaded into the Multibuffer End Address Register for the various multibuffer sizes.

Multibuffer Size	Max. Multibuffer End Address Value
4 Megabytes (1M Longwords)	0x000FFFFF
16 Megabytes (4M Longwords)	0x003FFFFF

The data value written into the Multibuffer End Address Register is the last longword memory location written to with digitized data. After the buffer memory address specified in this register is written with digitized data , the digitized data storage address is reset to zero and data storage continues. The data loaded in this register does not need to be the last physical location of the DRAM. It can be set to any value less than the maximum value as long as the buffer is evenly divisible by the number of segments in use.

The following diagram shows the bit layout for the Multibuffer End Address Register.

0x20	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	BEA 21	BEA 20	BEA 19	BEA 18	BEA 17	BEA 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	BEA 15	BEA 14	BEA 13	BEA 12	BEA 11	BEA 10	BEA 9	BEA 8	BEA 7	BEA 6	BEA 5	BEA 4	BEA 3	BEA 2	BEA 1	BEA 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	BEA21-0	GROUP A MULTIBUFFER END ADDRESS 21 THROUGH 0 are write/read bits used to specify the entire length of the multibuffer memory.

Group A Multibuffer Segment Size Register

The Group A Multibuffer Segment Size Register is a write/read register located at an offset of 0x24 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. This register is used to specify the size of each segment in the multibuffer for Group A ADC channels. This value is the number of longwords (32-bit words) that are written to the multibuffer memory with digitized data before the segment is considered full. Once a buffer segment has been filled with digitized data, the next sequential multibuffer flag bit is set to a one. As additional multibuffer segments are filled, an incremental flag bit is set. This continues until the Multibuffer End Address is reached, at which time the digitized data storage memory address is reset to zero and the internal flag counter is reset to zero. After the Multibuffer End Address is reached, the next buffer segment filled causes the first flag to again be set.

The individual buffer segment size can be calculated using the following relationship:

$$MB\ Segment\ Size = ((MB\ End\ Address + 1) \div (\#\ of\ Desired\ Buffer\ Segments))$$

Note that the Multibuffer Segment Size in the above expression is the value that is to be loaded into the Multibuffer Segment Size Register. For example, assume a 4 Megabyte (1M Longwords) multibuffer is to be split into 4 segments, each segment containing 1 Megabyte. For this example, the Multibuffer End Address Register is loaded with data of 0x000FFFFF, indicating that the entire DRAM is used. The data to be loaded into the Multibuffer Segment Size Register is then calculated as follows:

$$Multibuffer\ Segment\ Size = ((0x000FFFFF + 1) \div (4))$$

resulting in a Multibuffer Segment Size = 0x00040000.

Using these values for the multibuffer setup, the multibuffer flags would be set as follows:

Flag1, then
Flag2, then
Flag3, then
Flag4, then
Flag1, and so on until the multibuffer operation ceases.

The following diagram shows the bit layout for the Group A Multibuffer Segment Size Register.

0x24	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	MSS 21	MSS 20	MSS 19	MSS 18	MSS 17	MSS 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	MSS 15	MSS 14	MSS 13	MSS 12	MSS 11	MSS 10	MSS 9	MSS 8	MSS 7	MSS 6	MSS 5	MSS 4	MSS 3	MSS 2	MSS 1	MSS 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	MSS 21-0	GROUP A MULTIBUFFER SEGMENT SIZE 21 THROUGH 0 are write/read bits used to specify the individual segment size of the multibuffer.

Group A Post Trigger Count Register

The Group A Post Trigger Count Register is a write/read register located at an offset of 0x28 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. During transient capture modes of multibuffer operation, the Post Trigger Count Register is used to specify the number of complete ADC scans that the V200 executes after a trigger event is received. After the Post Trigger Count decrements to zero, the transient capture is complete and the corresponding TRANSIENT ENABLE bit in the Control/Status Register is cleared. The following diagram shows the bit layout for the Group A Post Trigger Count Register.

0x28	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	PTG 21	PTG 20	PTG 19	PTG 18	PTG 17	PTG 16

( ) Power Up Value

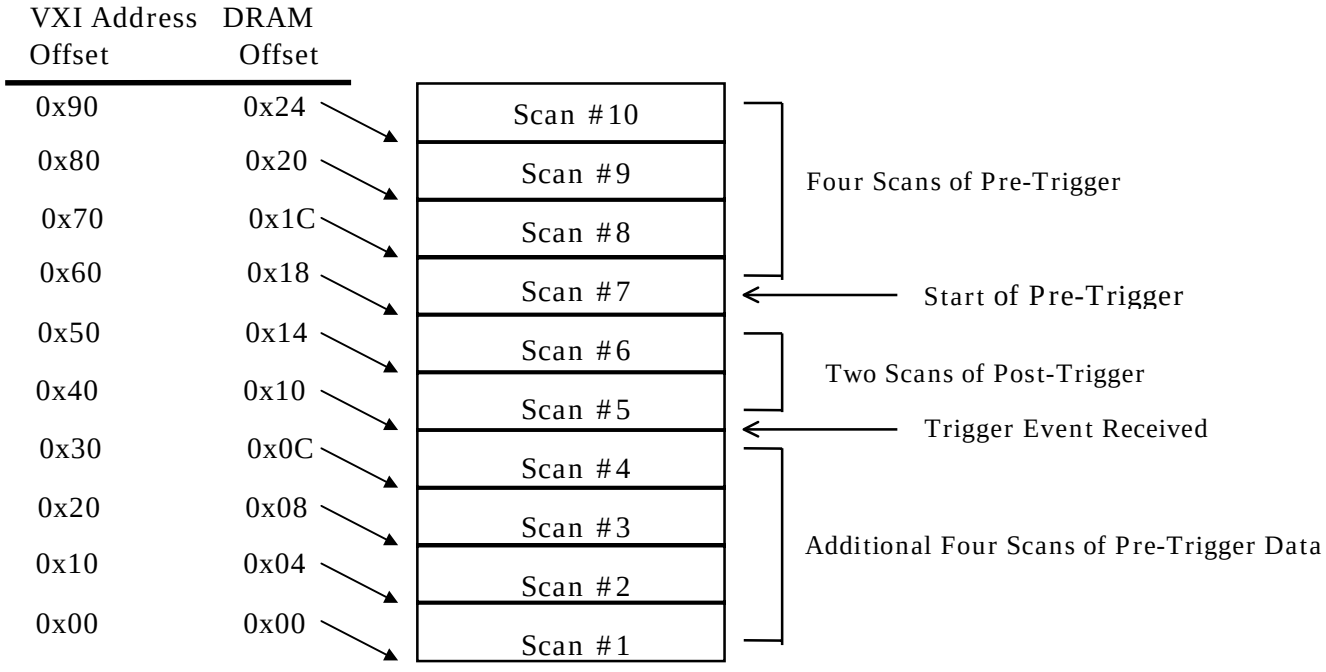
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	PTG 15	PTG 14	PTG 13	PTG 12	PTG 11	PTG 10	PTG 9	PTG 8	PTG 7	PTG 6	PTG 5	PTG 4	PTG 3	PTG 2	PTG 1	PTG 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	PTG 21-0	POST TRIGGER 21 THROUGH 0 are write/read bits that serve a dual purpose on the V200. When using the transient trigger mode of the V200, this register is used to specify the number of complete ADC scans stored into the multibuffer before the operation ceases.

Group A Trigger Address Register

The Group A Trigger Address Register is a read-only register located at an offset of 0x2C from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer for data storage and is used for transient capture modes of operation. After a trigger event is encountered during a transient operating mode, the V200 latches the DRAM storage address of the first digitized data element after the trigger occurs. This value is then used for determining the readout of the multibuffer for pre-trigger and post-trigger data. As an example, assume that 8 channels for a group are enabled and the digitized data is being stored in the multibuffer memory. For this example, the buffer is to hold 10 scans of each channels' ADC data. This buffer requires 80 16-bit words or 40 32-bit words of DRAM. The Multibuffer End Address must then be set to (40 - 1), or 39 (0x27). The Post Trigger Counter for this example is then set to 2. After a trigger event is received by the V200, the DRAM address at the time of the trigger is stored in the Trigger Address Register and the multibuffer continues to store data for two additional ADC scans as programmed in the Post Trigger Count Register. The address recorded in the Trigger Address Register is always on a scan boundary. After the transient event completes, the Trigger Address Register must be read to determine the point at which the trigger occurred. If the Trigger Address Register contained a value of 4, the initial address for readout would be at an offset of 16 (0x10) into the multibuffer. Since the address presented in the Trigger Address Register addresses longwords, the value must be multiplied by 4 to obtain the VXI offset in bytes. The multibuffer memory would then be read by incrementing the VXI longword address by four to retrieve the next longword of data. A total of 16 longwords ((16 channels times two) ÷ 2) would be read at sequential addresses to retrieve the two scans of post trigger data. The next 64 longwords ((16 channels times 8 scans) ÷ 2) read would then be the pre-trigger data. Note, that if during the readout process the address of the DRAM specified is beyond the programmed end of the buffer, the readout address must be set back to the beginning of the buffer. The following diagram illustrates the buffer showing pre-trigger and post-trigger data.



The following diagram shows the bit layout for the Group A Trigger Address Register.

0x2C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	TAD 21	TAD 20	TAD 19	TAD 18	TAD 17	TAD 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	TAD 15	TAD 14	TAD 13	TAD 12	TAD 11	TAD 10	TAD 9	TAD 8	TAD 7	TAD 6	TAD 5	TAD 4	TAD 3	TAD 2	TAD 1	TAD 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	TAD21-0	TRIGGER ADDRESS 21 THROUGH 0 are read-only bits used to reflect the DRAM address at which post-trigger data may be read. This address must be multiplied by 4 to calculate the VXI longword offset of the post-trigger data in the multibuffer.

Group A Multibuffer Control Register

The Group A Multibuffer Control Register is a write/read register located at an offset of 0x30 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. This register is used to configure and control various aspects of the multibuffer. The flag bits in this register are used to monitor the status of the multibuffer as it is filled with digitized data. A sequential flag is set when the Multibuffer Segment Size Register is counted down to zero, indicating that the preprogrammed number of digitized samples is available for readout. As additional segments of the multibuffer are filled, sequential flag bits are set to reflect the progress. The number of flags set before a rollover occurs and flag one is again set is determined by the setting of the Multibuffer End Address and the Multibuffer Segment Size. The Multibuffer End Address divided by the Multibuffer Segment Size determines the number of flags used. This result can range from one to eight.

The following diagram shows the bit layout of the Multibuffer Control Register.

0x30	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	XSN CMP	(0)	(0)	MBF ENA	(0)	(0)	CLR MBF	BUF OVN	FLG 7	FLG 6	FLG 5	FLG 4	FLG 3	FLG 2	FLG 1	FLG 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-16	Not Used	These bit are not used and read as zeros.
15	XSN CMP	TRANSIENT COMPLETE is a read-only bit used to indicate when a transient capture mode of operation has completed. The transient event is complete when the Multibuffer Post Trigger Counter decrements to zero.
14-13	Not Used	These bits are not used and must not be written to a one, they are read as zeros.
12	MBF ENA	MULTIBUFFER ENABLE is a read only bit used to indicate when multibuffer operation is enabled.
11-10	Not Used	These bits are not used and must not be written to a one, they are read as zeros.
9	CLR MBF	CLEAR MULTIBUFFER is a write only bit used to initialize the multibuffer memory. This bit, when written to a one, causes all the multibuffer flag bits to be cleared and initializes internal circuitry on the multibuffer. This bit should be set to a one prior to any continuous multibuffer acquisition or any transient capture

Bit(s)	Mnemonic	Meaning
		operation. This bit is not latched and read as a zero.
8	BUF OVN	BUFFER OVERRUN is a read/write-to-clear bit used to indicate when a segment of the multibuffer is overwritten before the host computer has read the segment. This overrun condition is typically caused by the host computer not sustaining the required data rate to read out the multibuffer memory segment before subsequent digitized data is stored in the segment. This bit is cleared by writing a one to this bit location or by setting the CLEAR MULTIBUFFER bit in this register.
7-0	FLG7-0	BUFFER FULL FLAG 7 through 0 are read/write-to-clear bits and are used to indicate when a particular segment of the multibuffer contains data available for readout. Once a flag is set, the host computer must read that segment of digitized data and clear the corresponding flag bit. The number of flag bits used for a multibuffer operation is determined by the dividing the Multibuffer End Address by the Multibuffer Segment Size. The result of this division indicates the number of the last flag set before the buffer rolls over and starts filling the lower buffer segment.

Group B Multibuffer End Address Register

The Group B Multibuffer End Address is a write/read register located at an offset of 0x40 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. The register is used to specify the entire length of the multibuffer memory. This effectively sets the size of the circular buffer for storing digitized data.

The data loaded into this register must not exceed the physical size of the buffer. The data for the Multibuffer Interval Counter multiplied by the number of buffer segments must not be greater than the size of the DRAM array. The following chart shows the maximum values loaded into the Multibuffer End Address Register for the various multibuffer sizes.

Multibuffer Size	Maximum Multibuffer End Address Value
4 Megabytes (1M Longwords)	0x000FFFFF
16 Megabytes (4M Longwords)	0x003FFFFF

The data value written into the Multibuffer End Address Register is the last longword memory location written to with digitized data. After the buffer memory address specified in this register is written with digitized data , the digitized data storage address is reset to zero and data storage continues. The data loaded in this register does not need to be the last physical location of the DRAM. It can be set to any value less than the maximum value as long as the buffer is evenly divisible by the number of segments in use.

The following diagram shows the bit layout for the Multibuffer End Address Register.

0x40	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	BEA 21	BEA 20	BEA 19	BEA 18	BEA 17	BEA 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	BEA 15	BEA 14	BEA 13	BEA 12	BEA 11	BEA 10	BEA 9	BEA 8	BEA 7	BEA 6	BEA 5	BEA 4	BEA 3	BEA 2	BEA 1	BEA 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	BEA21-0	GROUP A MULTIBUFFER END ADDRESS 21 THROUGH 0 are write/read bits used to specify the entire length of the multibuffer memory.

Group B Multibuffer Segment Size Register

The Group B Multibuffer Segment Size Register is a write/read register located at an offset of 0x44 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. This register is used to specify the size of each segment in the multibuffer for Group B ADC channels. This value is the number of longwords (32-bit words) that are written to the multibuffer memory with digitized data before the segment is considered full. Once a buffer segment has been filled with digitized data, the next sequential multibuffer flag bit is set to a one. As additional multibuffer segments are filled, an incremental flag bit is set. This continues until the Multibuffer End Address is reached, at which time the digitized data storage memory address is reset to zero and the internal flag counter is reset to zero. After the Multibuffer End Address is reached, the next buffer segment filled causes the first flag to again be set.

The individual buffer segment size can be calculated using the following relationship:

$$MB\ Segment\ Size = ((MB\ End\ Address + 1) \div (\#\ of\ Desired\ Buffer\ Segments))$$

Note that the Multibuffer Segment Size in the above expression is the value that is to be loaded into the Multibuffer Segment Size Register. For example, assume a 4 Megabyte (1M Longwords) multibuffer is to be split into 4 segments, each segment containing 1 Megabyte. For this example, the Multibuffer End Address Register is loaded with data of 0x000FFFFF, indicating that the entire DRAM is used. The data to be loaded into the Multibuffer Segment Size Register is then calculated as follows:

$$Multibuffer\ Segment\ Size = ((0x000FFFFF + 1) \div (4))$$

resulting in a Multibuffer Segment Size = 0x00040000.

Using these values for the multibuffer setup, the multibuffer flags would be set as follows:

Flag1, then
Flag2, then
Flag3, then
Flag4, then
Flag1, and so on until the multibuffer operation ceases.

The following diagram shows the bit layout for the Group B Multibuffer Segment Size Register.

0x44	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	MSS 21	MSS 20	MSS 19	MSS 18	MSS 17	MSS 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	MSS 15	MSS 14	MSS 13	MSS 12	MSS 11	MSS 10	MSS 9	MSS 8	MSS 7	MSS 6	MSS 5	MSS 4	MSS 3	MSS 2	MSS 1	MSS 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	MSS21-0	GROUP B MULTIBUFFER SEGMENT SIZE 21 THROUGH 0 are write/read bits used to specify the individual segment size of the multibuffer.

Group B Post Trigger Count Register

The Group B Post Trigger Count Register is a write/read register located at an offset of 0x48 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. During transient capture modes of multibuffer operation, the Post Trigger Count Register is used to specify the number of complete ADC scans that the V200 executes after a trigger event is received. After the Post Trigger Count decrements to zero, the transient capture is complete and the corresponding TRANSIENT ENABLE bit in the Control/Status Register is cleared.

The following diagram shows the bit layout for the Group B Post Trigger Count Register.

0x48	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	PTG 21	PTG 20	PTG 19	PTG 18	PTG 17	PTG 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	PTG 15	PTG 14	PTG 13	PTG 12	PTG 11	PTG 10	PTG 9	PTG 8	PTG 7	PTG 6	PTG 5	PTG 4	PTG 3	PTG 2	PTG 1	PTG 0

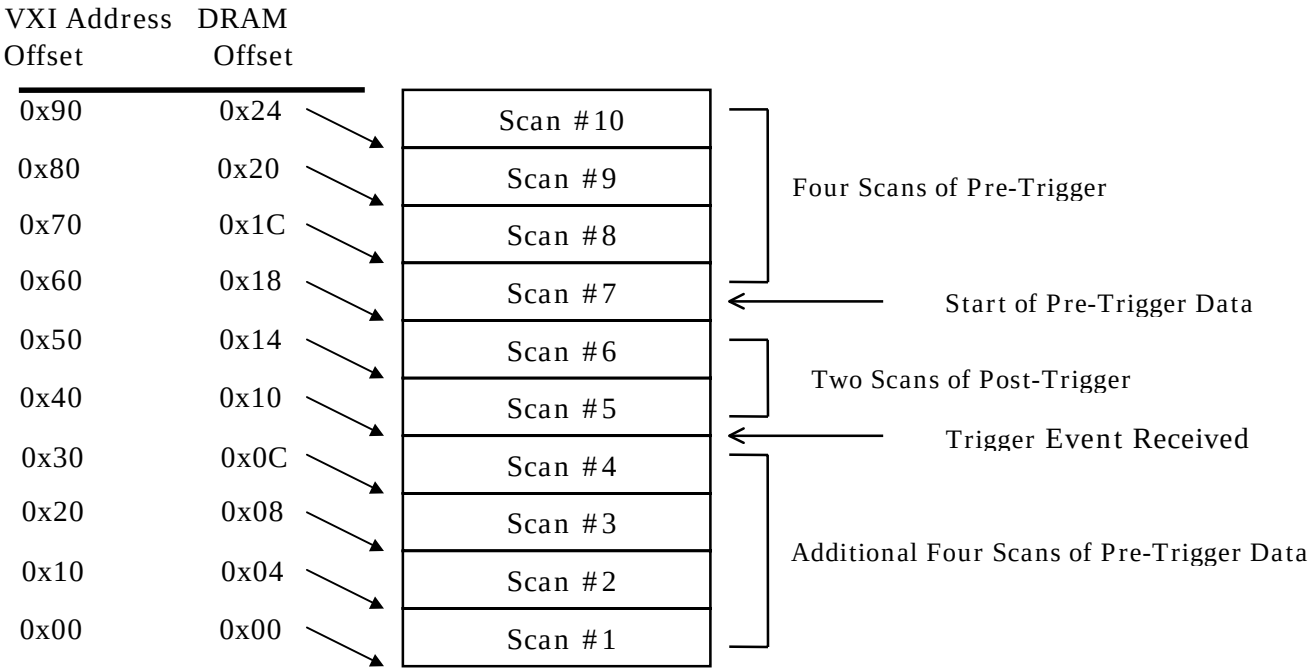
( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	PTG21-0	POST TRIGGER 21 THROUGH 0 are write/read bits that serve a dual purpose on the V200. When using the transient trigger mode of the V200, this register is used to specify the number of complete ADC scans stored into the multibuffer before the operation ceases.

Group B Trigger Address Register

The Group B Trigger Address Register is a read-only register located at an offset of 0x4C from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer for data storage and is used for transient capture modes of operation. After a trigger event is encountered during a transient operating mode, the V200 latches the DRAM storage address of the first digitized data element after the trigger occurs. This value is then used for determining the readout of the multibuffer for pre-trigger and post-trigger data.

As an example, assume that 8 channels for a group are enabled and the digitized data is being stored in the multibuffer memory. For this example, the buffer is to hold 10 scans of each channels' ADC data. This buffer requires 80 16-bit words or 40 32-bit words of DRAM. The Multibuffer End Address must then be set to 40 - 1, or 39 (0x27). The Post Trigger Counter for this example is then set to 2. After a trigger event is received by the V200, the DRAM address at the time of the trigger is stored in the Trigger Address Register and the multibuffer continues to store data for two additional ADC scans as programmed in the Post Trigger Count Register. The address recorded in the Trigger Address Register is always on a scan boundary. After the transient event completes, the Trigger Address Register must be read to determine the point at which the trigger occurred. If the Trigger Address Register contained a value of 4, the initial address for readout would be at an offset of 16 (0x10) into the multibuffer. Since the address presented in the Trigger Address Register addresses longwords, the value must be multiplied by 4 to obtain the VXI offset in bytes. The multibuffer memory would then be read by incrementing the VXI longword address by four to retrieve the next longword of data. A total of 16 longwords ((16 channels times two) ÷ 2) would be read at sequential addresses to retrieve the two scans of post trigger data. The next 64 longwords ((16 channels times 8 scans) ÷ 2) read would then be the pre-trigger data. Note, that if during the readout process the address of the DRAM specified is beyond the programmed end of the buffer, the readout address must be set back to the beginning of the buffer. The following diagram illustrates the buffer showing pre-trigger and post-trigger data.



The following diagram shows the bit layout for the Group B Trigger Address Register.

0x4C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	TAD 21	TAD 20	TAD 19	TAD 18	TAD 17	TAD 16

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	TAD 15	TAD 14	TAD 13	TAD 12	TAD 11	TAD 10	TAD 9	TAD 8	TAD 7	TAD 6	TAD 5	TAD 4	TAD 3	TAD 2	TAD 1	TAD 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-22	Not Used	These bits are not used and read as zeros.
21-0	TAD21-0	TRIGGER ADDRESS 21 THROUGH 0 are read-only bits used to reflect the DRAM address at which post-trigger data may be read. This address must be multiplied by 4 to calculate the VXI longword offset of the post-trigger data in the multibuffer.

Group B Multibuffer Control Register

The Group B Multibuffer Control Register is a write/read register located at an offset of 0x50 from the A32 base address of the V200 Operational Registers. This register is only available on V200s that contain a multibuffer card for data storage. This register is used to configure and control various aspects of the multibuffer. The flag bits in this register are used to monitor the status of the multibuffer as it is filled with digitized data. A sequential flag is set when the Multibuffer Segment Size Register is counted down to zero, indicating that the preprogrammed number of digitized samples is available for readout. As additional segments of the multibuffer are filled, sequential flag bits are set to reflect the progress. The number of flags set before a rollover occurs and flag one is again set is determined by the setting of the Multibuffer End Address and the Multibuffer Segment Size. The Multibuffer End Address divided by the Multibuffer Segment Size determines the number of flags used. This result can range from one to eight.

The following diagram shows the bit layout of the Multibuffer Control Register.

0x50	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R/W	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power Up Value

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R/W	XSN CMP	(0)	(0)	MBF ENA	(0)	(0)	CLR MBF	BUF OVN	FLG 7	FLG 6	FLG 5	FLG 4	FLG 3	FLG 2	FLG 1	FLG 0

( ) Power Up Value

Bit(s)	Mnemonic	Meaning
31-16	Not Used	These bit are not used and read as zeros.
15	XSN CMP	TRANSIENT COMPLETE is a read-only bit used to indicate when a transient capture mode of operation has completed. The transient event is complete when the Multibuffer Post Trigger Counter decrements to zero.
14-13	Not Used	These bits are not used and must not be written to a one, they are read as zeros.
12	MBF ENA	MULTIBUFFER ENABLE is a read only bit used to indicate when multibuffer operation is enabled.
11-10	Not Used	These bits are not used and must not be written to a one, they are read as zeros.
9	CLR MBF	CLEAR MULTIBUFFER is a write only bit used to initialize the multibuffer memory. This bit, when written to a one, causes all the multibuffer flag bits to be cleared and initializes internal circuitry on the multibuffer. This bit should be set to a one prior to any continuous multibuffer acquisition or any transient capture

Bit(s)	Mnemonic	Meaning
		operation. This bit is not latched and read as a zero.
8	BUF OVN	BUFFER OVERRUN is a read/write-to-clear bit used to indicate when a segment of the multibuffer is overwritten before the host computer has read the segment. This overrun condition is typically caused by the host computer not sustaining the required data rate to read out the multibuffer memory segment before subsequent digitized data is stored in the segment. This bit is cleared by writing a one to this bit location or by setting the CLEAR MULTIBUFFER bit in this register.
7-0	FLG7-0	BUFFER FULL FLAG 7 through 0 are read/write-to-clear bits and are used to indicate when a particular segment of the multibuffer contains data available for readout. Once a flag is set, the host computer must read that segment of digitized data and clear the corresponding flag bit. The number of flag bits used for a multibuffer operation is determined by the dividing the Multibuffer End Address by the Multibuffer Segment Size. The result of this division indicates the number of the last flag set before the buffer rolls over and starts filling the lower buffer segment.

Group A Ping-Pong Buffer Memory

The Group A Ping-Pong Buffer Memory is a read-only memory which starts at an offset of 0x4000 from the A32 base address of the V200 Operational Registers. This memory occupies offsets 0x4000 through 0x4024. This memory is used to store the digitized data from the Group A channels of the V200. This memory is dual-ported between the ADCs and VXI. This buffer is also split into two buffers, referred to as ping and pong. The digitized data from the ADCs fills one of the buffers while VXI reads out the other. The buffer storage/readout switches to the other half of the buffer when a sample clock occurs.

The number of elements stored in the ping-pong buffer depends on several factors. These factors include the number of active channels and whether the time tag is enabled. The number of actives channels that the V200 digitizes and stores in the ping-pong memory is setup through the DSP interface to the V200. Please refer to the DSP Opcodes section on page 70 of this manual for additional information.

Each ADC channel requires a 16-bit entry in the ping-pong buffer. If time tagging is enabled, a 32-bit value is entered into the ping-pong buffer Time tagging does not measure absolute time but is a 32-bit counter that is incremented at each sample clock. The counter is reset to zero when the V200 it taken out of run mode and is then enabled when the run mode is entered.

The following diagram shows a full ping-pong memory in which all 16-channels of Group A are used and time tagging is enabled.

	D31----------D0	
0x4000	ADC Channel 2	ADC Channel 1
0x4004	ADC Channel 4	ADC Channel 3
0x4008	ADC Channel 6	ADC Channel 5
0x400C	ADC Channel 8	ADC Channel 7
0x4010	ADC Channel 10	ADC Channel 9
0x4014	ADC Channel 12	ADC Channel 11
0x4018	ADC Channel 14	ADC Channel 13
0x401C	ADC Channel 16	ADC Channel 15
0x4020	Time Tag High	Time Tag Low

The previous diagram shows the 32-bit memory layout for a scan of data for 16 ADC channels and the time tag value. The V200 may also be configured to provide less than 16 channels of data in the ping-pong memory. If the number of channels to place in the ping-pong memory is an odd number, the ping-pong buffer is automatically realigned to a longword boundary before the time tag is inserted. The following diagram illustrates this function. The number of active channels for this diagram is 15.

	D31----------D0	
0x4000	ADC Channel 2	ADC Channel 1
0x4004	ADC Channel 4	ADC Channel 3
0x4008	ADC Channel 6	ADC Channel 5
0x400C	ADC Channel 8	ADC Channel 7
0x4010	ADC Channel 10	ADC Channel 9
0x4014	ADC Channel 12	ADC Channel 11
0x4018	ADC Channel 14	ADC Channel 13
0x401C	Not Used	ADC Channel 15
0x4020	Time Tag High	Time Tag Low

Group B Ping-Pong Buffer Memory

The Group B Ping-Pong Buffer Memory is a read-only memory which starts at an offset of 0x4040 from the A32 base address of the V200 Operational Registers. This memory occupies offsets 0x4040 through 0x4063. This memory is used to store the digitized data from the Group B channels of the V200. This memory is dual-ported between the ADCs and VXI. This buffer is also split into two buffers, referred to as ping and pong. The digitized data from the ADCs fills one of the buffers while VXI reads out the other. The buffer storage/readout switches to the other half of the buffer when a sample clock occurs.

The number of elements stored in the ping-pong buffer depends on several factors. These factors include the number of active channels and whether the time tag is enabled. The number of actives channels that the V200 digitizes and stores in the ping-pong memory is setup through the DSP interface to the V200. Please refer to the DSP Opcodes section of this manual for additional information.

Each ADC channel requires a 16-bit entry in the ping-pong buffer. If time tagging is enabled, a 32-bit value is entered into the ping-pong buffer. Time tagging does not measure absolute time but is a 32-bit counter that is incremented at each sample clock. The counter is reset to zero when the V200 it taken out of run mode and is then enabled when the run mode is entered.

The following diagram shows a full ping-pong memory in which all 16-channels of Group B are used and time tagging is enabled.

	D31----------D0	
0x4040	ADC Channel 2	ADC Channel 1
0x4044	ADC Channel 4	ADC Channel 3
0x4048	ADC Channel 6	ADC Channel 5
0x404C	ADC Channel 8	ADC Channel 7
0x4050	ADC Channel 10	ADC Channel 9
0x4054	ADC Channel 12	ADC Channel 11
0x4058	ADC Channel 14	ADC Channel 13
0x405C	ADC Channel 16	ADC Channel 15
0x4060	Time Tag High	Time Tag Low

The previous diagram shows the 32-bit memory layout for a scan of data for 16 ADC channels and the time tag value. The V200 may also be configured to provide less than 16 channels of data in the ping-pong memory. If the number of channels to place in the ping-pong memory is an odd number, the ping-pong buffer is automatically realigned to a longword boundary before the time tag is inserted. The following diagram illustrates this function. The number of active channels for this diagram is 15.

	D31----------D0	
0x4040	ADC Channel 2	ADC Channel 1
0x4044	ADC Channel 4	ADC Channel 3
0x4048	ADC Channel 6	ADC Channel 5
0x404C	ADC Channel 8	ADC Channel 7
0x4050	ADC Channel 10	ADC Channel 9
0x4054	ADC Channel 12	ADC Channel 11
0x4058	ADC Channel 14	ADC Channel 13
0x405C	Not Used	ADC Channel 15
0x4060	Time Tag High	Time Tag Low

Group A Flash Memory

The Group A Flash Memory is a write/read memory which starts at an offset of 0x80000 from the A32 base address of the V200 Operational Registers. This memory occupies offsets 0x80000 through 0xBFFFF.

This memory is used by the Group A DSP to download initial code to the Static RAM of the DSP. This flash memory provides an easy mechanism for providing updates to users in the field. This memory is not normally accessible to VXI. Five strap locations on the V200 must be jumpered in order to allow VXI access to this memory. Additional information regarding the use of the flash memory will accompany any updates sent from the factory.

Group B Flash Memory

The Group B Flash Memory is a write/read memory which starts at an offset of 0xC0000 from the A32 base address of the V200 Operational Registers. This memory occupies offsets 0xC0000 through 0xFFFFF.

This memory is used by the Group A DSP to download initial code to the Static RAM of the DSP. This flash memory provides an easy mechanism for providing updates to users in the field. This memory is not normally accessible to VXI. Five strap locations on the V200 must be jumpered in order to allow VXI access to this memory. Additional information regarding the use of the flash memory will accompany any updates sent from the factory.

Group A/B Multibuffer Memory

The Group A Multibuffer Memory is read-only memory which starts at an offset of 0x2000000 from the A32 base address of the V200 Operational Register. The Group B Multibuffer Memory is read-only memory which starts at an offset of 0x3000000 from the A32 base address of the V200 Operational Register. This size of this memory depends on the multibuffer memory option ordered. The buffer may be either 4 megabytes or 16 megabytes in length. The following chart shows the two memory options along with their addressing range offsets.

Group A:

Multibuffer Memory Size	A32 Address Offset Range
4 Megabytes (1M Longwords)	0x2000000 – 0x23FFFFC
16 Megabytes (4M Longwords)	0x2000000 – 0x2FFFFFC

Group B:

Multibuffer Memory Size	A32 Address Offset Range
4 Megabytes (1M Longwords)	0x3000000 – 0x33FFFFC

16 Megabytes (4M Longwords)	0x3000000 – 0x3FFFFFC

This memory contains the data digitized by the ADCs for both transient and continuous storage applications. The format of data storage in the multibuffer is shown in the following diagram. This example assumes that 8 channels of data are stored in multibuffer for a particular group.

	D31----------D0	
0x2000000	ADC Channel 2	ADC Channel 1
0x2000004	ADC Channel 4	ADC Channel 3
0x2000008	ADC Channel 6	ADC Channel 5
0x200000C	ADC Channel 8	ADC Channel 7
0x2000010	ADC Channel 2	ADC Channel 1
0x2000014	ADC Channel 4	ADC Channel 3
0x2000018	ADC Channel 6	ADC Channel 5
0x200001C	ADC Channel 8	ADC Channel 7
0x2000020	ADC Channel 2	ADC Channel 1

NOTE: When using multibuffer memory, only an even number of channels is allowed.

DSP Opcodes

The following is a list of opcodes the fixed point DSPs on the base card of the V200 for which the V200 will respond. For each opcode or value written to the Group A/B Communication I/O Register, the DSP will send a response back through the Communication I/O register. If data is available in the Communication I/O Register, the corresponding Groups' VXI Buffer Full bit is set in the Control/Status Register. In all cases, the response should be zero, but should a problem occur, the following are other responses the DSP might give.

Table 1 DSP Status Codes

Response	Meaning
0	**Operation Successful**.
-1	**Invalid Opcode**. The DSP was expecting an opcode instruction, but did not receive a valid opcode.
-2	**Invalid Clock Mode.** The DSP responds with this error return when a <mode> selection for an ADC Clock Selection Opcode is out of range or unsupported.
-3	**Invalid Frequency Range.** The DSP returns this error code when an ADC Clock Selection Opcode is executed and the <value> parameter for the selected mode is out of range.
-4	**Invalid Frequency Divisor.** The DSP responds with this error code when an ADC Clock Selection Opcode is executed and the <value> parameter specifies a clock rate divisor that is not supported.
-5	**Invalid Sample Period.** The DSP responds with this error code when an ADC Clock Selection Opcode us executed and the <value> parameter specifies a sample period outside of the legal range.
-6	**Invalid Clock Value.** This error is returned when the DSP is executing an ADC Clock Selection Opcode and the <value> parameter is indeterminate.
-7	**Invalid Channel.** The DSP returns this error code when a request is made to alter a particular channel and the channel specified is out of range.
-8	**Invalid Gain.** The DSP responds with this error code when a request is made to alter a channel' gain and the specification is out of range.
-9	**No Daughter Card.** The DSP responds with this error code when a request is made to alter a parameter on an expansion card and the expansion card is not supported or installed.
-10	**Not Supported by Group B.** The Group B DSP responds with this error code when a request is made to alter setup information and the operation is not supported by Group B.

General Purpose Opcodes:

Self-Test

Opcode = 0x01
Input type = None
Return type = None

This opcode will cause the DSP to perform a self-test. SYSFAIL will be asserted during the self-test, and cleared if self-test passed. (Note that each DSP has access to SYSFAIL and that if either self-test fail then SYSFAIL will remain asserted). While self-test is running the appropriate run light (A or B) will be on.

Return Self-Test Result

Opcode = 0x02
Input type = None
Return type = Unsigned 16 bit integers

This opcode will return the status plus 3 arrays of 10 words each. The words contain details of self-test performance.

For each of the 10 gain ranges, three input voltages are input into each channel, corresponding to positive full scale, zero input and negative full scale. Readings are taken for each case and the ADC value obtained is compared to predetermined test limits.

The first 10 words read (after reading back the status) correspond to the self-test results for positive full-scale voltages. The second set of 10 words correspond to the self-test results for negative full scale voltages, while the third set of 10 words correspond to the self-test results for zero volts applied.

A “zero” in a bit location means that the channel passed, a “one” means a failure. Within a word, each channel occupies one bit location such that channel 1 occupies bit location 0, channel 2 occupies location 1 etc.

The 10 words record results for the 10 gain ranges in increasing order, such that the first word contains results for gain equals 1, the second for gain equals 2 etc.

All 30 words must be read back.

Example:

posCalTest[0] = 0x0000	negCalTest[0] = 0x0000	zeroCalTest[0] = 0x0000
posCalTest[1] = 0x0000	negCalTest[1] = 0x0000	zeroCalTest[1] = 0x0000

posCalTest[2] = 0x00FF	**negCalTest[2] = 0x00FF**	zeroCalTest[2] = 0x0000
posCalTest[3] = 0x0000	negCalTest[3] = 0x0000	zeroCalTest[3] = 0x0000
posCalTest[4] = 0x0000	negCalTest[4] = 0x0000	zeroCalTest[4] = 0x0000
posCalTest[5] = 0x0000	negCalTest[5] = 0x0000	**zeroCalTest[5] = 0x0008**
posCalTest[6] = 0x0000	negCalTest[6] = 0x0000	zeroCalTest[6] = 0x0000
posCalTest[7] = 0x0000	negCalTest[7] = 0x0000	zeroCalTest[7] = 0x0000
posCalTest[8] = 0x0000	**negCalTest[8] = 0x0040**	zeroCalTest[8] = 0x0000
posCalTest[9] = 0x0000	negCalTest[9] = 0x0000	zeroCalTest[9] = 0x0000

These results would indicate that the first 8 channels failed both positive and negative full scale tests at a gain of 5 (third range), the seventh channel failed the negative full scale test at a gain of 500 and the fourth channel failed the zero volt test at a gain of 50.

Return Firmware Revision

Opcode = 0x03
Input type = None
Return type = Unsigned 16 bit integer

This opcode is used to return the current revision level of the firmware installed on the V200. This command returns one 16-bit value that reflects the revision level. Bits 04-07 contain the major revision level and bits 00-03 contain the minor revision level.

Channel Setup

Opcode = 0x10 <*channel*> <*value*>
Input type = unsigned 16 bit integers
Return type = None

Channel number (0 - 15) = <*channel*>
An invalid channel entry will return a status value of 0xFFF9 (INVALID CHANNEL) or 0xFFF7 (NO DAUGHTER CARD).

Gain /Input Settings = <*value*>
An invalid value entry will return a status value of 0xFFF8 (INVALID GAIN).

The following is the bit layout for the Gain/Input Setting Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	CP1	CP0	G3	G2	G1	G0

The following chart shows the input selections based on the CP1 and CP0 bits.

CP1	CP0	Input Selection
0	0	Direct (DC)
0	1	AC Coupled
1	0	Calibration Signal
1	1	Analog Ground

Table 2 Input Path Selections

The following chart shows the gain selections based on the binary combinations of the G3 through G0 bits.

G3	G2	G1	G0	Gain
0	0	0	0	x1
0	0	0	1	x2
0	0	1	0	x5
0	0	1	1	x10
0	1	0	0	x20
0	1	0	1	x50
0	1	1	0	x100
0	1	1	1	x200
1	0	0	0	x500
1	0	0	1	x1000

Table 3 Gain Selections

Front End Active Channel Select

Opcode = 0x11 <*value*>
Input type = unsigned 16 bit integer
Return type = None

These registers are used for specifying the number of front-end active channels that are entered into the front-end FIFO after an ADC conversion occurs. The following diagram shows the bit layout of this register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

The CH8 through 1 bits correspond to the actual channels that each individual register addresses. Any bit set to a one enables the corresponding channel and a zero disables the channel. The CH16 through CH9 are only valid if the additional channels daughter card is in

use. Setting these bits when there is no daughter card will return a status of 0xFFF7 (NO DAUGHTER CARD).

Ping Pong Active Channel Select

Opcode = 0x12 <*value*>
Input type = unsigned 16 bit integer
Return type = None

This register is used for specifying how data is placed into the ping-pong buffer for a given group. The specification indicates the number of channels to take from the DSP output FIFO and placed in the Ping-Pong Memory (PPM). Once the appropriate number of channels has been read from each FIFO, the PPM will flip.

The register contains a specification for the number corresponding to the front end active channels set up. (opcode 0x11) The specification can range from 0 through 16.

The following diagram shows the bit layout of a Ping-Pong Active Channel Register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	PPA4	PPA3	PPA 2	PPA 1	PPA 0

PPA4 through 0 are used to specify the number of channels of data from the DSP output FIFO that is to be placed into the ping-pong memory before a ping-pong buffer flip occurs. The value range for this register is from 0 to 16.

ADC Clock Source Select

Opcode = 30_{16} <mode> <value>
Input type = unsigned 16 bit integer
Return type = None

This instruction is used to determine the clock source for the ADCs. The clock source may be generated from several sources. The Group A ADC clock source can come from an on-board clock source, a front panel supplied clock source, or by a TTL trigger line. In the various modes, either a sample clock or an oversampling clock is specified. The sample clock is the rate at which the ADCs on the V200 convert data. This can range from 5 kHz to 200 kHz. This sample clock is then multiplied by 64 by a Phase Lock Loop to generate the oversampling clock required by the ADCs. The oversampling clock specification is the rate at which the ADCs run. This rate is divided by 64 to determine the sampling rate.

The Group A ADCs can be configured to run from any of the aforementioned sources. The Group B ADCs can either be configured to run from either the Group A ADCs clock or run from an internal oscillator on the V200. This oscillator runs at 12.8Mhz, which provides the 200 kHz sampling rate (200Khz times 64) as full speed. A divisor specification can control the sampling rate for the ADCs down to 6.25 kHz.

The following modes are available for configuring the ADC clock sources for each Group. The mode entry in the first column of the table is used for the <mode> parameter. The <value> parameter for the instruction varies according to the <mode> selected.

Mode	Group A ADC Clock Source	Group B ADC Clock Source
0	Internal Sample Clock for Group A	Internal Oversampling Clock for Group B
1	Internal Sample Clock for Group A	Internal Sample Clock for Group A
2	Internal Oversampling Clock for Group A	Internal Oversampling Clock for Group B
3	Internal Oversampling Clock for Group A	Internal Oversampling Clock for Group A
4	External Sample Clock for Group A	Internal Oversampling Clock for Group B
5	External Sample Clock for Group A	External Sample Clock for Group A
6	External Oversampling Clock for Group A	Internal Oversampling Clock for Group B
7	External Oversampling Clock for Group A	External Oversampling Clock for Group A
8	TTL Trigger Line sample Clock for Group A	Internal Oversampling Clock for Group B
9	TTL Trigger Line sample Clock for Group A	TTL Trigger Line sample Clock for Group A

Table 4 Clock Modes

In Clock Select Modes 1, 3, 5, 7 and 9 the Group B ADC Clock Source Select instruction does not need to be executed since the Group A selection has connected its clock source to Group B. The remaining Clock Select Modes of 0, 2, 4, 6 and 8 require the ADC Clock Source Select instruction for Group B be executed with the appropriate mode selection <mode> and the <value> set to reflect the divisor for the 12.8 MHz clock. The following table shows the specification that yields the indicated sample rates. The value for the Clock Divisor Select in the following table is then placed in the <value> field for the ADC Clock Source Select instruction.

Clock Divisor Select	Clock Divisor	Oversample Clock Frequency	Sample Rate
0	1	12.8 MHz	200 kHz
1	2	6.4 MHz	100 kHz
2	4	3.2 MHz	50 kHz
3	8	1.6 MHz	25 kHz
4	16	800 kHz	12.5 kHz
5	32	400 kHz	6.25 kHz

Table 5 Oversample Clock Divisors

The following section describes how the V200 is configured for the 10 clock operating modes. The legal mode selections can range from 0 to 9. The <value> selection is determined by the type of clock mode. When a clock mode is selected that uses the internal crystal controlled clock oscillator, the <value> parameter describes the divisor applied to the 12.8 MHz clock. The previous chart shows the Clock Divisor Select that must be used for the <value> parameter.

When a clock mode is selected that uses the internal sample clock source, the <value> parameter specifies the number of 100 nanosecond increments between the period of the clock rate. This specification has an offset of 4 counts. For example, to select a 100Khz clock, this specification is set to 100 – 4 = 96.

When a clock mode is selected that uses an external source to supply a sample clock rate to the V200, the <value> parameter must be set to indicate the frequency range of the input signal. This parameter is used for both the TTL trigger line input and the front panel SMB input. The <value> parameter is shown in the following table.

External Sample Clock Rate Source Range	<value> parameter for the ADC Clock Source Select Instruction
100 kHz to 200 kHz	1
50 kHz to 99.99 kHz	2
25 kHz to 49.99 kHz	3
12.5 kHz to 24.99 kHz	4
6.25 kHz to 12.49 kHz	5
5 kHz to 6.24 kHz	6

Table 6 External Sample Clock Range

When the clock mode of 6 or 7 is selected to supply the oversampling clock rate for the

ADCs through the front panel SMB. At the same time, the 12.8 MHz clock is switched to the "ClockOut" SMB. The <value> is the divisor for the 12.8 MHz out. It is the same divisor value used in Table 5.

The following is a summary of the various clock-operating modes:

Mode 0: In this mode, the Group A clock uses the internal sample clock source. The <mode> parameter is set to 0x0000 and the <value> is set to the number of 100 nanosecond increments for the period of the sample rate minus 4. In this mode, the Group B clock uses the internal crystal controller oscillator as an oversampling clock source. The ADC Clock Source Select instruction must also be executed to Group B with the <mode> set to 0x0000 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5.

Mode 1: In this mode, the Group A and Group B clocks use the internal sample clock source. The <mode> parameter is set to 0x0001 and the <value> parameter is set to the number of 100 nanosecond increments for the period of the sample rate minus 4. In this mode, the Group B clock is routed from the Group A clock source. Therefore, the ADC Clock Source Select instruction does not need to be executed for Group B.

Mode 2: In this mode, the Group A clock uses the internal crystal controller oscillator as an oversampling clock source. The <mode> parameter is set to 0x0002 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5. In this mode, the Group B clock uses the internal crystal controller oscillator as an oversampling clock source. The ADC Clock Source Select instruction must also be executed to Group B with the <mode> set to 0x0002 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5.

Mode 3: In this mode, the Group A and Group B clocks use the internal crystal controller oscillator as an oversampling clock source. The <mode> parameter is set to 0x0003 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5. In this mode, the Group B clock is routed from the Group A clock source. Therefore, the ADC Clock Source Select instruction does not need to be executed for Group B.

Mode 4: In this mode, the Group A clock uses the front panel SMB as an input to generate the sample rate. The mode parameter is set to 0x0004 and the <value> parameter (chosen from Table 6) is set to reflect the frequency range of the input signal. In this mode, the Group B clock uses the internal crystal controller oscillator as an oversampling clock source. The ADC Clock Source Select instruction must also be executed to Group B with the <mode> set to 0x0004 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5.

Mode 5: In this mode, the Group A and Group B clocks use the front panel SMB as an input to generate the sample rate. The mode parameter is set to 0x0005 and the <value> parameter (chosen from Table 6) is set to reflect the frequency range of the input signal. In this mode, the Group B clock is routed from the Group A clock source. Therefore, the ADC

Clock Source Select instruction does not need to be executed for Group B.

Mode 6: In this mode, the Group A clock uses the front panel SMB as an input to generate the oversampling clock and switches a divided 12.8 MHz oversample clock to the Clock Out SMB. The mode parameter is set to 0x0006 and the <value> parameter is set to reflect the frequency divisor of clock out (See Table 5). In this mode, the Group B clock uses the internal crystal controller oscillator as an oversampling clock source. The ADC Clock Source Select instruction must also be executed to Group B with the <mode> set to 0x0006 and the <value> parameter set to the desired Clock Divisor Select chosen from Table 5.

Mode 7: In this mode, the Group A and Group B clocks use the front panel SMB as an input to generate the oversampling clock and switches a divided 12.8 MHz oversample clock to the Clock Out SMB. The mode parameter is set to 0x0007 and the <value> parameter is set to reflect the divisor of clock out (See Table 5). In this mode, the Group B clock is routed from the Group A clock source. Therefore, the ADC Clock Source Select instruction does not need to be executed for Group B.

Mode 8: In this mode, the Group A clock uses a preselected TTL trigger line to supply the sample rate. The <mode> parameter is set to 0x0008 and the <value> parameter is set to reflect the frequency range of the input signal. In this mode, the Group B clock uses the internal crystal controller oscillator as an oversampling clock source. The ADC Clock Source Select instruction must also be executed to Group B with the <mode> set to 0x0008 and the <value> parameter set to the desired Clock Divisor Select.

Mode 9: In this mode, the Group A and Group B clocks use a preselected TTL trigger line to supply the sample rate. The <mode> parameter is set to 0x0009 and the <value> parameter is set to reflect the frequency range of the input signal. In this mode, the Group B clock is routed from the Group A clock source. Therefore, the ADC Clock Source Select instruction does not need to be executed for Group B.

Synchronize ADCs

Opcode = 0x15
Input type = None
Return type = None

Executing this opcode causes the DSP to synchronize the ADCs in that group (A or B).

Enable/Disable Time Tag

Opcode = 0x1A <*value*>
Input type = unsigned 16 bit integer
Return type = None

<value> is 0 to disable or 1 to enable time tagging. Enabling this function causes the on-board time tag tick counter to be inserted into the data stream.

Synchronize Group A and Group B ADCs

Opcode = 0x1C
Input type = None
Return type = None

Executing this opcode causes the DSP to synchronize the ADCs in both Groups A and B.

Enable External Synchronize ADCs

Opcode = 0x1E
Input type = None
Return type = None

Executing this opcode enables an external event to synchronize the ADCs in that Group (A or B). A Sync to the ADCs (A or B) will be generated upon the receipt of the front panel Sync In or the pre-selected trigger as setup in that Group (A or B) Trigger Reception Register bits 23-20.

Enable External Synchronize Group A and Group B ADCs

Opcode = 0x1F
Input type = None
Return type = None

Executing this opcode enables an external event to synchronize the ADCs in both Group A and B. A Sync to both groups ADCs will be generated upon the receipt of the front panel Sync In or the pre-selected trigger as setup in the Group A and B Trigger Reception Register bits 32-20. This opcode provides the means by which you can synchronize the Group A and B ADCs across multiple V200s to achieve simultaneous sampling.

Calibration Opcodes

Reflect Serial Port data to Calibrator

Opcode = 0x100
Input type = None
Return type = None

This command applies only to DSP A. When enabled, DSP B can control the calibrator voltage by writing to its serial port. This happens automatically when Opcode 0x104 is executed to DSP B.

While DSP A is in this mode, no communication with DSP A is possible. This mode can be terminated by writing a zero to this port (writing a zero to DSP B via a 0x104 opcode).

Set Calibrator

Opcode = 0x104 <*value*>
Input type = unsigned 16 bit integer
Return type = None

The Calibration Register is used to apply a calibration voltage to the CALIBLO and CALIBHI internal signals on the V200. The following diagram shows the bit layout for this register.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	CAL 9	CAL 8	CAL 7	CAL 6	CAL 5	CAL 4	CAL 3	CAL 2	CAL 1	CAL 0

The CAL9 bit is used to select between the internal calibration reference and the external reference. This bit is set to a one to select the internal reference and a zero to select the external reference.

The CAL8 through 0 bits correspond to the signal inputs of the calibrator hybrid as follows:

CAL8 CAL-
CAL7 CAL+
CAL6 V.2
CAL5 V.5
CAL4 V1
CAL3 X.001
CAL2 X.01
CAL1 X.1
CAL0 X1

Calibration Voltage	Calibration Register Value (Internal Source)
+10.0 Volts	0x0291
+5.0 Volts	0x02A1
+2.0 Volts	0x02C1
+1.0 Volts	0x0292
+0.5 Volts	0x02A2
+0.2 Volts	0x02C2
+0.1 Volts	0x0294
+0.05 Volts	0x02A4
+0.02 Volts	0x02C4
+0.01 Volts	0x0298
+0.005 Volts	0x02A8
+0.002 Volts	0x02C8
-0.002 Volts	0x0348
-0.005 Volts	0x0328
-0.01 Volts	0x0318
-0.02 Volts	0x0344
-0.05 Volts	0x0324
-0.1 Volts	0x0314
-0.2 Volts	0x0342
-0.5 Volts	0x0322
-1.0 Volts	0x0312
-2.0 Volts	0x0341
-5.0 Volts	0x0321
-10.0 Volts	0x0311

Table 7 Calibration Register Values, Internal Source

This opcode is only used for debugging purposes. Normally the Calibrate Channels command (opcode 0x120) would be used.

Calibrate Channels

Opcode = 0x120
Input type = None
Return type = None

This command causes the DSP to calibrate all channels. The gain of the channels must be setup before executing this opcode.

This command causes the DSP to measure the transfer function of the channels and store the gain and offset of the channels as floating point values (M and B).

Return M and B
Opcode = 0x121
Input type = None
Return type = IEEE single precision floating point format (list of 16 bit unsigned integers)

Returns the transfer function of the channels in the form:

$$y = Mx + B$$

where y is in ADC counts and x is in volts.

This opcode returns a list of 32 unsigned integer values (for 8 channels) representing four integer values per channel.

For each channel the floating point value for M is built up from the first two integers, least significant word first. The next two integer words form the floating-point value for B.

The list looks like this:

unsigned integer (0)	Least significant word, M, channel 0
unsigned integer (1)	Most significant word, M, channel 0
unsigned integer (2)	Least significant word, B, channel 0
unsigned integer (3)	Most significant word, B, channel 0
unsigned integer (4)	Least significant word, M, channel 1
unsigned integer (5)	Most significant word, M, channel 1
unsigned integer (6)	Least significant word, B, channel 1
unsigned integer (7)	Most significant word, B, channel 1
.	.
.	.
.	.
.	.
.	.
unsigned integer (31)	Most significant word, B, channel 7

Limit Checking/Acquire Data Opcodes

Limit checking on the V200 is of the level/slope variety or minimum/maximum. If a signal crosses a predetermined level (threshold) in the appropriate direction (slope) then a limit event is generated. For minimum/maximum, a limit event is generated when the signal is greater than the maximum or less than or equal to the minimum. For sample clock speeds above 100 kHz, there are limitations to how limit checking is performed. The following tables show these different cases for Threshold/Slope and Min/Max.

Number of active channels per group	Limitation when sampling > 100kHz
13, 14, 15, or 16	Every fourth sample on the main card channels is checked and NO samples on the daughter card are checked.
9, 10, 11, or 12 with more than 4 active channels on the main card	Every fourth sample on the main card channels is checked and NO samples on the daughter card are checked.
9, 10, 11, or 12 with 4 or less active channels on the main card	Every other sample on the main card channels is checked and NO samples on the daughter card are checked.
8 channels all on the daughter card	Every other sample is checked.
8 channels all on the main card	Every other sample is checked
All other configurations	Every sample is checked

Table 8 Threshold/Slope Limit Checking Exceptions when sample rate > 100kHz

Number of active channels per group	Limitation when sampling > 100kHz
13, 14, 15 or 16	Every fourth sample is checked.
9, 10, 11 or 12	Every other sample is checked.
All other configurations	Every sample is checked.

Table 9 Minimum/Maximum Limit Checking Exceptions when sample rate > 100kHz

Set Threshold

Opcode = 0x224 <*channel*> <*value*>
Input type = unsigned 16 bit integers
Return type = None
This opcode sets the 16 bit limit value (corresponds to ADC counts). A count of 0xFFFF disables limit checking on a given channel. This is the default value.

Set Slope

Opcode = 0x226 <*channel*> <*value*>
Input type = unsigned 16 bit integers
Return type = None
This opcode sets the slope polarity: 0x0000 for a negative slope, 0xFFFF for a positive slope.

Acquire Data

Opcode = 0x280
Input type = None
Return type = None
This opcode causes the DSP to enter its data-taking mode. Limit checking is always performed on all active channels, however if the threshold value has been set to 0xFFFF a limit condition will never be generated.

The run light for the appropriate group (A or B) will turn on while data collection is occurring.

To exit this mode, execute any write to the communication port from the VXI bus.

Arm and Acquire Data

Opcode = 0x281
Input type = None
Return type = None

This opcode causes the DSP to enter its data taking mode once the preselected trigger line is asserted to place the selected group into Run mode. The selection is made through the Group A/Group B Trigger Reception Register. As with the Acquire Data Opcode, limit checking is always performed on all active channels, however if the threshold value has been set to 0xFFFF a limit condition will never be generated.

The run light for the appropriate group (A or B) will turn on while data collection is occurring.

To exit this mode, execute any write to the communication port from the VXI bus.

Set MAXIMUM

Opcode = 0x228 <*channel*> <*value*>
Input type = unsigned 16 bit integers
Return type = None

This opcode sets the 16-bit maximum limit value (corresponds to ADC counts). The default value is 0xFFFF.

Set MINIMUM

Opcode = 0x22A <*channel*> <*value*>
Input type = unsigned 16 bit integers
Return type = None

This opcode sets the 16-bit minimum limit value. The default value is 0x0000.

Acquire Data (MIN/MAX)

Opcode = 0x283
Input type = None
Return type = None

This opcode causes the DSP to enter its data-taking mode. Limit checking is always performed on all active channels, however if the maximum value has been set to 0xFFFF and minimum value set to 0x0000 a limit condition will never be generated.

The run light for the appropriate group (A or B) will turn on while data collection is occurring.

To exit this mode, execute any write to the communication port from the VXI bus.

Arm and Acquire Data(MIN/MAX)
Opcode = 0x284
Input type = None
Return type = None

This opcode causes the DSP to enter its data taking mode once the preselected trigger line is asserted to place the selected group into Run mode. The selection is made through the Group A/Group B Trigger Reception Register. As with the Acquire Data Opcode, limit checking is always performed on all active channels, however if the maximum value has been set to 0xFFFF and a minimum value set to 0x0000 a limit condition will never be generated.

The run light for the appropriate group (A or B) will turn on while data collection is occurring.

To exit this mode, execute any write to the communication port from the VXI bus.

Appendix A: Example Setup Procedures

Group A No Limit Checking Example

This setup example assumes an application requiring eight Group A channels to be active and sampling at a rate of 50 kHz. This procedure describes the steps necessary to setup and retrieve the data for this example.

1.) The first step in this example is to select the clock rate for the V200. A 50 kHz sampling rate is selected and both Groups are to run at the same rate. This corresponds to Mode 3 for the ADC clock selection.

Load the Clock Selection:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x0030 for the ADC Clock Source Select instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group A Communication I/O Register with the data set to 0x0003 to select clocking mode 3.
- Execute a write operation to the group A Communication I/O Register with the data set to two to select a 50 kHz sample clock rate (3.2 MHz oversampling clock).
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

2.) After the clock selection is made in step 1, setup each channels gain and input coupling by using the following sequence for each channel that is to be configured.

Setup Gain/Coupling for Each Channel:

- Execute a write operation to the Group A Communication I/O Registers with an Opcode of 0x0010 for the Channel Setup instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.

- Execute a write operation to the Group A Communication I/O Register with the data set to the desired channel that is to be altered.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.
- Execute a write operation to the group A Communication I/O Register with the data set to the desired gain/coupling value.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

3.) Now that all the preliminary operating parameters have been defined, the V200 must be calibrated. This is done by a two step process which includes executing the calibration and reading back the transfer function coefficients (Return M and B Values). Please note that when reading back the M and B values, all eight channels must be read back, even if Gain settings for the unused channels have not been specified.

Execute Calibration:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x0120 for the Calibrate Channels instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read Back the Transfer Function Coefficients:
- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x0121 for Return M and B.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.

Execute the following procedure for all eight channels:

- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the least significant 16-bits of the M value for the channel ready for readout.
- Read the Group A Communication I/O Register and retrieve the lower 16-bits of the M value for the channel.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the most significant 16-bits of the M value for the channel ready for readout.
- Read the Group A Communication I/O Register and retrieve the upper 16-bits of the M value for the channel.

- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the least significant 16-bits of the B value for the channel ready for readout.
- Read the Group A Communication I/O Register and retrieve the lower 16-bits of the B value for the channel.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the most significant 16-bits of the B value for the channel ready for readout.
- Read the Group A Communication I/O Register and retrieve the upper 16-bits of the B value for the channel.

4.) Now that the V200 has had the gain settings loaded, a calibration cycle executed and the transfer function read back, it is time to setup the V200 for acquiring data. The sequence is to Select Active Front End Channels, Select Ping-Pong Active Channels, Disabling Limit Checking and then enabling the V200 to acquire data. The following procedure executes these events.

Select Active Front End Channels:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x0011 for the Front-End Active Channel Select instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group A Communication I/O Register with data set to 0xFF to select channels 1 through 8 as active. This data is a bit mask, 1 bit for each active channel.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Select Ping Pong Active Channels:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x0012 for the Ping-Pong Active Channel Select instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.

- Execute a write operation to the Group A Communication I/O Register with data set to 0x0008 to select channels 1 through 8 from the main card as active. This data corresponds to enabling 8 active channels from the main card and 0 channels from the daughter card.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Disable Limit Checking:

- This is done by using the Set Threshold instruction with data set to 0xFFFF. The following procedure is used and must be executed for each channel:
- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x224 for the Set Threshold instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group A Communication I/O Register with data set to the channel number to be altered.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.
- Execute a write operation to the Group A Communication I/O Register with data set to 0xFFFF to disable limit checking.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Enable the V200 to Acquire Data:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x280 for the Acquire Data instruction.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.

At this point, the ADCs are converting data and placing the results in the Ping Pong Memory. Data can be retrieved from the V200 by reading the Ping-Pong memory. To read data asynchronously from the V200, the Ping-Pong memory may be read at any time. To ensure that no samples are missed from the ADCs, the Ping-Pong memory should be read

synchronously after each scan is completed. This can be done by using the interrupt capability of the V200 or by polling. The interrupt/polling mechanism should wait for the Group A Buffer Flip signal in the Interrupt Status Register before dumping the Ping Pong Memory. This ensures that a complete scan of each ADC channel has been entered into the memory and available for readout.

The following diagram shows how the data is stored in the Ping Pong Memory for this example.

	D31----------D0	
0x4000	ADC Channel 2	ADC Channel 1
0x4004	ADC Channel 4	ADC Channel 3
0x4008	ADC Channel 6	ADC Channel 5
0x400C	ADC Channel 8	ADC Channel 7
0x4010		
0x4014		
0x4018		
0x401C		
0x4020		

While the Group A DSP is busy moving data from the ADC FIFO to the Ping-Pong FIFO, it may not be interrupted to perform any commands. At this point, any write to the Group A Communication I/O Register causes the V200 to stop moving data.

Group B No Limit Checking Example

This setup example assumes an application requiring eight Group A channels to be active and sampling at a rate of 50 kHz. This procedure describes the steps necessary to setup and retrieve the data for this example. The most notable difference between this procedure and the one for Group A is that in order to calibrate Group B, the Group A DSP must be enabled to write to the Calibrator when the Group B DSP requests the update. This is done through a bi-directional serial port interface between the DSPs. Prior to Group B calibration, the group A DSP must be in a mode to Reflect Serial Port Data to Calibrator.

1.) The first step in this example is to select the clock rate for the V200. A 50 kHz sampling rate is selected and both Groups are to run at independent rates. In order for each Group to run at independent rates, the Group A Clock Selection Mode must be set to either mode 0,2,4,6 or 8. The Group B Clock Selection mode can then be set to either mode 0,2,4,6, or 8.

Load the Clock Selection:

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x0030 for the ADC Clock Source Select instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with the data set to 0x0000 to select clocking mode 0.
- Execute a write operation to the group B Communication I/O Register with the data set to two to select a 50 kHz sample clock rate (3.2 MHz oversampling clock).
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

1) After the V200 clock rate is selected in step 1, setup each channels gain and input coupling by using the following sequence for each channel that is to be configured.

- Execute a write operation to the Group B Communication I/O Registers with an Opcode of 0x10 for the Channel Setup instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with the data set to the desired channel that is to be altered.

- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.
- Execute a write operation to the Group B Communication I/O Register with the data set to the desired gain/coupling value.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted indicating that the DSP has responded to the data sent.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

2.) Now that all the preliminary operating parameters have been defined, the V200 must be calibrated. This is done by a two step process which includes executing the calibration and reading back the transfer function coefficients (Return M and B Values). Please note that when reading back the M and B values, all eight channels must be read back, even if Gain settings for the unused channels have not been specified. As previously noted, the Group A DSP must be placed in the Reflect Serial Port to Calibrator Mode.

Execute Calibration:

- Execute a write operation to the Group A Communication I/O Register with an Opcode of 0x100 to enable the Group A DSP to receive Calibration data from the serial port.
- Wait for the Group A VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group A Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x120 for the Calibrate Channels instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read back is a zero, indicating that the command was accepted.

Read Back the Transfer Function Coefficients:

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x121 for Return M and B.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.

Execute the following procedure for all eight channels:

- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the least significant 16-bits of the M value for the channel ready for readout.
- Read the Group B Communication I/O Register and retrieve the lower 16-bits of the M value for the channel.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the most significant 16-bits of the M value for the channel ready for readout.
- Read the Group B Communication I/O Register and retrieve the upper 16-bits of the M value for the channel.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the least significant 16-bits of the B value for the channel ready for readout.
- Read the Group B Communication I/O Register and retrieve the lower 16-bits of the B value for the channel.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has the most significant 16-bits of the B value for the channel ready for readout.
- Read the Group B Communication I/O Register and retrieve the upper 16-bits of the B value for the channel.

3.) Now that the V200 has had the gain settings loaded, a calibration cycle executed and the transfer function read back, it is time to setup the V200 for acquiring data. The sequence is to Select Active Front End Channels, Select Ping-Pong Active Channels, Disabling Limit Checking and then enabling the V200 to acquire data. The following procedure executes these events.

Select Active Front End Channels:

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x11 for the Front-End Active Channel Select instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with data set to 0xFF to select channels 1 through 8 as active. This data is a bit mask, 1 bit for each active channel. The data of 1 through 8 for Group B corresponds to V200 channels 9 through 16.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.

- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Select Ping Pong Active Channels:

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x12 for the Ping-Pong Active Channel Select instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with data set to 0x08 to select channels 1 through 8 from the main card as active. This data corresponds to enabling 8 active channels from the main card and 0 channels from the daughter card.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Disable Limit Checking:

This is done by using the Set Threshold instruction with data set to 0xFFFF. The following procedure is used and must be executed for each channel.

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x224 for the Set Threshold instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.
- Execute a write operation to the Group B Communication I/O Register with data set to the channel number to be altered.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.
- Execute a write operation to the Group B Communication I/O Register with data set to 0xFFFF to disable limit checking.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the data was accepted.

Enable the V200 to Acquire Data:

- Execute a write operation to the Group B Communication I/O Register with an Opcode of 0x280 for the Acquire Data instruction.
- Wait for the Group B VXI Buffer Full bit in the Control/Status Register to be asserted, indicating the DSP has responded to the request.
- Read the Group B Communication I/O Register and ensure that the data read is a zero, indicating that the command was accepted.

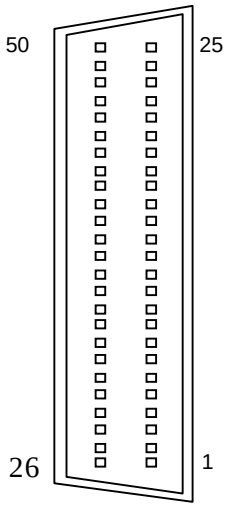
At this point, the ADCs are converting data and placing the results in the Ping Pong Memory. Data can be retrieved from the V200 by reading the Ping-Pong memory. To read data asynchronously from the V200, the Ping-Pong memory may be read at any time. To ensure that no samples are missed from the ADCs, the Ping-Pong memory should be read synchronously after each scan is completed. This can be done by using the interrupt capability of the V200 or by polling. The interrupt/polling mechanism should wait for the Group A Buffer Flip signal in the Interrupt Status Register before dumping the Ping Pong Memory. This ensures that a complete scan of each ADC channel has been entered into the memory and available for readout.

The following diagram shows how the data is stored in the Ping Pong Memory for this example.

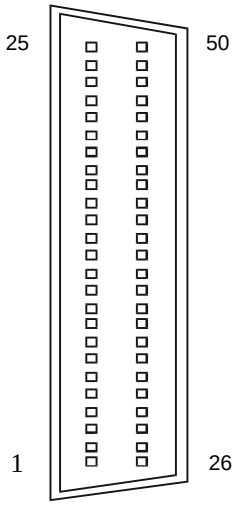
	D31----------D0	
0x4040	ADC Channel 10	ADC Channel 09
0x4044	ADC Channel 12	ADC Channel 11
0x4048	ADC Channel 14	ADC Channel 13
0x404C	ADC Channel 16	ADC Channel 15
0x4050		
0x4054		
0x4058		
0x405C		
0x4060		

While the Group B DSP is busy moving data from the ADC FIFO to the Ping-Pong FIFO, it may not be interrupted to perform any commands. At this point, any write to the Group B Communication I/O Register causes the V200 to stop moving data.

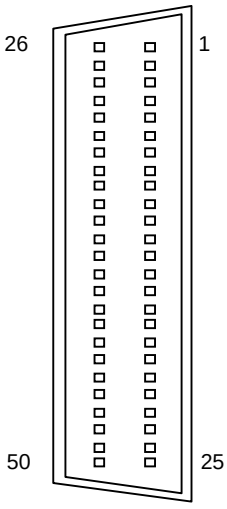
Appendix B: Connector Pinouts



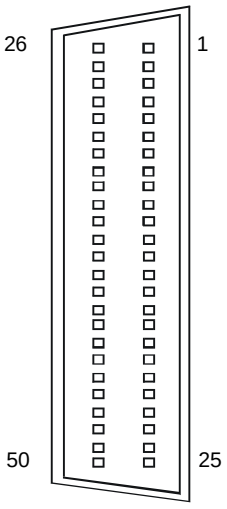
P3
Connector
Sockets



P3
Connector
Pins



P4
Connector
Pins



P4
Connector
Pins

Figure 9a - 50 Pin High Density Connector P3 and P4 for 16 channel V200

Figure 9b - 50 Pin High Density Connector P3 and P4 for 32 channel V200

Table 10 - 50 Pin High Density Connector: P4 Pinout

Pin Number	Signal Description	Pin Number	Signal Description
1	Group A - Channel 1 + Input	**26**	Group A - Channel 1 - Input
2	Ground	**27**	Ground
3	Group A - Channel 2 + Input	**28**	Group A - Channel 2 - Input
4	Group A - Channel 3 + Input	**29**	Group A - Channel 3 - Input
5	Ground	**30**	Ground
6	Group A - Channel 4 + Input	**31**	Group A - Channel 4 - Input
7	Group A - Channel 5 + Input	**32**	Group A - Channel 5 - Input
8	Ground	**33**	Ground
9	Group A - Channel 6 + Input	**34**	Group A - Channel 6 - Input
10	Group A - Channel 7 + Input	**35**	Group A - Channel 7 - Input
11	Ground	**36**	Ground
12	Group A - Channel 8 + Input	**37**	Group A - Channel 8 - Input
13	Group B - Channel 1 + Input	**38**	Group B - Channel 1- Input
14	Ground	**39**	Ground
15	Group B - Channel 2 + Input	**40**	Group B - Channel 2- Input
16	Group B - Channel 3 + Input	**41**	Group B - Channel 3- Input
17	Ground	**42**	Ground
18	Group B - Channel 4 + Input	**43**	Group B - Channel 4- Input
19	Group B - Channel 5 + Input	**44**	Group B - Channel 5- Input
20	Ground	**45**	Ground
21	Group B - Channel 6 + Input	**46**	Group B - Channel 6 - Input
22	Group B - Channel 7 + Input	**47**	Group B - Channel 7 - Input
23	+24 Volt Output (ICP)	**48**	Ground
24	Group B -Channel 8 + Input	**49**	Group B - Channel 8 - Input
25	Reference Input +	**50**	Reference Input -

Table 11 - 50 Socket High Density Connector: P3 Pinout for 16 Channel V200

Pin Number	Signal Description	Pin Number	Signal Description
1	Group A - Channel 1 + Output	**26**	Group A - Channel 1 - Output
2		**27**	
3	Group A - Channel 2 + Output	**28**	Group A - Channel 2 - Output
4	Group A - Channel 3 + Output	**29**	Group A - Channel 3 - Output
5		**30**	
6	Group A - Channel 4 + Output	**31**	Group A - Channel 4 - Output
7	Group A - Channel 5 + Output	**32**	Group A - Channel 5 - Output
8		**33**	
9	Group A - Channel 6 + Output	**34**	Group A - Channel 6 - Output
10	Group A - Channel 7 + Output	**35**	Group A - Channel 7 - Output
11		**36**	
12	Group A - Channel 8 + Output	**37**	Group A - Channel 8 - Output
13	Group B -Channel 1 + Output	**38**	Group B - Channel 1 - Output
14		**39**	
15	Group B - Channel 2 + Output	**40**	Group B - Channel 2 - Output
16	Group B - Channel 3 + Output	**41**	Group B - Channel 3 - Output
17		**42**	
18	Group B - Channel 4 + Output	**43**	Group B - Channel 4 - Output
19	Group B - Channel 5 + Output	**44**	Group B - Channel 5 - Output
20		**45**	
21	Group B - Channel 6 + Output	**46**	Group B - Channel 6 - Output
22	Group B - Channel 7 + Output	**47**	Group B - Channel 7 - Output
23		**48**	
24	Group B - Channel 8 + Output	**49**	Group B - Channel 8 - Output
25	Reference Output +	**50**	Reference Output -

Table 12 - 50 Pin High Density Connector: P3 Pinout for 32 Channel V200

Pin Number	Signal Description	Pin Number	Signal Description
1	Group A - Channel 9 + Input	**26**	Group A - Channel 9 - Input
2	Ground	**27**	Ground
3	Group A - Channel 10 + Input	**28**	Group A - Channel 10 - Input
4	Group A - Channel 11 + Input	**29**	Group A - Channel 11 - Input
5	Ground	**30**	Ground
6	Group A - Channel 12 + Input	**31**	Group A - Channel 12 - Input
7	Group A - Channel 13 + Input	**32**	Group A - Channel 13 - Input
8	Ground	**33**	Ground
9	Group A - Channel 14 + Input	**34**	Group A - Channel 14 - Input
10	Group A - Channel 15 + Input	**35**	Group A - Channel 15 - Input
11	Ground	**36**	Ground
12	Group A - Channel 16 + Input	**37**	Group A - Channel 16 - Input
13	Group B - Channel 9 + Input	**38**	Group B - Channel 9 - Input
14	Ground	**39**	Ground
15	Group B - Channel 10 + Input	**40**	Group B - Channel 10 - Input
16	Group B - Channel 11 + Input	**41**	Group B - Channel 11 - Input
17	Ground	**42**	Ground
18	Group B - Channel 12 + Input	**43**	Group B - Channel 12 - Input
19	Group B - Channel 13 + Input	**44**	Group B - Channel 13 - Input
20	Ground	**45**	Ground
21	Group B - Channel 14 + Input	**46**	Group B - Channel 14 - Input
22	Group B - Channel 15 + Input	**47**	Group B - Channel 15 - Input
23	Ground	**48**	Ground
24	Group B - Channel 16 + Input	**49**	Group B - Channel 16 - Input
25	Ground	**50**	Ground

VXI*bus* Connectors P1, P2 Pinouts

Table 13 - VXI*bus* P1 Connector

Pin number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin number
1	D00	BBSY*	D08	1
2	D01	BCLR*	D09	2
3	D02	ACFAIL*	D10	3
4	D03	BG0IN*	D11	4
5	D04	BG0OUT*	D12	5
6	D05	BG1IN*	D13	6
7	D06	BG1OUT*	D14	7
8	D07	BG2IN*	D15	8
9	GND	BG2OUT*	GND	9
10	SYSCLK	BG3IN*	SYSFAIL*	10
11	GND	BG3OUT*	BERR*	11
12	DS1*	BR0*	SYSRESET*	12
13	DS0*	BR1*	LWORD*	13
14	WRITE*	BR2*	AM5	14
15	GND	BR3*	A23	15
16	DTACK*	AM0	A22	16
17	GND*	AM1	A21	17
18	AS*	AM2	A20	18
19	GND	AM3	A19	19
20	IACK*	GND	A18	20
21	IACKIN*	SERCLK (1)	A17	21
22	IACKOUT*	SERDAT* (1)	A16	22
23	AM4	GND	A15	23
24	A07	IRQ7*	A14	24
25	A06	IRQ6*	A13	25
26	A05	IRQ5*	A12	26
27	A04	IRQ4*	A11	27
28	A03	IRQ3*	A10	28
29	A02	IRQ2*	A09	29
30	A01	IRQ1*	A08	30
31	-12 V	+5 V STDBY	+12 V	31
32	+5 V	+5 V	+5 V	32

Table 14 - VXI*bus* P2 Connector

Pin number	ROWa Signal Mnemonic	ROWb Signal Mnemonic	ROWc Signal Mnemonic	Pin number
1	ECLTRG0	+5 V	CLK10+	**1**
2	-2 V	GND	CLK10-	**2**
3	ECLTRIG1	RSV1	GND	**3**
4	GND	A24	-5.2 V	**4**
5	LBUSA00	A25	LBUSC00	**5**
6	LBUSA01	A26	LBUSC01	**6**
7	-5.2 V	A27	GND	**7**
8	LBUSA02	A28	LBUSC02	**8**
9	LBUSA03	A29	LBUSC03	**9**
10	GND	A30	GND	**10**
11	LBUSA04	A31	LBUSC04	**11**
12	LBUSA05	GND	LBUSC05	**12**
13	-5.2 V	+5 V	-2 V	**13**
14	LBUSA06	D16	LBUSC06	**14**
15	LBUSA07	D17	LBUSC07	**15**
16	GND	D18	GND	**16**
17	LBUSA08	D19	LBUSC08	**17**
18	LBUSA09	D20	LBUSC09	**18**
19	-5.2 V	D21	-5.2 V	**19**
20	LBUSA10	D22	LBUSC10	**20**
21	LBUSA11	D23	LBUSC11	**21**
22	GND	GND	GND	**22**
23	TTLTRG0*	D24	TTLTRG1*	**23**
24	TTLTRG2*	D25	TTLTRG3*	**24**
25	+5 V	D26	GND	**25**
26	TTLTRG4*	D27	TTLTRG5*	**26**
27	TTLTRG6*	D28	TTLTRG7*	**27**
28	GND	D29	GND	**28**
29	RSV2	D30	RSV3	**29**
30	MODID	D31	GND	**30**
31	GND	GND	+24 V	**31**
32	SUMBUS	+5 V	-24 V	**32**

Appendix C: Register Maps

Configuration Registers, A16 Space

The following diagram shows the registers located in the V200 along with their offsets from the A16 base address.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0x00	0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1
0x02	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
0x04	A32 ENA	Modid											Ready	Pass	Sys Inb.	Soft Reset
0x06	OFF 15	OFF 14	OFF 13	OFF 12	OFF 11	OFF 10										
0x08														IR*	IH*	IC*
0x0A	SER 31	SER 30	SER 29	SER 28	SER 27	SER 26	SER 25	SER 24	SER 23	SER 22	SER 21	SER 20	SER 19	SER 18	SER 17	SER 16
0x0C	SER 15	SER 14	SER 13	SER 12	SER 11	SER 10	SER 09	SER 08	SER 07	SER 06	SER 05	SER 04	SER 03	SER 02	SER 01	SER 00
0x0E	Firmware Version #				Firmware Revision #				Hardware Version #				Hardware Revision #			
0x10-18	**Reserved**															
0x1A	GPB XSNT CMPL	GPB BUF FULL	GPB LMT ALM	GPB BUF FLIP	GPA XSNT CMPL	GPA BUF FULL	GPA LMT ALM	GPA BUF FLIP	Logical Address							
0x1C	MSK GPB XCMP*	MSK GPB BFUL*	MSK GPB LMT*	MSK GPB BFLP*	MSK GPA XCMP*	MSK GPA BFUL*	MSK GPA LMT*	MSK GPA BFLP*	EN*		IRQ2	IRQ1	IRL0			
0x1E	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
0x20	**Suffix High Register**															
0x22	**Suffix Low Register**															
0x24 - 0x3E	**User Defined Registers**															

Operational Registers, A32 Space

The following register map is based on the default Motorola word packing format. If the Intel format is used then the high and low words in each 32-bit register are swapped.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0x00																
0x02		GPB STG	GPB ARM	GPB TRE	GPB MBE	GPB DSF	GPB VXF	GPB RUN		GPA STG	GPA ARM	GPA TRE	GPA MBE	GPA DSF	GPA VXF	GPA RUN
0x04													FTG ENA	FTG 2	FTG 1	FTG 0
0x06	LMT ENA	LMT 2	LMT 1	LMT 0	SYN ENA	SYN 2	SYN 1	SYN 0	PPF ENA	PPF 2	PPF 1	PPF 0	SCK ENA	SCK 2	SCK 1	SCK 0
0x08													FTG ENA	FTG 2	FTG 1	FTG 0
0x0A	LMT ENA	LMT 2	LMT 1	LMT 0	SYN ENA	SYN 2	SYN 1	SYN 0	PPF ENA	PPF 2	PPF 1	PPF 0	SCK ENA	SCK 2	SCK 1	SCK 0
0x0C													ASR ENA	ASR 2	ASR 1	ASR 0
0x0E	SPM ENA	SPM 2	SPM 1	SPM 0	STM ENA	STM 2	STM1	STM 0	XST ENA	XST 2	XST 1	XST 0	RSK ENA	RSK 2	RSK 1	RSK 0
0x10													ASR ENA	ASR 2	ASR 1	ASR 0
0x12	SPM ENA	SPM 2	SPM 1	SPM 0	STM ENA	STM 2	STM1	STM 0	XST ENA	XST 2	XST 1	XST 0	RSK ENA	RSK 2	RSK 1	RSK 0
0x14																
0x16	GPA C15	GPA C14	GPA C13	GPA C12	GPA C11	GPA C10	GPA C9	GPA C8	GPA C7	GPA C6	GPA C5	GPA C4	GPA C3	GPA C2	GPA C1	GPA C0
0x18																
0x1A	GPB C15	GPB C14	GPB C13	GPB C12	GPB C11	GPB C10	GPB C9	GPB C8	GPB C7	GPB C6	GPB C5	GPB C4	GPB C3	GPB C2	GPB C1	GPB C0
0x1C-1E	**Reserved**															
0x20											BEA 21	BEA 20	BEA 19	BEA 18	BEA 17	BEA 16
0x22	BEA 15	BEA 14	BEA 13	BEA 12	BEA 11	BEA 10	BEA 9	BEA 8	BEA 7	BEA 6	BEA 5	BEA 4	BEA 3	BEA 2	BEA 1	BEA 0
0x24											MSS 21	MSS 20	MSS 19	MSS 18	MSS 17	MSS 16
0x26	MSS 15	MSS 14	MSS 13	MSS 12	MSS 11	MSS 10	MSS 9	MSS 8	MSS 7	MSS 6	MSS 5	MSS 4	MSS 3	MSS 2	MSS 1	MSS 0
0x28											PTG 21	PTG 20	PTG 19	PTG 18	PTG 17	PTG 16
0x2A	PTG 15	PTG 14	PTG 13	PTG 12	PTG 11	PTG 10	PTG 9	PTG 8	PTG 7	PTG 6	PTG 5	PTG 4	PTG 3	PTG 2	PTG 1	PTG 0
0x2C											TAD 21	TAD 20	TAD 19	TAD 18	TAD 17	TAD 16
0x2E	TAD 15	TAD 14	TAD 13	TAD 12	TAD 11	TAD 10	TAD 9	TAD 8	TAD 7	TAD 6	TAD 5	TAD 4	TAD 3	TAD 2	TAD 1	TAD 0
0x30-3C	**Reserved**															
0x40											BEA 21	BEA 20	BEA 19	BEA 18	BEA 17	BEA 16
0x42	BEA 15	BEA 14	BEA 13	BEA 12	BEA 11	BEA 10	BEA 9	BEA 8	BEA 7	BEA 6	BEA 5	BEA 4	BEA 3	BEA 2	BEA 1	BEA 0
0x44											MSS 21	MSS 20	MSS 19	MSS 18	MSS 17	MSS 16

0x46	MSS 15	MSS 14	MSS 13	MSS 12	MSS 11	MSS 10	MSS 9	MSS 8	MSS 7	MSS 6	MSS 5	MSS 4	MSS 3	MSS 2	MSS 1	MSS 0

0x48											PTG 21	PTG 20	PTG 19	PTG 18	PTG 17	PTG 16
0x4A	PTG 15	PTG 14	PTG 13	PTG 12	PTG 11	PTG 10	PTG 9	PTG 8	PTG 7	PTG 6	PTG 5	PTG 4	PTG 3	PTG 2	PTG 1	PTG 0
0x4C											TAD 21	TAD 20	TAD 19	TAD 18	TAD 17	TAD 16
0x4E	TAD 15	TAD 14	TAD 13	TAD 12	TAD 11	TAD 10	TAD 9	TAD 8	TAD 7	TAD 6	TAD 5	TAD 4	TAD 3	TAD 2	TAD 1	TAD 0
0x50																
0x52	XSN CMP						CLR MBF	BUF OVN	FLG 7	FLG 6	FLG 5	FLG 4	FLG 3	FLG 2	FLG 1	FLG 0
0x54-3FFE	**Reserved**															
0x4000 - 0x4022	**Group A Ping-Pong Buffer Memory**															
0x4024 - 0x403E	**Reserved**															
0x4040 - 0x4062	**Group B Ping-Pong Buffer Memory**															
0x4064 - 0x7FFFE	**Reserved**															
0x80000 - 0xBFFFE	**Group A Flash Memory**															
0xC0000 - 0xFFFFE	**Group B Flash Memory**															
0x100000 - 0x1FFFFE	**Reserved**															
0x2000000 - 0x2FFFFFE	**Group A Multibuffer Memory Data**															
0x3000000 - 0x3FFFFFE	**Group B Multibuffer Memory Data**															

Appendix D: Switch and Strap Locations

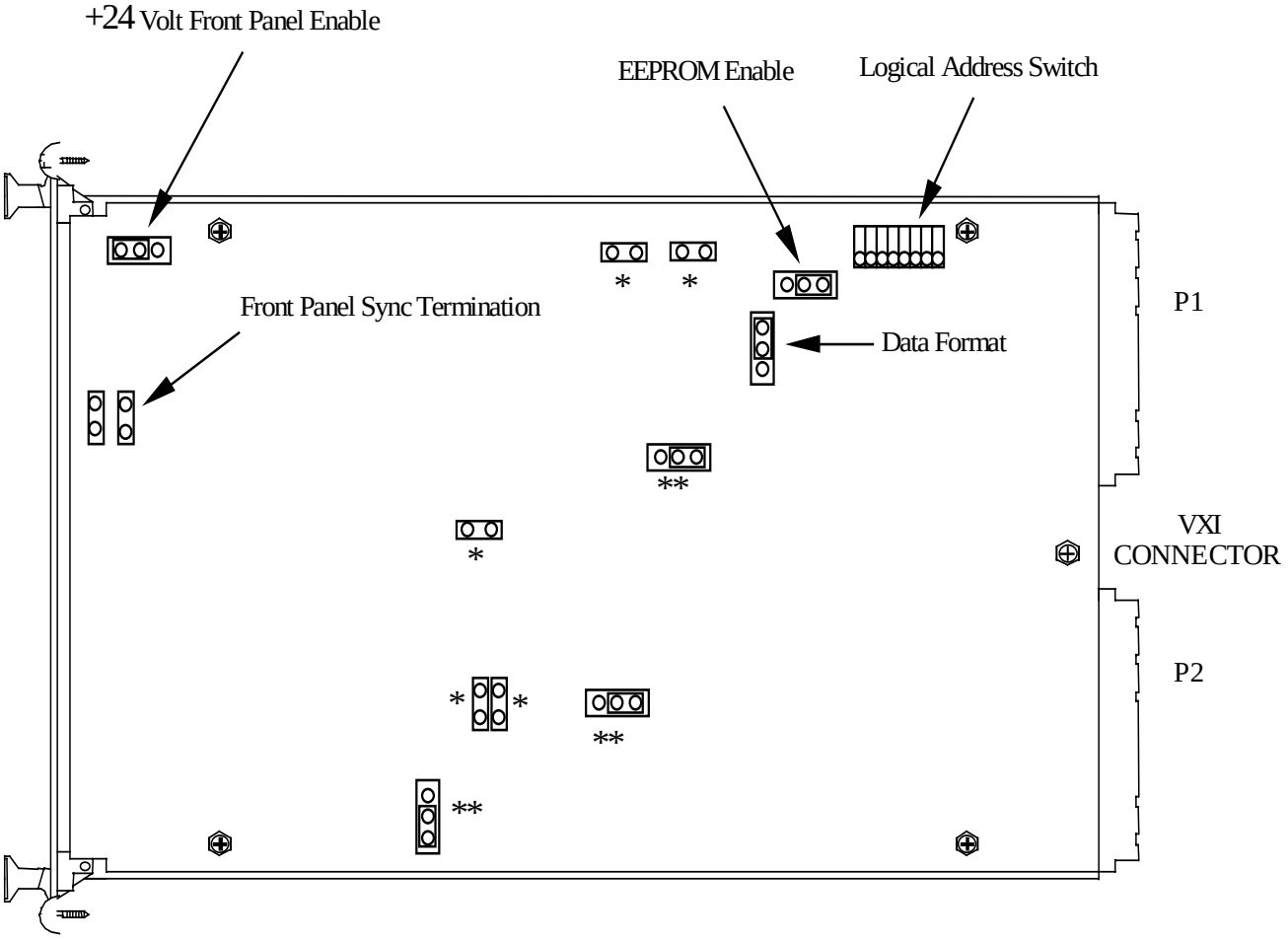


FIGURE 10 - V200 Switch and Strap Locations

Notes:

* Indicates strap locations that are normally removed. These straps are only installed in order to reprogram the flash memory.

** Indicates strap locations that are for factory testing only. These straps must be left in the indicated positions.

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