Model V205

32-channel, 10 Msample/s, 16-Bit ADC

User's Manual

November 22, 2000

*****Special Option*****

Model V205-S001

32-channel, 10 Msample/s, 16-Bit ADC

November 22, 2000

*****Special Option*****

Model V205-S001

The Model V205-S001 is the same as the V205-AA11 except it has been modified to have a 10 K ohm input impedance.

*****Special Option*****

Model V205-S002

32-channel, 10 Msample/s, 16-Bit ADC

November 6, 2000

*****Special Option*****

Model V205-S002

The Model V205-S002 is the same as the V205-CA11 except it has been modified to have 32-channel, 2.5 MHz, 16-Bit Sigma Delta ADC with 50 ohm input impedance instead of 500 ohm.

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About This Manual

Organization

Chapter 1, ***Introduction and General Description***, gives you a brief overview of the Model V205, lists items you need to get started, and explains how to safely unpack your module.

Chapter 2, ***Installation and Configuration***, explains how to configure the V205 and correctly insert it into a C-size VXIbus mainframe.

Chapter 3, ***Configuration and Operational Registers***, explain how to access and control the V205.

Chapter 4, ***Programming Information***, gives you example setup procedures for preparing the V205 to acquire data.

Appendix A, explains V205 connector information.

Warranty, provides information that may be helpful in learning more about KineticSystems and its products, and in quickly reaching us.

Glossary

Following is a glossary of some of the terms and conventions used throughout this manual:

*	An indicator that a register bit contains low-true data. For example, writing a **"0"** to a bit labeled Enable* would cause a function to be enabled.
A16 Space	The first 64 Kbytes of address space, accessible with 16-bit addressing. The configuration registers of VXI devices occupy 64-byte blocks of this address space. The Logical Address of a device determines which 64-byte block is associated with that device.
A32 Space	The 4 Gbyte address space, accessible with 32-bit addressing. A module can request a block of this address space via information contained in its *Configuration* registers. *Operational* registers, if present, reside in this space.
Configuration Registers	Setup registers located in **A16** space. Some are mandatory; some are optional.
D16	A single 16-bit data transfer.
D16 BLK	A block transfer of 16-bit words.
D32	A single 32-bit data transfer. Not all Slot-0 controllers support **D32**.
D32 BLK	A block transfer of 32-bit words. Not all Slot-0 controllers support **D32** BLK.

Device One of 255 devices that a VXIbus system can support. The term is often used interchangeably with "module." The distinction is that a VXIbus module can consist of more than one device.

Dynamic Addressing The VXIbus addressing mode in which the address of a device is stored in a write-able register. See also Static Addressing.

hexadecimal A base-16 number. The suffix, "h," indicates that a number is hexadecimal. For example, 1Ah = 26_{10}; FFh = 255_{10}; 1000h = 4096_{10}.

Logical Address A VXIbus module's unique address. A VXIbus system has 254 logical addresses that are available. **"0"** is the address of the Slot-0 controller. **"255"** specifies that dynamic addressing be used to address that module.

Operational Registers Setup and data-transfer registers that are located in A24 address space.

Resource Manager Software that sets logical addresses and optimally configures Operational register addresses and memory-block addresses in a system. The manufacturer of the Slot-0 controller provides this software, often referred to as "RESMAN."

Static Addressing The VXIbus addressing mode in which the address of a device is stored in a switch register. See also Dynamic Addressing.

Chapter 1: Introduction

About the V205

Features

- 8, 16 or 32 channels
- Simultaneous sampling at output rates up to 10 Msamples/s per channel
- External or programmable internal clock and trigger
- 1 megasample on-board buffer
- Multiple board synchronization
- Transient mode of data collection
- Pre- and post-trigger data collection (circular buffering)

Applications

- Radar systems
- Sonar (hydroacoustic) systems
- High-speed communications systems
- High Energy Physics experiments
- Instrumentation requiring high-bandwidth analog conversion

General Description

Figure 1 shows a simplified block diagram of the V205 board. The board uses 32 16-bit oversampling ADCs (Analog Devices AD9260) to provide simultaneous sampling at rates of up to 10.0 MSamples/sec. on each channel. The oversampling ratio of the ADC can be selected as 2, 4 or 8.

ADC data is buffered in the dual-ported buffer memories for read out via the VXIbus. The sampling clock and the trigger can be either internal or external. The internal ADC clock is user programmable in steps of less than 250Hz at the output rate. Whether the internal clock or an external clock is used, the frequency must be set to twice the desired oversampling rate (i.e., 16x, 8x, or 4x the output word rate). When the software device driver is used, the frequency provided by the user to the internal clock programming function is the actual output word rate required; the function takes care of multiplying this by the required factor.

The ADCs can only be operated in transient mode. In transient mode, a fixed number of samples are acquired upon each application of the trigger. Capture mode has two sub-modes; with pre-trigger data storage and without pre-trigger data storage. When using pre-trigger storage, the V205 stores samples continuously before the trigger and acquires a programmable number of samples following the trigger (to a maximum of 32,768 samples/channel if all 32 channels are active). When pre-trigger storage is not used, conversion starts at each application of the trigger and a programmable number of samples (again, to a maximum of 32,768) are acquired.

In transient mode, the acquisition count and buffer length must be programmed separately. When using capture mode without pre-trigger storage, the buffer length must be an integral multiple of the acquisition count. Thus, it is possible to perform multiple capture sequences at each occurrence of the trigger, until the buffer is filled to the programmed length.

The V205 board can generate VXIbus interrupts at any user programmed buffer length.

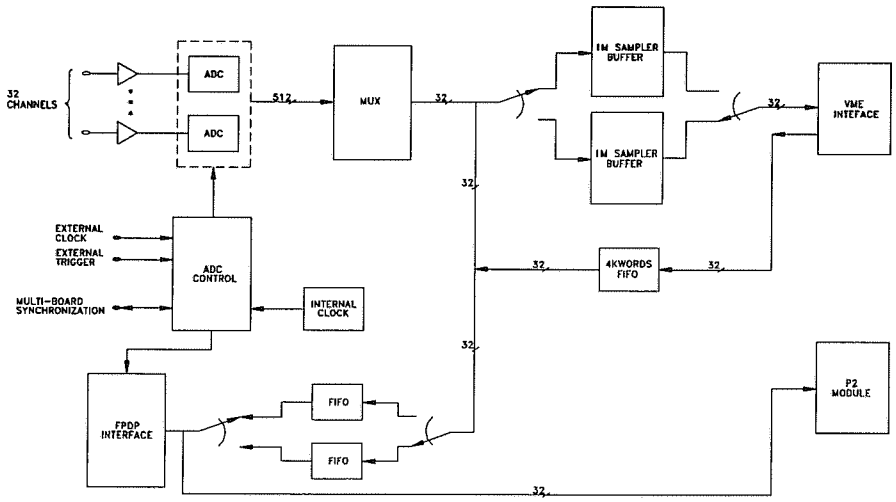


Figure 1-1 V205 Simplified Block Diagram

Ordering Information

Model V205-AA11	8-channel, 10 MSa/s, 16-bit ADC
Model V205-BA11	16-channel, 10 MSa/s, 16-bit ADC
Model V205-CA11	32-channel, 10 MSa/s, 16-bit ADC

Board Specifications

Specifications subject to change without notice.

V205 Board Specifications

Analog Input

Number of Analog Input Channels:	8, 16 or 32
Input Impedance:	500 Ohms
Full Scale Input:	± 1.0 V
Maximum Input Sample Rate (Fs):	20 MHz
Oversampling Ratio:	2, 4, or 8
Maximum Input Signal Bandwidth:	0.430 x Fo (-0.1dB 8x Oversampling)
Maximum Input Signal Bandwidth	0.480 x Fo (-3.0dB 8x Oversampling)
Maximum Input Signal Bandwidth	0.410 x Fo (-0.1dB 4x Oversampling)
Maximum Input Signal Bandwidth	0.478 x Fo (-3.0 dB 4x Oversampling)
Maximum Input Signal Bandwidth	0.323 x Fo (-0.1dB 2x Oversampling)
Maximum Input Signal Bandwidth	0.453 x Fo (-3.0dB 2x Oversampling)
	where Fo = Fs/2, Fs/4 or Fs/8
Maximum Channel Output Rate:	2.5 MHz/ch. for 32 channels (2x oversampling)
	5.0 MHz/ch. for 16 channels (4x oversampling)
	10.0 MHz/ch. for 8 channels (8x oversampling)
	0.125 kHz/ch. for 32 channels (8x oversampling using external clock)
Minimum Channel Output Rate:	24 kHz/ch. For 32 channels (8x oversampling using internal clock)
Maximum Decimation:	256
Settling Time:	312/Fs (8x oversampling)
	112/Fs (4x oversampling)
	26/Fs (2x oversampling)
Signal/(Noise+Distortion+Crosstalk):	>TBD (Fs/8)
	>TBD (Fs/4)
	>TBD (Fs/2)
Inter-channel Cross-talk:	<TBD
On-board Storage:	1 Msample
	(32 Ksample/channel, all 32 chan's active

V205 Board Specifications

General	
VXIbus Interface:	A32/D32/Slave
Environmental:	Temp: 0° to +50°C operating (at entry point of forced air, approximately 490 LFM)
	-40° to +85°C Storage
	Humidity <95% non-condensing
Power:	6.75 Amps @ +5 V
	0.3 Amp @ +12 V
	0.3 Amp @ -12 V

Detailed Description

ADC Section

The V205 board uses 32 16-bit ADCs (Analog Devices AD9260). The maximum input clock frequency for the ADC is 20 MHz. Thus, the maximum output rate (2x oversampling V205 mode) if 10 Msamples/sec for each channel. Note that, at an oversampling ratio of 2, the V205 will operate with a maximum of 8 channels, and at an oversampling ratio of 4, the V205 with a maximum of 16 channels, as a result of limited bus bandwidth on the board. The minimum sampling rate for the ADCs is 1.0 kHz, giving a minimum output rate of 125 Hz in 8x oversampling mode with an external clock source of 2 kHz. However, the ADC data stream may be subsequently decimated by a factor of up to 256. Decimation is accomplished by storing one out of every N samples where N is programmable from 1 to 256. This programmable decimation feature should not be confused with the decimation provided on the chip that is carried out after digital filtering of the signals.

The board accepts unbalanced (single-ended) analog inputs with a full-scale input signal level of 2 Vpp; the input impedance is 500 Ohm. Figure 2 shows the input buffer stage for one channel. Two 44-pin connectors (marked P6 and P7) are provided on the front panel for applying the analog input signals.

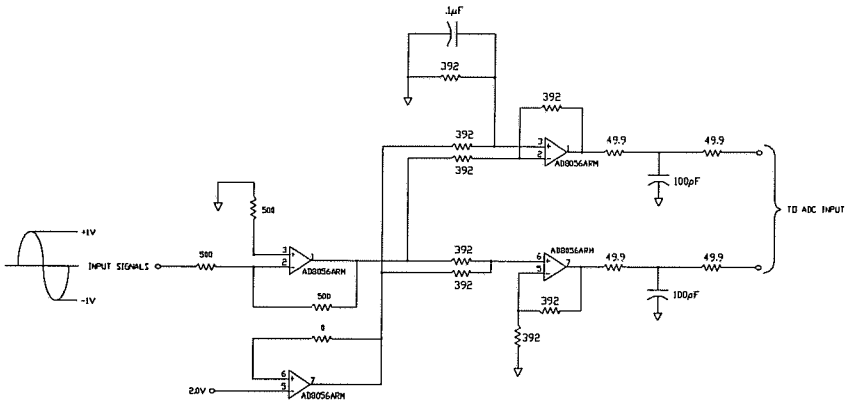


Figure 1-2 V205 Analog Input Stage (One Channel Only)

Input Bandwidth and Sample Rate

The AD9260 ADC chip employs three cascaded digital lowpass filters to achieve the desired decimation. The composite response of these filters governs the input signals bandwidth.

The choice of decimation (oversampling) ratio may be selected using the ADC Oversampling Ratio field of the V205 Control register. Further details on the converter characteristics are available from the manufacturer, Analog Devices, at the following website address:

http://products.analog.com/products/info.asp?product=AD9260

The outputs of the ADCs are combined to produce up to 32 32-bit words, depending on the number of channels selected to be active in the Channel Count register. The selected data are transmitted to the VXI buffer memory. The packed output data format is as follows:

D31——D16	D15————D0	
Channel 1	Channel 2	Word 1
Channel 3	Channel 4	Word 2
....	....	Word 2
Channel N-1	Channel N	Word 2
Channel 1	Channel 2	Word 2
....	....	Word 2

Clock/Trigger Options

The V205 offers a number of clock and trigger options. The card has an internal sampling clock provided by a programmable oscillator giving a resolution of less than 1 kHz at the output rate, over the range 24kHz to 10 MHz. Alternatively, an external sampling clock may be applied at pin 25 of the P4 front panel connector. The minimum output rate using an external clock is 125 Hz (1kHz/8x oversample). **In either case, the clock frequency must be set to twice the required oversampling frequency.**

The trigger can be programmed to be internal (i.e., software controlled) or external. If using the external trigger, the user should supply a positive-going TTL pulse on pin 23 or the P4 connector, the pulse must be at least one sample period long. The trigger is internally synchronized to the sampling clock by the V205. Acquisition starts with the first valid data word after the application of the trigger.

Both external clock and trigger signals must conform to standard TTL levels and drive capability. The relevant connections are listed in a later section.

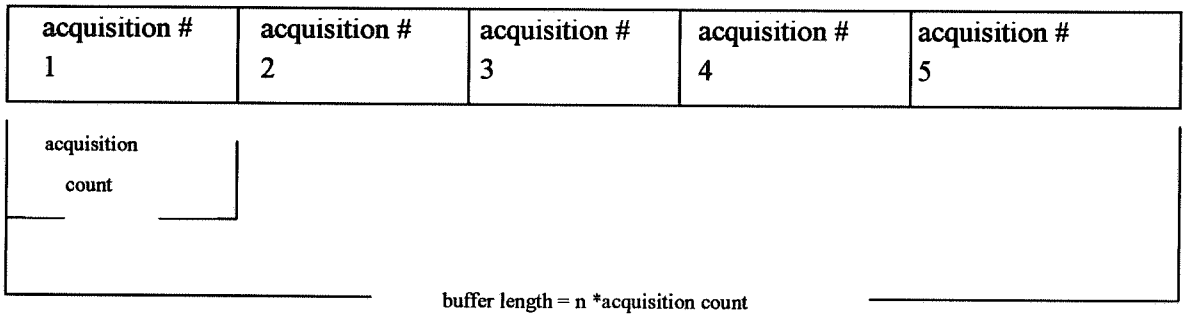
Modes of Operation

Two modes of operation are provided in the V205 design:

- Transient mode without pre storage,
- Transient mode with pre storage.

In the transient mode *without* pre storage, data is acquired for a programmable number of samples following the application of each trigger. The maximum number of samples that can be stored for all active channels is 1048576 (32768 x 32). Because the size of the memory buffer, and the count of samples acquired are both programmable, multiple capture acquisitions may be stored in the V205 memory.

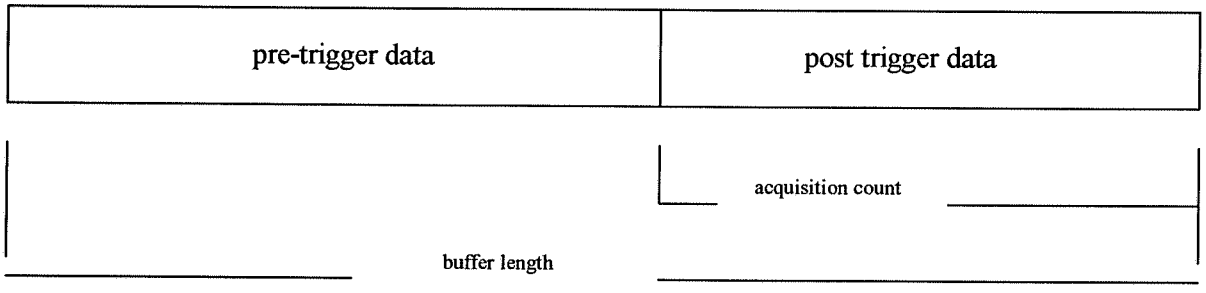
Important note: When using transient mode without pre-trigger storage, the memory buffer length programmed must *always* be an integral number of acquisition counts.



In the transient mode *with* pre storage, the V205 memory is used as a circular buffer of programmable length. The V205 is "armed" by the user, and the control logic continuously fills the circular buffer with fresh data samples in anticipation of the trigger signal. When the trigger signal is received, the final "acquisition count" number of samples are stored in memory, and acquisition is automatically terminated.

To select pre-trigger storage of data in transient mode, the Arm register must be written to as the last action of configuring the board. This will cause the board to start acquiring data. If the Arm register is not written, pre-trigger storage will not occur.

The basic idea: When using pre-trigger storage, acquisition count and memory buffer size may be independently set. Data stored in the memory buffer will be divided into two sections: data acquired *before* the application of the trigger, and data acquired *after* the application of the trigger.



Cascading Multiple Boards

The V205 provides simultaneous sampling not only on all channels on one board, but also on all channels across multiple boards. The V205 PLL clock circuitry allows multiple board systems to have simultaneous triggering (± 0 samples) and less than 1.5 ns board to board sampling skew.

In order to achieve multiple board synchronization, one board is designated as the "Master" and provides clock and trigger signals to the other ("Slave") boards in the group. As with single boards, either internal or external clock and trigger signals may be used with multiple board configurations. In the case of external clock and/or trigger, the user supplies the external signal(s) to the master, which in turn distributes the clock and trigger to the slaves. Master/slave status must be programmed in the Control register. The P4 connector on the front panel of the V205 provides access to all signals necessary for multiple card synchronization. Details of the P4 pinout are given in appendix. The term "Master" in this context should not be confused with VXIbus bus mastership.

Important note: All boards to be synchronized must be located in the same VXIbus chassis in order to avoid violation of signal timing requirements.

Related products

Getting Started

To set up and use your V205 VXIbus module, you will need most or all of the following:

- The V205 16-bit ADC module and this User Manual
- Your VXIbus system with its Resource Manager and high-level test and/or application software

Unpacking the V205

The V205 comes in an anti-static bag to avoid electrostatic damage. Electrostatic discharge to the module can damage components on it. Please take the following precautions when unpacking the module:

- Ground yourself with a grounding strap or by touching a grounded object.
- Touch the anti-static package to a metal part of your VXIbus chassis before removing the module from the package.
- Remove the module from the package and inspect the module for damage.
- Do not install the module into the VXIbus chassis until you are satisfied that the module exhibits no obvious mechanical damage and is configured to conform to the desiring operating environment. The next chapter describes installation and configuration.

Chapter 2: Installation and Configuration

Setting the Logical Address Switches

A VXI system can have as many as 255 devices, with each having a unique number in the range from 0 to 254. Eight bits represent the number, which is the Logical Address of the device.

VXIbus defines two concepts of addressing: "static" and "dynamic." All VXIbus devices *must* allow static addressing, in which the address is determined by the setting of a switch register. VXIbus devices may, but are not required to, support dynamic addressing. In dynamic addressing, the Logical Address is stored in a software-addressable register.

Before installing the V205 in the VXIbus chassis, you must set the switch register to an appropriate value. If you wish to employ static addressing you must make sure you set the switch register to a unique value other than 0 or 255. It is a good idea to note module addresses in an accessible log, because if you replace a module, it is very important that the new module have the same address as the replaced one.

If your system employs dynamic addressing, which delegates the task of assigning device addresses to the Resource Manager software, then make sure the address switch is set to 255 (all "1"s).

Note: To set a Logical Address bit to "1" depress the bottom segment of the switch.

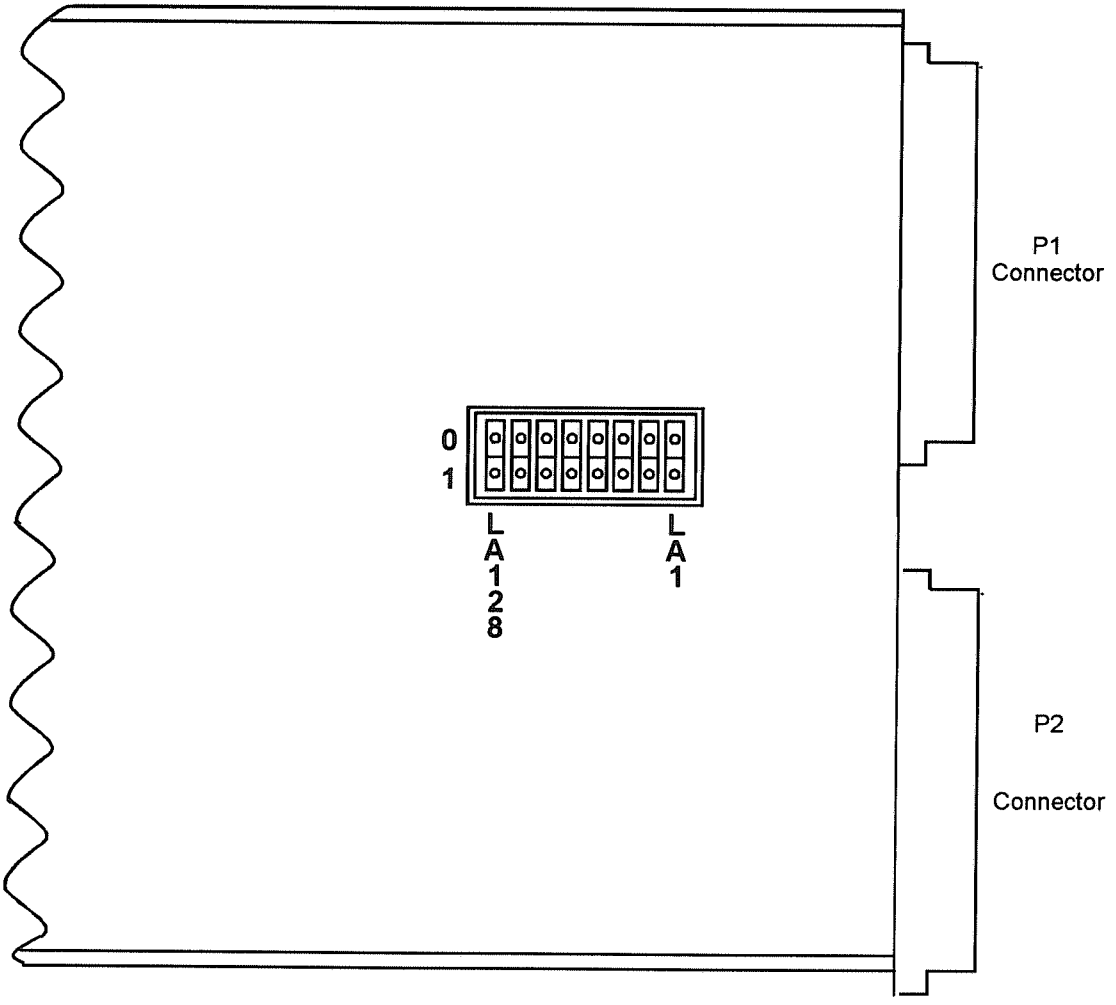


Figure 2-1: V205 Logical Address Switch Locations

Module Insertion

Before inserting your VXIbus module into the chassis, make sure that the chassis is plugged into electrical power but *not turned on*. The power cord provides a ground connection for the mainframe and protects the equipment and you from electrical harm.

In a VXI system, the Bus Grant and IACK signals are received and transmitted by each of the modules. These signals must be jumpered around any vacant slots in the mainframe. Most current mainframes, including our V194 and V195, contain jumperless backplanes, where the Bus Grant and IACK signals are automatically jumpered when a slot is empty.

If your mainframe does not contain a jumperless backplane, you must position certain jumpers correctly on the chassis backplane to assure that the V205 acknowledges interrupts properly. Remove the Interrupt Acknowledge (IACK) jumper from the slot selected for the V205 and install daisy-chain jumpers in any empty slots between the V205 and the Slot 0 Controller.

You can now insert the V205 into the chassis. Slowly push it in until its plug connectors are resting against the backplane connectors. Then, using evenly distributed pressure, press the module straight in until it seats in the slot and the module front panel is even with the chassis front panel. Tighten the top and bottom screws. *You may now safely apply power to the V205.*

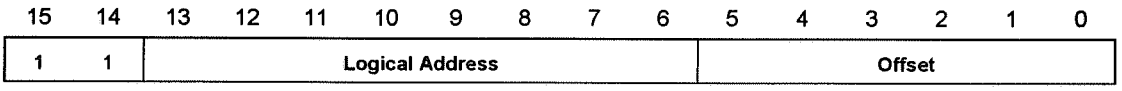
Module Configuration

Setting the VXI Logical Address

You, or your software, must perform two types of module configuration. The first has to do with VXIbus-related items and involves communication with V205 *configuration* registers. The second deals with setting parameters related to module operation and involves communication with V205 *operational* registers.

VXIbus-related configuration includes setting the logical address, specifying the amount of memory space required, specifying where in memory the V205 registers and memory blocks are located, and setting interrupt levels.

VXIbus devices occupy system memory space. The configuration registers for each VXIbus device have 64 bytes of memory space in the upper 16 Kbytes of the 64-kbyte **A16** memory space. Whether you set the 8-bit Logical Address statically in the switch register or dynamically in the Logical Address register, those eight bits determines the base address of the 64-byte block of memory as follows:



Each 64-byte block contains several registers that supply information about the module, such as the manufacturer, the module identifier (i.e., "205h"), its class (register-based or message-based), serial number, and the amount of memory space it requires.

In addition to **A16** addressing, a VXIbus device can also support **A24** or **A32** addressing. The V205 supports both A16 and A32 addressing.

Most operational registers are all in **A32** space. To access them, one must first write a proper offset value to the Offset register in **A16** space. One operational register for configuring VXI trigger functions is lo-

cated in the A16 address space.

Refer to Chapter 3 for details relating to the *configuration* and *operational* registers.

Chapter 3: Configuration and Operational Registers

Address Space

VXIbus uses the VMEbus protocol for data transfer and therefore supports 32-bit addressing to access I/O slave devices. 32-bit addressing provides direct access to memory space of four Gigabytes.

Slave devices such as VXIbus data acquisition modules exist for a variety of purposes and can be simple or very complex. Communication between host and slave can require access to several registers in one device or access to many Mbytes of memory in another. ("Devices" and "modules" are terms often used interchangeably. The distinction is that more than one VXIbus device *can* reside in a VXIbus module. However, there is generally one device per module.)

To minimize the amount of address-decoding hardware needed, simpler slave devices use addressing modes that fully decode only 16 or 24 address lines rather than 32. Therefore, there are three defined addressing modes...**A16**, **A24** and **A32**...having address spaces of 64 Kbytes, 16 Mbytes and 4 Gbytes, respectively.

All VXIbus devices have registers located within 64-byte blocks in **A16** address space and therefore support **A16** addressing. Devices requiring no more than 64 bytes of address space need only support **A16** addressing. Devices needing more than the 64 bytes to accommodate additional registers or blocks of memory *must* also support **A24** or **A32** addressing, but not both.

VXIbus devices that use **A24** or **A32** addressing modes are required to have four registers in **A16** space for parameter definition. One such parameter is Required Memory, which uses four bits (*m*) to specify the size of the memory in **A24** or **A32** space required by the device. A device *may not* use more than one-half of the memory space, and it *should not* use more than one-fourth. Table 3-1 shows the relationship between the four-bit parameter, *m*, and the memory required by the device. Note that $m = 0$ defines the case for maximum usage, i.e.; half of the memory space. Required Memory is specified in bits 15 – 12 in the Device Type register at offset 02h.

m	Required Memory A24		Required Memory A32		*m*	Required Memory A24		Required Memory A32	
0	8	Mbytes	2	Gbytes	8	32	Kbytes	8	Mbytes
1	4	"	1	"	9	16	"	4	"
2	2	"	512	Mbytes	10	8	"	2	"
3	1	"	256	"	11	4	"	1	"
4	512	Kbytes	128	"	12	2	"	512	Kbytes
5	256	"	64	"	13	1	"	256	"
6	128	"	32	"	14	512	bytes	128	"
7	64	"	16	"	15	256	"	64	"

Table 3-1: Relationship between the "*m*" Parameter and Required Memory

One of the four registers is the Offset register, which is needed only for devices using **A24** or **A32** address space. This 16-bit read/write register defines the base address of the device's **A24** or **A32** operational registers. The *m+1* most significant bits of the Offset register provide the values of the *m+1* most significant bits of the device's **A24** or **A32** register addresses, where *m* is as defined in Table 4-1 above.

Static and Dynamic Configuration

A VXIbus system can have up to 255 devices. Therefore, eight bits define the device address, which is called the "Logical Address." The Logical Address can be "static" or "dynamic." A static address resides in an 8-bit switch register; a dynamic address resides in a write-only register. Setting the switch register to 255 (all "1"s) causes dynamic addressing to be enabled. Any other setting enables static addressing, in which case the value held in the switch register is the Logical Address.

With the Logical Address set to 255, a device responds to accesses at address 255 only when the MODID line is asserted as a qualifier by the Slot-0 controller. After a new Logical Address is written to the device, the device responds to the new address independent of the state of the MODID line.

For data acquisition and control applications, dynamic configuration is an important concept. A system often contains more than one module of a given type, and it can be easy, and sometimes desirable, to swap positions of two modules after removing them from the mainframe. If dynamic configuration is not employed, one must make sure that the switch register is correctly set when inserting or re-inserting a device. Dynamic configuration greatly simplifies system setup, since the software can assure that the devices are located in the desired slots. Dynamic configuration also allows a system's Resource Manager to configure memory usage optimally in a system.

Communication Protocol

VXIbus allows communication over the backplane by either register-based or message-based protocols. With register-based protocol, the communication is via an 8-, 16- or 32-bit parallel path directly to I/O registers within the modules. With message-based protocol, an ASCII interpreter is included on each module, and the binary representations of ASCII characters are transmitted over the backplane. The advantage of message-based protocol is that English-like commands and responses can be used.

High-performance data acquisition and control modules are usually register-based because the data throughput is usually several orders of magnitude greater than with message-based devices. All Kinetic-Systems VXIbus devices are register-based.

Register Addressing

The user assigns each device in a VXIbus system a unique number between 1 and 254. This 8-bit number, called the Logical Address, defines the base address for the VXIbus device registers located on the module. Each device has a 64-byte block of memory reserved for these registers. The memory blocks, called configuration space, are located in the upper 16 Kbytes of the 64-kbyte **A16** address space.

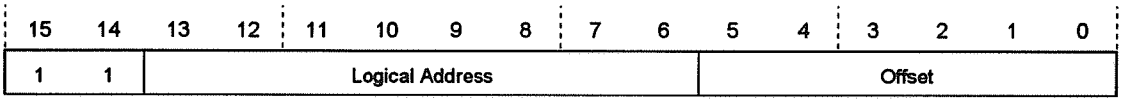
Every device has at least three configuration registers: ID / Logical Address, Device Type, and Status / Control. Modules using **A24** or **A32** addressing must also have an Offset register. The rest of the 64-byte block can contain registers or memory appropriate for the operation of the specific device.

A device's Logical Address occupies bits 13 - 6 of the register address. Bits 15 and 14 of the address are both "1's," and the base address of the register block is therefore:

$$V*40h+C000h$$

where V is the Logical Address of the device and C000h is the starting address of the top 16-kbyte block.

The address of a specific register is the base address plus an offset address. The offset is bits 5 - 0 of the register address and ranges from 00h to 3Eh.



The V205 also uses *operational* registers in **A32 space; therefore,** it is an "Extended" register-based device.

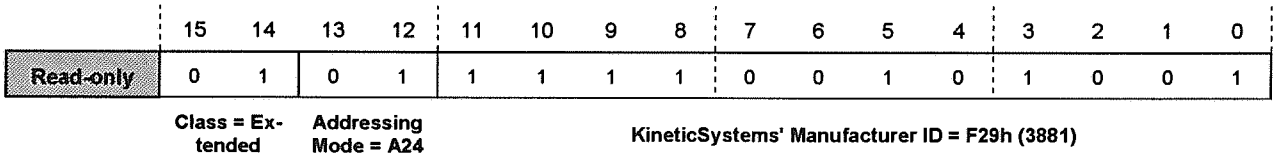
Required Configuration Registers

The four required VXIbus registers are ID / Logical Address, Device Type, Status / Control, and Offset. You can access these registers by **D16** transfers only.

ID Register *00h*

This read-only register returns 5F29h.

Fields are Device Classification, Addressing Mode and Manufacturer ID.



Device Classification *Bits 15 and 14*

00 Memory device

01 Extended device

10 Message-based device

11 Register-based device

The V205 is an *Extended device.*

Addressing Mode *Bits 13 and 12*

00 A24

01 A32

10 Reserved

11 A16

The V205 uses *A32 addressing.*

Manufacturer ID *Bits 11 through 0*

KineticSystems' Manufacturer ID is *3881*, which corresponds to F29h.

Logical Address Register 00h

This write-only register holds the Logical Address. In systems using Dynamic Configuration, the system Resource Manager uses this register to set the Logical Address of the device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	Not Used								Logical Address							

Logical Address Bits 7 through 0

Device Type Register 02h

This read-only register contains the Required Memory and Model Code for the V205. It returns C205h.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	0	0	0	0	1	0	0	0	0	0	0	1	0	1
	Required Memory (*m*)				Model Code = 205h											

Required Memory Bits 15 – 12

A value of **Ch** is returned (*m* = 12 decimal), indicating that the V205 is allocated 512 Kbytes in **A32** space.

Model Code Bits 11 – 0

The model code for the V205 is 205h.

Status Register 04h

This read-only register provides binary information about the status of the V205.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	A32 Active	MODID*	Not Used										Ready	Passed	Sysfail Inhibit	Soft Reset

A32 Active Bit 15

"1" in this field indicates that the **A24** registers of the V205 can be accessed. This bit reflects the state of the Control register's **A32** Enable bit.

MODID* Bit 14

"1" in this field indicates that the V205 is *not* selected via the P2 MODID line. A "**0**" indicates that the device is selected by a high state on the P2 MODID line. The Resource Manager uses this bit to configure the V205 dynamically.

Ready Bit 3

"1" in this field indicates that the registers have been successfully initialized. The V205 is ready for access.

Passed Bit 2

"1" in this field indicates that the device self-test has passed. A "0" indicates that the V205 has failed—or is currently executing—its self-test. Since the V205 does not have a power-up self-test mechanism, this bit is always read back as a "1".

Sysfail Inhibit Bit 1

"1" in this field indicates that the V205 is disabled from driving the SYSFAIL* line. This bit reflects the state of the Sysfail Inhibit line in the Control register.

Soft Reset Bit 0

"1" in this field indicates that the V205 is in a reset state. While in this state, the V205 will allow access only to its Configuration registers.

Control Register 04h

This write-only register causes execution of specific actions by the V205.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	A32 Enable	Not Used													Sysfail Inhibit	Soft Reset

A32 Enable Bit 15

Setting this bit to "1" enables access of the **A32** registers of the V205.

Sysfail Inhibit Bit 1

Setting this bit to "1" disables the V205 from driving the SYSFAIL* line.

Soft Reset Bit 0

Setting this bit to "1" forces the V205 into a reset state.

Offset Register 06h

This read/write register determines and reports the device base address in **A32** memory space.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Base Address in A32 memory space								0	0	0	0	0	0	0	0

Additional Configuration Registers

Additional configuration registers are:

- Attribute register
- Serial Number High & Low registers
- Version Number register
- Interrupt Status register
- Interrupt Control register
- Subclass register, and
- Suffix High and Low registers.
- Trigger Mapping Register

Note that you can access these registers by **D16** transfers only.

Attribute Register *08h*

This read-only register provides low-true information about the V205's interrupt handling capabilities. A read of this register returns FFFAh.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
	Reserved													Interrupt Capability*	Interrupt Handler Control*	Interrupt Status Reporting*

Reserved *Bits 15 - 3*

These bits are reserved for future use and return "1"s when read.

*Interrupt Capability** *Bit 2*

"**0**" signifies that the V205 is capable of generating interrupts.

*Interrupt Handler Control** *Bit 1*

"1" indicates that the V205 is *not* capable of Interrupt Handler Control.

*Interrupt Status Reporting** *Bit 0*

"**0**" indicates that the V205 has Interrupt Status Reporting capability.

Serial Number Register — 0Ah, 0Ch

The read-only Serial Number registers (high and low words) store the 32-bit hexadecimal value of the V205's decimal serial number.

0Ah

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	SN7	SN6	SN5	SN4

High word

0Ch

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	SN3	SN2	SN1	SN0

Low word

Version Number Register — 0Eh

This read-only register gives the hardware and firmware revision numbers of the module.

	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Read-only	Firmware Version	Firmware Revision	Hardware Version	Hardware Revision

Firmware Version ***Bits 15 - 12***

Firmware Revision ***Bits 11 - 8***

Hardware Version ***Bits 7 - 4***

Hardware Revision ***Bits 3 - 0***

Each field is a four-bit integer indicating the version or revision number.

Interrupt Status Register 1Ah

This read-only register provides information about the state of the interrupt source within the V205.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	0	0	0	0	0	0	IRQ	Logical Address							

Not Used Bits 15-9

These bits are not used and returned as zeros, but should also be written as zero.

Interrupt Request Bit 8

A "1" read back from this bit location indicates that an interrupt is pending due to a request from the V205. This bit is latched and auto-cleared when this register is read or an interrupt acknowledge cycle is executed.

Logical Address Bits 7 - 0

During a programmed control read operation, these bits return all "1's." During an interrupt acknowledge cycle, these bits return the V205's Logical Address.

Interrupt Control Register 1Ch

The read/write register contains mask bits for the interrupt source, a bit for disabling interrupts and three bits that determine interrupt level. All of the bits in this register are set to "1" on the assertion of SYSRESET.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	1	1	1	1	1	1	1	*IRQ ENA	EN*	1	Interrupt Req. Level			1	1	1

Not Used Bit 15 – 9

These bits are not used and should be written as "1"'s when writing to this register.

Interrupt Request Enable ***Bit 8***

Writing a "1" to this bit *prevents* the V205 from generating an interrupt request. Writing a **"0"** enables the interrupt source to generate an interrupt request.

Interrupt Enable ***Bit 7***

Writing a "1" to this bit disables interrupt generation. Writing a **"0"** enables interrupt generation.

Interrupt Request Level ***Bits 5 - 3***

These bits determine the interrupt request level.

Bits 5	4	3	Interrupt Request Level
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

Table 3-2: Interrupt Request Levels

Not Used **Bits 2 – 0**

Bits 2 – 0 are not used and return **"1"**s when read.

Note: Prior to configuring the interrupt selection and enables in this register, the interrupts MUST be enabled prior to configuration through the Interrupt Configuration Register in A32 address space.

Subclass Register *1Eh*

This read-only register provides information about the Subclass of the VXIbus device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	Extended Device	Extended Register-based Device														

Bit 15 indicates that the V205 is a VXIbus-defined Extended Device.

Bits 14 through 0 indicate that the V205 is an Extended Register-based Device.

Suffix Register 20h, 22h

The Suffix read-only register (high and low words) holds the ASCII codes for the four characters of the V205's suffix. The suffix defines the optional characteristics of the module.

20h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	1	0	0	1	1	0	0	0	1	0	0	0	0	x	x

ASCII code for A, B, or C = 41h , 42h or 43h (1st character) ASCII code for A = 41h (2nd character)

22h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	0	1	1	0	0	x	x	0	0	1	1	0	0	x	x

ASCII code for 1 = 31h (3rd character) ASCII code for 1, 2, etc. = 31h, 32h, etc. (4th character)

The suffix options for the V205 are:

1st character: Specifies the number of ADC Channels

"A" indicates a module with 8 channels.

"B" indicates a module with 16 channels.

"C" indicates a module with 32 channels.

2nd character: "A" for all options.

3rd character: "1" for all options.

4th character: Revision level

The number, "1," "2," etc., gives the module revision level.

Trigger Mapping Register 36h

The Trigger Mapping Register is a write/read register used to control the configuration of the Front Panel Mounted Trigger OUT B and Trigger OUT A SMB's. Under software control, these two SMB's can be mapped as outputs from the VXI trigger lines. The triggers can be mapped to either the TTL or ECL trigger lines. The following shows a bit layout for the Trigger Mapping Register.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	0	0	OUT ENA B	0	S3 B	S2 B	S1 B	S0 B	0	0	OUT ENA A	0	S3 A	S2 A	S1 A	S0 A

Trigger OUT B SMB Trigger OUT A SMB

Not Used Bits 15-14

These bits are not used and read as "0"s.

Output Enable B ***Bit 13***

This write/read bit is used to enable the Front Panel Trigger OUT B SMB as an output. The SMB signal is asserted by the V205 when the trigger line configured by bits 11 through 8 is asserted. The SMB is configured as an output of the V205 when this bit is set to a "1" and disabled from being an output when set to "0".

Not Used ***Bit 12***

This bit is not used and should be written to a "0".

Select 3B through Select 0B ***Bits 11-8***

These write/read bits are used to configure the VXI Trigger Line mapping when enabled as an output from the V205. The binary combination of these bits determine the mapping as shown in the following table.

Bits				Mapped Trigger Line
11	10	9	8	
0	0	0	0	TTL Trigger Line 0
0	0	0	1	TTL Trigger Line 1
0	0	1	0	TTL Trigger Line 2
0	0	1	1	TTL Trigger Line 3
0	1	0	0	TTL Trigger Line 4
0	1	0	1	TTL Trigger Line 5
0	1	1	0	TTL Trigger Line 6
0	1	1	1	TTL Trigger Line 7
1	0	0	0	ECL Trigger Line 0
1	0	0	1	ECL Trigger Line 1

Table 3-3: V205 Bits 11-8 Mapped Trigger Line

Not Used ***Bits 7-6***

These bits are not used and read as "0"s.

Output Enable A ***Bit 5***

This write/read bit is used to enable the Front Panel Trigger I/O A SMB as an output. The SMB signal is asserted by the V205 when the trigger line configured by bits 3 through 0 is asserted. The SMB is configured as an output of the V205 when this bit is set to a "1" and disabled from being an output when set to "0".

Not Used ***Bit 4***

This bit is not used and should be written to a "0".

Select 3A through Select 0A ***Bits 3-0***

These write/read bits are used to configure the VXI Trigger Line mapping when enabled as an output from the V205. The binary combination of these bits determine the mapping as shown in the following:

Bits				Mapped Trigger Line
3	2	1	0	
0	0	0	0	TTL Trigger Line 0
0	0	0	1	TTL Trigger Line 1
0	0	1	0	TTL Trigger Line 2
0	0	1	1	TTL Trigger Line 3
0	1	0	0	TTL Trigger Line 4
0	1	0	1	TTL Trigger Line 5
0	1	1	0	TTL Trigger Line 6
0	1	1	1	TTL Trigger Line 7
1	0	0	0	ECL Trigger Line 0
1	0	0	1	ECL Trigger Line 1

Table 3-4: V205 3-0 Mapped Trigger Line Bits

Operational Registers

The following sections describe the set of Operational Registers on the V205. This set of registers is located in **A32** address space and must be accessed by **D32** transfers only. Accessing these registers by any other data word size than **D32** will result in erroneous behavior.

The following table is a summary of registers available on the V205. Additional information on each register is available under its individual description.

Register	Offset	Access Type
Status Register	Base + 00004h	Read-Only
Interrupt Mask Register	Base + 00008h	Read/Write
Control Register	Base + 0000Ch	Read/Write
Channel Count Register	Base + 00010h	Read/Write
Buffer Length Register	Base + 00014h	Read/Write
Acquisition Count Register	Base + 00018h	Read/Write
Decimation	Base + 0001Ch	Read/Write
ADC Clock Register	Base + 00024h	Write-Only
Arm Register	Base + 0002Ch	Write-Only
ADC Reset Register	Base + 00030h	Write-Only
Buffer Reset Register	Base + 00034h	Write-Only
Board Reset Register	Base + 00038h	Write-Only
Interrupt Configuration Register	Base + 1008Ch	Write-Only
ADC Data Register	Base + 40000h	Read-Only/Write-Only

Status Register (SR) 00004h

The Status Register contains information about the state of the V205, including the status of events, which may cause VXIbus interrupts, if the appropriate bits of the Interrupt Mask register (IMR) are set. The Status Register should be used to determine the interrupt status of the V205. Several other indicators exist in this register for status and error reporting.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Read-Only	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	CLK BUSY	SYNC ERR	DIAG FIFO EMP	IRQ	0	0	0

Not Used Bit 31-7

These bits are not used and should be ignored.

CLK BUSY Bit 6

This bit indicates that the programmable clock is busy. Whenever accessing the ADC CLOCK registers, this bit is monitored between successive writes until it is low.

SYNC ERR Bit 5

This bit indicates that a synchronization error has occurred among the ADCs. This indicates that one or more ADCs on this board is out of sync with respect to the oversampling decimation of other ADCs in the system. In order to correct this, the user should resynchronize the converters by means of a write to the ADC Reset register.

DIAG FIFO EMPTY Bit 4

This bit indicates that the Diagnostics FIFO is empty and is ready for more data.

IRQ Bit 3

This bit indicates that the V205 is asserting a VXIbus interrupt from any source.

Not Used Bits 2-0

These bits are not used and read as "0".

Interrupt Mask Register (IMR) 00008h

Read/Write

The Interrupt Mask register is used to enable and disable VXIbus interrupts. The status of interrupts (asserted/not asserted) may be read in the corresponding bits of the status register, but no interrupt will occur unless the appropriate mask bit is set in this register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ADC IRQ ENA	0

ADC IRQ Enable Bit 1

This bit enables the ADC control unit controller to generate VXIbus interrupts. Setting this bit to a "1" enables the interrupt source and a "0" disable the source.

Not Used — Bit 0

This bit is not used and read as a "0".

Control Register (CR) — 0000Ch

The Control Register is a write/read register that is used to control the overall configuration of the V205. The following is the bit layout for the Control Register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	ENA	INT TRIG	1	ADC OSAMPLE		0	0	ADC CLK TERM	ADC MSTR	0	0	0	DIAG ENA	CLK SEL	TRIG SEL

Not Used — Bits 31-15

These bits are not used and should be ignored.

Enable — Bit 14

This bit is used to enable the ADC's to acquire data and move it into the storage buffer. After this bit is set to a "1"and external triggering is selected, the acquisition will start following the next rising edge of the external trigger input. After this bit is set to a "1" and internal triggering is selected, acquisition will start with the first valid data after the trigger bit, bit 13, has been set. This bit should be cleared to a "0" disable acquisition.

Internal Trigger — Bit 13

This bit is the internal trigger signal that can be used to initiate a transient capture. The Enable bit , bit 14 of this register, must have been previously set to a "1", and Trigger Select, bit 0 of this register, must be set to internal trigger, in order for this bit to be effective. This bit is automatically cleared after acquisition is started.

Reserved — Bit 12

This bit is reserved and MUST be set to a "1" in order for the V205 to properly function.

ADC Oversampling Ratio — Bit 11-10

These bits select the oversampling ratio of the converters. All converters on the board are programmed to the same ratio. The valid selections for the oversampling ratios are 8x, 4x, and 2x. To determine the output rate for a given channel, one must divide the oversample clock to the ADC's by the oversampling

ratio. For example, an ADC running with a 10 MHz oversample clock, the output rate at 8x oversample is 1.25 MHz, at 4x is 2.5 MHz , and at 2x is 5 MHz. The following table shows the various binary combinations of these bits that yield the indicated oversampling ratios.

Bits		Oversampling Ratio
11	10	
0	0	8x Oversampling
0	1	4x Oversampling
1	0	2x Oversampling
1	1	Reserved

Reserved ***Bit 9-8***

These bits are reserved and MUST be set to "**0**".

ADC Clock Termination ***Bit 7***

This bit is used to connect the resistive termination to the P4 ADC_CLK line. This bit is only useful in configurations using multiple V205's that are to run off the same sample clock signal. This bit must be set to a "1" on the End Slave board only, and only in multiple board configurations. The End Slave refers to the last physical V205 in a multiple module configuration.

ADC Sampling Master Enable ***Bit 6***

This bit is used to select a board as a Sampling Master or Slave, when operating in a multiple V205 board acquisition cluster. In the cluster, only one board can be set as a Master. The Master board sends the ADC_CLK signal (pin 1 and 2 on the P4 connector) and the Trigger signal (pin 10 on the P4 connector) to all slaves. The ADC_CLK signal is in PECL format. Slaves receive the ADC_CLK on the P4 connector pin 1 and 2 and the Trigger signals on pin 10. The Master must be located at one physical end of the P4 Local Bus cable. When using a single V205, the board must be configured as Sampling Master. This bit is set to a "**1**" to configure the V205 as a Sampling Master and reset to a "**0**" to configure the V205 as a Sampling Slave.

Reserved ***Bit 5-3***

These bits are reserved and MUST be set to "**0**".

Diagnostic Mode Enable ***Bit 2***

This bit is used to enable the Diagnostic mode. The Diagnostic Mode is enabled by setting this bit to a "**1**" and disable by resetting this bit to a "**0**". In this mode, VXIbus data can be written to the buffer and verified for consistency. Once the mode is cleared, the data can be read back from the buffer. Details of the use of diagnostic mode are given in the section of this manual entitled *Using Diagnostic Mode*.

Sampling Clock Select ***Bit 1***

This bit selects between internal and external sampling clocks for the ADC. Resetting this bit to a "**0**" selects the internal sample clock and setting this bit to a "**1**" selects external sample clock. Note that when using the external sample clock, that the clock input to the V205 must be twice that of the actual desired

sample rate.

Trigger Select — Bit 0

This bit determines if the external ADC Trigger is used to start an acquisition. When using an external trigger, triggering occurs following the rising edge of the trigger signal. The signal must remain high for at least one complete acquisition (clock) cycle. External trigger events are enabled by setting this bit to a "1" and disabled by setting the bit to a "0".

Channel Count Register — 00010h

This write/read register determines the number of active channels on the board to participate in conversions. Only the samples coming from the active channels are stored in the buffer and moved to the output interface. A value (N-1) written in this register will activate channels 1 to N. N must be an even number. The valid range of numbers that may be programmed to this register is 1 to 31.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	Channel Count				

Not Used — Bits 31-5

These bits are not used and should be ignored.

Channel Count — Bits 4-0

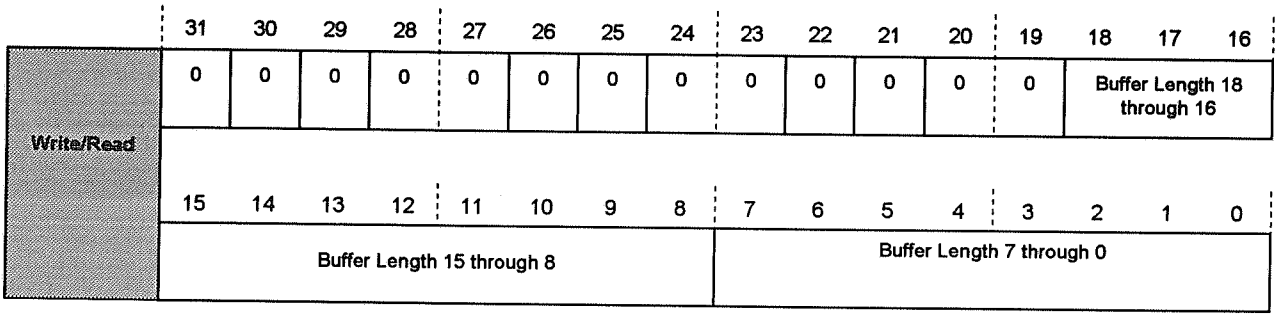
These write/read bits are used to configure the number of active channels on a V205. The actual value loaded into this register is one less than the desired parameter. The legal values for data loaded into this register range from 0 to 31.

Buffer Length Register — 00014h

The Buffer Length is a write/read register used to specify the total number of sample pairs acquired for all active channels before acquisition terminates. When operating in transient mode without pre-trigger storage, the buffer length selected must be an integral multiple of the Acquisition Count. The value written to this register must be one less than the required buffer length. If the ADC interrupt is enabled, a VXIbus

interrupt will occur when the programmed length is reached. The valid range of numbers that may be programmed to this register is 0 to 524287. The maximum value is equivalent to the maximum buffer capacity of 1Msample.

The user must perform a Buffer Reset (by writing to the Buffer Reset register) after loading the Buffer Length, Acquisition Count, Decimation and Frame Count registers in order for the new values to take effect.



Not Used ***Bits 31-19***

These bits are not used and should be ignored.

Buffer Length ***Bits 18-0***

These write/read bits are used to specify the total number of sample pairs acquired for all active channels before the operation terminates. The value in this register can range from 0 to 524287.

Acquisition Count Register *00018h*

The Acquisition Count Register is a write/read register that determines the number of 32-bit words to be stored in the buffer following each application of a trigger when operating in transient mode with no pre-trigger storage. When operating in transient mode with pre-trigger storage, it determines the number of 32-bit words acquired after the (single) occurrence of the trigger. Two samples are stored in each 32-bit buffer word. The value is programmed as one less than the required length. The relationship between samples acquired on each channel, and the value programmed to this register is therefore as follows:

$AC = (S \times C/2) - 1,$

where AC = Value programmed to Acquisition Count register

S = Number of samples to be acquired on each channel

C = Number of active channels selected in Channel Count register

The valid range of numbers that may be programmed to this register is 0 to 524287. The user must perform a Buffer Reset (by writing to the Buffer Reset register) after loading the Buffer Length, Acquisition

Count, Decimation and Frame Count register is order for the new values to take effect.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	0	Acquisition Count 18 through 16		
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Acquisition Count 15 through 8								Acquisition Count 7 through 0							

Not Used ***Bits 31-19***

These bits are not used and should be ignored.

Acquisition Count ***Bits 18-0***

These write/read bits are used to specify the number of 32-bit data words to be stored upon each application of a trigger.

Decimation Count Register *0001Ch*

This write/read register programs the eight-bit decimation count. The real output rate is the ADC output rate divided by the decimation factor. The decimation factor is one greater than the value written to this register. Therefore, setting this register to zero disables decimation, while writing one to this register will result in decimation by a factor of 2. This feature enables the output rate to be reduced, allowing operation of the V205 with an effective sample output rate below the converter minimum for the selected oversampling ratio. However, the user is cautioned that decimating the output in this way interacts with the oversampling technology of the converters, and may cause aliasing of any signals that are in the ADC's bandwidth. The valid range of numbers that may be programmed to this register is 0 to 255, corresponding to decimation factors of 1 to 256.

The user must perform a Buffer Reset (by writing to the Buffer Reset register) after loading the Buffer Length, Acquisition Count and Decimation register in order for the new values to take effect.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Write/Read	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	Decimation Count							

Not Used ***Bits 31-8***

These bits are not used and should be ignored.

Decimation Count ***Bits 7-0***

These write/read bits are used to specify output decimation factor. The value loaded into this register is actually 1 less than the desired factor. Loading a value of zero disables decimation.

ADC Clock Frequency Register 00024h

This write/read register allows the user to program the internal sampling (conversion) frequency. This is done by writing a 22-bit programming word to the on-board programmable oscillator. Data is written serially to the oscillator, least significant bit first. One write to the register must occur for each bit of data to be written to the oscillator, with the data to be programmed in bit 0. Note that the frequency programmed must be *twice the oversampling frequency*, rather than the output rate. See details for programming the oscillator in the section entitled *Programming the Internal Clock Generator.*

Arm Register 0002Ch

This write-only register is used to initiate pre-storage of data when the V205 is used in transient mode with pre-trigger storage. Any data pattern may be written to this register to place the V205 in an armed state. See details on using pre-trigger storage in section entitled *Modes of Operation.*

ADC Reset Register 00030h

A write to this register synchronizes all onboard ADC's. It does not alter memory contents or the values of control registers. The data written to the register is unimportant. The register should be written to after the board is configured and before acquisition is started.

Buffer Reset Register 00034h

A write to this register resets the ADC buffer memory pointers and validates configuration settings. It does not alter memory contents or the values of control registers. The value written to the register is un-

important. This register must be written to **after** configuring the ADC section and **before** enabling acquisition in order for the buffer memory to be correctly initialized.

Board Reset Register 00038h

A write to this register masks all interrupts, resets all control register bits to their power-up defaults (zero) and resets all on-board memory. The data written to the register is unimportant. The register should only be written to in order to perform a complete reset of the board prior to changing the board configuration.

Interrupt Configuration Register 1008Ch

This write-only register MUST be written with data set to 10 (0Ah) in order for the V205 to generate VXI*bus* interrupts. This write operation is used to enable hardware specific interrupt circuitry on the V205.

ADC Data 40000

This section of the V205 VXIbus memory map is used to read data from the ADC memory over the VXIbus. The VXIbus ADC Data area is 40000h bytes (256KB) in size. Therefore, the ADC Data locations can be accessed from address offset 40000h to 7FFFFh. The ADC memory buffers are strictly read only. The same area of the memory map allows test pattern data to be written to the diagnostic FIFO, which is strictly write only. See the section entitled *Using Diagnostic Mode* for details on using the built-in diagnostics.

The data is organized as one sample in each 16-bit word, with "big endian" ordering. i.e.; odd channels occupy the most significant 16 bits and even channels occupy the least significant 16 bits of a 32-bit longword, where channels are numbered from 1 to 32.

The data area appears to the user as FIFO type memory. In other words, random access to samples in the memory is not available. Data access is always sequential regardless of the address used for read or write, as long as the address used falls within the ADC Data area.

Each time a data word is read from the buffer, the data is removed from memory and buffer pointers are modified. The user must be careful to read the exact number of 32-bit words corresponding to the programmed buffer length, otherwise buffer overflow or underflow will occur.

The user should perform a reset of the memory (ADC Reset and Buffer Reset) after programming the ADC configuration and before enabling acquisition. This is necessary to ensure that the buffer pointers are correctly aligned prior to buffer access by the ADC circuits and that the ADCs are synchronized.

Addresses presented by the bus master when reading data may be either incremental of repetitive (i.e.; always the same address). Provided the addresses fall within the ADC Data area, consecutive data will be read from the board regardless of the addressing mode. This allows for standard addressing and block transfers with devices that either increment addresses or repetitively present the same address.

Using Diagnostic Mode

The V205 has built in digital diagnostic circuitry that allows the user to test all functionality of the board with the exception of the ADCs. This is accomplished by feeding the V205 with simulated ADC data from an on-board 4 Kword FIFO memory.

The diagnostic mode is used by first configuring the V205 registers and then setting the DIAG ENABLE bit , bit 2, of the Control Register. Data may then be written to the board in the ADC Data window in blocks not exceeding 4096 words. Between each block the board must be enabled and triggered until the Diag FIFO Empty bit , bit 4, in the Status register is set. The board can then be disabled and the next block written. Once all the data has been written, the DIAG ENABLE bit can then be reset, and the data written to the board can then be read back.

Chapter 4: Programming the Internal Clock Generator

Introduction

The frequency of the V205 internal sampling clock is controlled by programming the programmable oscillator through the Clock Frequency register of the VXIbus memory map. The device is programmed not in engineering units, but by means of a complex programming word whose construction is described below; a series of control words must also be written to the device. Data is transferred to the device serially; it is necessary to write the data to the V205 ADC Clock register one bit at a time; bit 0 of the register is the relevant bit. Thus, the programming sequence should normally be done by repeatedly writing each control or programming word to the ADC Clock register, shifting the data right by one bit after each write, until all bits of the word have been written.

Programming Summary

The programmable oscillator contains two registers, the Control Register and the Programming Word Register. The programming sequence is as follows:

1. Write to Control Register to configure device and prepare the device to receive the Programming Word.
2. Write Programming Word.
3. Write to Control Register to load Programming Word data into device.
4. Wait at least 5mS for device Voltage Controlled Oscillator (VCO) frequency to stabilize.
5. Write to Control Register to enable device output of new frequency.

When writing data to the Control Register, it is necessary to include a Protocol Field to identify the data as Control Register data.

Protocol Field (6 bits) = 0 1 1 1 1 0

It is important that the sequence of four ones contained in the protocol field never be sent except as part of the Protocol Field. Thus, when writing programming word data to the device, it is necessary to use a technique of inserting an extra zero after a run of three ones; this technique is called "bit stuffing", and is described in more detail in the Programming Register section.

The control register contains eight bits that are defined as shown in Table 4.1

Bit No.	Description	Function	Power-up Default
0	Enable Programming Word register to be written by next data	0 = Program Register Disabled 1 = Program Register Enabled to Receive Data	0
1	Internal Output Disable	0 = Output is VCO or f_{REF} 1 = Output is tri-stated	0
2	Internal Multiplexer	0 = Output is VCO frequency 1 = Output is f_{REF}	1
3	Device pin 12 usage	Set to zero only	0
4-7	Reserved	Must be set to 0 (reserved for future use and manufacturing test)	0000

Table 4.1

Control register data is written to the device starting with bit 0 of the control word, continuing to bit 7 of the control word, and followed by the 6 bits of the Protocol field, for a total of 14 bits.

Note that the default configuration of the device following power-up results in the output being at the frequency of the reference oscillator which is 14.31818 MHz.

Programming Register

The Programming register is written with a 22-bit word describing the required frequency of the output. However, it is essential that programming words do not mimic the Control word Protocol field by containing runs of four consecutive ones. Thus, the device specification requires that a zero must be inserted in the word after each occasion when three ones have been transmitted to the device. This procedure is known as "bit stuffing". For this reason, the actual length of a programming word may vary between 22 and 29 bits.

For example, to send this programming data:

Last Bit				First Bit
1111	0101	0111	1110	111111

Transmit this serial bit stream:

Last Bit				First Bit
10111	0101	00111	01110	01110111

The fields of the programming word are described in Table 4.2.

Field	Bits	# of Bits	Notes
P Counter value (P)	<21:15>	7	MSB (Most Significant Bits)
Reserved (R)	<14>	1	Set to logic 0
Mux (M)	<13:11>	3	
Q Counter Value (Q)	<10:4>	7	
Index (I)	<3:0>	4	LSB (Least Significant Bits)

Table 4.2

The frequency of the programmable oscillator f_{vco}, and the output frequency f_{out} are determined by these fields as follows:

$$Fvco = 2 * Fref * (P+3)/(Q+2)$$

$$Fout = Fvco/2^{M}$$

where, f_{REF} = Reference frequency (i.e., 14.31818 MHz)

The values of the P and Q parameters must be selected so that f_{vco} remains between 46 MHz and 120 MHz, inclusive. The value programmed to the M field programs a division register to allow sub-multiples of the VCO frequency to be obtained at the output; the maximum divisor possible is 128.

The **Index field (I)** is used to preset the VCO at an appropriate range. The value for this field should be chosen from the following table (Note that this table is referenced to f_{vco} rather than to the desired output frequency.)

I	f_{vco} (MHz)	I	f_{vco} (MHz)	I	f_{vco} (MHz)
0000	Shut down VCO	0110	56.6 - 59.0	1011	74.0 - 75.0
0001	.....	0111	59.0 - 60.0	1100	75.0 - 79.0
0010	.....	1000	60.0 - 63.7	1101	79.0 - 86.9
0011	.....	1001	63.7 - 70.1	1110	86.9 - 95.6
0100	46.0 - 51.0	1010	70.1 - 74.0	1111	95.6 - 120.0
0101	51.0 - 56.6				

Table 4.3

If the desired VCO frequency lies on a boundary in the table -- in other words, if it is exactly the upper limit of one entry and the lower limit of the next -- then either index value may be used (since both limits are tested), but the manufacturer recommends using the setting corresponding to the higher frequency range.

VCO Programming Constraints

There are three primary programming constraints.

1. $46MHz <= F_{vco} <= 120MHz$
2. $1 <= P <= 127$
3. $13 <= Q <= 69$

The constraints have to do with the trade-off between optimum speed with lowest noise, VCO stability and factors affecting the loop equation.

Program Register Example

The following is an example of the calculations performed by the Plug and Play driver routine.

Derive the proper programming word for 12.8 MHz clock frequency.

Since 12.8 MHz < 46 MHz, quadruple it to 51.2 MHz

Set M to 010_2

Set I to 0101_2

The result:

Fout = 12.8 = (2*14.31818*(P+3)/(Q+2)/2^m

where m = 0, 1, 2, 3, 4, 5, 6, 7

since m = 2: (P+3)/(Q+2) = 1.787936735

The two choices of P and Q giving the nearest to the required frequency are:

P	Q	f_{vco}	Error (PPM)
56	31	51.19834	32
124	69	51.22278	445

Taking the set of values which give the best accuracy, i.e., (P,Q) = (56,31):

P = 56 decimal = 0111000 binary = 0(0)111000

Q = 31 decimal = 0011111 binary = 0011(0)111

NOTE: The presence of three ones in a row in both P and Q values causes zero bit stuff values to be inserted in each. However, it is necessary to examine the values in the previous (I) field before inserting a zero in the least significant bits of the Q value. If the I field had contained a 1 in the most significant position the inserted zero would have been in a different position.

The full programming word, W is therefore:

W = P, R, M, Q, I = 00111000, 0, 010, 00110111, 0101

= 001110000010001101110101 (382375 Hex)

Oscillator Programming Example

The oscillator requires three control words plus the programming word in order to program a new output frequency (see programming sequence given in the VCO Programming Constraints section. The following paragraphs provide an overview of how the control words are built along side the programming word.

All data is written to the oscillator serially through the V205 ADC Clock register bit 0. The data is written least significant bit first. An example for programming the oscillator to an initial or new frequency is as follows:

1. Load Control register to enable loading of the Programming word register, enable the output and select the reference frequency for output from the Internal Multiplexer. The Protocol word follows the control word. All data is shifted in LSB (Least Significant Bit) first.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 1 0 1
	Protocol Word Control Reg. Data

2. Shift in the desired output frequency value via a programming word that is 22 bits in length, plus any required bit stuffs. (Up to 27 bits can be obtained with bit stuffing). The example programming word for 12.8 MHz, is shown below.

	Last Bit First Bit
Programming word for 12.8 MHz (0x382375)	0 0 1 1 1 0 0 0 0 0 1 0 0 0 1 1 0 1 1 1 0 1 0 1

3. Load the Control register to disable further loading of the Programming word register. This causes the required output frequency value to be programmed while keeping the output set to the reference frequency for the time being.

4. Wait at least 5mS for the VCO to settle to the new frequency. The value will be accurate to within 0.01% within this time.

5. Load the Control register to disable the Internal Multiplexer. This will cause the output to immediately swing to the new frequency.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 1 0 0 0
	Protocol Word Control Reg. Data

Order of Operations for Simple Acquisition

1.) Reset theV205 by writing to the Reset Board Register in A32 address space.

2.) Write the value of 10 (0Ah) to the Interrupt Configuration Register in A32 address space.

3.) Enable the Interrupt Source and select the Interrupt Request level in the Interrupt Control Register in A16 address space.

4.) Setup the V205 Control Register in A32 address space with:

   a.) Select the Trigger Source (Internal/External) using bit 0.

   b.) Select the Clock Source (Internal/External) using bit 1.

      i.) If using external clock, enable termination with bit 7.

   c.) Select the ADC oversampling ratio using bits 11 and 10.

   d.) Make **SURE** to set bit 12 to a "1".

   e.) Disable diagnostic mode with bit 2.

   f.) Clear the Enable with bit 14.

   g.) Clear the Internal Trigger with bit 13.

5.) Setup the Interrupt Mask Register to enable interrupts.

6.) Load the desired value into the Decimation Register.

7.) Setup the Acquisition Count Register.

8.) Setup the Buffer Length Register.

9.) If using the internal clock source, program the internal sample rate.

10.) Write to the ADC Reset Register, which synchronizes the converters.

11.)Write to the Buffer Reset Register, which loads the acquisition count, buffer length and frame count.

12.)Set the Enable bit, bit 14, in the Control Register.

13.)Write to the Arm Register, which starts filling the circular buffer.

14.)If using internal triggering, set the Internal Trigger bit, bit 13, in the Control Register. If external triggering is selected, this is the point in which it will be recognized.

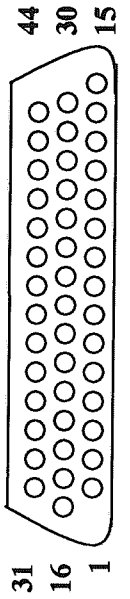
15.) Wait for the occurrence of the interrupt as a result of the trigger and the buffer being filled.

16.) If enough data has been acquired, disable acquisition by clearing the Enable bit in the Control Register. If additional data is required, repeat steps 11 through 15.

Appendix A: Connector Information

Analog Input Connectors

The Analog Inputs are brought into the module through two 44-position connectors. One connector handles inputs for channels 1 through 16 and the other handles inputs for channels 17 through 32. The following diagram shows the connector pin number for each connector.



Analog 1-16 Connector Details

Connector on board:	ODD44F4R7NTX
Mating connector:	ODD44M.....(consult Manufacturer's data for details)
Manufacturer:	Positronics Industries Inc., (417) 866-2322

Analog 1-16 Connector Signal Allocation

Pin	Signal	Pin	Signal
32	Channel 1 GND	33	Channel 1
18	Channel 2 GND	19	Channel 2
3	Channel 3 GND	4	Channel 3
34	Channel 4 GND	35	Channel 4
20	Channel 5 GND	21	Channel 5
5	Channel 6 GND	6	Channel 6
36	Channel 7 GND	37	Channel 7
22	Channel 8 GND	23	Channel 8
7	Channel 9 GND	8	Channel 9
38	Channel 10 GND	39	Channel 10
24	Channel 11 GND	25	Channel 11
9	Channel 12 GND	10	Channel 12
40	Channel 13 GND	41	Channel 13
26	Channel 14 GND	27	Channel 14
11	Channel 15 GND	12	Channel 15
42	Channel 16 GND	43	Channel 16

Note 1: All other pins are connected to analog ground on the board

Analog 17-32 Connector Details

Connector on board: Positronics ODD44F4R7NTX (see above)

Analog 17-32 Connector Signal Allocation

Pin	Signal	Pin	Signal
32	Channel 17 GND	33	Channel 17
18	Channel 18 GND	19	Channel 18
3	Channel 19 GND	4	Channel 19
34	Channel 20 GND	35	Channel 20
20	Channel 21 GND	21	Channel 21
5	Channel 22 GND	6	Channel 22
36	Channel 23 GND	37	Channel 23
22	Channel 24 GND	23	Channel 24
7	Channel 25 GND	8	Channel 25
38	Channel 26 GND	39	Channel 26
24	Channel 27 GND	25	Channel 27
9	Channel 28 GND	10	Channel 28
40	Channel 29 GND	41	Channel 29
26	Channel 30 GND	27	Channel 30
11	Channel 31 GND	12	Channel 31
42	Channel 32 GND	43	Channel 32

Note 1: All other pins are connected to analog ground on the board

P4 Local Bus Connector Details

Suitable mating connectors are available from a number of manufacturers. The one listed is an example only.

Connector on board:	8831E-026-170L (KEL Corporation
	P50E-026P1-RR1-TG (Robinson-Nugent)
Mating connector:	8825E-026-175 KEL (with strain relief)
	8825R-026-175 KEL (without strain relief)
Manufacturers:	KEL Corporation, (408) 720-9044
	Robinson-Nugent, (812) 945-0211

P4 Local Bus Connector Signal Allocation

Pin No.	Signal Name	Description
1	ADC_CLK	Distribution ADC Clock +ve. This PECL signal is used by sampling master to ensure all slaves sample at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
2	/ADC_CLK	Distribution ADC Clock -ve. This PECL signal is used by sampling master to ensure all slaves sample at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
3	GND	Digital Ground
4	SYNC	ADC Frame Sync. In multiple board systems, this signal is used by the sampling master to ensure the ADC's output synchronization on all boards. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
5	---	Not Used
6	---	Not Used
7	GND	Digital Ground
8	FSYNC	Decimation Sync. In multiple board systems, this signal is used by the sampling master to ensure TTL boards decimate on the same sample. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
9	GND	Digital Ground
10	TRIG	Distribution Trigger. This signal is used by the sampling master to ensure all boards trigger at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
11	GND	Digital Ground
12	FP_CLK	Distribution FPDP Clock +ve. The PECL signal is used by FPDP master to ensure FPDP data transfers. This signal is bussed from the FPDP master to all slaves, and is driven by the master only.
13	/FP_CLK	Distribution FPDP Clock -ve. The PECL signal is used by FPDP master to ensure FPDP data transfers. This signal is bussed from the FPDP master to all slaves, and is driven by the master only.
14	GND	Digital Ground

Pin No.	Signal Name	Description
15	FP_DV	FPDP Data Valid. This line is asserted by the FPDP transmitter. It signals valid data on the FPDP bus.
16	GND	Digital Ground
17	CHAN5	Signal used in FPDP board addressing
18	CHAN6	Signal used in FPDP board addressing
19	CHAN7	Signal used in FPDP board addressing
20	CHAN8	Signal used in FPDP board addressing
21	CHAN9	Signal used in FPDP board addressing
22	GND	Digital Ground
23	EXT_TRIG	External Trigger. The user drives this TTL signal to supply an external trigger. In multiple board systems, only the sampling master receives the external trigger signal.
24	GND	Digital Ground
25	EXT_CLK	External Clock. The user drives this TTL signal to supply an external sampling clock. In multiple board systems, only the sampling master receives the external clock signal.
26	GND	Digital Ground

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2. Obtain a Return Authorization (RA) Number.
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5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com