Model V215

32-Channel, 16-bit A/D Converter

INSTRUCTION MANUAL

March, 1998

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FIGURES

TABLES

32-Channel, 16-bit Scanning ADC

A multichannel ADC with optional input filters

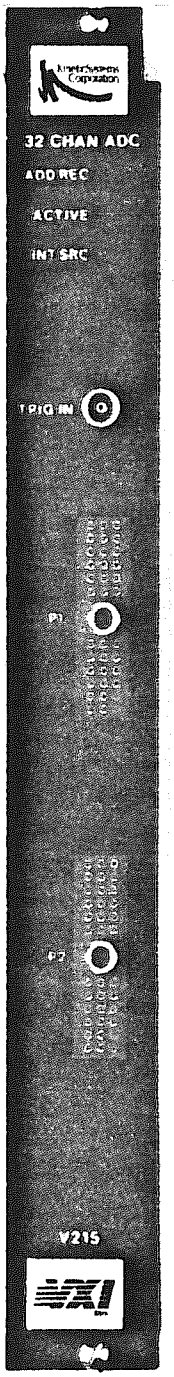
V215

Features

- **32-channel capability with differential inputs**
- **16-bit resolution**
- **Programmable gain (1 to 1024) per channel**
- **Programmable number of active channels**
- **Self-scan and triggered scan operation**
- **Dual-ported buffer memory**
- **Options with 6 Hz low-pass filter**
- **Options available with temperature reference inputs**

Typical Applications

- **Powertrain/engine testing**
- **Temperature measurements**
- **General-purpose data acquisition**



General Description

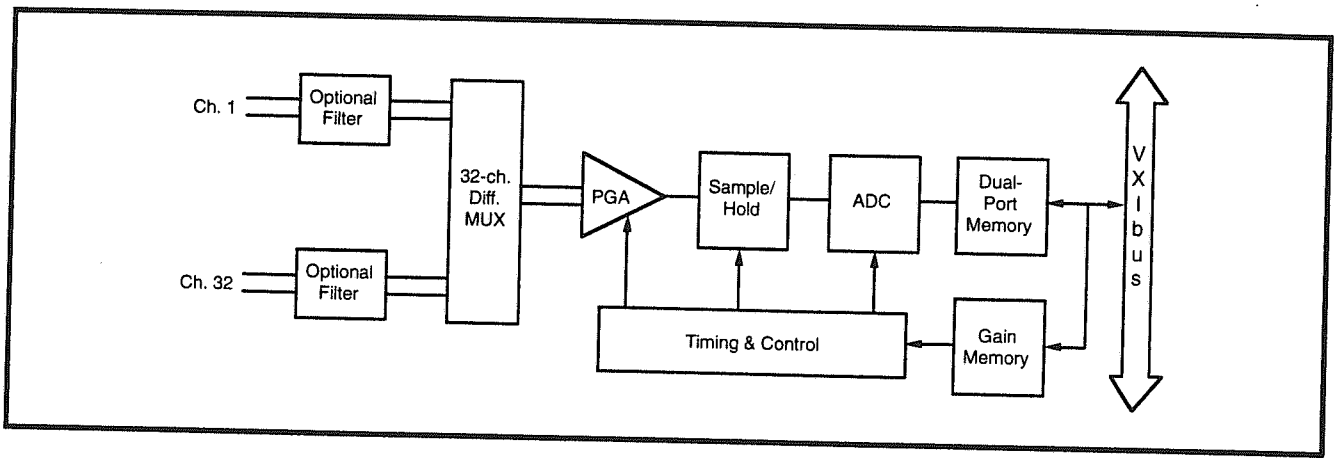
The V215 is a single width, C-size, register-based, VXIbus module that can digitize as many as 32 analog voltage channels. The resulting digital data can be read over the VXIbus. The module contains a 16-bit analog-to-digital converter capable of resolving one part in 65,536. The number of active (scanned) channels is software programmable. There are two software-selectable scan modes: continuous and single-scan. With continuous mode, VXIbus Read cycles are asynchronous with the conversion process, eliminating any overhead due to testing for "converter busy." If it is desirable to synchronize scanning and reading, single-scan mode can be used. In this mode, an interrupt is generated after the last channel has been converted. In addition, the external trigger input may be used to synchronously trigger a single scan on multiple V215s.

The V215 contains a 4-bit, 32-word memory which can be loaded on a channel-by-channel basis with an appropriate gain factor for each differential input signal. Eleven gain factors, from 1 to 1024, are available. This allows one V215 to measure a wide variety of input signal types (such as thermocouples, high-level inputs, etc.). Once channel scanning is initiated, each channel's input is selected, the pre-loaded gain factor is applied to it, the amplified signal is converted, and the resultant binary information is stored in the on-board memory. Conversions take place at the rate of one every 250 µs (all 32 channels in 8 ms). The memory is configured in a dual-ported fashion to facilitate the retrieval of data with block transfer operations.

All versions of the V215 are precalibrated for ±10 V inputs. The V215-VC11 and -VD11 options include a single-pole low-pass filter at the input of each channel. These filters provide a -3 dB cutoff frequency of 6 Hz. To facilitate the use of this module in temperature monitoring systems, the V215-VB11 and -VD11 options are available. On these options, both channels 1 and 17 are configured to power and receive an isothermal reference signal from a KineticSystems Model V792-ZA11 32-channel Isothermal Panel. For monitoring 4-20 mA current loop signals, it is common practice to mount a precision 250 Ω resistor external to the module (i.e., at a terminal strip). This allows the input to the V215 to be disconnected without disrupting the current loop. The loop must not exceed the maximum common-mode voltage rating of the V215. The KineticSystems Model 1854 Termination Panel may be used for this purpose.

All input signals are brought to the module through a pair of 36-pin AMP rectangular connectors mounted on the front panel. These connectors mate directly with the KineticSystems Model 5944-Z1A mating connectors and with the 5855-Series of cable assemblies. The external trigger is brought in through a single-pin LEMO connector. An LED flashes whenever the module is addressed, and an ACTIVE light indicates when the module is powered and scanning is activated. An interrupt LED is illuminated whenever an interrupt is pending.

The V215 supports both static and dynamic configuration. Access to the converted data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specifications
Inputs	
Number of input channels	32 differential inputs
Input signal range	±10 V dc, maximum
Input protection	±35 V, continuous; ±300 V for 100 µs
Common-mode input voltage	±10.5 V dc, maximum
Common-mode rejection	-110 dB at dc to 1 Hz; -6 dB/octave rolloff to -70 dB at 1 kHz
Input impedance	22 MΩ
Drift	
G = 1 to 16	±0.0013% FSR/°C, maximum
G = 32 to 256	±0.0018% FSR/°C, maximum
G = 512	±0.0030% FSR/°C, maximum
G = 1024	±0.0057% FSR/°C, maximum
Filtering (-VC11, -VD11 Options)	
Input filter	single-pole, low-pass RC type
-3dB cutoff frequency (f_c)	6 Hz
A/D Converter	
Resolution	16 bits (one part in 65,536)
Linearity error	±0.003% of Full Scale Range
Differential linearity error	±0.003% of Full Scale Range
Drift	±0.0018% FSR/°C, maximum
Quantization error	±½ LSB, typical
Conversion time	250 µs
On-board memory	32 16-bit words
Input connector type	36P AMP Rectangular
Power requirements	
+5 V	2.7A, typical
+24 V	80 mA, typical
-24 V	79 mA, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to +40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front panel potential	Chassis ground

Ordering Information

Model V215-VA11 32-channel, 16-bit A/D Converter; without filters or compensation reference
Model V215-VB11 32-channel, 16-bit A/D Converter; without filters, with compensation reference
Model V215-VC11 32-channel, 16-bit A/D Converter; with filters, without compensation reference
Model V215-VD11 32-channel, 16-bit A/D Converter; with filters and compensation reference

Related Products

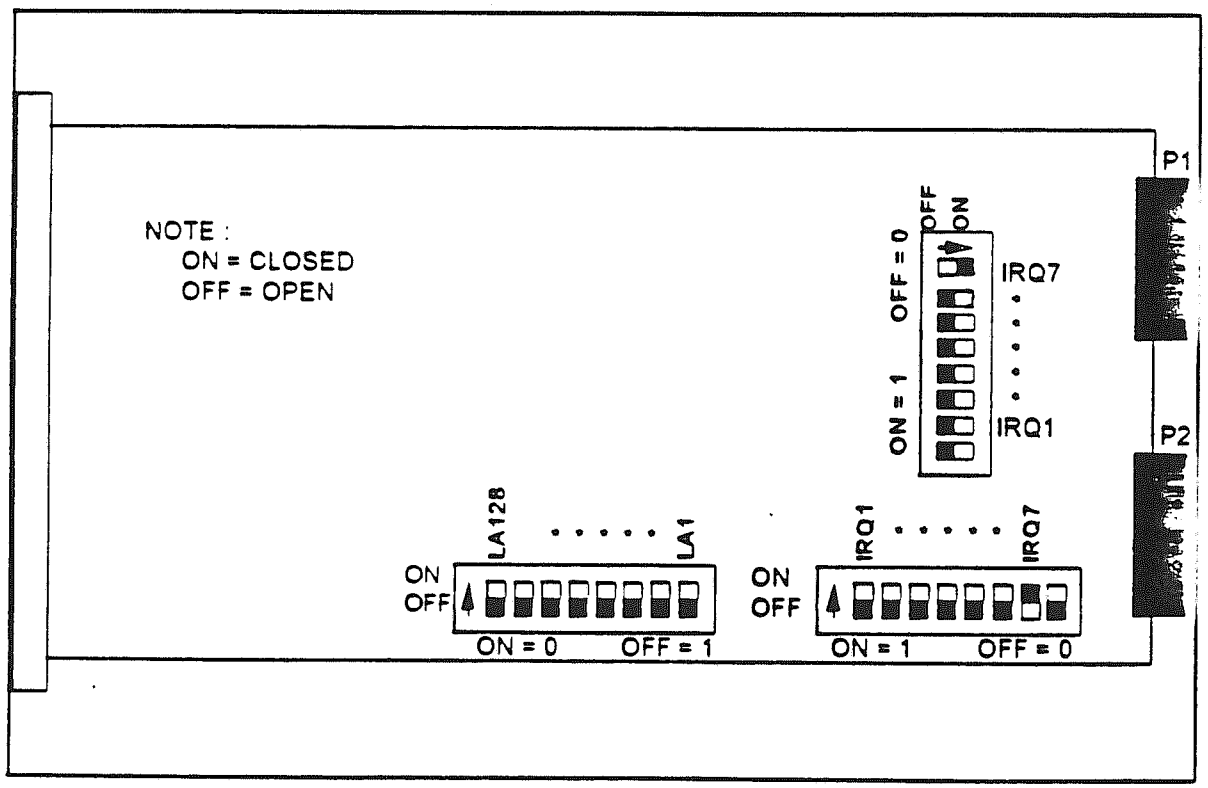
Model 5855-Axyz Cable—36P AMP Rectangular to Unterminated
Model 5855-Bxyz Cable—36P AMP Rectangular to 50S Amphenol Ribbon
Model 5855-Cxyz Cable—36P AMP Rectangular to 36P AMP Rectangular
Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO
Model 5944-Z1A Connector—36P AMP Rectangular
Model V765-ZA11 Rack-mount Termination Panel
Model V792-ZA11 Rack-mount Isothermal Panel

UNPACKING AND INSTALLATION

The Model V215 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V215 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V215 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. Refer to FIGURE 1.



The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V215 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 for the switch locations and switch settings. Both banks of eight-position switches must be set to the same value. As shown in Figure 1, IRQ 7 is set to the same position in both banks.

Module Insertion

The V215 is a C-sized, single width VXIbus module. It requires 2700 milliamperes of +5 volt power, 80 milliamperes ±25 power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

To insure proper interrupt acknowledge cycles from the V215 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Daisy-chain jumpers must be installed in any empty slot between the V215 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED is illuminated when the Operational Registers are being accessed.

ACTIVE — When this LED is on,the V215 is scanning the active channels.

INT SRC — This LED turns on when scanning has stopped and DONE Interrupt request is enabled.

Input Connectors

Trigger-In

An External Trigger source may be used to initiate a single scan operation. Scanning will start on the falling edge of a 100 nanosecond-wide (minimum) TTL level trigger pulse.

P1 PINOUT

The front panel P1 connector is used to connect analog signals to channels 1 through 16. Refer to Figure 3 (page 6) for the P1 connector pin assignments.

P2 PINOUT

The front panel P2 connector is used to connect analog signals to channels 17 through 32. Refer to Figure 4 (page 7) for the P2 connector pin assignments.

FIGURE 2 - V215 INPUT CONNECTORS

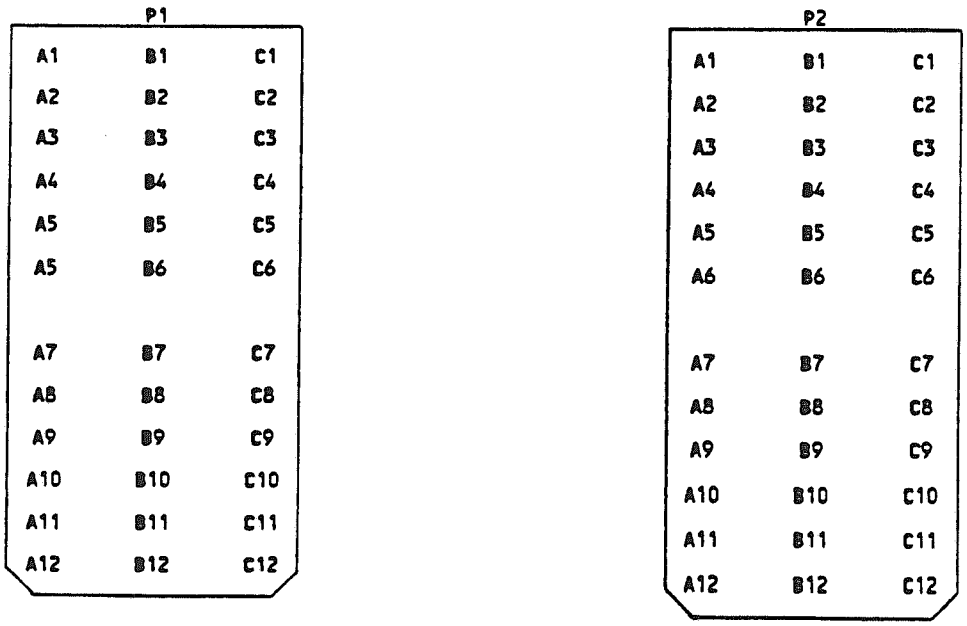


FIGURE 3 - INPUT CONNECTOR P1 PINOUT

PIN NO	NOMENCLATURE
A 1	CHANNEL 1 SIGNAL (INPUT)
A 2	CHANNEL 1 RETURN (INPUT)
A 3	CHANNEL 2 SIGNAL (INPUT)
A 4	CHANNEL 2 RETURN (INPUT)
A 5	CHANNEL 3 SIGNAL (INPUT)
A 6	CHANNEL 3 RETURN (INPUT)
A 7	CHANNEL 4 SIGNAL (INPUT)
A 8	CHANNEL 4 RETURN (INPUT)
A 9	CHANNEL 5 SIGNAL (INPUT)
A10	CHANNEL 5 RETURN (INPUT)
A11	CHANNEL 6 SIGNAL (INPUT)
A12	CHANNEL 6 RETURN (INPUT)
B 1	CHANNEL 7 SIGNAL (INPUT)
B 2	CHANNEL 7 RETURN (INPUT)
B 3	CHANNEL 8 SIGNAL (INPUT)
B 4	CHANNEL 8 RETURN (INPUT)
B 5	CHANNEL 9 SIGNAL (INPUT)
B 6	CHANNEL 9 RETURN (INPUT)
B 7	CHANNEL 10 SIGNAL (INPUT)
B 8	CHANNEL 10 RETURN (INPUT)
B 9	CHANNEL 11 SIGNAL (INPUT)
B10	CHANNEL 11 RETURN (INPUT)
B11	CHANNEL 12 SIGNAL (INPUT)
B12	CHANNEL 12 RETURN (INPUT)
C 1	CHANNEL 13 SIGNAL (INPUT)
C 2	CHANNEL 13 RETURN (INPUT)
C 3	CHANNEL 14 SIGNAL (INPUT)
C 4	CHANNEL 14 RETURN (INPUT)
C 5	CHANNEL 15 SIGNAL (INPUT)
C 6	CHANNEL 15 RETURN (INPUT)
C 7	CHANNEL 16 SIGNAL (INPUT)
C 8	CHANNEL 16 RETURN (INPUT)
C 9	DIGITAL GROUND
C10	DIGITAL GROUND
C11	DIGITAL GROUND
C12	DIGITAL GROUND

FIGURE 4 - INPUT CONNECTOR P2 PINOUT

PIN NO	NOMENCLATURE
A 1	CHANNEL 17 SIGNAL (INPUT)
A 2	CHANNEL 17 RETURN (INPUT)
A 3	CHANNEL 18 SIGNAL (INPUT)
A 4	CHANNEL 18 RETURN (INPUT)
A 5	CHANNEL 19 SIGNAL (INPUT)
A 6	CHANNEL 19 RETURN (INPUT)
A 7	CHANNEL 20 SIGNAL (INPUT)
A 8	CHANNEL 20 RETURN (INPUT)
A 9	CHANNEL 21 SIGNAL (INPUT)
A10	CHANNEL 21 RETURN (INPUT)
A11	CHANNEL 22 SIGNAL (INPUT)
A12	CHANNEL 22 RETURN (INPUT)
B 1	CHANNEL 23 SIGNAL (INPUT)
B 2	CHANNEL 23 RETURN (INPUT)
B 3	CHANNEL 24 SIGNAL (INPUT)
B 4	CHANNEL 24 RETURN (INPUT)
B 5	CHANNEL 25 SIGNAL (INPUT)
B 6	CHANNEL 25 RETURN (INPUT)
B 7	CHANNEL 26 SIGNAL (INPUT)
B 8	CHANNEL 26 RETURN (INPUT)
B 9	CHANNEL 27 SIGNAL (INPUT)
B10	CHANNEL 27 RETURN (INPUT)
B11	CHANNEL 28 SIGNAL (INPUT)
B12	CHANNEL 28 RETURN (INPUT)
C 1	CHANNEL 29 SIGNAL (INPUT)
C 2	CHANNEL 29 RETURN (INPUT)
C 3	CHANNEL 30 SIGNAL (INPUT)
C 4	CHANNEL 30 RETURN (INPUT)
C 5	CHANNEL 31 SIGNAL (INPUT)
C 6	CHANNEL 31 RETURN (INPUT)
C 7	CHANNEL 32 SIGNAL (INPUT)
C 8	CHANNEL 32 RETURN (INPUT)
C 9	DIGITAL GROUND
C10	DIGITAL GROUND
C11	DIGITAL GROUND
C12	DIGITAL GROUND

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V215 implements those required for register-based devices. The V215 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both registers sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short (A16) address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register, are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

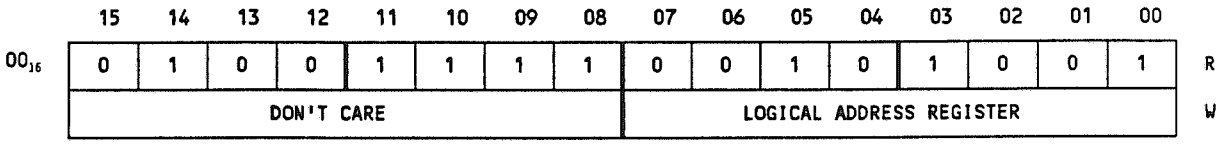
Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V215 are offset from the base address. **Note: The V215 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** TABLE 1 shows the applicable Configuration Registers present in the V215, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET (HEX)	W/R MODE	REGISTER NAME
00_{16}	W/R	ID/Logical Address Register
02_{16}	R	Device Type Register
04_{16}	W/R	Status/Control Register
06_{16}	W/R	Offset Register
08_{16}	R	Attribute Register
$1E_{16}$	R	Subclass Register

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:



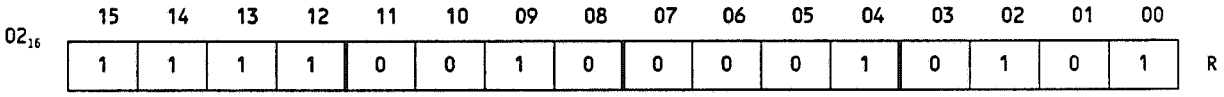
On READ transactions:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V215. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

The format and bit assignments for the ID/Logical Address Register are as follows:



On READ transactions:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V215 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V215 (215_{16}).

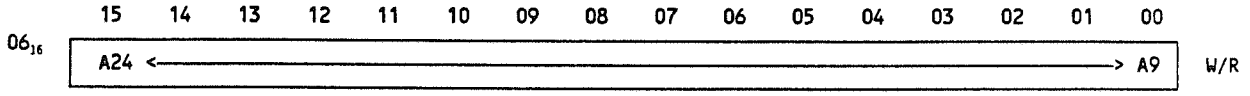
Status/Control Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	ZEROS								RDY	PASS	0	RST	R
	A24 ENA	N/U	N/U	1	NOT USED											RST	W

Bit	Mnemonics	Description
15	A24	Writing a "1" will enable A24 addressing and allow access to the Operational Registers. Reading a "1" indicates A24 addressing is active. This bit is reset to a "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on VXIbus P2 connector. A "0" will indicate that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V215. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".
11-4	N/U	Not used. Read as a "0".
3	RDY	READY. The V215 is always "ready". Read as a "1".
2	PASS	PASS. The V215 will always pass self tests. Read as a "1".
1	N/U	NOT USED. Read as a "0".
0	RST	RESET. This Read/Write bit controls the Soft Reset condition within the V215. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below), except for the Diagnostic and Interrupt Status registers, is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset

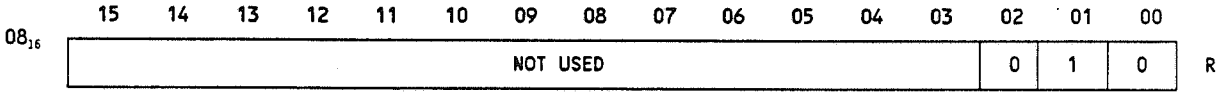
being enabled. This bit can be reset by writing a "0", on power-up, or the assertion of SYSRESET*.

Offset Register



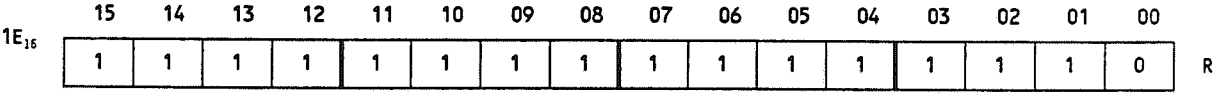
This 16-bit read/write register defines the base address of the A24 Operational Registers. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Attribute Register



Bit(s)	Mnemonic	Meaning
15 - 03	Not Used	These bits are not used by the V215, and are read as zeros.
02	Intr Control	The V215 does not have any Interrupt Control capabilities.
01	Intr Handler	The V215 does not have Interrupt Handler capabilities.
00	Intr Status	The V215 does not have an Interrupt Status register.

Subclass Register



Bit(s)	Mnemonic	Meaning
15	Extended Device	"1" indicates this to be a VXIbus defined Extended Device.

OPERATIONAL REGISTERS

The Operational Registers are the method of accessing the functional registers of the V215. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V215 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 62 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V215, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2
V215 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	W/R MODE	REGISTER NAME
00_{16}	W/R	Diagnostic Register
02_{16}	R	Interrupt Status Register
12_{16}	R	Channel 1 Memory Data
16_{16}	R	Channel 2 Memory Data
$1A_{16}$	R	Channel 3 Memory Data
$1E_{16}$	R	Channel 4 Memory Data
22_{16}	R	Channel 5 Memory Data
26_{16}	R	Channel 6 Memory Data
$2A_{16}$	R	Channel 7 Memory Data
$2E_{16}$	R	Channel 8 Memory Data
32_{16}	R	Channel 9 Memory Data
36_{16}	R	Channel 10 Memory Data
$3A_{16}$	R	Channel 11 Memory Data
$3E_{16}$	R	Channel 12 Memory Data
42_{16}	R	Channel 13 Memory Data
46_{16}	R	Channel 14 Memory Data
$4A_{16}$	R	Channel 15 Memory Data
$4E_{16}$	R	Channel 16 Memory Data
52_{16}	R	Channel 17 Memory Data
56_{16}	R	Channel 18 Memory Data
$5A_{16}$	R	Channel 19 Memory Data
$5E_{16}$	R	Channel 20 Memory Data
62_{16}	R	Channel 21 Memory Data
66_{16}	R	Channel 22 Memory Data
$6A_{16}$	R	Channel 23 Memory Data
$6E_{16}$	R	Channel 24 Memory Data
72_{16}	R	Channel 25 Memory Data
76_{16}	R	Channel 26 Memory Data
$7A_{16}$	R	Channel 27 Memory Data
$7E_{16}$	R	Channel 28 Memory Data
82_{16}	R	Channel 29 Memory Data
86_{16}	R	Channel 30 Memory Data
$8A_{16}$	R	Channel 31 Memory Data
$8E_{16}$	R	Channel 32 Memory Data
92_{16}	W	Control Memory Address
96_{16}	W	Control Memory Data
$9A_{16}$	R	Control Memory Data
$9E_{16}$	W	Last Channel Register
$A2_{16}$	R	Single Scan
$A6_{16}$	R	Stop Scan
AA_{16}	R	Clear Control Memory Address
AE_{16}	R	Enable Continuous Scanning
$B2_{16}$	R	Disable Continuous Scanning
$B6_{16}$	R	Enable DONE INT Request
BA_{16}	R	Disable DONE INT Request
BE_{16}	R	Clear DONE INT Status
$C6_{16}$	R	Test DONE INT Status

Diagnostic Register 00_{16}

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	INT ENA	INT SRC	0	0	0	R
00_{16}	Don't Care								0	0	0	INT ENA	0	0	0	INIT	W

Bit	Mnemonic	Description
15-8	Don't Care	Not used, read as "0".
7	Diagnostic	When this bit is set to a "1", the last register access to an Operational Register (at offsets 12_{16} through $6C_{16}$) was valid.
6	Status	When this bit is set to a one, the last register access to an Operational Register (at offsets 12_{16} through $6C_{16}$) was accepted.
5	N/U	Not used, read as "0".
4	INT ENA	Interrupt Enable: Setting this bit to a "1" will enable interrupts.
3	INT SRC	Interrupt Source: When this bit is set to a "1", the V215 has completed a scan of the input channels.
2,1	N/U	Not used, read as "0".
0	INIT	Setting this bit to a "1" will only reset the Operational Registers (12_{16} through $6C_{16}$). The Configuration Registers and the Diagnostic Registers are unaffected.

Interrupt Status/ID Register 02_{16}

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	STATUS								ID								R

This is a Read-Only 16-bit Interrupt Status Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit	Mnemonic	Description
15-8	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
7-0	ID	These eight bits represent the Logical Address of the V215 Configuration Registers.

Channel Memory Data Registers (OFFSETS 12_{16} - $8E_{16}$)

There are 32 channels on the V215 that are updated during a scan operation. Each channel has its own data register as shown on Table 2 (page 12). These 32 data registers can be read anytime when the status bit in the Diagnostic register set to a "1".

Control Memory Address Register (OFFSET 92_{16})

A write to this register will select the channel to be accessed for control purposes (see below). Data will range from 0-31 to represent channels 1-32. Writing to the Control Memory Address Register is only accepted when the V215 is not scanning its inputs. If the status bit in the Diagnostic Register equals "1", the command was accepted. A "0" would indicate the command was not accepted because the V215 was in scan mode.

Write Control Memory Data Register (OFFSET 96_{16})
Read Control Memory Data Register (OFFSET $9A_{16}$)

After writing the Control Memory Address register, data can be written to the Control Memory Data register. The Control Memory Data register is used to set the gain for the channel of interest. It is described later in the Control Memory Data section (Page 16). After each write to the Control Memory Data register, the Memory Address register will increment by one. The Control Memory Data register can be read in a similar fashion to verify the contents. A write or read to the Control Memory Data register is only accepted when the V215 is not scanning. If the status bit in the Diagnostic Register equals "1", the command was accepted. A "0" would indicate the command was not accepted because the V215 was in the scan mode.

Last Channel Register (OFFSET $9E_{16}$)

This register will select the channel scan size by writing the channel number to be scanned last. Data range is 0-31 is used to represent channel 1-32. A write to this register is only accepted when the V215 is not in a scan operation. If the status bit in the Diagnostic Register

equals "1", the command was accepted. A "0" would indicate the command was not accepted because the V215 was in the scan mode.

OPERATIONAL CONTROL REGISTERS

The V215 has nine Operational Control Registers at offset $A2_{16}$ through $C6_{16}$. These registers are Read-Only and return a 16-bit data code. There are only two possible codes that can be returned. The first data code will return a value of "0" and has the same meaning as the Status bit in the Diagnostic Register. The second data code will return a value of "one" and has the same meaning as the Status bit in the Diagnostic Register. This data code will indicate the command was accepted or a test condition is true when equal to one. These nine Operational Control Registers are described below:

Single Scan (OFFSET $A2_{16}$)

A read from this register will initiate a single scan operation and clear the SCAN DONE status bit. A data code of "1" indicates the command was accepted. A data code of "0" indicates the V215 is already in SCAN mode.

Stop Scan (OFFSET $A6_{16}$)

A read from this register will immediately stop channel scanning and initialize the Control Memory Address register (92_{16}) to "0". A data code of "1" indicates the command was accepted. A data code of "0" indicates the V215 was not scanning prior to this Stop command.

Clear Control Memory Address Register (OFFSET AA_{16})

A read from this register will initialize the Control Memory Address register to zero. A data value of "1" indicates the command was accepted. A data code of "0" indicates the V215 is still scanning and this clear command was not accepted.

Enable Continuous Scanning (OFFSET AE_{16})

A read from this register will enable the V215 to scan continuously and clear the SCAN DONE status bit. A data code of "1" indicates the command was accepted.

Disable Continuous Scanning (OFFSET $B2_{16}$)

A read from this register will disable the V215 from scanning. The V215 will continue scanning until the last channel is scanned. At this time the SCAN DONE status bit will be set. A data code of "1" indicates the command was accepted.

Enable DONE INT Request (OFFSET $B6_{16}$)
Disable DONE INT Request (OFFSET BA_{16})

A read from either register will enable or disable SCAN DONE INTERRUPT Request. SCAN DONE INT Request must be enabled if the V215 is to generate an interrupt. Both registers will return a data code of "1". A data code of "1" indicates the command was accepted.

Clear Scan DONE Status (OFFSET BE_{16})

A read from this register will clear the SCAN DONE status bit. A data code of "1" indicates the command was accepted.

Test Scan DONE Status (OFFSET $C6_{16}$)

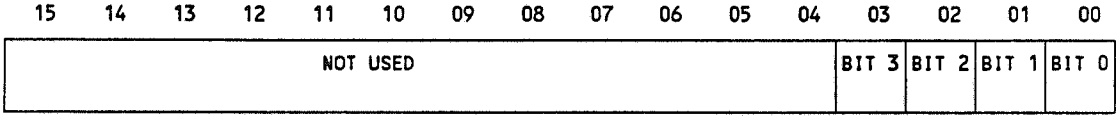
A read from this register will test whether the SCAN DONE status is set or not. If the data code is set to "1", then SCAN DONE Status is set.

SCAN SIZE PROGRAMMING

The first step in using the Model V215 is to select the number of channels to be scanned. Any number of channels, from 1 to 32, is allowable. A write to the Last Channel register (OFFSET $9E_{16}$) is used to select the number of active channels on the V215. Data values ranging from 0 to 31 are used to select a scan size from 1 to 32. Note that the V215 will automatically default to scanning all 32 channels after a reset, or from a power-up state.

The next step is to set the appropriate gain factor for each channel. The Control Memory of the Model V215 contains the GAIN settings for each of the 32 channels. This is a four-bit memory which can be loaded using the Control Memory Data Register (OFFSET 96_{16}). By using the Control Memory Address register (OFFSET 92_{16}), any channel may be selected with write data. Data will range from 0-31 to represent channels 1-32. Then write to the Control Memory Data register with the appropriate GAIN factor for the selected channel. There are eleven GAIN settings, from one to 1024, available in a binary progression, as listed below:

CONTROL MEMORY DATA



CONTROL MEMORY GAIN FACTORS

DATA	GAIN FACTOR	FULL-SCALE INPUT VALUE	LSB
0	1	±10.000 v	305.175 μv
1	2	± 5.000 v	152.580 μv
11	4	± 2.500 v	76.290 μv
101	8	± 1.250 v	38.150 μv
110	16	±625.000 mv	19.073 μv
1000	32	±312.500 mv	9.536 μv
1001	64	±156.250 mv	4.768 μv
1011	128	±78.125 mv	2.384 μv
1100	256	±39.0675 mv	1.192 μv
1101	512	±19.530 mv	596.046 nv
1111	1024	± 9.765 mv	298.023 nv

After a write to the Control Memory Data register, the Control Memory Address register will increment by one, thereby allowing the user to execute successive writes to the Control Memory Data register at the next consecutive channel. This feature eliminates the need to execute another write to the Control Memory Data register to set the next channel. It is advisable at this point, if any of the 32 channels will not be used, to set those channel gain factors to a value of one.

NOTE:	**In order to write to the Control Memory Address and Control Memory Data registers, V215 scanning must be disabled.**

SCANNING FORMATS

Once all the gains are set, the module is ready for scanning. There are two scanning formats. The first is a single scan operation initiated by reading the Single Scan register (OFFSET $A2_{16}$), or by an external trigger. In this format, the module will scan all 32 channels once, store the converted data for each channel, and then set the SCAN DONE status to indicate that the single scan operation is complete. The second format is continuous scanning which is initiated by reading the Enable Continuous Scanning register (OFFSET AE_{16}). In this mode, the channels are continuously scanned, and the converted data for each channel is updated every 8 milliseconds.

READING OF DATA

The V215 has the capabilities of being read while the module is in a scanning process. Any channel's converted memory data can be read by its appropriate Channel Memory Data register (OFFSET $12_{16}8E_{16}$). Refer to Table 2 (page 13) for the correct offset value for a given channel number.

DISABLING SCAN

There are two ways of disabling a continuous scan process. The first method is by reading the STOP SCAN register (OFFSET $A6_{16}$) which will stop scanning immediately. When this command is initiated, the module will stop scanning after the present channel is converted. The Control Memory Address will be reset to zero and the Scan DONE status bit will be set to indicate that scanning has been disabled. The other method is to read the Disable Continuous Scanning register (OFFSET $B2_{16}$) which will disable scanning after all 32 channels have been scanned. For example, if the Model V215 scanning sequence is at channel 9 when register at offset $B2_{16}$ is read, the module will continue on until the 32^{nd} channel is scanned. The Scan Done status bit will be set at this time to indicate that scanning is disabled.

INTERRUPTS

The V215 must be set properly to generate an interrupt on the VXIbus. First, the interrupt switches must select one of seven Interrupt Requests by switching the appropriate IRQ switches to the "ON" position. (Refer to the Interrupt Request Switch Section (Page 4) for further information.) Next, enable interrupts in the following manner:

> Enable the Interrupt Request by reading the ENA INT Request Register (OFFSET 00_{16}).
>
> Enable Interrupts to the VXIBUS by writing Bit 4 in the Diagnostic Register (OFFSET 00_{16}) to a Logical "1".

The V215 is now able to cause an interrupt on the VXIbus. Once the V215 sets an interrupt, an interrupt handler will read the Status/ID Register and reset the Enable Interrupt bit in the Diagnostic Register to a Logical "0". At this time, the interrupt request should be cleared which will also clear INT SRC in the Diagnostic Register (OFFSET 00_{16}) to a Logical "0". To clear an Interrupt request, read the Clear DONE INT Status Register (OFFSET BE_{16}). Once INT SRC Bit 3 in the Diagnostic Register is set to a Logical "0", the Interrupt Enable Bit 4 in the Diagnostic Register can be set to a Logical "1". If INT SRC is a Logical "1" when INT ENA is set to a Logical "1", an interrupt will occur instantly.

APPENDIX

V215 REGISTER LAYOUT

CONFIGURATION REGISTERS

ID/Logical Address Register (OFFSET 00_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	R
00_{16}	DON'T CARE								LOGICAL ADDRESS REGISTER								W

Device Type (OFFSET 02_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	0	0	0	0	1	0	1	0	1	R

Status/Control Register (OFFSET 04_{16})

	15	14	13	12	11 10 09 08 07 06 05 04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	ZEROS	RDY	PASS	0	RST	R
	A24 ENA	N/U	N/U	1	NOT USED				RST	W

Offset Register (OFFSET 06_{16})

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A24 <----------															A9	W/R

Attribute Register (OFFSET 08_{16})

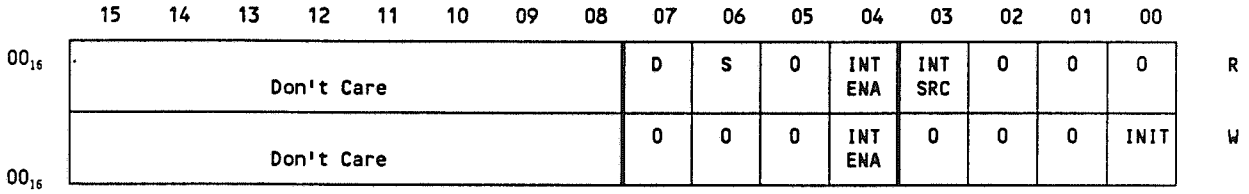
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	NOT USED													0	1	0	R

Subclass Register (OFFSET $1E_{16}$)

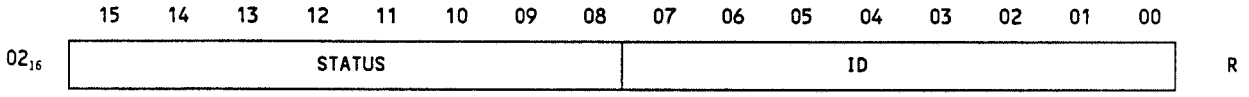
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

OPERATIONAL REGISTERS

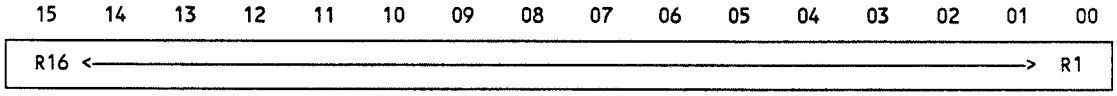
Diagnostic Register (OFFSET 00_{16})



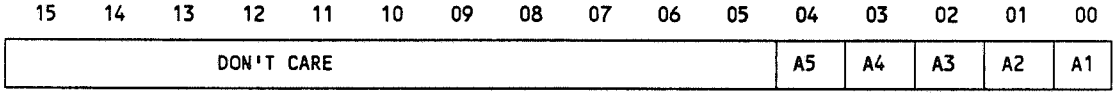
Interrupt Status/ID Register (OFFSET 02_{16})



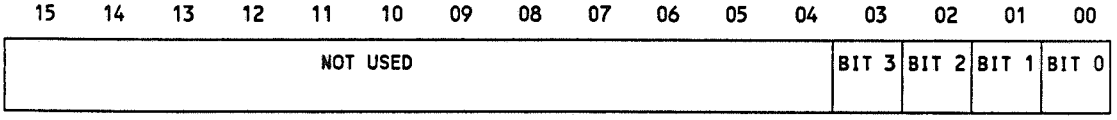
Channel Memory Data Register (OFFSET 12_{16} - $8E_{16}$)



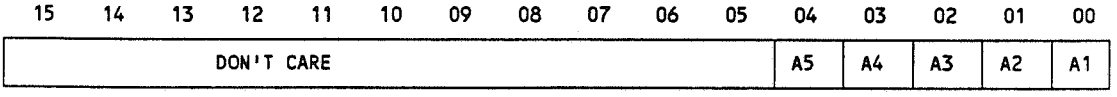
Control Memory Address Register (OFFSET 92_{16})



Control Memory Data Register (OFFSET $W96_{16}$ - $R9A_{16}$)



Last Channel Register (OFFSET $9E_{16}$)



OPERATIONAL CONTROL REGISTERS

Single Scan (OFFSET $A2_{16}$)
Stop Scan (OFFSET $A6_{16}$)
Clear Control Memory Address (OFFSET AA_{16})
Enable Continuous Scanning (OFFSET AE_{16})
Disable Continuous Scanning (OFFSET $B2_{16}$)
Enable DONE INT Request (OFFSET $B6_{16}$)
Disable DONE INT Request (OFFSET BA_{16})
CLEAR Scan DONE Status (OFFSET BE_{16})
Test Scan DONE Status (OFFSET 66_{16})