16-channel, 24-bit Sigma-Delta ADC

A multichannel ADC with more than 19 bits of resolution

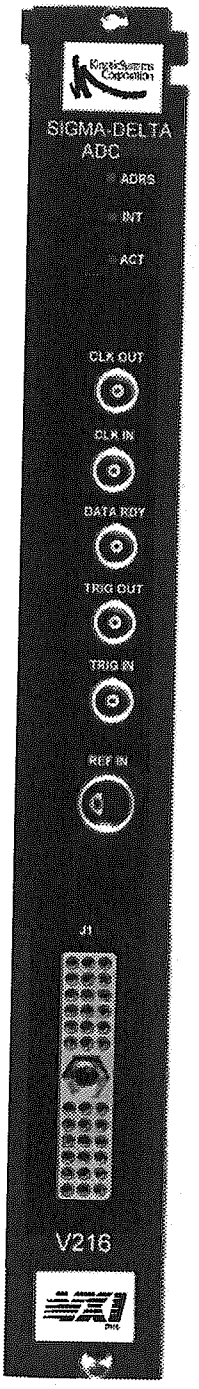
V216

Features

- **16-channels, 24-bit data fields (up to 19 bits single-shot resolution—more with sample averaging)**
- **Automatic tracking filtering (-3 dB at 0.262 × sample rate)**
- **Channel-by-channel programmable pre-gain (1 or 100)**
- **Channel-by-channel programmable post-gain (1 through 128)**
- **Continuous scan mode at 9.76 Hz to 1.028 kHz sampling rates (per channel)**
- **Single-scan mode through synchronizing front-panel trigger (in and out) or VXI command**
- **Two calibration modes—internal zero/full-scale references or external (front-panel LEMO) full-scale reference**

Typical Applications

- **Magnetic modeling**
- **Systems requiring very high resolution**



General Description *(Product specifications and descriptions subject to change without notice.)*

The Model V216 is a single-width, C-size, register-based, VXIbus module that functions as either a single-scan or continuously active 16-channel Sigma-Delta ADC. Sigma-Delta conversion is a technique which attains its very high accuracy by digitally decimating and filtering the output of a fast, single-bit converter. This eliminates the need for expensive tracking filter, sample/hold, and gain functions allowing a simple ADC-per-channel structure. This further eliminates the need to multiplex inputs to a common ADC and thereby reduces crosstalk effects to negligible levels. Another important consequence of the digital filtering is that filter notches are produced which can be made to coincide with 60 Hz (or 50 Hz) power line frequencies and their harmonics. Thus, even in environments with severe signal corruption due to power line noise, very good results are possible.

The V216 module provides for independently selectable post-gains of 1 to 128 on differentially-received inputs which accept up to ±10 V full-scale. A common sampling rate should be chosen for all channels that may range from 9.76 Hz to 1.028 kHz. These frequencies also define the first notch in the built-in, low-pass tracking filters. The -3 dB bandwidth is consequently always 0.262 times the selected sampling rate. The effective resolution of each channel is derated by increased gain and sampling rate, and ranges from 19 bits at a gain of one and a 10 Hz rate to 8 bits at a gain of 128 and a 1 kHz rate. For all gains at rates of 100 Hz and below, resolution is at least 15 bits. In addition, a channel-by-channel programmable pre-gain of 100 may be selected with only minimal reduction of effective resolution. The effect on resolution under various sampling rate conditions is described in the specifications.

When a single-scan operation is triggered, a single conversion cycle takes place and one sample point for each channel is recorded. The channels are first synchronized so that these samples correspond to the same point in time. This synchronization process causes the data to remain invalid for four sample intervals of the sample rate selected. When all 16 channel samples have been recorded after this interval, an Interrupt Request signal, if enabled, is issued to indicate that the channels are ready for read-out. Alternatively, the Interrupt Status condition may be polled by waiting for a "valid data" response from a read of the VXI Interrupt Status Operational Register to indicate that data is available. In addition to these indications, a TTL *Data Ready* trigger output is provided on the front panel which may be used to trigger a VXI processing device such as the KineticSystems Model V160 Slot-0 Controller.

If active-scanning is initiated, the channels are first synchronized, causing the first valid sample of each channel to be inaccessible for a period of four sample intervals. Thereafter, new valid samples appear in

the space of each sample interval. Once again, when all 16 channels have deposited valid data for a given sample interval, an interrupt, if enabled, will be issued (or Interrupt Status may be polled) to indicate that read-out may commence. The front-panel *Data Ready* trigger is also activated.

The V216 module provides for two mechanisms of offset and gain calibration. A self-calibration mode uses a mid-scale (0 V) and positive full-scale reference internal to each channel's Sigma-Delta converter to calculate offset and gain for that converter. Alternatively, a system calibration mode may be selected which connects mid- and full-scale voltages through the entire front-end circuitry of each channel for greater absolute accuracy. This method uses the module's analog ground as the mid-scale voltage and an external full-scale reference through the *Reference In* front-panel, two-conductor LEMO connector.

The Interrupt and Overwrite Status Registers may be used to avoid rereading "stale" data and to indicate if samples were missed (overwritten before being read). A full complement of clock and trigger inputs and outputs are available to allow synchronous data acquisition over many V216 modules.

The V216 supports both static and dynamic configuration. It may be accessed using A24/A16, D16 data transfers.

Item	Specifications
Number of Inputs	16
Type of input	Differential
Input Impedance	10^{10} Ω ‖ 35 pF
Full-scale Range	±10 V @ unity gain
Conversion Data Rate	10...25...30...50...60...100...1028 Hz; programmable as 19531.25/n where n = {19, 20,...,2000}
Resolution	19 bits minimum (10 Hz data rate, Gain = 1) 18 bits minimum (30 Hz data rate, Gain = 1) 17 bits minimum (60 Hz data rate, Gain = 1)
Missing Codes	None below 60 Hz data rate
Cross-talk	-130 dB (measured at unity gain with full-scale change applied to adjacent channels)
Programmable Gain Pre: Post:	 1 or 100, ±0.025% uncalibrated 1, 2, 4, 8, 16, 32, 64, 128
Pre-gain settling time	140 µsec to 0.01%
Offset Drift Error	± 0.4% + 3/G µV/ºC, typical
50 Hz normal-mode attenuation	-100 dB minimum (@ 50, 25, ..., 50/N data rates)
60 Hz normal-mode attenuation	-100 dB minimum (@ 60, 30, ...,60/N data rates)
Common-mode rejection ratio	-80 dB (DC to 60 Hz at all data rates)
Effective Bandwidth (-3 dB)	0.262 converter data rate (e.g., 2.62 Hz @ 10 Hz rate)
Power Requirements +5 V -5 V +24 V -24 V	 2.9 A 24 mA 110 mA 80 mA
Environmental and Mechanical Temperature range Operational Storage Relative humidity Cooling requirements Dimensions Front-panel potential	 0°C to 50°C -25°C to +75°C 0 to 85%, non-condensing, to 40°C 10 CFM 340 mm x 233.35 mm x 30.48 mm (C-size VXIbus) Chassis ground

Ordering Information

Model V216-ZA11 24-bit, 16-channel Sigma-Delta ADC Module

Related Products

Model 5855-Axyz Cable—36P AMP Rectangular to Unterminated
Model 5855-Bxyz Cable—36P AMP Rectangular to 50S Amphenol Ribbon
Model 5855-Cxyz Cable—36P AMP Rectangular to 36P AMP Rectangular
Model 5857-Axyz Cable—1-contact LEMO to Unterminated
Model 5857-Bxyz Cable—1-contact LEMO to 1-contact LEMO
Model 5857-Cxyz Cable—2-contact LEMO to Unterminated
Model 5857-Dxyz Cable—2-contact LEMO to 2-contact LEMO
Model 5857-Gxyz Cable—2-contact LEMO to BNC shielded
Model 5857-Hxyz Cable—1-contact LEMO to BNC shielded
Model 5910-Z1A Connector—1-contact LEMO
Model 5911-Z1A Connector—2-contact LEMO
Model 5944-Z1A Connector—36P AMP Rectangular
Model V765-ZA11 Rack-mount Termination Panel
Model V792-ZA11 Rack-mount Isothermal Termination Panel