Model V241

24 to 96-channel MUX-bus™
Multiplexer Module

INSTRUCTION MANUAL

April 11, 2002

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*****Special Option*****

Model V241-S001

24 to 96-channel, MUX-bus™
Multiplexer Module

May 15, 1996

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*****Special Option*****

Model V241-S001

The Model V241-S001 is the same as the V241-ZA41 except it has been modified to have conformal coating.

CONTENTS

FIGURES

TABLES

96-channel, High-level, Scanning MUX

Acquire data economically from pre-conditioned channels

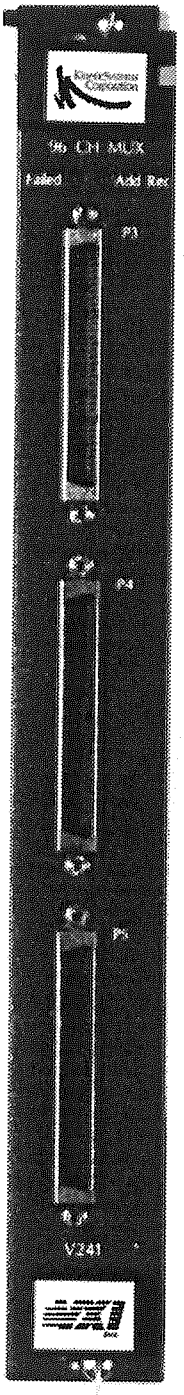
V241

Features

- **Use with V207 or V208 host ADCs**
- **24, 48, and 96-channel input options**
- **Differential inputs on all channels**
- **Interface high level inputs (±10.24 V)**
- **2 programmable calibration channels (an internal precision voltage source as well as the source on the V207 or V208 host ADC)**

Typical Applications

- **Automotive body engineering tests**
- **Automotive powertrain testing**
- **Aircraft engine testing**
- **Rocket engine testing**
- **Wind tunnel data acquisition**
- **Automatic Test Equipment (ATE)**



General Description *(Product specifications and descriptions subject to change without notice.)*

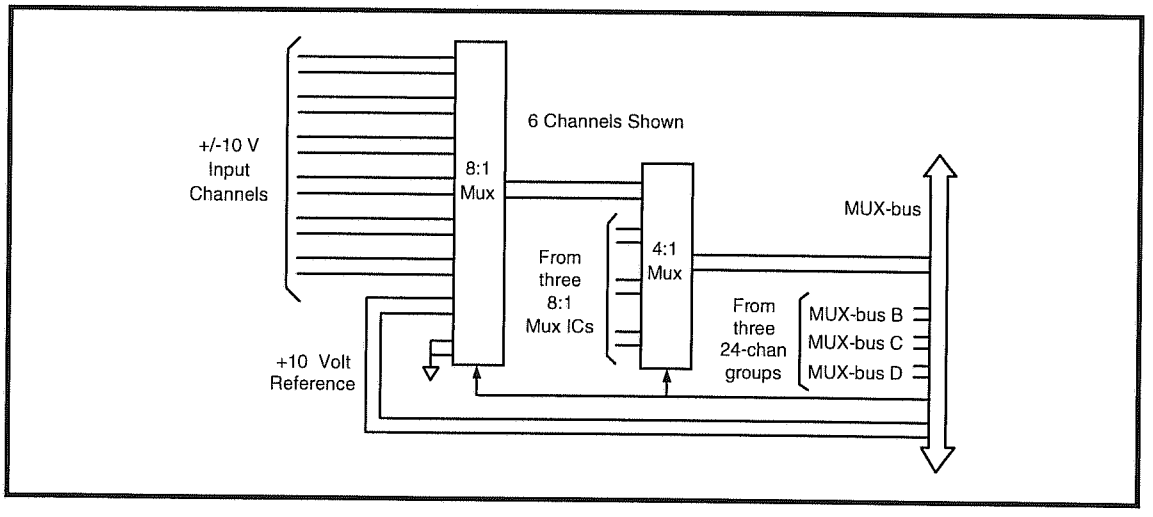
The Model V241 is a single-width, C-size, register-based, VXIbus module that is a front-end multiplexer for the V207 ADC or V208 MUX-bus™ compatible ADC. This multiplexer is intended for medium to high channel count applications with high-level signals (±10.24 V). The V241 provides up to 96 high-level, differentially-received input channels. Up to three V241s can be used with the V207 for a maximum of 256 active channels. The V241 utilizes the KineticSystems MUX-bus concept which allows cableless analog signal transfer by way of the VXI Local Bus. A Scan RAM table on each module in the system provides the necessary multiplexing and synchronization mechanisms to transfer analog signals from MUX-bus source modules (V241, V252, V246, etc.) to MUX-bus sink modules (V207, V208).

On the V241, two calibration channels are provided for each block of 6 input channels on a common multiplexer. One of each pair is internally set to analog ground (0 V differentially) while the other receives the MUX-bus system calibration voltage from the ADC card (+10 V differentially). This method allows end-to-end calibration of the V241 and V207or V208.

Alternatively, if no MUX-bus reference exists, the V241 injects its own reference to these calibration channels. This facilitates a completely independent self-test procedure on board the module which ensures that each multiplexer is responding to a scanning address and its output is switching between its two calibration inputs. In addition, the power-up or software-initiated self-test checks the operational registers of the device and its MUX-bus capabilities.

The V241 utilizes a two-stage multiplexing strategy to maximize channel count and minimize bandwidth limiting capacitance. The front end includes current and voltage protection (to ±35 V) and the intermediate signals are buffered by operational amplifiers for high accuracy and signal integrity.

The V241 supports both static and dynamic configuration. It may be accessed using A24/A16, D16 data transfers.



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Item	Specification
Number of Channels	24, 48 or 96, differential input
Input	
Input range	Differential : ±10.24 V Common mode: ±10.24 V
Maximum input voltage	±35 V continuous
Input impedance	20 MΩ minimum
Linearity Error	±0.002% FSR, Typical
Output	MUX-bus only
Monotonicity	16-bit
Settling Time	6 µs
Input Connector Type	3 - 68P High Density
Power Requirements (typical)	
+5 V	1.9 A
+24 V	150 mA
-24 V	150 mA
Environmental and Mechanical	
Temperature range	
Operational	0ºC to 50ºC
Storage	-25ºC to +75ºC
Relative humidity	0 to 85%, non-condensing, to +40ºC
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V241-ZA11 24-channel, High-level, Scanning MUX
Model V241-ZA21 48-channel, High-level, Scanning MUX
Model V241-ZA41 96-channel, High-level, Scanning MUX

Related Products

Model V207 16-bit, 500,000 Sample/second ADC Subsystem
Model V208 16-bit, 100,000 Sample/second ADC Subsystem
Model 5868-Bxyz Cable—68S High Density to Unterminated
Model 5868-Dxyz Cable—68S High Density to 68P High Density
Model 5868-Exyz Cable—68S High Density to 68S High Density
Model V765-ZA11 Rack-mount Termination Panel

04/11/02

UNPACKING AND INSTALLATION

At KineticSystems, static precautions are observed during all phases of production, test, and packaging of each module. This includes using static proof mats and wrist straps. Please observe these same precautions when unpacking and installing the module whenever possible.

The Model V241 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the logical address switches to the appropriate value.

Configuration

There is one set of user configurable switches on the V241. All eight switches, #1 (msb) to #8 (lsb), are for the logical address. The logical address may be set from 1 to 254 as a statically configured device. If the module is set for logical address 255 (all switches open), then the V241 will be dynamically configured by the resource manager. Logical address 255 is the factory default setting. (See Figure 1, page 4)

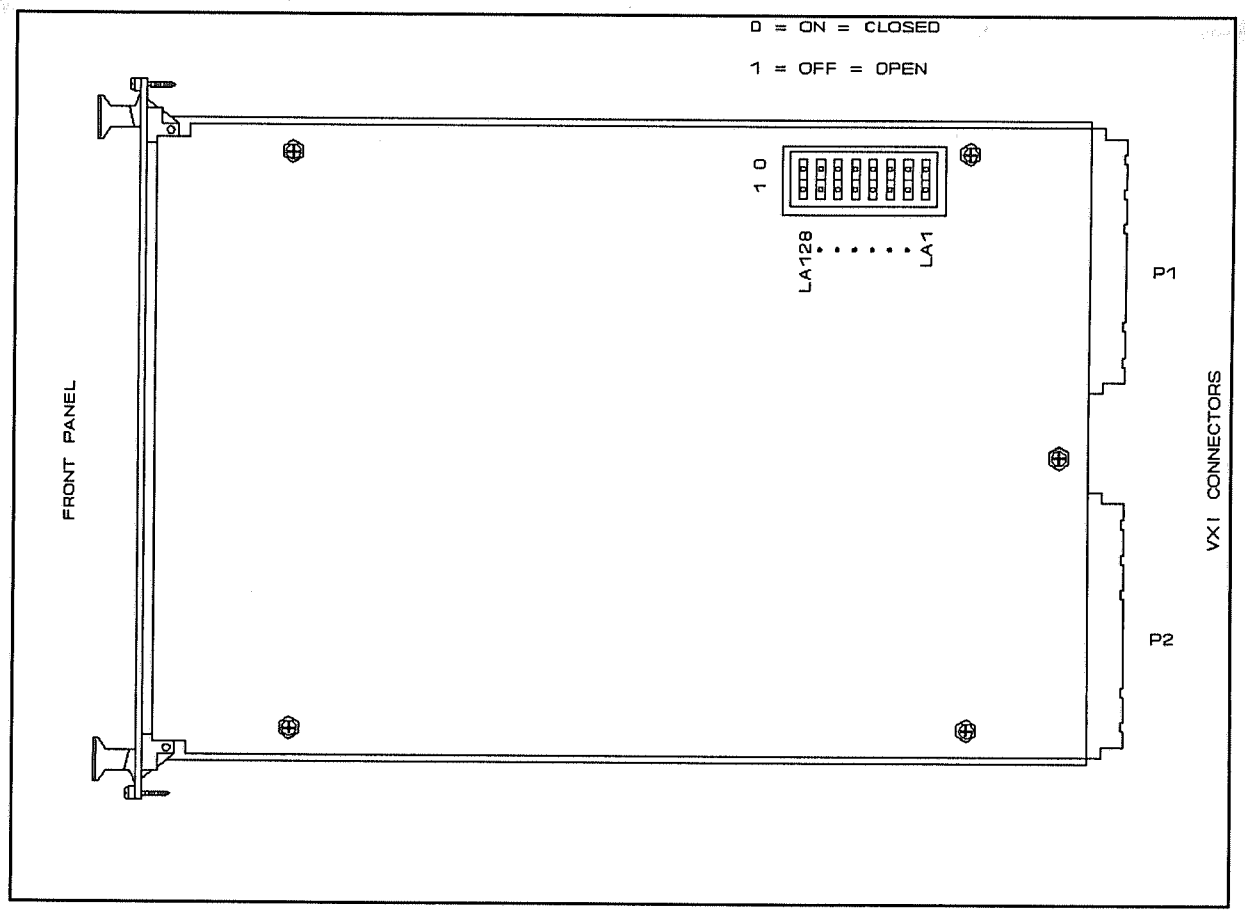


FIGURE 1 - V241 Switch Locations

Module Insertion

The V241 is a C-sized, single width, VXIbus module. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame. Since the V241 is a signal conditioning module that uses MUX-bus, this module must be plugged into the crate only to the right of the V207 (or any other MUX-bus compatible ADC module) in order to use MUX-bus.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

To insure proper interrupt acknowledge cycles from the V241 module, a slot daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in that slot. Conversely, daisy-chain jumpers must be installed in all empty slots between the V241 and the Slot 0 Controller. The preceding jumper instructions may be ignored if using a crate with a "jumperless" backplane like the KSC Model V195 series of crates.

FRONT PANEL DESCRIPTION

LEDs

After power up, the Failed LED will be on for at most five seconds while self tests are being run. If the Failed LED stays on after five seconds, then the self test failed. When the self test is complete, the Add Rec (Address Received) LED will be off. The Add Rec LED lights to indicate that the V241 is being accessed through VXI. The Failed LED will blink to indicate an "overlap detected" condition. This occurs when another module attempted to assert its voltage out on the MUX-bus at the same time that the V241 did.

Connectors

The V241 utilizes both of the standard 96-socket connectors to the VXI backplane. The upper P1 connector serves as the main slot-to-slot computer bus link. The lower P2 connector includes, among other things, the KineticSystems' defined MUX-bus analog link on the daisy-chained local bus. This will be described in detail below.

The V241 has three 68 pin, high density SCSI II type connectors. Beginning at the top of the module, connector P3 receives the differential input pairs for channels 1 through 32, connector P4 receives channels 33 through 64, and connector P5 receives channels 65 through 96. See Figure 3 and Tables 3, 4, and 5 (beginning on page 14) for the precise pinout descriptions.

PROGRAMMING INFO

VXIbus Addressing

The V241 is classified as an extended register device which means it has registers that occupy A16 and A24 space.

The configuration registers are located in A16 space and include the standard registers defined by VXI as well as additional registers to help identify the module. An additional register defined by KineticSystems is the Suffix Register. The Suffix Register includes the model suffix number which indicates the model option. The User Defined Registers at the end of the configuration space can also be used to identify the module (i.e., with an internal identification number). The operational registers are located in A24 space and include the registers specific to V241 modules.

Appendix A includes a C/C++ code example using NI-VXI routines with V241. It includes codes which will use the configuration registers to help identify the specific module and access both configuration and operational registers.

Resetting the V241

The V241 can be put into soft reset by setting the Reset bit of the Status Control Register. Once taken out of soft reset, the module will initiate self test.

Self Tests

On the V241, each group of six front-panel channels share the same multiplexer and buffer chips. Associated with each of these groups (and using the identical devices) are two calibration channels. The first of these two is internally connected as a differential pair to a ground potential. The second of the two connects to an internal 10-volt reference which is superseded automatically by any MUX-bus reference voltage asserted by another module (e.g., the V207). During self test, each calibration pair (a total of 32 calibration channels numbered from 97 through 128–Scan RAM values 96 through 127) is checked to ensure that multiplexer addressing is occurring correctly and that the outputs of each multiplexer swing above and below +5 volts at the appropriate times.

The results of these tests appear in the Self-Test registers 06_{16} through $0E_{16}$ under A24 addressing space. The first of these (06_{16}) contains pass bits for each of the 16 grounded calibration channels. The mapping of these channels and their correlation to external six-channel groups is defined in Table 1. A "0" indicates an error (not below +5V) for the corresponding calibration channel.

Register 08_{16} contains the pass bits for each of the 16 reference voltage (normally +10V) calibration channels. The mapping of these channels and their correlation to external six-channel groups is defined in Table 1. Once again, a "0" indicates an error (not ABOVE +5V) for the corresponding calibration channel.

In addition to these indications, two bits in register $0E_{16}$ provide concise indications for the calibration channel test results. Bit 02 represents a NAND function of the bits in register 06_{16}. Consequently, it will contain a logical "0" only when all the grounded calibration channels have tested correctly. Similarly, bit 03 represents a NAND function of the bits in register 08_{16}. It will thus contain a logical "0" only when all the reference voltage calibration channels have tested correctly.

NOTE:	**DURING SELF TEST, SCAN RAM IS OVERWRITTEN. ALL OTHER REGISTERS WILL REMAIN UNCHANGED EXCEPT THE V241 WILL BE TAKEN OUT OF RUN MODE.**

If the Scan RAM passes the self test, it is automatically configured to enable all of the V241's channels in sequential order as the first scanned channels of the companion ADC module. The Scan RAM element for the last V241 channel will contain the End-Of-List marker as well. In the case where one V241 is used with one MUX-bus ADC module, the RUN bit in the Configuration Register need only be set (put in Run Mode). In any case, the Scan RAM may be read in order to see how it was configured on the V241 to work with the ADC.

The results of the Scan RAM self test appear in two bits of Self Test Register $0E_{16}$ (described in detail on page 30). Bit 00 will contain a logical "0" only when no data errors were detected in the Scan RAM. Bit 01 will contain a logical "0" only when no address errors were detected.

Finally, as an overall indication of self test status, registers $0A_{16}$ and $0C_{16}$ will contain the ASCII encoded equivalent of the letters "P", "a", "s", "s", or "F", "a", "i", "l", if all self tests passed or at least one did not, respectively. The "Pass" entry corresponds to data of 5061_{16} in register $0A_{16}$ and data of 7373_{16} in register $0C_{16}$. The "Fail" entry corresponds to data of 4661_{16} in register $0A_{16}$ and data of $696C_{16}$ in register $0C_{16}$.

MUX-bus

The MUX-bus makes use of the VXI P2 connector lines LBUSC00 - LBUSC11 on this module. Signal conditioning modules supporting the MUX-bus may be plugged into the crate only to the right of the V207 (or any other ADC module using MUX-bus).

The MUX-bus pin definition (P2) is:

LBUSC00 MUX path A signal Hi

LBUSC01 MUX path A signal Lo

LBUSC02 MUX path B signal Hi

LBUSC03 MUX path B signal Lo

LBUSC04 MUX path C signal Hi

LBUSC05 MUX path C signal Lo

LBUSC06 MUX path D signal Hi

LBUSC07 MUX path D signal Lo

LBUSC08 Reference Hi

LBUSC09 Reference Lo

LBUSC10 Overlap Detect

LBUSC11 MUX-bus CLOCK

The MUX-bus clock (usually provided by an ADC module such as the V207) is the control signal that causes the output multiplexers on signal conditioning modules to access the bus at the appropriate time.

Reference Hi and **Reference Lo** (usually asserted by an ADC module such as the V207) provide a +10 volt differential signal to adjacent signal conditioning modules, allowing all channels to be referenced to a common standard. This greatly simplifies system calibration.

Overlap Detect is used by the signal conditioning modules to detect if two or more modules are attempting to output their voltages at the same time. This helps prevent conflicts caused by incompatibly programmed Scan RAM among the MUX-bus modules in a system.

Scan RAM

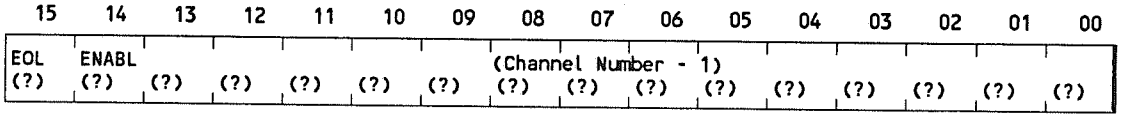
FIGURE 2 (page 9) shows an example of how Scan RAM might be setup in a case using a V241, V252, and a V207. In the example, the first 16 channels of V241 are assigned to the first 16 channels of V207. The V252 (16 channel filter module) is then assigned to the next eight channels on the V207 for a total of 24 channels.

FIGURE 2 - Scan RAM/Scan Table Example

Scan Table Pointer	V241 Scan Table Data	V252 Scan Table Data	V207 Scan Table Data	Channel Enabled
$2E_{16}$	$1000\ 0000\ 0000\ 0111_2$	$1100\ 0000\ 0000\ 0111_2$	$1000\ 0000\ 0000\ 0111_2$	V252 Channel 8
$2C_{16}$	$0000\ 0000\ 0000\ 0110_2$	$0100\ 0000\ 0000\ 0110_2$	$0000\ 0000\ 0000\ 0110_2$	V252 Channel 7
$2A_{16}$	$0000\ 0000\ 0000\ 0101_2$	$0100\ 0000\ 0000\ 0101_2$	$0000\ 0000\ 0000\ 0101_2$	V252 Channel 6
28_{16}	$0000\ 0000\ 0000\ 0100_2$	$0100\ 0000\ 0000\ 0100_2$	$0000\ 0000\ 0000\ 0100_2$	V252 Channel 5
26_{16}	$0000\ 0000\ 0000\ 0011_2$	$0100\ 0000\ 0000\ 0011_2$	$0000\ 0000\ 0000\ 0011_2$	V252 Channel 4
24_{16}	$0000\ 0000\ 0000\ 0010_2$	$0100\ 0000\ 0000\ 0010_2$	$0000\ 0000\ 0000\ 0010_2$	V252 Channel 3
22_{16}	$0000\ 0000\ 0000\ 0001_2$	$0100\ 0000\ 0000\ 0001_2$	$0000\ 0000\ 0000\ 0001_2$	V252 Channel 2
20_{16}	$0000\ 0000\ 0000\ 0000_2$	$0100\ 0000\ 0000\ 0000_2$	$0000\ 0000\ 0000\ 0000_2$	V252 Channel 1
$1E_{16}$	$0100\ 0000\ 0000\ 1111_2$	$0000\ 0000\ 0000\ 1111_2$	$0000\ 0000\ 0000\ 1111_2$	V241 Channel 16
$1C_{16}$	$0100\ 0000\ 0000\ 1110_2$	$0000\ 0000\ 0000\ 1110_2$	$0000\ 0000\ 0000\ 1110_2$	V241 Channel 15
$1A_{16}$	$0100\ 0000\ 0000\ 1101_2$	$0000\ 0000\ 0000\ 1101_2$	$0000\ 0000\ 0000\ 1101_2$	V241 Channel 14
18_{16}	$0100\ 0000\ 0000\ 1100_2$	$0000\ 0000\ 0000\ 1100_2$	$0000\ 0000\ 0000\ 1100_2$	V241 Channel 13
16_{16}	$0100\ 0000\ 0000\ 1011_2$	$0000\ 0000\ 0000\ 1011_2$	$0000\ 0000\ 0000\ 1011_2$	V241 Channel 12
14_{16}	$0100\ 0000\ 0000\ 1010_2$	$0000\ 0000\ 0000\ 1010_2$	$0000\ 0000\ 0000\ 1010_2$	V241 Channel 11
12_{16}	$0100\ 0000\ 0000\ 1001_2$	$0000\ 0000\ 0000\ 1001_2$	$0000\ 0000\ 0000\ 1001_2$	V241 Channel 10
10_{16}	$0100\ 0000\ 0000\ 1000_2$	$0000\ 0000\ 0000\ 1000_2$	$0000\ 0000\ 0000\ 1000_2$	V241 Channel 9
E_{16}	$0100\ 0000\ 0000\ 0111_2$	$0000\ 0000\ 0000\ 0111_2$	$0000\ 0000\ 0000\ 0111_2$	V241 Channel 8
C_{16}	$0100\ 0000\ 0000\ 0110_2$	$0000\ 0000\ 0000\ 0110_2$	$0000\ 0000\ 0000\ 0110_2$	V241 Channel 7
A_{16}	$0100\ 0000\ 0000\ 0101_2$	$000\ 0000\ 0000\ 0101_2$	$0000\ 0000\ 0000\ 0101_2$	V241 Channel 6
8_{16}	$0100\ 0000\ 0000\ 0100_2$	$0000\ 0000\ 0000\ 0100_2$	$0000\ 0000\ 0000\ 0100_2$	V241 Channel 5
6_{16}	$0100\ 0000\ 0000\ 0011_2$	$0000\ 0000\ 0000\ 0011_2$	$0000\ 0000\ 0000\ 0011_2$	V241 Channel 4
4_{16}	$0100\ 0000\ 0000\ 0010_2$	$0000\ 0000\ 0000\ 0010_2$	$0000\ 0000\ 0000\ 0010_2$	V241 Channel 3
2_{16}	$0100\ 0000\ 0000\ 0001_2$	$0000\ 0000\ 0000\ 0001_2$	$0000\ 0000\ 0000\ 0001_2$	V241 Channel 2
0_{16}	$0100\ 0000\ 0000\ 0000_2$	$0000\ 0000\ 0000\ 0000_2$	$0000\ 0000\ 0000\ 0000_2$	V241 Channel 1

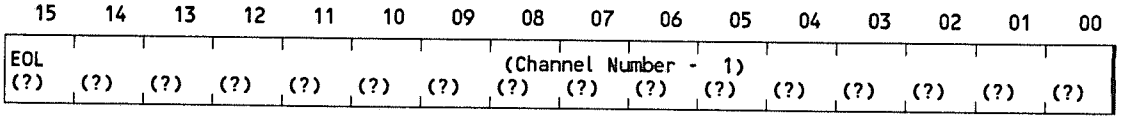
Please Note: The Scan Tables for each MUX-bus module are identical except only one module has the enable bit set at any one time. If this rule is not observed, an overlap condition will occur because two modules will try to output voltages on MUX-bus at the same time.

V241 and V252 Scan RAM (starts at A24 offset 200_{16})



() power up value

V207 Scan RAM (starts at A32 offset 1000_{16})



() power up value

For this example:

MUX-bus on the V207 always scans at 200 Khz (5 uS convert time)

If there are 24 channels in the Scan Table and since the V207 is a scanning ACD, then the scan rate must be less than or equal to 200 kHz / 24 channels = 8333 Hz. The scan rate determines how offen the MUX-bus modules run through the Scan Table.

Let scan rate = 8 kHz, t_{SCAN} = 1 / 8 kHz = 125 µS.

Every 125 µS:

1.) Scan Table Pointer is set to 0_{16}.

V241 reads 4000_{16}. Enable bit is set. Channel 1 is indicated.

V241 outputs its channel 1 voltage.

V252 reads 0000_{16}. Enable bit is not set.

V252 waits.

V207 reads 0000_{16}.

V207 reads its channel 1 voltage.

2.) Scan Table Pointer is set to 2_{16}.

V241 reads 4001_{16}. Enable bit is set. Channel 2 is indicated.

V241 outputs its channel 2 voltage.

V252 reads 0001_{16}. Enable bit is not set.

V252 waits.

V207 reads 0001_{16}.

V207 reads its channel 2 voltage.

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.

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24.) Scan Table Pointer is set to $2E_{16}$.

V241 reads 8007_{16}. End of list bit is set. Enable bit is not set.

V241 waits for next tick of MUX-bus clock to start at beginning of Scan Table

V252 reads $C007_{16}$. End of list bit is set. Enable bit is set. Channel 8 is indicated.

V252 outputs its channel 8 voltage, and waits for next tick of MUX-bus clock to start at beginning of Scan Table.

V207 reads 8007_{16}. End of list bit is set.

V207 reads its channel 24 voltage and waits for next tick of MUX-bus clock to start at beginning of Scan Table.

> NOTE: As a general rule, the V207 or any other receiving MUX module, should be the FIRST to be put in "setup" mode and the LAST to be put in "run" mode.

The Scan RAM contains the Scan Table which must be set up properly on all MUX-bus modules. The Scan RAM is 2048 words long, and the Scan Table is a subset (as determined by the placement of the first End-of-List bit) of the Scan RAM. Each module completes a scan through its Scan Table in each ADC clock period. At any time, the currently addressed data in the table dictates which module and channel is to connect to the MUX-bus.

Before the Scan Table can be written into Scan RAM, the V241 and the V207 must be put in "setup" mode by resetting the Run/Setup bit in the MUX-bus Configuration Register. As a general rule, the V207 (or any other receiving MUX-bus module), should be the first to be put in "setup" mode, and the last to be put in "run" mode. The Scan RAM is organized the same on all modules whether it sources or receives voltages on the MUX-bus. Bit 14 is the enable bit which connects the specified channel to MUX-bus. The enable bit must be set on only one sourcing module for a given element in the Scan Tables (only one voltage source may be enabled on a MUX-bus path at one time). If two or more modules attempt to output voltages on the same MUX-bus path at the same time, an overlap error condition will occur.

The source module channel is specified by the lower 14 bits of each element in the Scan RAM. (An actual Scan RAM value of "0" refers to channel 1, data of "1" to channel 2 and so on). However, not all 96 channels of the V241 are available at any one time. The MUX-bus is comprised of four paths, and the 96 channels of the V241 (128 channels when including calibration) are distributed evenly among them. For instance, channels 1, 5, 9, and 13 of the V241 are accessible only through path A of the MUX-bus. On the V207 ADC module, the MUX-bus paths A through D are scanned repeatedly in order and without variation. Consequently, although source modules like the V241 may have Scan Tables which skip or otherwise address front panel channels out of order, some limitations are imposed by the V207 MUX-bus scanning order. For example, since the first MUX-bus path to be scanned after entering "run" mode must be path A, the first element in a V241 Scan Table must call out a channel from the series "1, 5, 9,...4n+1". Furthermore, since the first hardware channel corresponds to a channel address (Scan Table data) of "0", the actual value to be written to the first element is from the series "0, 4, 8,...4n". The second element corresponds to a V207 read of MUX-bus path B and must contain a V241 channel from the series "2, 6, 10,...4n+2" (Scan Table elements of the series "1, 5, 9,...4n+1). The fifth element of the V241 Scan Table would once again correspond to a read of MUX-bus path A (1-A, 2-B, 3-C, 4-D, 5-A, 6-B, etc.) and, thus, must contain a channel number from the series "1, 5, 9,..." again.

These limitations hold even if the V241 is not the enabled source module at these elements because the order also has effects concerning channel setup time and MUX-bus overlap conditions. Thus, in the example above, the first element in the V246 Scan Table should contain a number from the series "0, 4, 8,...4n" corresponding to a channel number from among the series, "1, 5, 9, 13,..." even though the V241 is the enabled module for the first element. In light of this limitation, it is easiest to copy the channel address portion of the Scan Table identically in all the source modules within a MUX-bus connected system. This works even when specifying channel numbers beyond the range of another source module because unused channel-address bits of a source module are ignored. Only the Enable bit of each element need be modified from one module's Scan Table to another to

guarantee one active source module on MUX-bus at a time. Another method is to fill all the Scan RAMs of the source modules from arrays containing the pattern "0, 1, 2, 3, 0, 1, 2, 3, 0, 1,..." and then overwrite with Enable bits and channel addresses only those elements of each module's Scan RAM which will be used to enable a channel of the resident module to MUX-bus.

Bit 15 is the End-Of-List bit. This bit must be set on the last location of the Scan Table on all MUX-bus modules including the ADC module. Finally, all modules using MUX-bus should be put in "run" mode starting with the sourcing (V241, V246, V252, etc.) modules first.

Overlap Detect

If the "Failed" LED is blinking, an overlap condition involving the V241 has occurred and the V241 will stop exerting voltages out to the MUX-bus. Overlap occurs as a result of one or more of these conditions:

1.) A channel was entered at a Scan Table position which is inconsistent with the MUX-bus path associated with that position. Only certain channels are available for each MUX-bus path. For example, if channel 2 was requested out using a Scan Table element corresponding to MUX-bus path A, C, or D, an overlap would occur.

2.) Two or more modules attempted to output voltages out on MUX-bus at the same time because the Enable bits (bit 14) in equivalent Scan Table locations were set on multiple source modules.

3.) Not all modules had their End-of-List bit (bit 15) set at the same location in their Scan Tables. The Scan Tables must all be the same length.

The overlap condition will be reset by writing a logical "0" to bit 06 of the MUX-bus Configuration Register (Operational Register 00_{16}), asserting SYSRESET*, or entering the module's Soft Reset state by setting bit 00 in the Status/Control Register (Configuration Space Register 04_{16}). Note however that the overlap condition will continue to reoccur until the underlying problem with the Scan Table(s) is corrected.

Calibration

Although some users may opt for complete system calibration where software and external instrumentation interact to multiplex calibration voltages directly into the 96 data inputs of the V241, a "chip level" mode is also available. On each 8-to-1 multiplexer chip used on the V241, two input channels are hard-wired to calibration voltages. The first is connected (both signal and return) to analog ground internally on the module. The other is connected to a +10 volt reference on the module which is automatically superseded by an external MUX-bus differential reference signal (if asserted by a neighboring ADC module). Thus, for every six data channels, there exists a zero and full-scale reference which may be used to calibrate out chip-level errors at the front-end multiplexers and **all** errors in the remaining analog paths to the ADC module with no additional precision source or multiplexing instrumentation. The V241 on-board +10 volt source is not a precision source and is **not** recommended for calibration purposes. It exists primarily to ease module Self-Test as described in that section of this manual.

Model V241-Zxy1

The mapping of each Calibration channel to its six architecturally associated input channels is itemized below in Table 1. For the algorithmically inclined, a closed form follows:

INCHAN = V241 input channel (INCHAN ϵ {1,...,96}) whose associated Calibration channels are to be calculated.

ZCAL = Scan RAM value corresponding to the Zero (mid-scale) Calibration channel associated with the given INCHAN.

FCAL = Scan RAM value corresponding to the full-scale Calibration channel associated with the given INCHAN.

ZCAL = 96 + INT((INCHAN-1)/24) * 8 + (INCHAN-1)modulo 4

FCAL = 100 + INT((INCHAN-1)/24) * 8 + (INCHAN-1)modulo 4

TABLE 1 - Calibration Channel Mapping

Input Channel to Calibrate	Mid-scale Calibration Scan RAM Value	Full-Scale Calibration Scan RAM Value
1, 5, 9, 13, 17, 21	96	100
2, 6, 10, 14, 18, 22	97	101
3, 7, 11, 15, 19, 23	98	102
4, 8, 12, 16, 20, 24	99	103
25, 29, 33, 37, 41, 45	104	108
26, 30, 34, 38, 42, 46	105	109
27, 31, 35, 39, 43, 47	106	110
28, 32, 36, 40, 44, 48	107	111
49, 53, 57, 61, 65, 69	112	116
50, 54, 58, 62, 66, 70	113	117
51, 55, 59, 63, 67, 71	114	118
52, 56, 60, 64, 68, 72	115	119
73, 77, 81, 85, 89, 93	120	124
74, 78, 82, 86, 90, 94	121	125
75, 79, 83, 87, 91, 95	122	126
76, 80, 84, 88, 92, 96	123	127

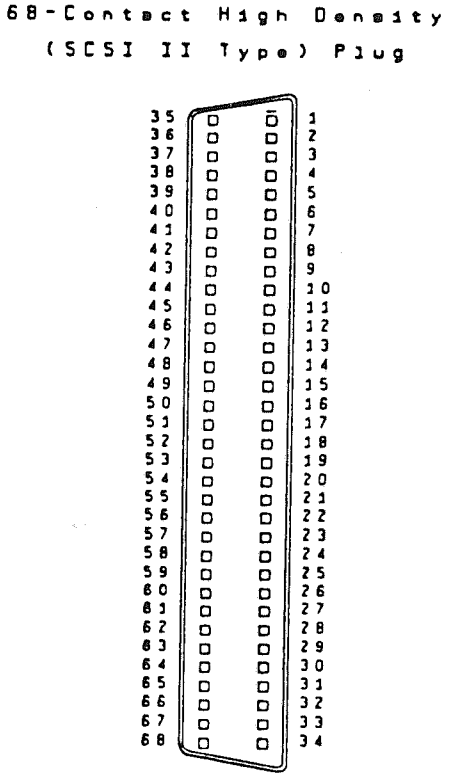


Figure 3 - 68 Socket SCSI II Mating Connector

TABLE 2 - P3 68-Pin SCSI II Connector Pinout (Front View)

Pin #	Description	Pin #	Description
35	Channel 1 In -	1	Channel 1 In +
36	Channel 2 In -	2	Channel 2 In +
37	Channel 3 In -	3	Channel 3 In +
38	Channel 4 In -	4	Channel 4 In +
39	Channel 5 In -	5	Channel 5 In +
40	Channel 6 In -	6	Channel 6 In +
41	Channel 7 In -	7	Channel 7 In +
42	Channel 8 In -	8	Channel 8 In +
43	Channel 9 In -	9	Channel 9 In +
44	Channel 10 In -	10	Channel 10 In +
45	Channel 11 In -	11	Channel 11 In +
46	Channel 12 In -	12	Channel 12 In +
47	Channel 13 In -	13	Channel 13 In +
48	Channel 14 In -	14	Channel 14 In +
49	Channel 15 In -	15	Channel 15 In +
50	Channel 16 In -	16	Channel 16 In +
51	Channel 17 In -	17	Channel 17 In +
52	Channel 18 In -	18	Channel 18 In +
53	Channel 19 In -	19	Channel 19 In +
54	Channel 20 In -	20	Channel 20 In +
55	Channel 21 In -	21	Channel 21 In +
56	Channel 22 In -	22	Channel 22 In +
57	Channel 23 In -	23	Channel 23 In +
58	Channel 24 In -	24	Channel 24 In +
59	Channel 25 In -	25	Channel 25 In +
60	Channel 26 In -	26	Channel 26 In +
61	Channel 27 In -	27	Channel 27 In +
62	Channel 28 In -	28	Channel 28 In +
63	Channel 29 In -	29	Channel 29 In +
64	Channel 30 In -	30	Channel 30 In +
65	Channel 31 In -	31	Channel 31 In +
66	Channel 32 In -	32	Channel 32 In +
67	Digital Ground	33	Digital Ground
68	Reserved	34	Reserved

TABLE 3 - P4 68-Pin SCSI II Connector Pinout (Front View)

Pin #	Description	Pin #	Description
35	Channel 33 In -	1	Channel 33 In +
36	Channel 34 In -	2	Channel 34 In +
37	Channel 35 In -	3	Channel 35 In +
38	Channel 36 In -	4	Channel 36 In +
39	Channel 37 In -	5	Channel 37 In +
40	Channel 38 In -	6	Channel 38 In +
41	Channel 39 In -	7	Channel 39 In +
42	Channel 40 In -	8	Channel 40 In +
43	Channel 41 In -	9	Channel 41 In +
44	Channel 42 In -	10	Channel 42 In +
45	Channel 43 In -	11	Channel 43 In +
46	Channel 44 In -	12	Channel 44 In +
47	Channel 45 In -	13	Channel 45 In +
48	Channel 46 In -	14	Channel 46 In +
49	Channel 47 In -	15	Channel 47 In +
50	Channel 48 In -	16	Channel 48 In +
51	Channel 49 In -	17	Channel 49 In +
52	Channel 50 In -	18	Channel 50 In +
53	Channel 51 In -	19	Channel 51 In +
54	Channel 52 In -	20	Channel 52 In +
55	Channel 53 In -	21	Channel 53 In +
56	Channel 54 In -	22	Channel 54 In +
57	Channel 55 In -	23	Channel 55 In +
58	Channel 56 In -	24	Channel 56 In +
59	Channel 57 In -	25	Channel 57 In +
60	Channel 58 In -	26	Channel 58 In +
61	Channel 59 In -	27	Channel 59 In +
62	Channel 60 In -	28	Channel 60 In +
63	Channel 61 In -	29	Channel 61 In +
64	Channel 62 In -	30	Channel 62 In +
65	Channel 63 In -	31	Channel 63 In +
66	Channel 64 In -	32	Channel 64 In +
67	Digital Ground	33	Digital Ground
68	Reserved	34	Reserved

TABLE 4 - P5 68-Pin SCSI II Connector Pinout (Front View)

Pin #	Description	Pin #	Description
35	Channel 65 In -	1	Channel 65 In +
36	Channel 66 In -	2	Channel 66 In +
37	Channel 67 In -	3	Channel 67 In +
38	Channel 68 In -	4	Channel 68 In +
39	Channel 69 In -	5	Channel 69 In +
40	Channel 70 In -	6	Channel 70 In +
41	Channel 71 In -	7	Channel 71 In +
42	Channel 72 In -	8	Channel 72 In +
43	Channel 73 In -	9	Channel 73 In +
44	Channel 74 In -	10	Channel 74 In +
45	Channel 75 In -	11	Channel 75 In +
46	Channel 76 In -	12	Channel 76 In +
47	Channel 77 In -	13	Channel 77 In +
48	Channel 78 In -	14	Channel 78 In +
49	Channel 79 In -	15	Channel 79 In +
50	Channel 80 In -	16	Channel 80 In +
51	Channel 81 In -	17	Channel 81 In +
52	Channel 82 In -	18	Channel 82 In +
53	Channel 83 In -	19	Channel 83 In +
54	Channel 84 In -	20	Channel 84 In +
55	Channel 85 In -	21	Channel 85 In +
56	Channel 86 In -	22	Channel 86 In +
57	Channel 87 In -	23	Channel 87 In +
58	Channel 88 In -	24	Channel 88 In +
59	Channel 89 In -	25	Channel 89 In +
60	Channel 90 In -	26	Channel 90 In +
61	Channel 91 In -	27	Channel 91 In +
62	Channel 92 In -	28	Channel 92 In +
63	Channel 93 In -	29	Channel 93 In +
64	Channel 94 In -	30	Channel 94 In +
65	Channel 95 In -	31	Channel 95 In +
66	Channel 96 In -	32	Channel 96 In +
67	Digital Ground	33	Digital Ground
68	Reserved	34	Reserved

V241 Configuration Registers, A16 Space

V241 Configuration Registers, A16 Space

(R)	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	00_{16}
(W)	Don't Care								LA 128	LA 64	LA 32	LA 16	LA 08	LA 04	LA 02	LA 01	
(R)	1	0	1	0	0	0	1	0	0	1	0	0	0	0	0	1	02_{16}
(R)	A24 ENA	MODID *	1	1	1	1	1	1	1	1	1	1	Ready	Pass	Sys. Inb.	Soft Reset	04_{16}
(W)	A24 ENA	Not Used													Sys. Inb.	Soft Reset	
(W/R)	OF 15	OF 14	OF 13	OF 12	OF 11	OF 10	OF 09	OF 08	OF 07	OF 06	OF 05	OF 04	Not Used				06_{16}
(R)	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	08_{16}
(R)	Serial Number High																$0A_{16}$
(R)	Serial Number Low																$0C_{16}$
(R)	Firmware Version #				Firmware Revision #				Hardware Version #				Hardware Revision #				$0E_{16}$

Offsets 10_{16} - 18_{16} Reserved

(R)	1	1	1	1	1	1	1	Over Lap	Logical Address								$1A_{16}$
(R)	Write Data							INT MASK	IREN *	1	IRL2 *	IRL1 *	IRL0 *	1	1	1	$1C_{16}$
(W)	Unused Mask Bits							INT MASK	IREN *	Not Used	IRL2 *	IRL1 *	IRL0 *	Not Used			
(R)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	$1E_{16}$
(R)	Suffix High Register																20_{16}
(R)	Suffix Low Register																22_{16}

User Defined Registers 24_{16} - $3E_{16}$

V241 Operational Registers, A24 Space

Muxbus Configuration Register

0000_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	1	1	1	1	1	1	1	1	1	Over Lap	Run/ Setup	1	*Ena Trig	TTL2	TTL1	TTL0
(W)	Not Used									Over Lap	Run/ Setup	Not Used	*Ena Trig	TTL2	TTL1	TTL0

Self Test Status Zero Volts Calibration Channels

0006_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	CH 124	CH 123	CH 122	CH 121	CH 116	CH 115	CH 114	CH 113	CH 108	CH 107	CH 106	CH 105	CH 100	CH 99	CH 98	CH 97

Self Test Status +10 Volts Calibration Channels

0008_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	CH 128	CH 127	CH 126	CH 125	CH 120	CH 119	CH 118	CH 117	CH 112	CH 111	CH 110	CH 109	CH 104	CH 103	CH 102	CH 101

Results Register High

$000A_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Self Test - 'P'-'a'-ss (5061 Hex) or 'F'-'a'-il (4661 Hex)															

Results Register Low

$000C_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Self Test - Pa-'s'-'s' (7373 Hex) or Fa-'i'-'l' (696C Hex)															

Failure Summary Register

$000E_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	0	0	0	0	0	0	0	0	0	0	0	0	+10V Error	0V Error	Add. Error	Data Error

Scan RAM

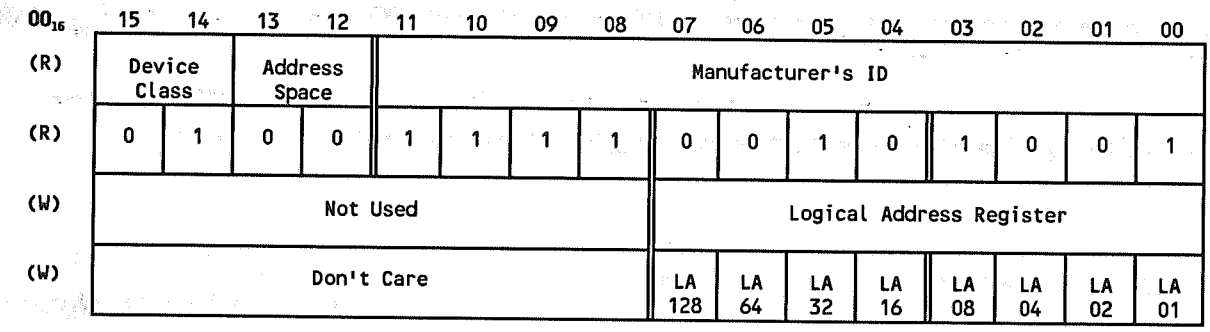
0200_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Scan RAM															

.
.
.

$11FE_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Scan RAM															

V241 Configuration Registers, A16 Space

ID/Logical Address Register

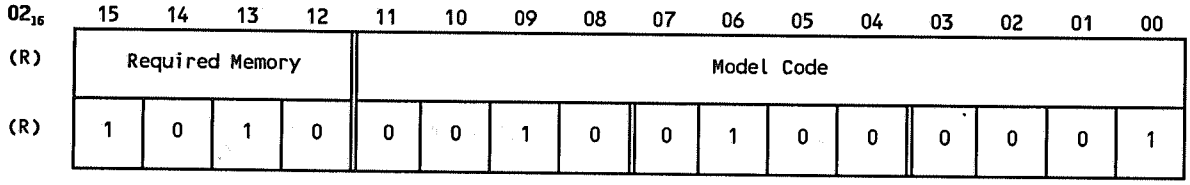


On READ transactions the V241 returns $4F29_{16}$.

Bit(s)	Mnemonic	Meaning
15,14	Device Class	This is an Extended Register-Based Device.
13,12	Address Space	This module requires the use of A16/A24 address space.
11-00	Manufacture's ID	3881 ($F29_{16}$) for KineticSytems.

For WRITE transactions, bits fifteen through eight are not used. These bits may be written with any data pattern. In Dynamically Configured systems (and the Logical Address switches were set to a value of 255), bits seven through zero are written with the Logical Address value.

Device Type Register



This READ ONLY register returns $A241_{16}$.

Bit(s)	Mnemonic	Meaning
15-12	Required Memory	The V241 requires 8192 bytes of additional memory space.
11-00	Model Code	Identifies this device as a V241 (241_{16}).

Status/Control Register

04_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	A24 ENA	MODID *	1	1	1	1	1	1	1	1	1	1	Ready	Pass	Sys. Inb.	Soft Reset
(W)	A24 ENA	Not Used													Sys. Inb.	Soft Reset

The bit assignments for the Status/Control register are defined as follows:

Bit(s)	Mnemonic	Meaning
15	A24 ENA	This bit is written with a "1" to enable A24 addressing and reset to "0" to disable these registers. **This bit must be set to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" by the assertion of SYSRESET*.
14	MODID*	This read only bit is set to a "1" if the module is <u>not</u> selected with the MODID line on P2. A "0" in this bit location indicates the device is selected via a high state on its P2 MODID line.
13-04	Not Used	These bits are not used and are read as "1s".
03	Ready	A "1" in this bit indicates the successful completion of register initialization.
02	Pass	A "0" indicates the V241 has failed or is currently executing its self test. A "1" in this bit indicates the module's self test has passed. Refer to the self test registers in the Operational Registers for further explanation.
01	Sys. Inb.	(Sysfail Inhibit)Writing a "1" to this bit disables the V241 from driving the SYSFAIL* line. Reads of this bit indicate its current state.
00	Soft Reset	Writing a "1" to this bit forces the device into the Soft Reset State. While in this state, the module will only allow access to its Configuration Registers. Writing a "0" to this bit will the signal the V241 to begin executing its self test. **This bit must be cleared along with the Pass and Ready bits set before any access to the Operational Registers is allowed.**

Offset Register

06_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(W/R)	OF 15	OF 14	OF 13	OF 12	OF 11	OF 10	OF 09	OF 08	OF 07	OF 06	OF 05	OF 04	Not Used			
Address Mapping	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	Not Used			

After SYSRESET* and prior to self test all bits are reset to "0". Otherwise, a read or write defines the base address of the module's A24 registers. Bits 03-00 of this register are not used and should always be written with zeros. As shown above bits 15-04 map directly onto VME address lines A23-A12. For example, if bits OF15-0F04 contain 243_{16} the base address for the module's Operational Registers becomes 243000_{16}.

Attribute Register

08_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	Reserved													IR*	IH*	IC*
(R)	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0

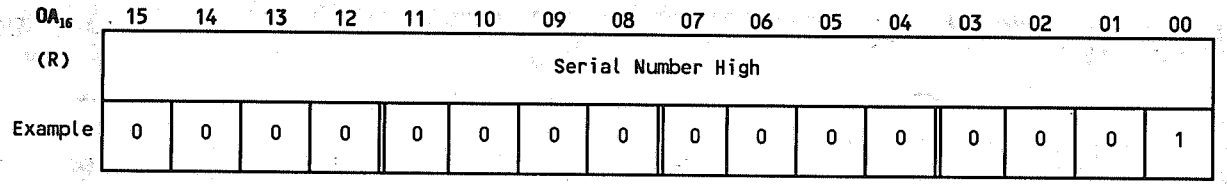
This read only register returns $FFFA_{16}$ on READ transactions. Write transactions to this register have no effect and its usage is reserved for future definition.

Bit(s)	Mnemonic	Meaning
15-03	Reserved	These bits are read as "1s" and reserved for future definition.
02	IR*	This bit is read as a "0" to signify that the V241 is capable of generating interrupts.
01	IH*	This bit is read as a "1" and indicates the V241 is not capable of Interrupt Handler Control.
00	IS*	This bit is set to "0" to indicate the V241 has Interrupt Status Reporting capability.

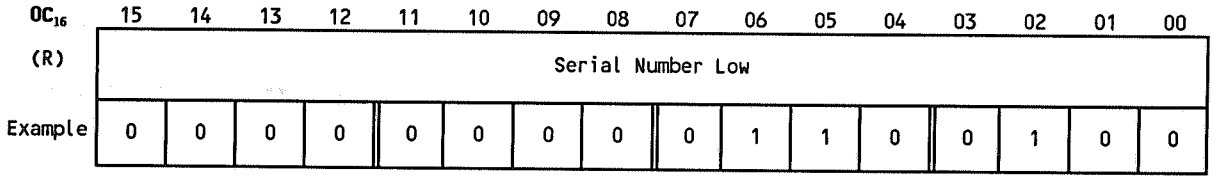
The following two READ ONLY registers indicate the serial number of the module. Each module is given a unique serial number. The serial number is represented by a 32-bit unsigned integer. The least significant bits (LSBs) reside in the Serial Number Low register while the most significant bits (MSBs) are in the Serial Number High register. Writing to these registers will have no effect and its use is reserved. For example, assume the module's serial number is 10064_{16} (65636). A read of the Serial Number High register returns 0001_{16} (1 => 1 * 65536); and the Serial Number Low register returns 0064_{16} (100). This example is illustrated below.

Model V241-Zxy1

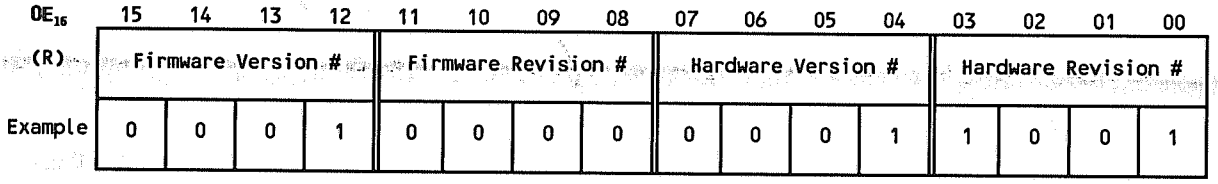
Serial Number High



Serial Number Low



Version Number Register



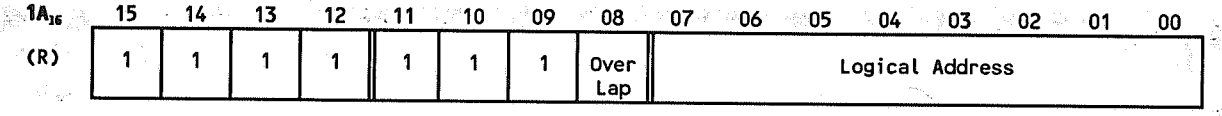
This READ ONLY register indicates the hardware and firmware revision number of the module. A write to this register has no effect on its contents. The fields of this register are explained as follows:

Bits	Mnemonic	Meaning
15-12	Firmware Version #	Firmware Version Number
11-08	Firmware Revision #	Firmware Revision Number
07-04	Hardware Version #	Hardware Version Number
03-00	Hardware Revision #	Hardware Revision Number

The combination of Firmware Version Number and Firmware Revision Number indicate the module's firmware version level. These two fields contain two four bit integers and are joined to form the level. An example of data returned for a firmware version number of 1.0 is shown above.

The combination of Hardware Version Number and Hardware Revision Number indicate the module's hardware version level. These two fields contain two four bit integers and are joined to form the level. An example of data returned for a hardware version number of 1.9 is shown above.

Interrupt Status Register



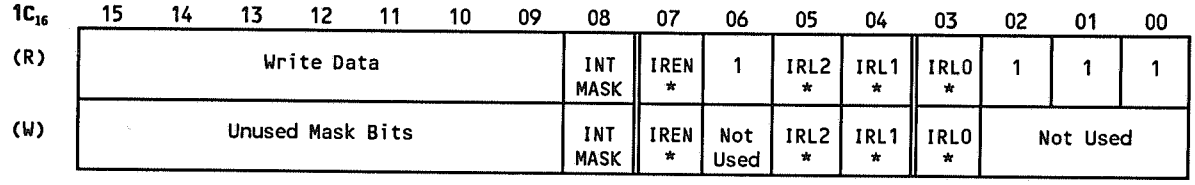
This READ ONLY register is defined as follows:

Bit(s)	Mnemonic	Meaning
15-09	Not Used	These bits are not used and read as "1s".
08	Over Lap	Overlap - This bit is set to a "1" if the V241 detects an overlap condition. This bit is cleared by asserting SYSRESET*, putting the V241 in Soft Reset, or by writing a "0" to the Over Lap bit in the Muxbus Configuration Register.
07-00	Logical Address	These bits contain the Logical Address of the V241.

During an interrupt acknowledge cycle the V241 enables this register onto the D15-D00 data lines. As shown above, the data returned will indicate the current status of overlap as well as the V241's current logical address.

This register may also be polled for its current status while interrupt generation is disabled. Enabling interrupts, disabling the Interrupt Mask, and selecting an Interrupt Request Line is controlled by the Interrupt Control Register.

Interrupt Control Register



Interrupts are used by the V241 to indicate an overlap condition. While the Interrupt Status may simply be polled for the current status, utilizing interrupts can eliminate unnecessary reads, increasing the controller's efficiency. Using this register to control interrupts is defined as follows:

Bits(s)	Mnemonic	Meaning
15-09	Not Used	These bits are reserved for use as interrupt mask bits. Although their function is currently unimplemented, they should be written with "1s" to prevent incompatibility with future enhancements.
08	INT MASK	A "1" in this bit masks (prevents) the V241's overlap detection circuitry from generating an interrupt request. This bit must be written with a "0" to allow overlap detect to generate an interrupt.

07 IREN* A one in this bit is used to disable interrupt generation. If the V241 had more than one interrupt source, this bit would prevent any source from generating an interrupt. A zero in this field enables interrupt generation (currently caused only by overlap detection).

06 Not Used This bit is reserved for use during interrupt handling. Since the V241 is not capable of interrupt handling, this bit should always be written with a "1".

05-03 IRL2*-IRL0* This 3-bit field selects the VXIbus interrupt line associated with the interrupt according to the following table:

Bit			Interrupt Request Line
IRL2* (D05)	IRL1* (D04)	IRL0* (D03)	
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

02-00 Not Used These bits are reserved for selecting an interrupt handler line. Since the V241 does not have interrupt handler capabilities, these bits should always be written with "1s".

All bits in this register are set to "1" on the assertion of SYSRESET* or if the SOFT RESET bit in the Status/Control register is written with a "1". If an overlap condition is to generate an interrupt, the INT MASK and IREN* bits must be cleared and IRL2*-IRL0* must be a value other than 111_2. The mask bits and interrupt enable bits do not effect the current Cause/Status. For example, if an overlap has occurred, changing the interrupt mask bit from a one to a zero will cause the pending interrupt to generate a VXI interrupt. Similarly, if an interrupt request is pending and the interrupt enable bit is changed from a zero to a one, the interrupt request will not be cleared. An interrupt request pending on any particular line is cleared by the assertion of SYSRESET*, putting the module into Soft Reset, changing IRL2*-IRL0*, or if the interrupt is properly acknowledged.

Subclass Register

$1E_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	VXI E.D.	Extended Register Based Device														
(R)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Reads of this register return $FFFE_{16}$. Writes to this register have no effect.
The read contents are defined as follows:

Bit(s)	Meaning
15	VXI E.D. = 1 indicates that the V241 is a VXIbus defined Extended Device.
14-00	Extended Register Based Device = $7FFE_{16}$ indicate that this is an Extended Register Based Device.

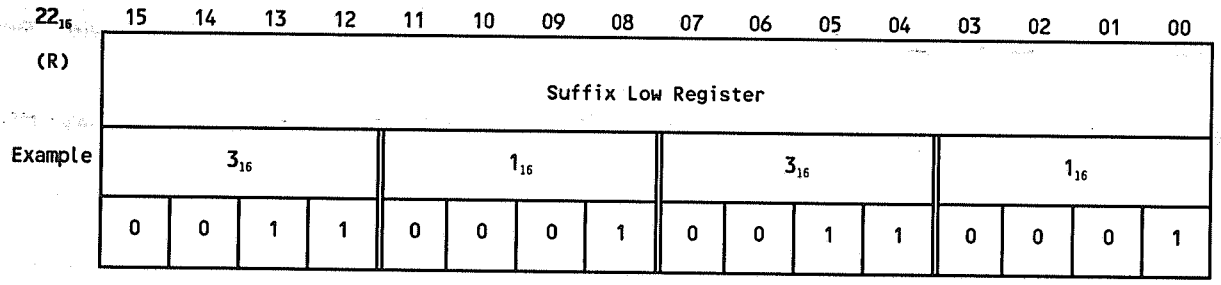
The following two registers are KineticSystems defined and hold the module's suffix. The suffix determines the particular option of the module. This information can be used remotely establish available channel count, filtering options, etc. of the module. For further information on each option, refer to the Ordering Information section of this manual.

The module's suffix is always composed of four ASCII characters. The Suffix High register contains the first two characters; while, the last two characters are in the Suffix Low register. For instance, assume the module is a model V241-ZA11. The module's suffix is "ZA11". Converting this to ASCII yields $5A413131_{16}$. This value is divided among the upper and lower registers as shown below.

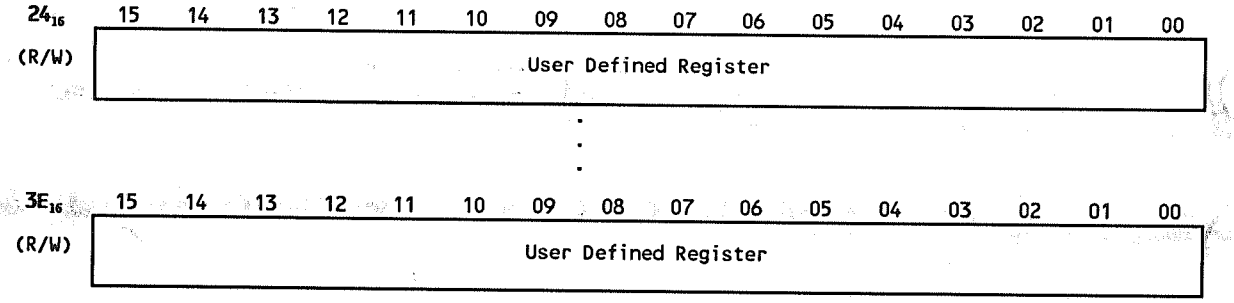
Suffix High Register

20_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	Suffix High Register															
Example	5_{16}				A_{16}				4_{16}				1_{16}			
	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	1

Suffix Low Register



Offsets 24_{16} through $3E_{16}$ are READ/WRITE registers and may be used to store user defined data. These registers are contained in non-volatile EEPROM. A typical use for these registers would be to hold calibration information such as date, time, etc.



V241 Operational Registers, A24 Space

Muxbus Configuration Register

0000_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R)	1	1	1	1	1	1	1	1	1	Over Lap	Run/ Setup	1	*Ena Trig	TTL2	TTL1	TTL0
(W)	Not Used									Over Lap	Run/ Setup	Not Used	*Ena Trig	TTL2	TTL1	TTL0

The Muxbus Configuration register is used to monitor and control the V241's Muxbus activities. This register and the Scan RAM are used to control the multiplexing of the analog inputs over Muxbus and to an ADC such as the Model V207. The bits are defined as follows:

Bit(s)	Mnemonic	Meaning
15-07	Not Used	These bits are not used and are read as 00_{16}. Writes to these bits will have no effect on the V241.
06	Over Lap	Overlap - Reading this bit location as a "1" indicates the V241 has detected an overlap condition. This bit is cleared by writing it with a zero, the assertion of SYSRESET*, or putting the module into the Soft Reset state.
05	Run/Setup	A "1" (Run Mode) in this bit enables the Muxbus circuitry. This state allows the V241 to direct analog signals (as defined by the contents of Scan RAM) to Muxbus at the appropriate time. Writing a "0" (Setup Mode) to this bit disables the Muxbus circuitry. This prevents the V241 from placing analog signals onto the Muxbus, regardless of the current activity of other modules. This bit must be zero to access Scan RAM locations. The assertion of SYSRESET*, or putting the module into Soft Reset will clear this bit. Reads will indicate the current state.
04	Not Used	This bit is not used and read as "1".
03	*ENA TRIG	*Enable TTL Trigger Lines to Sample/Hold - A "1" in this bit disables all trigger lines from affecting the Sample/Hold circuitry. A "0" allows the selected trigger line (specified by bits TTL2-TTL0), when asserted, to direct the V241 to sample the inputs. Reads indicate the current state of this bit. It is cleared by the assertion of SYSRESET*, or placing the module into Soft Reset.

02-00 TTL2-TTL0

Reads of this field indicate its current state. All bits are cleared by the assertion of SYSRESET*, or during the Soft Reset state. The TTL Trigger Line * to be used for Sample/Hold purposes is defined as follows:

TTL2	TTL1	TTL0	TTL TRIGGER LINE *
0	0	0	TTLTRG0*
0	0	1	TTLTRG1*
0	1	0	TTLTRG2*
0	1	1	TTLTRG3*
1	0	0	TTLTRG4*
1	0	1	TTLTRG5*
1	1	0	TTLTRG6*
1	1	1	TTLTRG7*

The following five registers contain the module's self test results. They are useful in verifying the successful completion of a self test as well as helpful in diagnosing problems. In the event of a self test failure, these registers may become inaccessible. If this occurs, consult the factory for assistance regarding the use of these registers.

Self Test Status Zero Volts Calibration Channels

0006_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	CH 124	CH 123	CH 122	CH 121	CH 116	CH 115	CH 114	CH 113	CH 108	CH 107	CH 106	CH 105	CH 100	CH 99	CH 98	CH 97

A "1" indicates that this calibration channel (zero volts) has passed its test, confirming the analog path to Muxbus. Some calibration channels are not used on certain options. For instance, channel 124 (CH 124) is not physically present on a 48 channel option. These channels will not be tested and their status will default to a passed state.

Self Test Status +10 Volts Calibration Channels

0008_{16}	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	CH 128	CH 127	CH 126	CH 125	CH 120	CH 119	CH 118	CH 117	CH 112	CH 111	CH 110	CH 109	CH 104	CH 103	CH 102	CH 101

This register is similar in operation to the above register, except this register contains the results for +10 volt calibration channels. Again, the same rules apply for unused channels and their status will default to a passed (1) state.

The Results Registers (High and Low) demonstrate the V241's ability to execute a self test. As shown below, the combination of these two registers should always yield the ASCII equivalent of 'Pass' or 'Fail'. By defining this 32 bit value as only valid with two of a possible 2^{32} combinations, the odds of false status indications are greatly reduced.

Results Register High

$000A_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Self Test - 'P'-'a'-ss (5061 Hex) or 'F'-'a'-il (4661 Hex)															

Results Register Low

$000C_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	Self Test - Pa-'s'-'s' (7373 Hex) or Fa-'i'-'l' (696C Hex)															

Failure Summary Register

$000E_{16}$	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(R/W)	0	0	0	0	0	0	0	0	0	0	0	0	+10V Error	0V Error	Add. Error	Data Error

Upon successful completion of a self test this register should contain 0000_{16}. The bit locations are defined as follows:

Bit(s) Meaning

15-04 These bits are not used and should be read as 000_{16}.

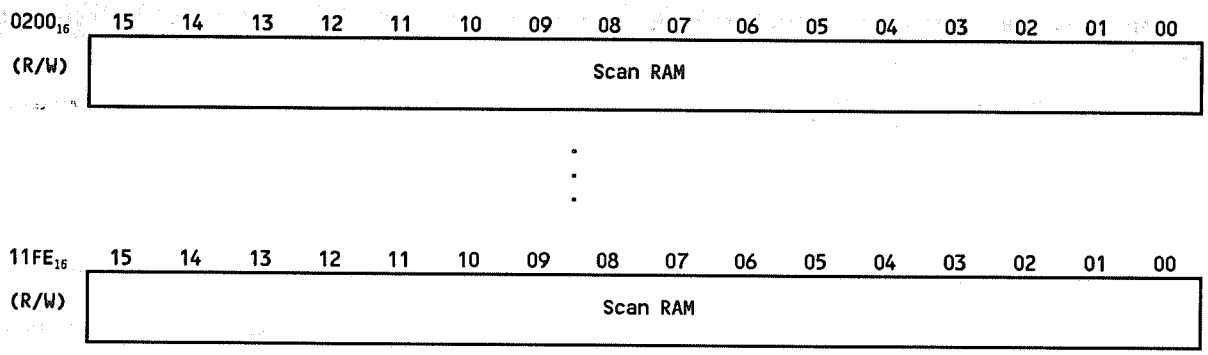
03 +10 Volt Error - This bit is the logical NAND of the +10 volts calibration channels' status. If any channel fails, this bit will be set to a "1".

02 0 Volt Error - This bit is the logical NAND of the 0 volts calibration channels' status.

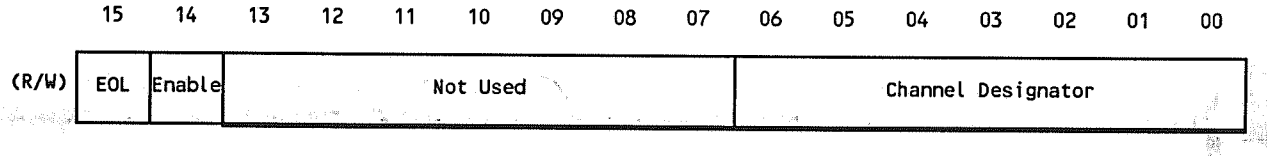
01 Add. Error - A "1" in this bit indicates the V241 failed its internal register addressing test.

00 Data Error - A "1" in this bit indicates the V241 failed its internal register data tests.

Scan RAM



The format and bit assignments for Scan RAM locations are defined as follows:



Bit(s)	Mnemonic	Meaning
15	EOL	End of List - Set to a "1" to indicate the last channel to be scanned. The first Scan RAM location having this bit set signifies the end of the scan list and all subsequent Scan RAM locations become unused.
14	Enable	A "1" enables the V241 to enable the given channel (as specified in the Channel Designator field) onto the Muxbus at the appropriate time.
13-07	Not Used	These bits are not used and should be written with "0s". Reads will return their current state.
06-00	Channel Designator	This field is used to specify the channel. Channel 1 is represented by 00_{16}, Channel 2 by 01_{16}, while, Channel 128 is designated by placing $7F_{16}$ in this field.

APPENDIX A

```
#include <stdio.h>

typedef unsigned short uint16;
typedef unsigned long uint32;
typedef short int16;

uint16 const A24SuperData = 0x6;
uint16 const A32SuperData = 0x7;
uint32 const V241_serial = 1234;
uint32 const V207_serial = 3456;
uint16 const V241_suf_high = 'ZD11';
uint16 const V241_suf_low = '11';
uint16 const V207_suf_high = 'ZB';
uint16 const V207_suf_low = '11';

void reportError() {
   printf("Error: closing VXIlibrary\n");
   CloseVXIlibrary();
   exit(1);
   }

uint16 find_la (
uint16 model,
uint32 serial_numb,
uint16 suf_high_numb,
uint16 suf_low_numb
) {
   int16  i,error;
   uint16 data,id,dev_type,la;
   uint16 serial,suf_high,suf_low;

   la = 0xFF;
   for (i=0; i<0xFF; i++) {
        error = VXIinReg(i,0x0,&id);
        id &= 0xFFF;

        if (error ==0) {
           /* get device type value */
           error = VXIinReg(i,0x2,&dev_type);
           dev_type &= 0xFFF;
           if (error != 0)
                reportError();

           /* get serial number */
           error = VXIinReg(i,0xA,&(uint16)serial);
           if (error != 0)
                reportError();
           error = VXIinReg(i,0xC,&data);
```

```
            if (error != 0)
                reportError();
            serial = (serial << 16) + (uint32)data;


            /* get suffix number */
            error = VXIinReg(i,0x20,&suf_high);
            if (error != 0)
                reportError();
            error = VXIinReg(i,0x22,&suf_low);
            if (error != 0)
                reportError();

            if (id==0xF29 && dev_type==model && serial==serial_numb
            && suf_high==suf_high_numb && suf_low==suf_low_numb) {
                la = i;
                printf("V%x found at logical address 0x%x\n",model,la);
                }
            }
        }
    if (la == 0xFF) {
        printf("V%x not found, search parameters incorrect\n",model);

        reportError();
        }

    return la;
    }

/*      The main program will assign all 16 channels of the V241 to    */
/* the first 16 channels of V207.  MUX-bus will be enabled after both  */
/* Scan Tables has been written                                        */
main () {
  uint16 V241,V207,data;
  uint32 address;

  error = InitVXIlibrary();
  if (error != 0) {
    printf("Error: opening InitVXIlibrary()\n");
    exit(1);
    }

  V241 = find_la ( 0x252, V241_serial, V241_suf_high, V241_suf_low);
  error = GetDevInfo(V241,12,&A24_V241);
  if (error != 0)
    reportError();

  V207 = find_la ( 0x207, V207_serial, V207_suf_high, V207_suf_low);
  error = GetDevInfo(V241,12,&A32_V207);
  if (error != 0)
```

```
   reportError();

 address =  A32_V207 + 0x6;          /* V207 in setup mode          /*
 data = 0;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
  reportError();

 address =  A24_V241;          /* V241 in setup mode          /*
 data = 0;
 error = VXIout(A24SuperData,address,2,data);
 if (error != 0)
  reportError();

 address = A32_V207 + 0x200;          /* set V207 for 16 channels   /*
 for (i=0; i<15; i++) {
  data =  i;
  error = VXIout(A32SuperData,address,2,data);
  if (error != 0)
   reportError();
  address += 2;
  }
 data = 0x800F;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
  reportError();

 address = A24_V241 + 0x200;          /* set V241 for 16 channels   /*
 for (i=0; i<15; i++) {
  data = 0x4000 | i;
  error = VXIout(A24SuperData,address,2,data);
  if (error != 0)
   reportError();
  address += 2;
  }
 data = 0xC00F;
 error = VXIout(A24SuperData,address,2,data);
 if (error != 0)
  reportError();

 address =  A24_V207;          /* V241 in run mode  /*
 data = 0x20;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
  reportError();
```

Model V241-Zxy1

```
address =  A32_V207 + 0x6;          /* V207 in run mode  /*
data = 0x20;
error = VXIout(A32SuperData,address,2,data);
if (error != 0)
  reportError();

CloseVXIlibrary();
}
```

APPENDIX B

V241 Quick Reference Guide

Function Categories

Category	Name	Function
Initialize	Initialize	ksv241_init
Configuration	Set Sample/Hold Trigger Line	ksv241_setSmplHldTrgLn
Action/Status	Initialize Scan RAM	ksv241_initScnRAM
	Load Scan RAM	ksv241_loadScnRAM
	Enable Run Mode	ksv241_enableRnMd
	Set Up Channel Internal Cal	ksv241_setupChnlCal
	Calculate Calibration Factors	ksv241_calculateCalFctrs
Utilities	Get Device List	ksv241_getDeviceList
	Get Module Attribute	ksv241_getMdlAttrb
	Get Module Suffix	ksv241_getMdlSfx
	Get Channel Attribute	ksv241_getChnlAttrb
	Error Message	ksv241_error_message
	Query Error	ksv241_error_query
	Query Over Lap	ksv241_queryOverlap
	Query Revision	ksv241_revision_query
	Reset	ksv241_reset
	Self Test	ksv241_self_test
Close	Close	ksv241_close

V241 Quick Reference Guide

Function Descriptions

Function	Description
ksv241_calculateCalFctrs	Calculates internal gain (M2), gain correction coefficient (N2), internal offset (B2), and offset correction coefficient (F2) for a channel.
ksv241_close	Closes communications with the module
ksv241_enableRnMd	Places the module into run (or setup) mode.
ksv241_error_message	Translates the status codes returned by the driver functions into diagnostic messages.
ksv241_error_query	Queries the instrument and returns instrument-specific error information (not supported).
ksv241_getChnlAttrb	Returns a module input attribute
ksv241_getDeviceList	Finds the number of available V241 modules, their slot numbers, and their logical addresses
ksv241_getMdlAttrb	Returns a module attribute
ksv241_getMdlSfx	Returns module code suffix and data decoded from the suffix
ksv241_init	Establishes communications and initializes module. Resets hardware if specified, and loads default values into internal memory.
ksv241_initScnRAM	Clears module scan ram and configures it for a specified number of channels. Initially, all channels are disabled. The scan list will be loaded into this module scan ram.
ksv241_loadScnRAM	Loads scan list channel into the module scan ram.
ksv241_queryOverlap	Queries the module for an overlap condition
ksv241_reset	Resets module hardware registers to a predefined state.
ksv241_revision_query	Queries the module and returns the versions of the module hardware and instrument driver software

V241 Quick Reference Guide

Function	Description
ksv241_self_test	Performs a module self-test
ksv241_setSmplHldTrgLn	Enables module sample and hold trigger and sets sample/hold trigger line
ksv241_setupChnlCal	Sets up the calibration for a channel. Since this module has separate module input channels for zero and full scale calibration, the source for each channel is always set to Line regardless of the channel source selection.

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2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com