Model V246

8-Channel Bridge Signal Conditioner

User's Manual

February 9, 2004

This manual describes operation of current versions of the V246:

- **V246-BAA2 –** V246 with 6-pole Bessel filter, tri-filar transformer, no bridge completion resistors, no simultaneous sampling, version 2
- **V246-BAB2 –** V246 with 6-pole Bessel filter, tri-filar transformer, no bridge completion resistors, simultaneous sampling, version 2
- **V246-BBA2 –** V246 with 6-pole Bessel filter, tri-filar transformer, 100-ohm bridge completion resistors, no simultaneous sampling, version 2
- **V246-BBB2 –** V246 with 6-pole Bessel filter, tri-filar transformer, 100-ohm bridge completion resistors, simultaneous sampling, version 2
- **V246-BCA2 –** V246 with 6-pole Bessel filter, tri-filar transformer, 350-ohm bridge completion resistors, no simultaneous sampling, version 2
- **V246-BCB2 –** V246 with 6-pole Bessel filter, tri-filar transformer, 350-ohm bridge completion resistors, simultaneous sampling, version 2
- **V246-BCB3 –** V246 with 6-pole Bessel filter, tri-filar transformer, 350-ohm bridge completion resistors, simultaneous sampling, version 3

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Organization

Chapter 1*,* ***Introduction***, gives you a brief overview of the Model V246, lists items you need to get started, and explains how to safely unpack your module.

Chapter 2*,* ***Installation and Configuration***, explains how to configure the V246 and correctly insert it into a C-size VXIbus mainframe.

Chapter 3*,* ***Understanding the V207/V208 Family***, provides information about the V207/V208 family, about the V246 as used with the V207/V208, about associated signal-conditioning modules (such as the V241, V243, V252 and V253), and about interconnection methods.

Chapter 4, ***Understanding the V246***, describes the operation and performance of the V246.

Chapter 5, ***Configuration and Operational Registers****,* shows how to access and control the V246 from software.

The ***Appendices*** provide additional information that may be helpful in the use of the Model V246, in learning more about KineticSystems and its products, and in quickly reaching us.

Glossary

Following is a glossary of some of the terms and conventions used throughout this manual:

*****	An indicator that a register bit contains low-true data. For example, writing a **"0"** to a bit labeled Enable* would cause a function to be enabled.
A16 Space	The first 64 Kbytes of address space, accessible with 16-bit addressing. The configuration registers of VXI devices occupy 64-byte blocks of this address space. The Logical Address of a device determines which 64-block block is associated with that device.
A24 Space	The 16 Mbyte address space accessible with 24-bit addressing. A module can request a block of this address space via information contained in its *Configuration* registers. *Operational* registers, if present, reside in this space.
A32 Space	The 4 Gbyte address space accessible with 32-bit addressing. A module can request a block of this address space via information contained in its *Configuration* registers. *Operational* registers, if present, reside in this space.
ADC Clock	The rate at which data is presented to the ADC for digitization. The ADC clock rate is also equal to the maximum rate of aggregate data throughput for all digitized channels.
Configuration Registers	Setup registers located in **A16** space. Some are mandatory; some are optional.

D16	A single 16-bit data transfer.
D16 BLK	A block transfer of 16-bit words.
D32	A single 32-bit data transfer. Not all Slot-0 controllers support **D32**.
D32 BLK	A block transfer of 32-bit words. Not all Slot-0 controllers support **D32** BLK.
Device	One of 255 devices that a VXIbus system can support. The term is often used interchangeably with "module." The distinction is that a VXIbus module can consist of more than one device.
Digi-bus™	A high-speed digital bus protocol developed by KineticSystems and implemented on the VXI Local Bus. The **Digi-bus** protocol allows an ADC to transmit digital data to DSP and memory devices at high speeds without external wiring.
DSP	Digital Signal Processor. Usually refers to VXIbus devices that perform autonomous digital signal processing of digital data.
Dynamic Addressing	The VXIbus addressing mode in which the address of a device is stored in a write-able register. See also Static Addressing.
hexadecimal	A base-16 number. The suffix, "h," indicates that a number is hexadecimal. For example, 1Ah = 26_{10}; FFh = 255_{10}; 1000h = 4096_{10} .
Local Bus	A user-definable 12-line bus implemented on the P2 connectors of the VXIbus.
Logical Address	A VXIbus module's unique address. A VXIbus system has 254 logical addresses that are available. **"0"** is the address of the Slot-0 controller. **"255"** specifies that dynamic addressing be used to address that module.
MUX-bus™	A four-channel analog bus protocol developed by Kinetic Systems and implemented on the VXI Local Bus. The **MUX-bus** protocol allows signal-conditioning modules to transmit analog data to an ADC module at high speeds with high accuracy without external wiring.
Operational Registers	Setup and data-transfer registers that are located in **A24** or **A32** address space.
RAM	Random Access Memory. RAM refers to a memory block that has direct addressable access, as opposed to sequential access.
Resource Manager	Software that sets logical addresses and optimally configures Operational register addresses and memory-block addresses in a system. The manufacturer of the Slot-0 controller provides this software, often referred to as "RESMAN."
Sample Clock or Scan Clock	The rate at which each channel is digitized. Each tick of the sample clock initiates digitization of the channels in the order defined in Scan RAM. Digitization occurs at the rate of the ADC clock. Note that, in this context, "sample" and "scan" are interchangeable, as in "sample clock" and "scan clock" or as in "sample rate" and "scan rate."

Static Addressing The VXIbus addressing mode in which the address of a device is stored in a switch register. See also Dynamic Addressing.

Chapter 1: Introduction

About the V246

The V246 is a single-width, C-size, register-based VXIbus module that provides eight channels of bridge signal conditioning. It accommodates transducers that are one, two, or four active arms of a bridge circuit. An option is available for 3- or 4-wire RTD's.

This module is designed for use as a front-end signal conditioner for the KineticSystems V207 and V208 ADC modules. This combination permits the digitization of properly conditioned inputs from high-frequency strain gages, RTDs and other bridge-type sensors. No inter-module wiring is necessary since this module is fully compatible with the KineticSystems-specified **MUX-bus**. The V246 can provide front-end bridge signal conditioning for VXIbus-based ADCs other than the V207/8 as well.

The V246 Signal Conditioner provides bridge completion, excitation, anti-aliasing filtering and amplification for bridge-type inputs. It contains provisions for 2-point shunt calibration, automatic voltage and excitation calibration, as well as excitation alarms. Bridge offsets of up to 70 mvolts may be nulled with a per-channel 12-bit DAC current source. Each channel may be programmed independently. Cables and termination panels are available for convenient wiring of sensor leads.

The V246 supports both static and dynamic configuration. Access to digitized data and to operational registers is via **A24** memory space. All data transfers use **D16** protocol.

The V246 is available with several signal conditioning and sampling options. The part number is V246-*wxyz*, where:

w specifies the filter type:

"B" indicates that the filters are 6-pole Bessel.

"K" indicates that the filters are 6-pole Chebyshev.

x selects the front-end option:

	Trifilar transformers	Bridge completion
A	yes	no
B	yes	120 Ω
C	yes	350 Ω
D	no	no
E	no	120 Ω
F	no	350 Ω

y specifies the simultaneous sampling options:

"A" indicates no simultaneous sampling.

"B" indicates simultaneous sampling capability.

z specifies the revision level:

The number, **"1," "2" or "3,"** etc., gives the revision level.

Getting Started

To set up and use your V246 VXIbus module, you will need most or all of the following:

- The V246, configured with any appropriate options, and its User Manual
- One or more of the following **MUX-bus**-compatible data acquisition and signal-conditioning modules and their User Manuals:
  - V207
  - V208
  - V241 - 96-channel, high-level, scanning MUX
  - V243 - 96-channel, low-level signal conditioner
  - V252 - 8 or 16-channel, 8-pole analog filter
  - V253 - 16-channel, programmable gain / analog filter
- One or more of the following software packages:
  - DAQ Director
  - VXI*plug&play* instrument driver(s)
  - VISA software associated with a computer interface or Slot-0 controller that supports the VXI *plug&play* standards.
  - LabVIEW for Windows
  - LabWindows/CVI
  - MS Visual Basic
- "VXI Data Acquisition Handbook" by Dr. J. W. Tippie
- Your VXIbus system with its Resource Manager and high-level test and/or application software (such as DAQ Director)

Unpacking the V246

The V246 comes in an anti-static bag to avoid electrostatic damage. Electrostatic discharge (ESD) to the module can damage components on it. Please take the following precautions when unpacking the module:

- Ground yourself with a grounding strap or by touching a grounded object.
- Touch the anti-static package to a metal part of your VXIbus chassis before removing the module from the package.
- Remove the module from the package and inspect the module for damage.
- Do not install the module into the VXIbus chassis until you are satisfied that the module exhibits no obvious mechanical damage and is configured to conform to the desiring operating environment. The next chapter describes installation and configuration.

Chapter 2: Installation and Configuration

Setting the Logical Address Switches

A VXI system can have as many as 255 devices, with each having a unique number in the range from zero to 254. Eight bits represent the number, which is the Logical Address of the device. VXIbus defines two concepts of addressing: "static" and "dynamic." All VXIbus devices *must* allow static addressing, in which the address is determined by the setting of a switch register. VXIbus devices may, but are not required to, support dynamic addressing. In dynamic addressing, the Logical Address is stored in a software-addressable register. For reasons discussed in Chapter 5, all KineticSystems VXIbus devices support dynamic as well as static addressing.

Before installing the V246 in the VXIbus chassis, you must set the switch register to an appropriate value. If you wish to employ static addressing you must make sure you set the switch register to a unique value other than 0 or 255. It is a good idea to note module addresses in an accessible log, because if you replace a module, it is very important that the new module have the same address as the replaced one.

If your system employs dynamic addressing, which delegates the task of assigning device addresses to the Resource Manager software, then make sure the address switch is set to 255 (all **"1"**s).

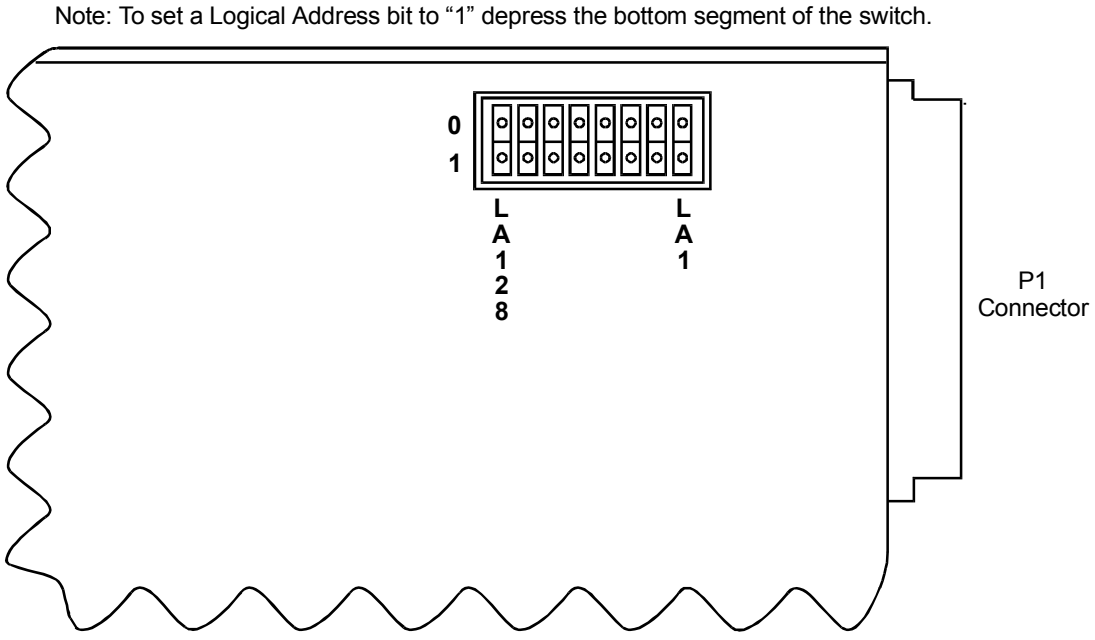


Figure 2-1. V246 Switch Locations

Module Insertion

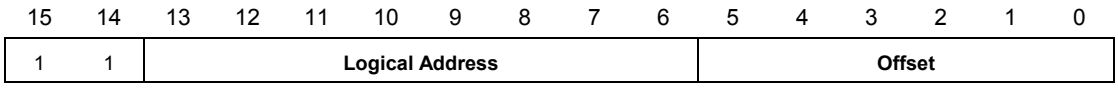
Before inserting your VXIbus module into the chassis, make sure that the chassis is plugged into electrical power but *not turned on*. The power cord provides a ground connection for the mainframe and protects the equipment and you from electrical harm.

In a VXI system, the Bus Grant and IACK signals are received and transmitted by each of the modules.

These signals must be jumpered around any vacant slots in the mainframe. Most current mainframes, including our V194 and V195, contain jumperless backplanes, where the Bus Grant and IACK signals are automatically jumpered when a slot is empty.
If your mainframe does not contain a jumperless backplane, you must position certain jumpers correctly on the chassis backplane to assure that the V246 acknowledges interrupts properly. Remove the Interrupt Acknowledge (IACK) jumper from the slot selected for the V246 and install daisy-chain jumpers in any empty slots between the V246 and the Slot 0 Controller.
You can now insert the V246 into the chassis. Slowly push it in until its plug connectors are resting against the backplane connectors. Then, using evenly distributed pressure, press the module straight in until it seats in the slot and the module front panel is even with the chassis front panel. Tighten the top and bottom screws.
You may now safely apply power to the V246.

Module Configuration

You, or your software, must perform two types of module configuration. The first has to do with VXIbus-related items and involves communication with V246 "configuration" registers. The second deals with setting parameters related to data acquisition and involves communication with V246 "operational" registers.
VXIbus-related configuration includes setting the logical address, specifying the amount of memory space required, specifying where in memory the V246 registers and memory blocks are located, and setting interrupt levels.
When you configure the V246 for data-acquisition, you must also load the scan list information in Scan RAM.
VXIbus devices occupy system memory space. The configuration registers for each VXIbus device have 64 bytes of memory space in the upper 16 kbytes of the 64-kbyte **A16** memory space. Whether you set the 8-bit Logical Address statically in the switch register or dynamically in the Logical Address register, those eight bits determines the base address of the 64-byte block of memory as follows:



Each 64-byte block contains several registers that supply information about the module, such as the manufacturer, the module identifier (i.e., "246h"), its class (register-based or message-based), serial number, and the amount of memory space it requires.
In addition to **A16** addressing, a VXIbus device can also support **A24** or **A32** addressing. If a Multi-buffer option is chosen in a data acquisition device, that device usually requires either 16 or 32 Mbytes of memory space. The V246 requires no more than 64 kbytes of memory space. Therefore, **A24** addressing is sufficient for the V246 since the maximum size of **A24** memory is 16 Mbytes.
The operational registers are all in **A24** space in the V246. To access them, one must first write a proper offset value to the Offset register in **A16** space. Refer to Chapter 5 for details relating to the *configuration* and *operational* registers.

Chapter 3: Understanding the V207/V208 Family

Overview

The V246 is a member of a versatile family of analog-to-digital converter (ADC) modules and signal conditioning modules. You can use from one to eleven signal-conditioning modules in a VXIbus mainframe with a single V207 or V208 scanning ADC module. The signal-conditioning modules transmit their analog data to the V207 or V208 over the VXI Local Bus using **MUX-bus** protocol.

A V207 or V208 ADC module transmits its digitized data to a slot-0 controller via the VXIbus backplane *or* to one or more companion modules via the Local Bus using **Digi-bus** protocol. The flow of data is from right to left. Signal conditioning modules using **MUX-bus** protocol, such as the V246, are positioned to the right of the ADC. Slot-0 controllers and modules receiving digitized data using **Digi-bus** protocol are positioned to the left of the ADC.

The V207 provides aggregate sampling rates to 500 ksamples/s. It supports up to 256 **MUX-bus** analog input channels. The V208 provides sampling rates to 100 or 200 ksamples/s. It supports up to 2048 **MUX-bus** channels.

The **MUX-bus** family of analog front-end modules includes:

- **V241** **96-channel multiplexer** for high-level signals that do not require conditioning;
- **V243** **96-channel signal conditioner** with programmable gain, programmable 2-pole active filters and precision calibration reference (for use with the V208 only);
- **V246** **8-channel, bridge-input, signal conditioner** with programmable gain, programmable 6-pole filters, per-channel excitation source and optional simultaneous sampling;
- **V252** **16-channel signal conditioner** with factory-installed 8-pole filters, optional programmable gain and optional simultaneous sampling; and
- **V253** **16-channel signal conditioner** with programmable gain, optional 6-pole filters and optional simultaneous sampling.

You can "mix and match" these front-end modules with a single V207 or V208. Note that the V243 is for use with the V208 only.

The **Digi-bus** family of modules includes:

- **V110** **RAM memory module** with capacity to 128 Mbytes, on-board DSP for data manipulation, and programmable pre-trigger and post-trigger sample sizes for transient recorder applications;
- **V165** **TI 'C30-based DSP** with 40 MFLOP processing power;
- **V168** **SHARC-based DSP** with up to 1.44 GFLOP processing power;
- **V285** **16-channel waveform generator** with programmable clock rates and programmable Bessel filters on each channel;
- **V387** **128-channel digital input/output module**.

Data streams from the ADC to **Digi-bus** family modules over the VXI Local Bus using **Digi-bus** protocol and extends as far as adjacent modules in the VXIbus backplane propagate the bus. Following are brief descriptions of the **MUX-bus**, the signal conditioning modules that use the **MUX-bus**, and the **Digi-bus.**

The MUX-bus

The **MUX-bus** is a four-channel, differential, analog bus implemented on the 12-line VXI Local Bus. Under control of the V207, signal-conditioning modules multiplex up to 256 analog signals onto the **MUX-bus**. The V207 controls the multiplexing process and provides the necessary synchronizing and address signals to the signal conditioning modules. The V208 does likewise but supports up to 2048 analog channels.

The **MUX-bus** operates as a four-phase bus to provide ample settling time before digitizing occurs. The four analog buses are referred to as A, B, C and D. Figure 3-1 below illustrates the **MUX-bus** cycle for an 8-channel system.

Each module that is a member of the **MUX-bus** family contains a scan table called "Scan RAM." Each table is 16 bits by 2048 words (256 words in the V207). These tables provide the means for specifying the channel scanning order and for assuring that only one channel presents its signal to a **MUX-bus** channel at a time.

On the signal-conditioning modules, channels 1, 5, 9, 13, etc., are associated with **MUX-bus** channel A. Channels 2, 6, 10, 14, etc., are associated with channel B, and so forth. The order of the channels in the scan list must be such that analog signals are presented to the **MUX-bus** channels in the order A, B, C, D, A, B, C, D, etc. In other words, the two least significant bits must follow the sequence 00, 01, 10, 11, 00, 01, 10, 11, etc. Other than this restriction, you can select any order of channel scanning that you wish within a group of signal conditioning modules on a common **MUX-bus**. An example of proper Scan RAM setup is given in the next chapter.

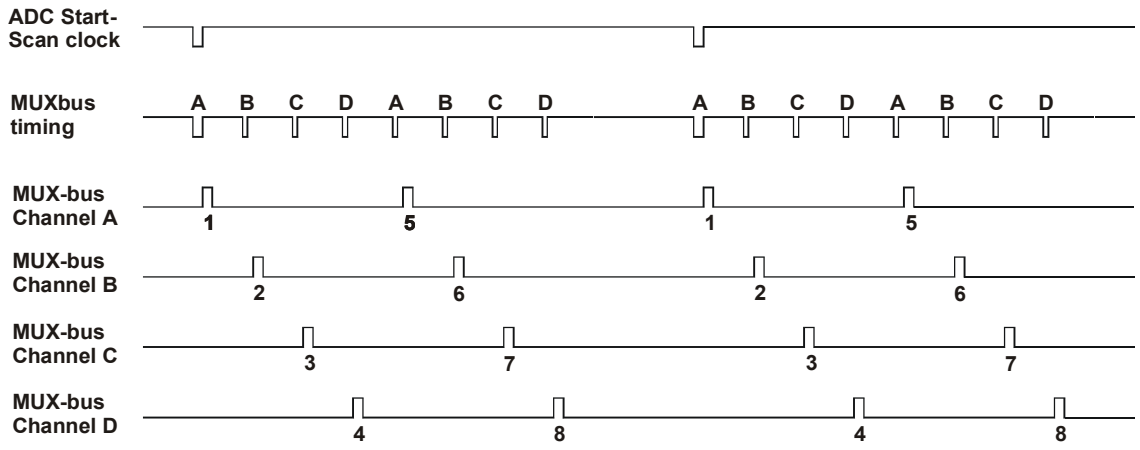


Figure 3-1. MUX-bus timing

The V207/V208 Family of Signal Conditioning and Multiplexing Modules

A number of multiplexing and signal-conditioning modules use the **MUX-bus** protocol to connect to a V207 or V208 ADC. The family consists of the V241 high-level scanning multiplexer, the V246 bridge signal conditioner, and the V252 and V253 gain and filter modules. All are single-width, C-size, register-based VXIbus modules that support both static and dynamic addressing. The V243 low-level, low-noise module is intended for use only with the V208.

V241

The V241 acquires data economically from pre-conditioned channels. It is intended for medium to high channel count applications with high-level signals (± 10.24 V full scale). The V241 provides up to 96 high-level, differential input channels.

Two calibration channels are provided for each block of six input channels on a common multiplexer. One of each pair is internally set to analog ground (0 V differentially) while the other receives the **MUX-bus** system calibration voltage from the ADC card (+ 10 V differentially). This method allows end-to-end calibration of the V241 and V207.

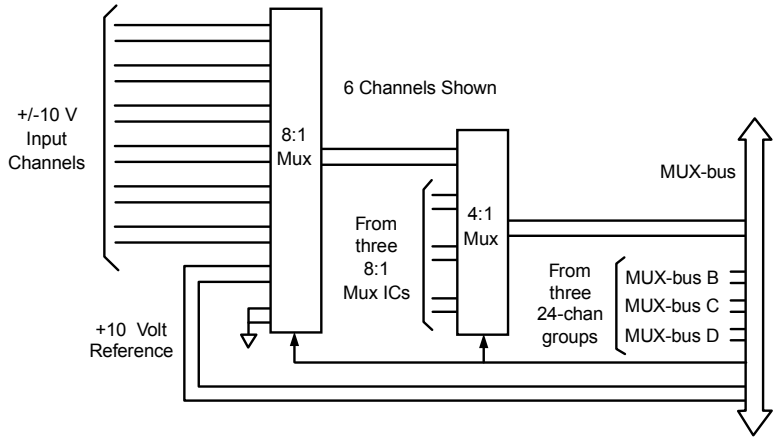


Figure 3-2. V241 Block Diagram

V243

The V243 acquires data from thermocouples and other low-bandwidth, low-level sensors. It provides up to 96 differential-input channels with programmable gain per channel and 2-pole, active, low-pass Butterworth filters on each channel. Filter cutoff frequencies of 10, 50, and 500 Hz (plus bypass) are software-selectable. Each channel has software-selectable pre-filter gains of 1, 10, and 100. Filter cutoff frequency and pre-filter gains are programmable in groups of eight channels. You can select a common, multiplexed, post-filter gain of 1, 2, 5, 10, or 20 per **MUX-bus** channel. Programmable gain per channel therefore ranges from 1 to 2000.

You can place as many as eleven V243s in neighboring slots to the right of the V208. This provides a maximum of 1056 channels.

V243s combined with the V208 provide a low-noise analog subsystem with built-in, per-channel calibration that is traceable to NIST standards. The V208 includes a factory-calibrated, precision reference source, and each V243 includes a precision calibrator. Each input channel connects to the calibrator output, ground, or the analog input under software control. For maximum accuracy, you can store in EEPROM memory a small gain-correction factor for each calibrator

output and a small offset correction for different grounding paths. You can apply these correction factors during the calibration process to obtain maximum accuracy.

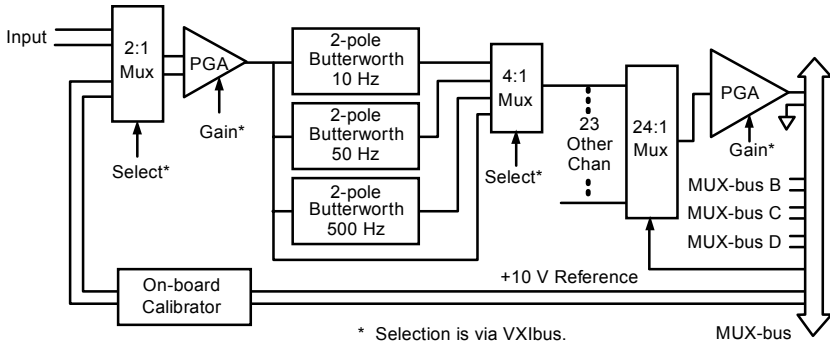


Figure 3-3. V243 Block Diagram

V246

The V246 provides eight channels of bridge signal conditioning. It accommodates transducers that represent one, two, or four active arms of a bridge circuit and permits the digitization of properly conditioned inputs from high-frequency strain gages, RTDs and other bridge-type sensors.

The V246 provides bridge completion, excitation, anti-aliasing filtering, and amplification for bridge-type inputs. It contains provisions for 2-point shunt calibration, automatic voltage and excitation calibration, as well as excitation alarms. The V765 termination panel is available for convenient connection of sensor wiring.

Optional trifilar transformers are available for applications where high frequency electro-magnetic interference is a concern. Simultaneous sampling is also an option.

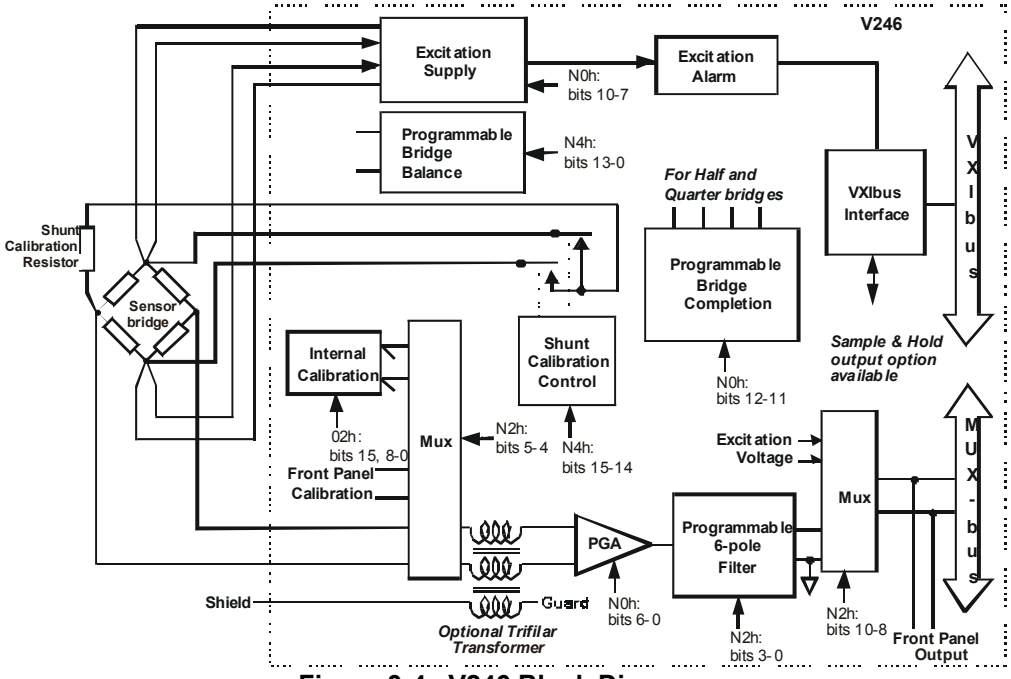


Figure 3-4. V246 Block Diagram

V252

The V252 provides eight or sixteen channels of fixed-frequency low-pass filtering. You can program the gain on a channel-by-channel basis. To provide high roll-off for anti-alias filtering, you can select an eight-pole, low-pass, Bessel, Butterworth, Elliptic, or Constant-delay filter for each channel. Plug-in filter blocks provide cutoff frequencies that range from 10 Hz to 100 kHz. Simultaneous sampling on all channels is available as an option. For calibration, the V207 provides a reference via the VXI Local Bus. An on-board reference can also provide a calibration input. The calibration signals can be applied to any channel.

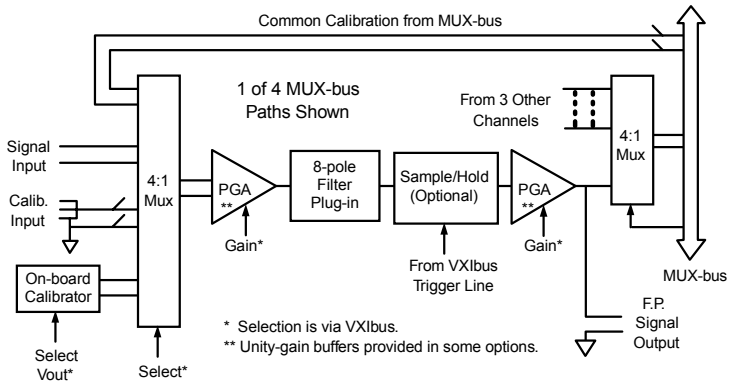


Figure 3-5. V252 Block Diagram

V253

The V253 contains sixteen channels of programmable-frequency, low-pass filtering. Gain is programmable on a channel-by-channel basis as well. Options provide low-pass 6-pole Bessel or Chebyshev filters for all channels.

Simultaneous sampling on all channels is available as an option. Calibration inputs are provided via the front-panel connector, a mainframe reference from the **MUX-bus**, or from an on-board reference. A removable termination housing is available for convenient I/O wiring.

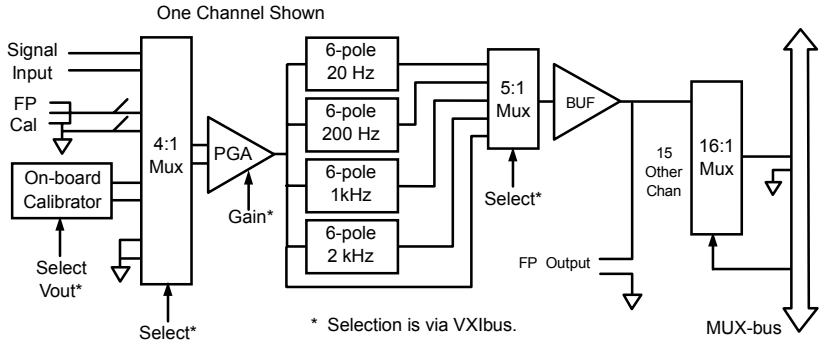


Figure 3-6. V253 Block Diagram

The Digi-bus

In multi-channel systems, the V207 or V208 (the DAC module) generates a digital stream of data with each tick of the sample clock. For applications that require further buffering and processing of the data, the **Digi-bus** option allows the digital data from the DAC to flow to other modules without being subject to the timing uncertainties of the VXI backplane.

Figure 3-7 illustrates the basic **Digi-bus** concept. The V207 or V208 is the source of the data stream and **Digi-bus** timing signals. The V387 digital input module can provide additional discrete data to the stream. The V110 memory module provides multi-buffered access to the data via the VXIbus. The data stream terminates at the V165 DSP, and the DSP software determines what passes on to the left. The V285 waveform generator and the V387 digital input/output module select items from the data stream for output.

The **Digi-bus** supports multiple data sources as well as multiple data sinks. The left-most module receiving digital data also must terminate the bus. The **Digi-bus** supports transfer rates up to 10 Mbytes/second.

The **Digi-bus** and Multi-buffer output options are mutually exclusive. Also, if you plan to use more than one V208 or V207 with **Digi-bus** output in the same mainframe, note that **Digi-bus** and **MUX-bus** use the VXIbus Local Bus. Therefore, if more than one ADC module has access to a **Digi-bus**, only the ADC module positioned at the right end of the **Digi-bus** group of modules can make use of the MUX-bus protocol.

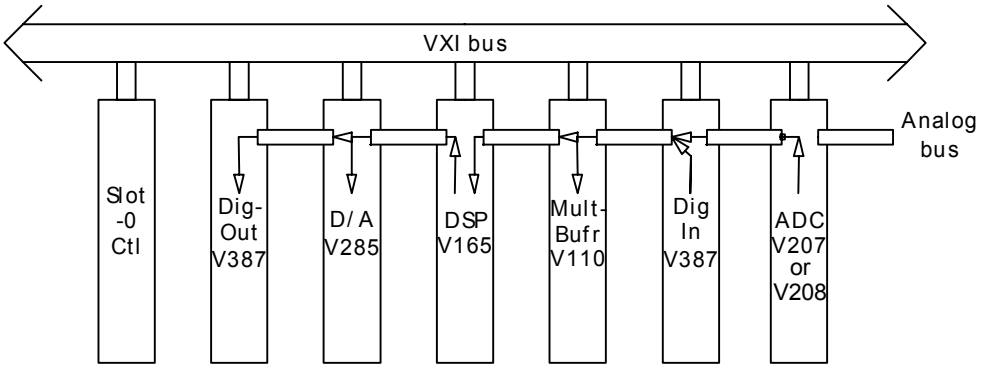


Figure 3-7. Digi-bus concept

Chapter 4: Understanding the V246

Overview

The V246 contains eight channels of bridge signal conditioning with optional bridge-completion resistors and independent bridge excitation. Each channel is capable of amplifying and filtering the input signal. Each channel contains a high-impedance, differential input stage that can withstand ± 35 volts without damage. Each channel is also protected against electrostatic discharge (ESD).

Termination panels and cables that allow you to easily and economically connect your transducers to the V246 are readily available. They are described later in this chapter.

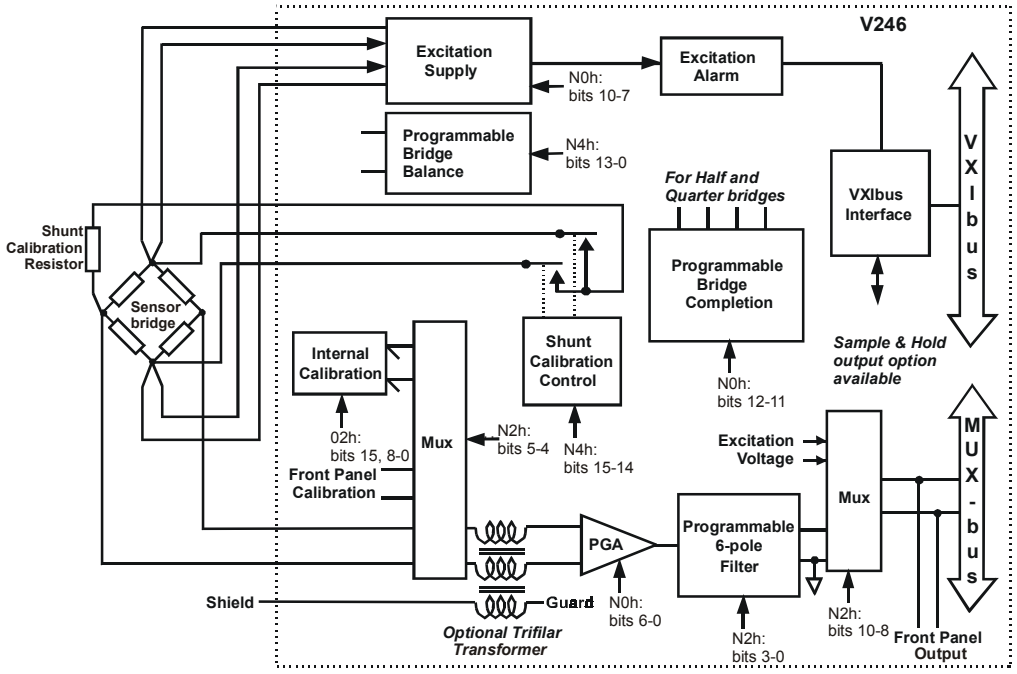


Figure 4-1. V246 block diagram

Bridge completion can be inserted, under software control, via low thermal-EMF, latching relays. Quarter, half or full bridge configurations can be selected. Bridge completion resistor option kits are available in 120-ohm and 350-ohm sets.

Each channel also provides you the ability to balance its bridge. A 12-bit DAC is used to inject current into the bridge to remove initial offset voltages, or pre-loads, of up to 70 mV.

The V246 uses two stages of gain. The first, a programmable instrumentation amplifier, provides gains of 1, 10 and 100. It features high input impedance and high common-mode rejection. The second stage is a programmable-gain amplifier with selectable gains of 1, 2, 5 and 10. Care should always be taken to select the highest gain in the first stage. For an overall gain of 100, for example, better performance will be achieved by selecting a gain of 100 for the first stage and a gain of one for the second, rather than gains of ten on both stages.

Shunt calibration may be performed across two arms of the bridge. Programmable solid state switches provide the switching.

The V246 provides programmable excitation voltages, balanced with respect to ground, of 0, 2.5, 5, 10, and 15 volts at currents of up to 50 mA per-channel. The bandwidth of the control loop exceeds two kHz. Over-current conditions or an open sense lead causes the supply to shut down and an Excitation Alarm interrupt to be generated.

Plug-in units provide filtering on each channel. Standard filters are 6-pole Bessel and 6-pole Chebyschev. Software-selectable cutoff frequencies are 20 Hz, 200 Hz, 1 kHz and 2 kHz.

An optional sample-and-hold plug-in module allows simultaneous sampling of data in the eight channels. If simultaneous sampling is not implemented, data is read from the eight channels sequentially to the ADC.

Optional tri-filar transformers are available for use in environments that are "noisy" or where long input cabling is required. These transformers reduce RF and common-mode voltages to the input of the V246.

Optional serial-number identification is available on both the P3 and P4 connectors to identify cables in large systems.

The instrumentation amplifiers used at the front end of the V246 exhibit low values of input bias current and offset current. For most applications, these currents are not of concern. However, these input currents, however small, must have a return path to ground or the amplifier will saturate. In general, the signal source will be ground-referenced and no problem will arise. If, however, the source is floating, then a return path must be provided. Since these currents are quite small (typically a few nanoamps), a large value of resistance may be added (on the order of megohms). Refer to Figure 4-2.

Voltage inputs should be limited to less than ± 10 volts.

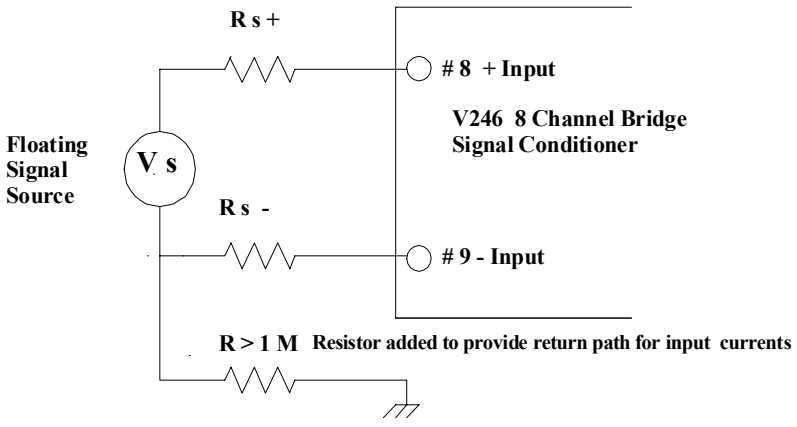
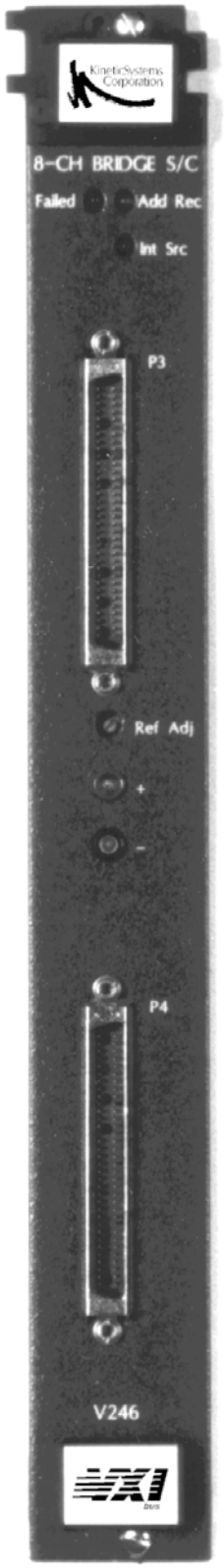


Figure 4-2. Providing Ground Path for Return Currents

Item	Specifications
Input Channels	
Number	Eight, differential
Impedance	20 megohms minimum, >100 megohms typical
Input protection	± 35 V, continuous
Gain Ranges	1, 2, 5, 10, 25, 50, 100, 200, 500, 1000
Frequency Response	± 10.24 V
Filter type	6-pole, Bessel or Chebyshev
Cutoff frequencies	The filter may be bypassed for an extended frequency response to a -3 dB point of 78 kHz.
Excitation	Independent excitation for each channel. Each channel provides ± excitation and sense leads. Excitation voltages of 0 V, 2.5 V, 5 V, 10 V and 15 V are available. Open sense lines or an over-current condition will shut down the supply automatically and signal the error condition. Excitation calibration is also provided.
Line regulation	0.003 %/V
Load regulation	0.00025 V/mA
Temperature coefficient	2 ppm/◦C
Bridge Completion	Eight channels of bridge completion are provided. 1/4-,1/2, and full-bridge configurations are supported. A matched pair of 120-ohm or 350-ohm resistors is provided for 1/2-bridge completion.
Shunt Calibration	± shunt calibration is performed on each channel. The customer-supplied resistors are installed on the termination panel. Switching is performed under software control.
Gain/Offset Accuracy	Referred to input (RTI), after automatic calibration: Gain — Accuracy (Typical) — Accuracy (Maximum) 1 ±(200 µV + 0.002% of reading) ±(200 µV + 0.006% of reading) 2 ±(200 µV + 0.002% of reading) ±(200 µV + 0.006% of reading) 5 ±(100 µV + 0.002% of reading) ±(100 µV + 0.006% of reading) 10 ±(100 µV + 0.002% of reading) ±(100 µV + 0.006% of reading) 20 ±(50 µV + 0.003% of reading) ±(50 µV + 0.009% of reading) 50 ±(50 µV + 0.003% of reading) ±(50 µV + 0.009% of reading) 100 ±(20 µV + 0.005% of reading) ±(20 µV + 0.012% of reading) 200 ±(10 µV + 0.03% of reading) ±(10 µV + 0.06% of reading) 500 ±(5 µV + 0.03% of reading) ±(5 µV + 0.06% of reading) 1000 ±(5 µV + 0.03% of reading) ±(5 µV + 0.06% of reading)
Gain Stability	Better than 20 ppm/◦C (typical)
Offset Voltage Stability	Less than 2 µV/◦C RTI at a gain of 1000
Noise	Less than 5 µV RTI at a gain of 1000 0.5 µV rms RTI (typical) @ gain = 1000 and 20 Hz filter
Linearity	0.005% FSR
CMRR	Typically better than -110 dB, dc to 120 Hz. Optional tri-filar-wound inputs provide excellent RF rejection to 100 MHz.
Bridge Balance	A 12-bit DAC allows removal of bridge offsets up to +/-70 mV with a 350-Ω bridge.
I/O Connector Type	68P High Density
Power Requirements	
+ 5 V	3 A
+12 V	200 mA
-12 V	200 mA
+24 V	350 mA
-24 V	350 mA
Environmental and Mechanical	
Temperature range	
Operational	0◦ C to + 50◦ C
Storage	-25◦ C to + 75◦ C
Relative humidity	0 to 85%, non-condensing to 40◦ C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-sized VXIbus card)
Front-panel potential	Chassis ground

Table 4-1. Performance Characteristics of the V246.

Front Panel



Product specifications and descriptions in this document subject to change without notice.

LEDs

Add Rec

Address Received

Illuminated when the module is being accessed.

Failed

Failed Selftest

Illuminated if the V246 has failed its self-test.

Int Src

Interrupt Source

Illuminated as long as the V246 has an interrupt pending.

Ovrlap

Overlap Detect

Illuminated when a timing violation is detected on the MUX-bus.

Connectors

P3 and P4

There are two high-density 68-pin connectors (AMP 2-174341) on the front panel

Reference Monitor

Ref Adj and "+" & "–"

The internal 10-volt reference may be monitored by connecting a high impedance digital voltmeter across the "+" and "–" terminals on the front panel. Adjustment to this reference voltage is made via the "Ref Adj" potentiometer.

Calibration

The V246 is designed for use with a V207 or V208, each of which contains a 16-bit ADC. A V246 in combination with a V207 or V208 is a highly accurate measuring device, and proper calibration is important. Since components are subject to drift as well as sensitivity to temperature and humidity, it is good practice to perform calibration at regular intervals. Calibration of a V246 is done under software control and can occur as often as required or desired.

The V246 provides for end-to-end calibration. End-to-end means that a known signal is provided to the input of the V246, and the resulting measurement in the V207 or V208 is checked against the known input.

The V246 can perform two types of calibration. *Shunt calibration* is used when the input sensors are configured as a Wheatstone bridge, and a resistor that represents a known transducer increment is switched in and out of a parallel connection with one of the resistors. *Voltage calibration* is a second type of calibration that precisely calibrates a voltage-input signal.

The V246 has been designed for ease of calibration. A multiplexer at the front end of each channel allows selection of one of four inputs to the ADC:

1) A line-level input signal (0- to ±10-volts)
2) A known reference voltage
3) A precision voltage derived from the internal programmable calibrator connected either to the on-board 10-volt reference or to the 10-volt reference provided by the ADC module via the MUX-bus. (Table 1 contains the necessary programming information.)
4) A ground reference (zero volts)

The excitation voltage selected can be measured by the associated ADC module by switching the excitation sense lines to the output multiplexer, allowing the user complete calibration of the channel.

Shunt calibration can be performed automatically on each channel. A customer-supplied shunt resistor may be placed in opposing arms of the bridge to provide ± shunt calibration. This resistor is installed either on the model 7765 termination strip or on the customer's transducer.

Basic Shunt Calibration

Illustrated below is the Wheatstone bridge circuit in a simple form.

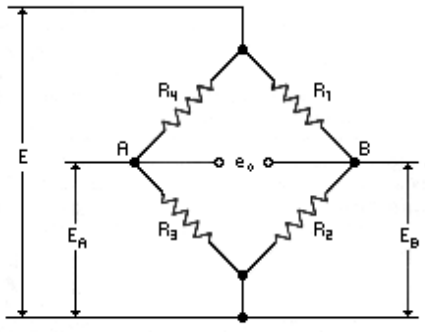


Figure 4.3. Basic Wheatstone bridge circuit

With the bridge excitation provided by the constant voltage E, the output voltage, e_o, is equal to the voltage difference between points A and B:

$$E_B = E\left(1 - \frac{R_1}{R_1 + R_2}\right)$$

$$E_A = E\left(1 - \frac{R_4}{R_4 + R_3}\right)$$

And,

$$e_o = E_A - E_B = E\left(\frac{R_1}{R_1 + R_2} - \frac{R_4}{R_4 + R_3}\right)$$

Or, in more convenient form,

$$\frac{e_o}{E} = \frac{R_1/R_2}{R_1/R_2 + 1} - \frac{R_4/R_3}{R_4/R_3 + 1}$$

It is evident from the form of this equation that the output depends only on the resistance ratios R_1/R_2 and R_4/R_3, rather than on the individual resistances. Furthermore, when $R_1/R_2 = R_4/R_3$, the output is zero and the bridge is described as resistively balanced. Whether the bridge is balanced or unbalanced, this equation permits calculating the change in output voltage due to decreeasing any one of the arm resistances by shunting. The equation also demonstrates that the sign of the change depends on which arm is shunted. For example, decreasing R_1/R_2 by shunting R_1, or increasing R_4/R_3 by shunting R_3 will cause a negative change in output. Correspondingly, a positive change in output is produced by shunting R_2 or R_4 (increasing R_1/R_2, and decreasing R_4/R_3, respectively).

Basic Voltage Calibration

Calibrator Calibration

To achieve the high degree of accuracy for the V246, one must store error coefficients for both gain and offset in the Correction Table (non-volatile RAM) on the V246.

Coefficients are stored for each Calibrator setting to compensate for any gain error in the calibrator itself. These coefficients are applied in software during channel calibration to compute the true voltage applied to a channel during gain calibration. The coefficients are stored in the Correction Table (Table 2) starting offset 2010h in **A24** space.

You must also store coefficients to compensate for channel-to-channel offset errors. These coefficients are applied in software during channel offset calibration and are stored starting at **A24** offset 2040h.

This calibration procedure should be performed approximately every six months. The calibration date is also stored in the Correction Table to help track the last calibration date. The date is stored at the beginning of the Correction Table starting at **A24** offset 2000h.

Calibrate Voltage	On-board Source	MUX-bus Source
+10.0 V	8091h	0091h
+5.0 V	80A1h	00A1h
+2.0 V	80C1h	00C1h
+1.0 V	8092h	0092h
+0.5 V	80A2h	00A2h
+0.2 V	80C2h	00C2h
+0.1 V	8094h	0094h
+0.05 V	80A4h	00A4h
+0.02 V	80C4h	00C4h
+0.01 V	8098h	0098h
+0.005 V	80A8h	00A8h
+0.002 V	80C8h	00C8h
-0.002 V	8148h	0148h
-0.005 V	8128h	0128h
-0.01 V	8118h	0118h
-0.02 V	8144h	0144h
-0.05 V	8124h	0124h
-0.1 V	8114h	0114h
-0.2 V	8142h	0142h
-0.5 V	8122h	0122h
-1.0 V	8112h	0112h
-2.0 V	8141h	0141h
-5.0 V	8121h	0121h
-10.0 V	8111h	0111h

Table 4.2 - Calibration Register Values

Offset	Function
2000h	The month of the last calibration date (1 - 12)
2002h	The day of the last calibration date (1 - 31)
2004h	The year of the last calibration date
2006h - 200Eh	User definable
2010h	Gain correction coefficient for +/- 10 v
2012h	Gain correction coefficient for +/- 5 v
2014h	Gain correction coefficient for +/- 2 v
2016h	Gain correction coefficient for +/- 1 v
2018h	Gain correction coefficient for +/- 500 millivolts
201Ah	Gain correction coefficient for +/- 200 mv
201Ch	Gain correction coefficient for +/- 100 mv
201Eh	Gain correction coefficient for +/- 50 mv
2020h	Gain correction coefficient for +/- 20 mv
2022h	Gain correction coefficient for +/- 10 mv
2024h	Gain correction coefficient for +/- 5 mv
2026h	Gain correction coefficient for +/- 2 mv
2028h - 203Eh	Reserved
2040h	Offset correction coefficient for channel 1
2042h	Offset correction coefficient for channel 2
2044h	Offset correction coefficient for channel 3
2046h	Offset correction coefficient for channel 4
2048h	Offset correction coefficient for channel 5
204Ah	Offset correction coefficient for channel 6

204Ch	Offset correction coefficient for channel 7
204Eh	Offset correction coefficient for channel 8
2050h - 21Feh	Reserved

Table 4.3. Correction Table

Following are the steps to follow in performing the V246 module calibration:

Note - A jumper must be installed at JMP1 before attempting to write to EEPROM locations. *Remove the jumper after completing the calibration procedure.*

1) Allow the V246 at least a 30-minute warm-up period.
2) Connect the "+" and "-" front panel test points to a precision voltage meter.
3) Adjust the "Ref Adj." potentiometer on the front panel for +10.0000 Volts DC.
4) Connect "Cal Ref Out" (P4 pin 33 is Hi, P4 pin 66 is Lo) to a precision voltage meter. All channel input pins must be connected to ground (use the "-" front panel test point for ground).
5) In software, for each channel of the V246 set input and output Mux to “line," "full bridge," "0 volts excitation," "gain x1000," "filter by-pass."
6) Gain Calibration - repeat steps 6a to 6c for all 12 differential calibrator voltages. In the following equation, these expected calibrator voltages are referred to as "CALIBRATOR," ranging from 10 volts to 2 millivolts. The calibrator voltages are set by writing to the Calibration Register (Operational register in A24 space at offset 0002h). Make sure to wait for the calibrator voltage to settle before any measurements are taken.
   a) Use a precision meter to measure the positive calibration voltage (average 10 points). The measured positive calibration voltage is referred to as PCAL in the equation of step 6c.
   b) Use a precision meter to measure the negative calibration voltage (average 10 points). The measured negative calibration voltage is referred to as NCAL in the equation of step 6c.
   c) Store the gain error coefficient into the Correction Table (Table 2) as a 16-bit signed integer according to the following equation:

$$GAIN\ COEFFICIENT = \left(\frac{PCAL - NCAL}{CALIBRATOR \times 2} - 1\right) \times 10^{6}$$

Note: You must wait a minimum of 3 ms after writing coefficient before writing again.

7) If offset calibration is not needed, then skip to step 9.
8) Offset calibration - for each channel repeat steps 8a through 8f.
   a) Install a V207 (or other ADC) to the left of the V246.
   b) In software, for each channel of the V246 set input and output Mux to “line," "full bridge," "0 volts excitation," "gain x1000," "filter by-pass."
   c) Measure the front panel offset voltage (RTO) using the V207 (average 10 points). Use this equation to convert the COUNTS read from the V207 into RTO voltage.

$$VOLTAGE(RTO) = (COUNTS - 32768) x 312.5 \mu Volts$$

This front panel ground measurement is referred to as FP OFFSET in the equation of step 8f.

d) On the V246, in software, connect all channels input Mux to "zero" (all other settings are the same as step 5).
e) Measure the zero offset voltage (RTO), using the equation in step 8c (average 10 points). The zero ground measurement is referred to as CAL OFFSET in the equation of step 8f.
f) Store the zero error coefficient into the Correction Table (Table 2) as a 16-bit signed integer according to the following equation:

$$OFFSET\ COEFFICIENT = \frac{(FP\ OFFSET - CAL\ OFFSET)}{1000} x\ 10^9$$

9) Store the calibration data in the Correction Table (Table 2).
Note: You must wait a minimum of 3 ms after writing coefficient before writing again.
10) End of calibration. Remove the jumper at JMP1**.**

Channel Calibration

Once the module has been calibrated, each channel on the V246 can be calibrated using the onboard calibrator under software control. Offset and gain error coefficients for each channel must be stored in software and be applied to any voltage readings from those channels. It is important not to confuse these error coefficients with those stored in non-volatile RAM on the V246. The error coefficients in non-volatile RAM are used during the channel calibration. Following are the steps to follow in performing the V246 channel calibration:

1) The V246 should be allowed at least a 30 minute warm-up period.
2) Set V246 channels to the desired gain and filter selection.
3) Gain Calibration - repeat the following steps *a* through *f* for channels one through eight.
   a) Set the channel to the calibration voltage. This is done by setting bit 14 (only) of the Prefilter Gain Register. Do not change the value of the other bits in this register.
   b) Set the calibration voltage so that channels have positive full scale voltage. The full scale voltage is dependent on the gain setting for that channel. The expected positive full scale calibration voltage will be referred to as $\text{POSCAL}_{\text{EXPECTED}}$ in the equation of step 3f. The calibration voltage is set by writing to the Calibration Register (at offset 2h in **A24** space). Be sure to wait for the voltage to settle to 16-bit accuracy once the calibration voltage is set.
   c) Measure the positive full scale voltage (average 20 points). Use the equation below to convert the COUNTS read from the V208 into voltage RTO. The measured positive full-scale calibration voltage is referred to as $\text{POSCAL}_{\text{MEASURED}}$ in the equation of step 3f.

$$VOLTAGE(RTO) = (COUNTS - 32768)x312.5\mu Volts$$

   d) Set the calibration voltage so that each channel has negative full-scale voltage. The full-scale voltage is dependent on the gain setting for that channel. The expected negative full scale calibration voltage will be referred to as $\text{NEGCAL}_{\text{EXPECTED}}$ in the equation as of step 3f. The calibration voltage is set by writing to the Calibration Register (at offset 2h in **A24** space). A table of the register settings is available. Be sure to wait for the voltage to settle to 16-bit accuracy once the calibration voltage is set.
   e) Measure the negative full-scale voltage (average 20 points). Use the equation in step 3c. The measured negative full-scale calibration voltage is referred to as $\text{NEGCAL}_{\text{MEASURED}}$ in the equation of step 3f.
   f) Read the gain error for the calibrator voltage from the Correction Table. The gain-error correction term is referred to as GAINCOEF in the following equation:

$$GAIN = \frac{POSCAL_{MEASURED} - NEGCAL_{MEASURED}}{(POSCAL_{EXPECTED} - NEGCAL_{EXPECTED}) \bullet (1 + GAINCOEF \bullet 10^{-6})}$$

   g) Record the "true" gain for the channel as calculated above.

4) Offset Calibration - repeat the following for channels one through eight.
   a) Set the calibration voltage to ground. Write 4000h to the Calibration Register. (Operation register in **A24** space at offset 0002h). Wait for the filter to settle to 16-bit accuracy.
   b) Measure the offset voltage (average 20 points). Use the equation in step 3c. The measured offset voltage is referred to as $OFFSET_{MEASURED}$ in the equation of step 4c.
   c) Read the offset error for the calibrator voltage from the Correction Table. The offset-error correction term is referred to as OFFSETCOEF in the following equation:

$$OFFSET = \frac{OFFSET_{MEASURED}}{GAIN} + (OFFSETCOEF \bullet 10^{-9})$$

   d) Record the "true" offset for the channel as calculated above.

Applying the Software Coefficients

When you have calculated the software gain and offset coefficients for each channel, they may be applied when taking data. Measure the counts from the V207/8. The V207/8 represents voltage in an offset binary format. In the following two equations, this variable will be referred to as COUNTS.

When calibration is unnecessary, the gain is derived simply from the gain settings in the Pre-filter Gain and Post-filter Gain Registers. This uncalibrated gain is represented with the variable $GAIN_{UNCALIBRATED}$ in the following equation:

$$UNCALIBRATEDVOLTAGE = \frac{(COUNTS - 32768) \bullet 312.5\mu Volts}{GAIN_{UNCALIBRATED}}$$

For best accuracy the calibration coefficients may be used to calculate the calibrated voltage using the following equation:

$$CALIBRATEDVOLTAGE = \frac{(COUNTS - 32768) \bullet 312.5\mu Volts}{GAIN} - OFFSET$$

Where GAIN is the "true" channel gain as calculated in step 3f above and OFFSET is the "true" channel offset as calculated in step 4c above.

MUX-bus

The **MUX-bus** is implemented on the 12-line VXI Local Bus. The P2 connector allows access by the V246 to Local-bus lines LBUSC00 - LBUSC11. Signal conditioning modules supporting the **MUX-bus** protocol may be plugged into the VXI mainframe only to the right of the V207 or V208.

The **MUX-bus** pin definition on the P2 connector is:

LBUSC00	**Channel-A +**
LBUSC01	**Channel-A** –
LBUSC02	**Channel-B +**
LBUSC03	**Channel-B** –
LBUSC04	**Channel-C +**
LBUSC05	**Channel-C** –
LBUSC06	**Channel-D +**
LBUSC07	**Channel-D** –
LBUSC08	**Reference +**
LBUSC09	**Reference** –
LBUSC10	**Overlap Detect**
LBUSC11	**Clock**

Table 4.4. MUX-bus Pin Definition, P2 Connector

The four **MUX-bus** channels A-D carry the multiplexed high-level signal-conditioned outputs to the ADC. The Reference + and Reference – signals provide a 10-volt differential signal to signal conditioning modules, allowing all channels to be referenced to a common standard. This simplifies system calibration in cases where the Correction Table is not used. However, for best accuracy the Correction Table and on-board reference should be used.

Overlap Detect is used by the signal conditioning modules to detect if two or more modules are attempting to output their voltages at the same time, thus alerting the user to conflicts caused by incorrectly programmed Scan RAM.

Clock is supplied by the ADC module. It is used by the conditioning modules for synchronization among adjacent modules utilizing the **MUX-bus**.

Scan RAM

You can multiplex up to 256 channels of conditioned analog signals into a V207 or V208 ADC module. The V246 is one of several signal-conditioning modules that can interface with a V207 or V208 via the **MUX-bus**.

The contents of the scan memory (called "Scan RAM") determine the sampling sequence of the channels, and you must write the desired sequence into the 256-word Scan RAM before acquisition can begin. As each channel is converted, an address register increments, and the next location in Scan RAM selects the channel to be digitized. The same address register routes the converted data to the appropriate sequential location in Ping-Pong, Multi-buffer, or **Digi-bus** memory.

Scan RAM exists in *all* **MUX-bus** modules, including the V246. You must write the *same* sampling sequence into each Scan RAM, with an important exception. You must set bit 14 to a "**1**" in a module's scan RAM to indicate when the sequence applies to that particular module. In other words, when bit 14 is set, that module gates its selected analog signal onto the **MUX-bus**. You must take care to *not* set bit 14 in more than one signal-conditioning module at the same address location.

Following is an example of loading the Scan RAM for the following module configuration:

- One V207 host ADC module and two V246 8-channel bridge signal conditioning modules.
- All 8 channels in each V246 are included in the scan list.
- V246 #1 is to be first in the list, followed by V246 #2.
- The channels in each V246 are to be scanned in order, 1 through 8.

The organization of the Scan RAM is as follows:

- Bit 15 is set to **"1"** to define the end of the list.
- Bit 14 is set to **"1"** in a signal conditioning module to connect a channel in *that module* to the **MUX-bus** at that point in the scan list.
- Bits 13 and 12 are not used in any Scan RAM and should be written as **"0."**
- Bits 11 through 0 define the channel to be scanned.
- Bits 1 and 0 *also* define the **MUX-bus** channel (A, B, C or D) being used.
- Bits 14 through 2 are ignored in the V207 ADC. Only the end-of-list flag (bit 15) and the **MUX-bus** channel selection (bits 1 and 0) are used in the V207's Scan RAM.

The Scan RAM setup considerations are:

- Bit 14 must be set to **"1"** in *only one* signal conditioning module at any Scan RAM address. Otherwise, more than one signal conditioning module will be connected to the MUX bus at the same time. This error will cause an "overlap" indication in one or more signal conditioning modules.
- Four **MUX-bus** channels are used to provide sufficient data settling time. If a sequence other than A, B, C, D (as defined by the two least significant bits in the channel address) is used, this sequence must be repeated throughout the scan list to produce predictable

results. This also means that the number of channels in a scan list must be divisible by 4 (4, 8, 12, 16, etc.).

- The end-of-list flag (bit 15 = **"1"**) must be in the same list location in the ADC and in all signal conditioning modules connected to it. This flag is placed in the list location that represents the last channel scanned in the scan list.
- There are many bits that are ignored in the V207's Scan RAM, and the channel address bits related to one signal conditioning module are ignored by others in the subsystem. However, a recommended convention is to write the same data pattern for bits 13-0 in the Scan RAM for the ADC and all signal conditioning modules, while writing "**0**" for bit 14 for all locations in the V207 Scan RAM and writing the appropriate values for bit 14 in the signal conditioning Scan RAM memories.
- All Scan RAM data is ignored for addresses beyond that which contains the end-of-list flag. Good convention would have those data words written with all "**0**'s."

The following charts show the bit patterns to be written in the Scan RAM memories for this V207-V246 example:

Scan RAM - V207 ADC

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Data	MUX	Selection
200h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h	A	
202h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001h	B	
204h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002h	C	
206h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0003h	D	
208h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0004h	A	
20Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0005h	B	
20Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0006h	C	
20Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0007h	D	
210h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h	A	
212h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001h	B	
214h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002h	C	
216h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0003h	D	
218h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0004h	A	
21Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0005h	B	
21Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0006h	C	
21Eh	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	8007h	D	End List
220h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		
	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•			
3FEh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		

Scan RAM - V246 Signal Conditioner #1

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Data	Mux	Selection
100h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000h	A	Channel 1
102h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4001h	B	Channel 2
104h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	4002h	C	Channel 3

106h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	4003h	D	Channel 4
108h	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	4004h	A	Channel 5
10Ah	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	4005h	B	Channel 6
10Ch	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	4006h	C	Channel 7
10Eh	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	4007h	D	Channel 8
110h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0000h	A	
112h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001h	B	
114h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002h	C	
116h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0003h	D	
118h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0004h	A	
11Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0005h	B	
11Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0006h	C	
11Eh	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	8007h	D	End List
120h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		
	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•			
10FEh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		

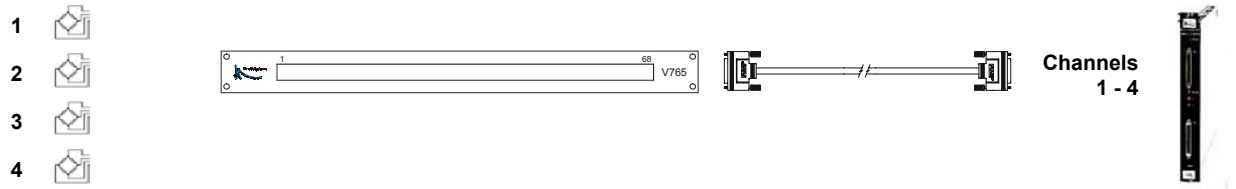
Scan RAM - V246 Signal Conditioner #2

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Data	Mux	Selection
100h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h	A	
102h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001h	B	
104h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002h	C	
106h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0003h	D	
108h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0004h	A	
10Ah	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0005h	B	
10Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0006h	C	
10Eh	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0007h	D	
110h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000h	A	Channel 1
112h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4001h	B	Channel 2
114h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	4002h	C	Channel 3
116h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	4003h	D	Channel 4
118h	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	4004h	A	Channel 5
11Ah	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	4005h	B	Channel 6
11Ch	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	4006h	C	Channel 7
11Eh	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	C007h	D	Channel 8 + End List
120h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		
	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•			
10FEh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h		

Connecting to the V246

The following pages show you how to connect your sensors to the V246. Tables 4.5 and 4.6 list the terminal numbers and pin numbers that you may encounter if you utilize all eight channels of the V246. Two V765 terminal strips and two 5868 cables are needed to accommodate eight channels.

Figures 4.4 through 4.11 show you how to utilize strain-gage sensors in a number of bridge configurations. Figures 4.12, 4.13 and 4.14 show you how to accommodate RTD sensors, potentiometer inputs and voltage inputs. The pin numbers shown are for Channel 1 of a V765-ZA11 terminal strip.

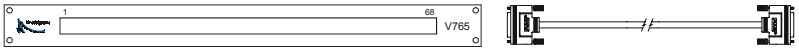


BRIDGE-TYPE SENSORS *(up to 4)*	**TERMINAL STRIP (V765–ZA11)** Left to Right	**TERMINAL STRIP (V765–ZA11)** Rear Conn. J4	**CABLE (5868–Fx0J)** *(x = length in meters)*	**V246** Front Conn. J3
Channel 1				
Input +	1	1	TAN / **WHITE**	3
Input –	2	35	**WHITE** / TAN	4
Excitation +	3	2	BROWN / **WHITE**	2
Excitation –	4	36	**WHITE** / BROWN	38
Sense +	5	3	PINK / **WHITE**	35
Sense –	6	37	**WHITE** / PINK	5
Monitor +	7	4	ORANGE / **WHITE**	1
Monitor –	8	38	**WHITE** / ORANGE	39
Calibrate Resistor	9	5	YELLOW / **WHITE**	36
Quarter Bridge	10	39	**WHITE** / YELLOW	6
Shield	11	6	GREEN / **WHITE**	37
Channel 2				
Shield	12	40	**WHITE** / GREEN	43
Input +	13	7	BLUE / **WHITE**	9
Input –	14	41	**WHITE** / BLUE	10
Excitation +	15	8	VIOLET / **WHITE**	8
Excitation –	16	42	**WHITE** / VIOLET	44
Sense +	17	9	GRAY / **WHITE**	41
Sense –	18	43	**WHITE** / GRAY	11
Monitor +	19	10	BROWN / **TAN**	7
Monitor –	20	44	**TAN** / BROWN	45
Calibrate Resistor	21	11	PINK / **TAN**	42
Quarter Bridge	22	45	**TAN** / PINK	12
Channel 3				
Input +	23	12	ORANGE / **TAN**	15
Input –	24	46	**TAN** / ORANGE	16
Excitation +	25	13	YELLOW / **TAN**	14
Excitation –	26	47	**TAN** / YELLOW	50
Sense +	27	14	GREEN / **TAN**	47
Sense –	28	48	**TAN** / GREEN	17
Monitor +	29	15	BLUE / **TAN**	13
Monitor –	30	49	**TAN** / BLUE	51
Calibrate Resistor	31	16	VIOLET / **TAN**	48
Quarter Bridge	32	50	**TAN** / VIOLET	18
Shield	33	17	GRAY / **TAN**	49

BRIDGE-TYPE SENSORS *(up to 4)*	**TERMINAL STRIP (V765–ZA11)** Left to Right	Rear Conn. J4	**CABLE (5868–Fx0J)** *(x = length in meters)*	**V246** Front Conn. J3
Channel 4				
Shield	34	51	**TAN** / GRAY	55
Input +	35	18	PINK / **BROWN**	21
Input –	36	52	**BROWN** / PINK	22
Excitation +	37	19	ORANGE / **BROWN**	20
Excitation –	38	53	**BROWN** / ORANGE	56
Sense +	39	20	YELLOW / **BROWN**	53
Sense –	40	54	**BROWN** / YELLOW	23
Monitor +	41	21	GREEN / **BROWN**	19
Monitor –	42	55	**BROWN** / GREEN	57
Calibrate Resistor	43	22	BLUE / **BROWN**	54
Quarter Bridge	44	56	**BROWN** / BLUE	24
No connection	45	23	VIOLET / **BROWN**	
No connection	46	57	**BROWN** / VIOLET	
No connection	47	24	GRAY / **BROWN**	
No connection	48	58	**BROWN** / GRAY	
No connection	49	25	ORANGE / **PINK**	
No connection	50	59	**PINK** / ORANGE	
Ser.#, P3 ID, High	51	26	YELLOW / **PINK**	58
Ser.#, P3 ID, Low	52	60	**PINK** / YELLOW	25
Ext. out, High, 1	53	27	GREEN / **PINK**	26
Ext. out, Low, 1	54	61	**PINK** / GREEN	30
Ext. out, High, 2	55	28	BLUE / **PINK**	27
Ext. out, Low, 2	56	62	**PINK** / BLUE	31
Ext. out, High, 3	57	29	VIOLET / **PINK**	28
Ext. out, Low, 3	58	63	**PINK** / VIOLET	32
Ext. out, High, 4	59	30	GRAY / **PINK**	29
Ext. out, Low, 4	60	64	**PINK** / GRAY	33
Ext. out, High, 5	61	31	YELLOW / **ORANGE**	60
Ext. out, Low, 5	62	65	**ORANGE** / YELLOW	64
Ext. out, High, 6	63	32	GREEN / **ORANGE**	61
Ext. out, Low, 6	64	66	**ORANGE** / GREEN	65
Ext. out, High, 7	65	33	BLUE / **ORANGE**	62
Ext. out, Low, 7	66	67	**ORANGE** / BLUE	66
Ext. out, High, 8	67	34	VIOLET / **ORANGE**	63
Ext. out, Low, 8	68	68	**ORANGE** / VIOLET	67

Table 4-5. Wiring from Sensors to V246 Channels 1 – 4

6
7
8



BRIDGE-TYPE SENSORS *(up to 4)*	**TERMINAL STRIP (V765–ZA11)** Left to Right	Rear Conn. J4	**CABLE (5868–Fx0J)** *(x = length in meters)*	**V246** Front Conn. J4
Channel 5				
Input +	1	1	TAN / **WHITE**	3
Input –	2	35	**WHITE** / TAN	4
Excitation +	3	2	BROWN / **WHITE**	2
Excitation –	4	36	**WHITE** / BROWN	38
Sense +	5	3	PINK / **WHITE**	35
Sense –	6	37	**WHITE** / PINK	5
Monitor +	7	4	ORANGE / **WHITE**	1
Monitor –	8	38	**WHITE** / ORANGE	39
Calibrate Resistor	9	5	YELLOW / **WHITE**	36
Quarter Bridge	10	39	**WHITE** / YELLOW	6
Shield	11	6	GREEN / **WHITE**	37
Channel 6				
Shield	12	40	**WHITE** / GREEN	43
Input +	13	7	BLUE / **WHITE**	9
Input –	14	41	**WHITE** / BLUE	10
Excitation +	15	8	VIOLET / **WHITE**	8
Excitation –	16	42	**WHITE** / VIOLET	44
Sense +	17	9	GRAY / **WHITE**	41
Sense –	18	43	**WHITE** / GRAY	11
Monitor +	19	10	BROWN / **TAN**	7
Monitor –	20	44	**TAN** / BROWN	45
Calibrate Resistor	21	11	PINK / **TAN**	42
Quarter Bridge	22	45	**TAN** / PINK	12
Channel 7				
Input +	23	12	ORANGE / **TAN**	15
Input –	24	46	**TAN** / ORANGE	16
Excitation +	25	13	YELLOW / **TAN**	14
Excitation –	26	47	**TAN** / YELLOW	50
Sense +	27	14	GREEN / **TAN**	47
Sense –	28	48	**TAN** / GREEN	17
Monitor +	29	15	BLUE / **TAN**	13
Monitor –	30	49	**TAN** / BLUE	51
Calibrate Resistor	31	16	VIOLET / **TAN**	48
Quarter Bridge	32	50	**TAN** / VIOLET	18
Shield	33	17	GRAY **/ TAN**	49
Channel 8				

BRIDGE-TYPE SENSORS *(up to 4)*	**TERMINAL STRIP (V765–ZA11)**		**CABLE (5868–Fx0J)** *(x = length in meters)*	**V246**
	Left to Right	**Rear Conn. J4**		**Front Conn. J4**
Shield	34	51	**TAN** / GRAY	55
Input +	35	18	PINK / **BROWN**	21
Input –	36	52	**BROWN** / PINK	22
Excitation +	37	19	ORANGE / **BROWN**	20
Excitation –	38	53	**BROWN** / ORANGE	56
Sense +	39	20	YELLOW / **BROWN**	53
Sense –	40	54	**BROWN** / YELLOW	23
Monitor +	41	21	GREEN / **BROWN**	19
Monitor –	42	55	**BROWN** / GREEN	57
Calibrate Resistor	43	22	BLUE / **BROWN**	54
Quarter Bridge	44	56	**BROWN** / BLUE	24
No connection	45	23	VIOLET / **BROWN**	
No connection	46	57	**BROWN** / VIOLET	
No connection	47	24	GRAY / **BROWN**	
No connection	48	58	**BROWN** / GRAY	
No connection	49	25	ORANGE / **PINK**	
No connection	50	59	**PINK** / ORANGE	
Ser.#, P4 ID, High	51	26	YELLOW / **PINK**	58
Ser.#, P4 ID, Low	52	60	**PINK** / YELLOW	25
Constat 1	53	27	GREEN / **PINK**	26
Front Panel Ref High	54	61	**PINK** / GREEN	30
Constat 3	55	28	BLUE / **PINK**	27
No connection	56	62	**PINK** / BLUE	31
No connection	57	29	VIOLET / **PINK**	28
No connection	58	63	**PINK** / VIOLET	32
No connection	59	30	GRAY / **PINK**	29
No connection	60	64	**PINK** / GRAY	33
Constat 2	61	31	YELLOW / **ORANGE**	60
Front Panel Ref Low	62	65	**ORANGE** / YELLOW	64
Digital Ground	63	32	GREEN / **ORANGE**	61
No connection	64	66	**ORANGE** / GREEN	65
No connection	65	33	BLUE / **ORANGE**	62
No connection	66	67	**ORANGE** / BLUE	66
Cal Ref Out High	67	34	VIOLET / **ORANGE**	63
Cal Ref Out Low	68	68	**ORANGE** / VIOLET	67

Table 4-6. Wiring from Sensors to V246 Channels 5 – 8

Transducer Interconnect Diagrams

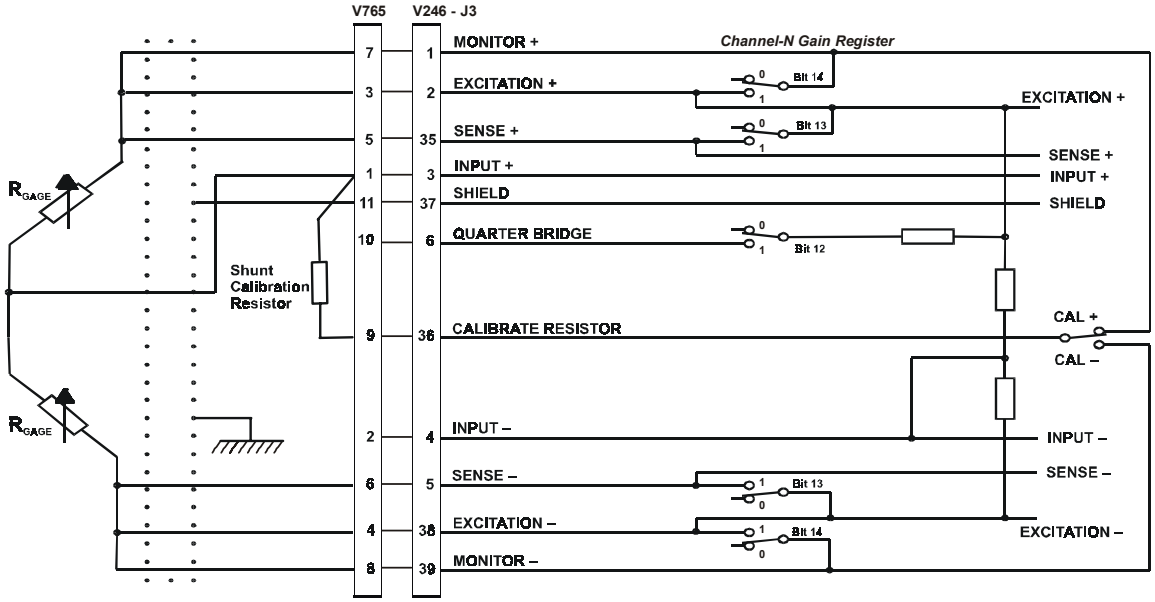


Figure 4-4. Half Bridge with Remote Sensing

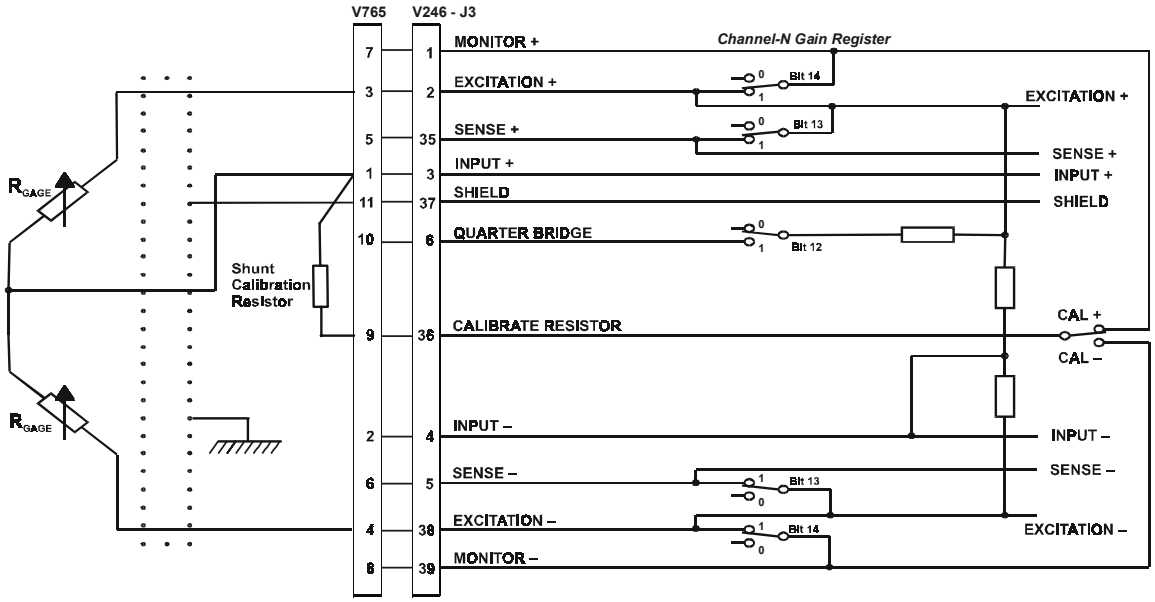


Figure 4-5. Half Bridge with Local Sensing

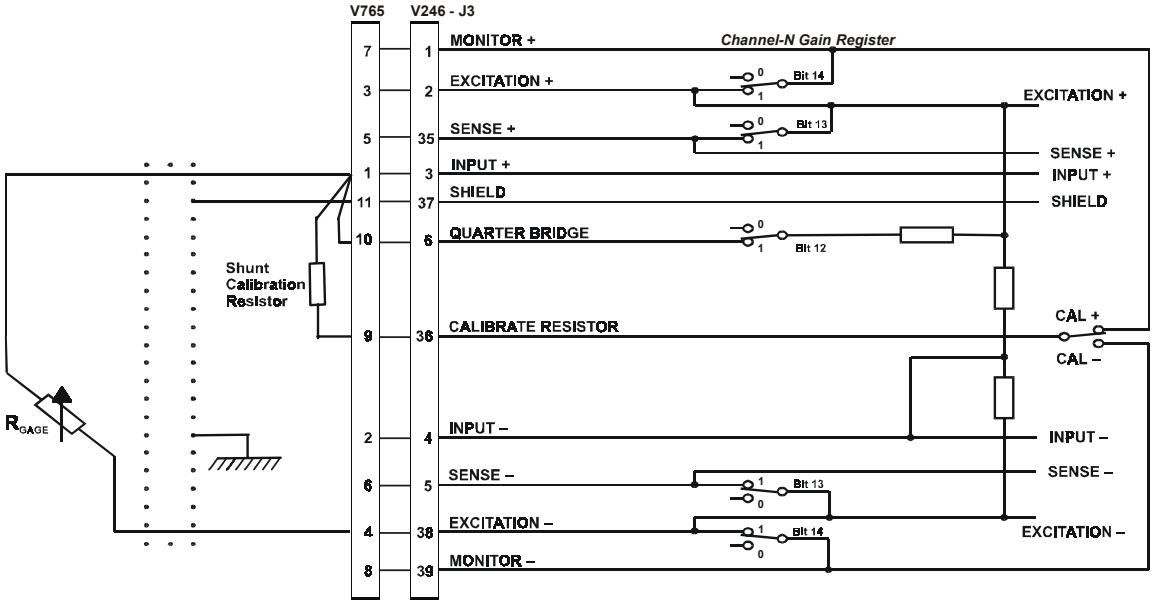


Figure 4-6. Quarter Bridge with Local Sensing

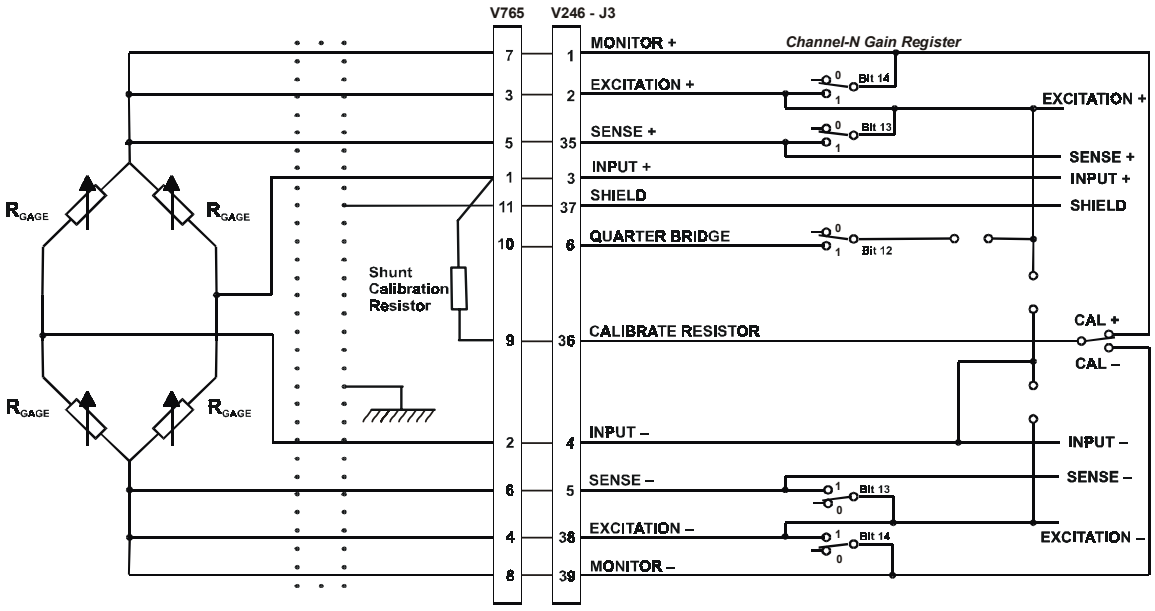


Figure 4-7. Full Bridge with Remote Sensing

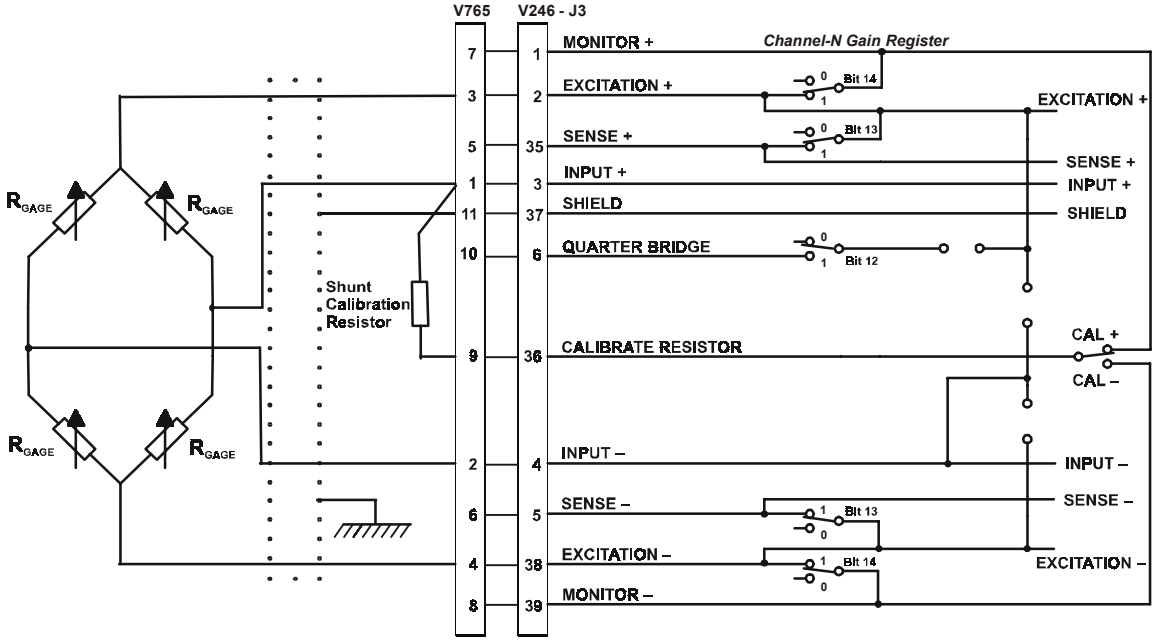


Figure 4-8. Full Bridge with Local Sensing

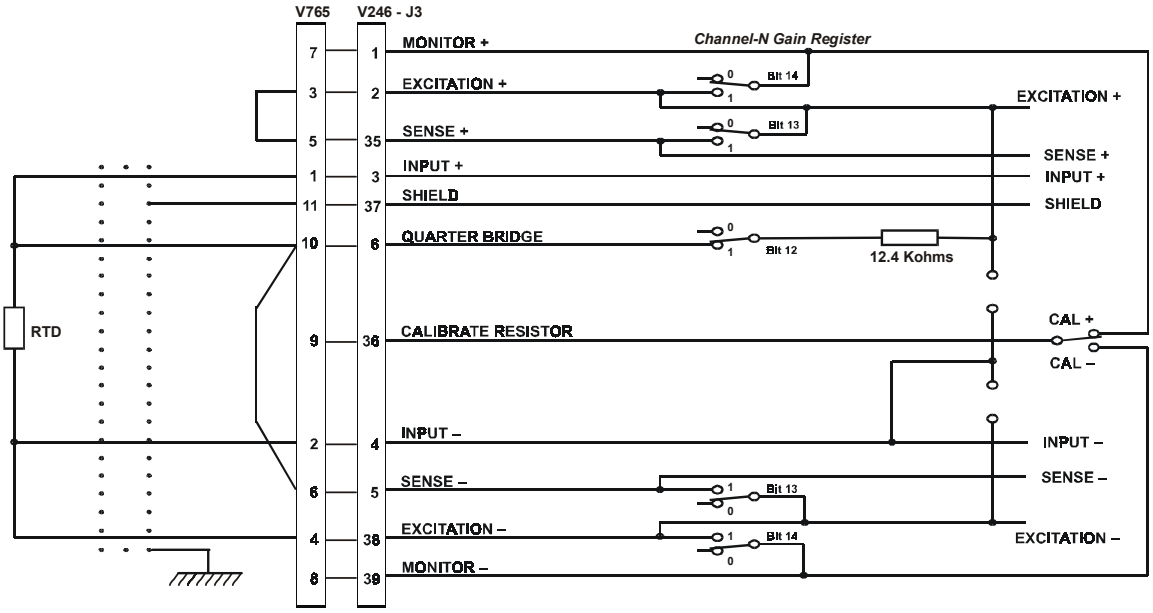


Figure 4-9. RTD Sensor

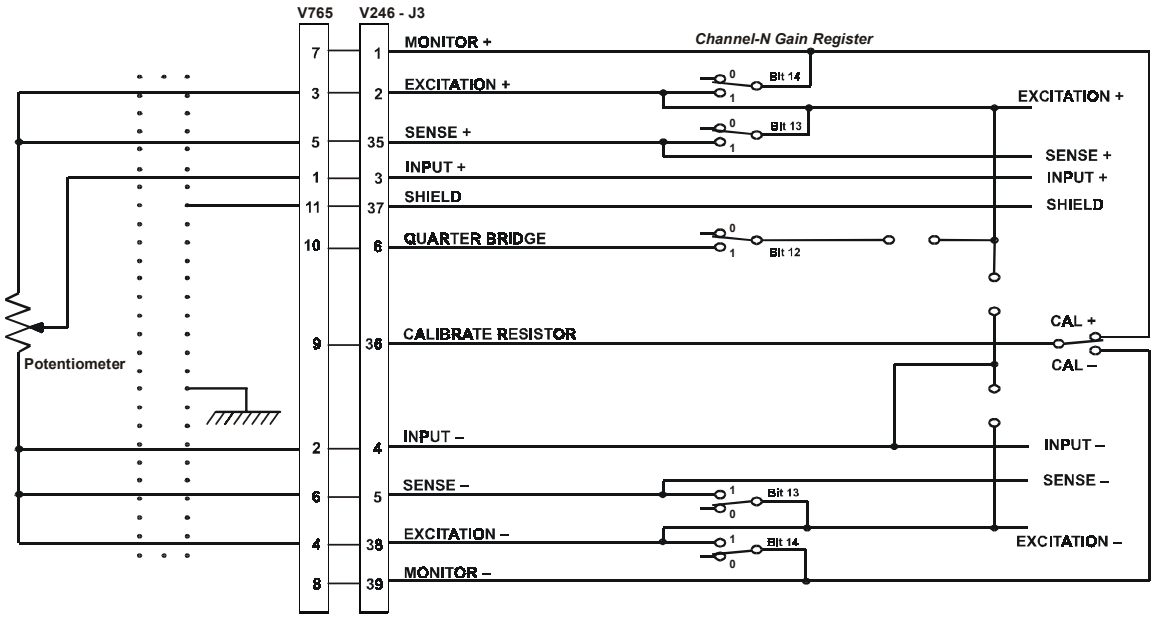


Figure 4-10. Potentiometer Input

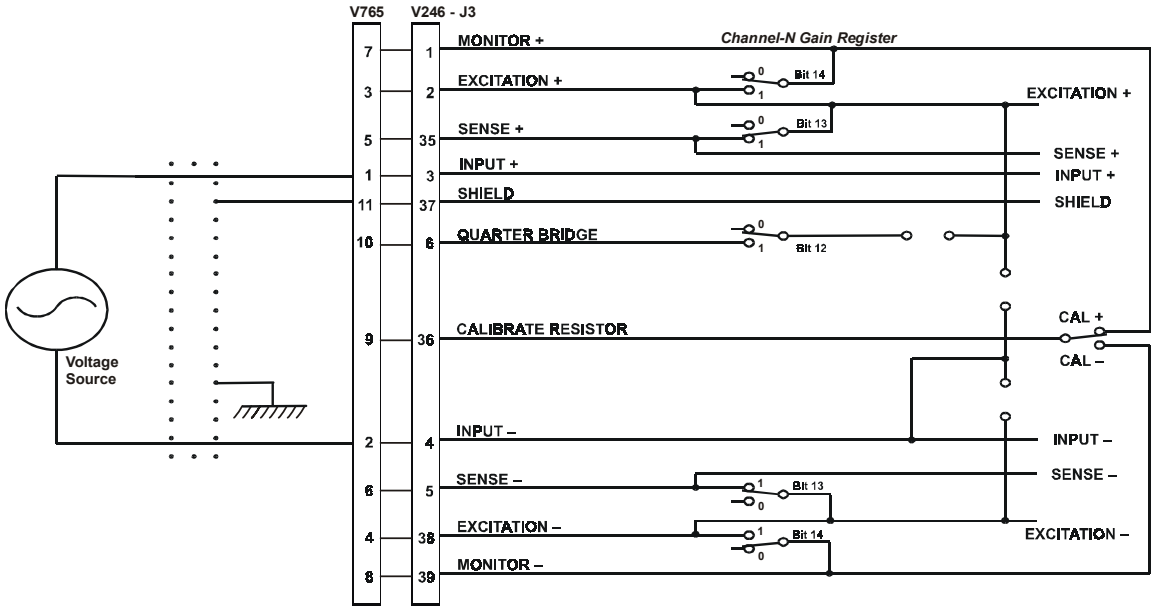


Figure 4-11. Voltage Input

Chapter 5: Configuration and Operational Registers

Address Space

VXIbus uses the VMEbus protocol for data transfer and therefore supports 32-bit addressing to access I/O slave devices. 32-bit addressing provides direct access to memory space of four Gigabytes.

Slave devices such as VXIbus data acquisition modules exist for a variety of purposes and can be simple or very complex. Communication between host and slave can require access to several registers in one device or access to many Mbytes of memory in another. ("Devices" and "modules" are terms often used interchangeably. The distinction is that more than one VXIbus device *can* reside in a VXIbus module. However, there is generally one device per module.)

To minimize the amount of address-decoding hardware needed, simpler slave devices use addressing modes that fully decode only 16 or 24 address lines rather than 32. Therefore, there are three defined addressing modes…**A16**, **A24** and **A32**…having address spaces of 64 kbytes, 16 Mbytes and 4 Gbytes, respectively.

All VXIbus devices have registers located within 64-byte blocks in **A16** address space and therefore support **A16** addressing. Devices requiring no more than 64 bytes of address space need only support **A16** addressing. Devices needing more than the 64 bytes to accommodate additional registers or blocks of memory *must* also support **A24** or **A32** addressing, but not both. VXIbus devices that use **A24** or **A32** addressing modes are required to have four registers in **A16** space for parameter definition. One such parameter is Required Memory, which uses four bits (*m*) to specify the size of the memory in **A24** or **A32** space required by the device. A device *may not* use more than one-half of the memory space, and it *should not* use more than one-fourth. Table 5-1 shows the relationship between the four-bit parameter, *m,* and the memory required by the device. Note that *m = zero* defines the case for maximum usage, i.e., half of the memory space. Required Memory is specified in bits 15 – 12 in the Device Type register at offset 02h.

m	Required Memory				*m*	Required Memory			
	A24		A32			A24		A32	
0	8	Mbytes	2	Gbytes	**8**	32	kbytes	8	Mbytes
1	4	"	1	"	**9**	16	"	4	"
2	2	"	512	Mbytes	**10**	8	"	2	"
3	1	"	256	"	**11**	4	"	1	"
4	512	kbytes	128	"	**12**	2	"	512	kbytes
5	256	"	64	"	**13**	1	"	256	"
6	128	"	32	"	**14**	512	bytes	128	"
7	64	"	16	"	**15**	256	"	64	"

Table 5-1. Relationship between the "*m*" Parameter and Required Memory

One of the four registers is the Offset register, which is needed only for devices using **A24** or **A32** address space. This 16-bit read/write register defines the base address of the device's **A24** or **A32**

operational registers. The *m+1* most significant bits of the Offset register provide the values of the *m+1* most significant bits of the device's **A24** or **A32** register addresses, where *m* is as defined in Table 5-1 above.

Static and Dynamic Configuration

A VXIbus system can have up to 255 devices. Therefore, eight bits define the device address, which is called the "Logical Address." The Logical Address can be "static" or "dynamic." A static address resides in an 8-bit switch register; a dynamic address resides in a write-only register. Setting the switch register to 255 (all **"1"**s) enables dynamic addressing. Any other setting enables static addressing, in which case the value held in the switch register is the Logical Address.

With the Logical Address set to 255, a device responds to accesses at address 255 only when the MODID line is asserted as a qualifier by the Slot-0 controller. After a new Logical Address is written to the device, the device responds to the new address independent of the state of the MODID line.

For data acquisition and control applications, dynamic configuration is an important concept. A system often contains more than one module of a given type, and it can be easy, and sometimes desirable, to swap positions of two modules after removing them from the mainframe. If dynamic configuration is not employed, one must make sure that the switch register is correctly set when inserting or re-inserting a device. Dynamic configuration greatly simplifies system setup, since the software can assure that the devices are located in the desired slots. Dynamic configuration also allows a system's Resource Manager to configure memory usage optimally in a system.

Communication Protocol

VXIbus allows communication over the backplane by either register-based or message-based protocols. With register-based protocol, the communication is via an 8-, 16- or 32-bit parallel path directly to I/O registers within the modules. With message-based protocol, an ASCII interpreter is included on each module, and the binary representations of ASCII characters are transmitted over the backplane. The advantage of message-based protocol is that English-like commands and responses can be used.

High-performance data acquisition and control modules are usually register-based because the data throughput is usually several orders of magnitude greater than with message-based devices. All KineticSystems VXIbus devices are register-based.

Register Addressing

The user assigns each device in a VXIbus system a unique number between 1 and 254. This 8-bit number, called the Logical Address, defines the base address for the VXIbus device registers located on the module. Each device has a 64-byte block of memory reserved for these registers. The memory blocks, called configuration space, are located in the upper 16 kbytes of the 64-kbyte **A16** address space.

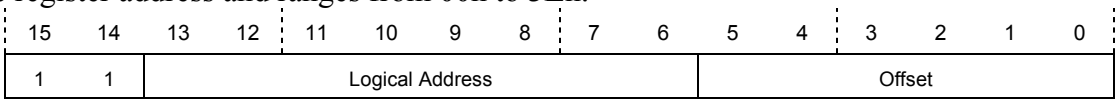
Every device has at least three configuration registers: ID / Logical Address, Device Type, and Status / Control. Modules using **A24** or **A32** addressing must also have an Offset register. The rest of the 64-byte block can contain registers or memory appropriate for the operation of the specific device.

A device's Logical Address occupies bits 13 - 6 of the register address. Bits 15 and 14 of the address are both **"1**'s,**"** and the base address of the register block is therefore:

***V**40h+C000h**

where *V* is the Logical Address of the device and **C000**h is the starting address of the top 16-kbyte block.

The address of a specific register is the base address plus an offset address. The offset is bits 5 - 0 of the register address and ranges from **00**h to **3E**h.



The V246 also uses *operational* registers in **A24** space; therefore, it is an "Extended" register-based device.

Required Configuration Registers

The four required VXIbus registers are ID / Logical Address; Device Type; Status / Control; and Offset. You can access these registers by **D16** transfers only.

ID Register *00h*

This read-only register returns **4F29**h.

Fields are Device Classification, Addressing Mode and Manufacturer ID.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1
	Class = Extended		**Addressing Mode = A24**		**KineticSystems' Manufacturer ID = F29h (3881)**											

Device Classification *Bits 15 and 14*

00 Memory device
01 Extended device
10 Message-based device
11 Register-based device

The V246 is an *Extended device.*

Addressing Mode *Bits 13 and 12*

00 A24
01 **A32**
10 Reserved
11 **A16**

The V246 uses *A24 addressing*.

Manufacturer ID *Bits 11 through 0*

KineticSystems' Manufacturer ID is *3881*, which corresponds to **F29**h.

Logical Address Register *00h*

This write-only register holds the Logical Address. In systems using Dynamic Configuration, the system Resource Manager uses this register to set the Logical Address of the device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	Not Used								Logical Address							

Logical Address *Bits 7 through 0*

Device Type Register *02h*

This read-only register contains the Required Memory and Model Code for the V246. It returns 9246h.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	0	0	1	0	0	1	0	0	1	0	0	0	1	1	0
	Required Memory				**Model Code = 246h**											

Required Memory *Bits 15 – 12*

A value of 9h indicates that the V246 uses 16 kbytes of **A24** memory space. Refer table 5-1 to understand the relationship between this 4-bit field and Required Memory.

Model Code *Bits 11 – 0*

The model code for the V246 is 246h.

Status Register *04h*

This read-only register provides binary information about the status of the V246.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	A24 Active	MODID*	Not Used										Ready	Not Used		Soft Reset

A24 Active *Bit 15*

"**1**" in this field indicates that you can access the **A24** registers of the V246. This bit reflects the state of the "**A24** Enable" bit of the Control register.

*MODID** *Bit 14*

MODID* is a low-true signal. A "**1**" read in this field indicates that the V246 is *not* selected via the P2 MODID line. A "**0**" indicates that the device *is* selected by a high state on the P2 MODID line. The Resource Manager uses this bit to configure the V246 dynamically.

Not Used *Bits 13 - 4*

These bits are not used and are each read as **"1."**

Ready *Bit 3*

"**1**" in this field indicates that the registers have been successfully initialized. The V246 is ready for access.

Not Used *Bits 2 & 1*

These bits are not used and are each read as **"1."**

Soft Reset *Bit 0*

"**1**" in this field indicates that the V246 is in a *reset* state. While in this state, the V246 allows access to its Configuration registers only.

Control Register *04h*

This write-only register causes execution of specific actions by the V246.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write-only	A24 Enable	Not Used														Soft Reset

A24 Enable *Bit 15*

Setting this bit to "**1**" enables access of the **A24** registers of the V246.

Soft Reset *Bit 0*

Setting this bit to "**1**" forces the V246 into a Reset state. In the Reset state, the module only allows access to its Configuration Registers.
Writing a "**0**" to this bit causes the module to begin its Self-test. In the Self-test state, the module allows access to its Operational registers only after the Ready bit in the Status register is set.

Offset Register *06h*

This read/write register determines and reports the device base address in **A24** memory space.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Base Address in A24 memory space										0	0	0	0	0	0

The V246 requires 16 kbytes of the 16-Mbyte **A24** memory space. Therefore, the Required Memory parameter, ***m***, in the Device Type register is 9 (See Table 5-1 on page 29.). The values written to the 10 (m+1=10) most significant bits of this register are the values of the 10 most significant bits of the device base address in **A24** memory space. The 6 least significant bits of the Offset register are meaningless. The actual base address is the above value in bits 15-6 shifted left 8 bits.
The Resource Manager uses this register to configure system memory as it sees fit.

Additional Configuration Registers

Additional configuration registers in **A16** space are:

- Attribute register
- Serial Number High & Low registers
- Version Number register
- Interrupt Status register
- Interrupt Control register
- Subclass register
- Suffix High & Low registers, and
- fourteen EEPROM user registers.

Note that you can access these registers by **D16** transfers only.

Attribute Register *08h*

This read-only register provides low-true information about the V246's interrupt handling capabilities. A read of this register returns FFFAh.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
	Reserved													**Interrupt Capability***	**Interrupt Handler Control***	**Interrupt Status Reporting***

Reserved *Bits 15 - 3*

These bits are reserved for future use and return **"1"**s when read.

*Interrupt Capability** *Bit 2*

"**0**" signifies that the V246 is capable of generating interrupts.

*Interrupt Handler Control** *Bit 1*

"**1**" indicates that the V246 is *not* capable of Interrupt Handler Control.

*Interrupt Status Reporting** *Bit 0*

"**0**" indicates that the V246 has Interrupt Status Reporting capability.

Serial Number Register *0Ah, 0Ch*

The read-only Serial Number registers (high and low words) store the 32-bit hexadecimal value of the V246's decimal serial number.

0Ah

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	SN7				SN6				SN5				SN4			

High word

0Ch

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	SN3				SN2				SN1				SN0			

Low word

Version Number Register *0Eh*

This read-only register gives the hardware and firmware revision numbers of the module.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	Firmware Version				Firmware Revision				Hardware Version				Hardware Revision			

Firmware Version ***Bits 15 - 12***

Firmware Revision ***Bits 11 - 8***

Hardware Version ***Bits 7 - 4***

Hardware Revision ***Bits 3 - 0***

Each field is a four-bit integer indicating the version or revision number.

Reserved *10h, 12h, 14h, 16h, 18h*

These five read-only registers are reserved for future use. They return FFFFh when read.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Interrupt Status Register *1Ah*

This read-only register provides information about the states of the two interrupt sources. It can be used for polling of interrupts. Interrupt bits are cleared by a read of this register or by an interrupt-acknowledge cycle.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	Not Used						Overlap Detect	Excitation Alarm	1	1	1	1	1	1	1	1
							Interrupt Sources						**Reserved / Logical Address**			

Not Used *Bits 15 - 10*

These bits are read as "**0**"s.

Interrupt Sources *Bits 9 - 8*

A "**1**" in either of these bit locations indicates that an action has occurred that can generate an interrupt.

Bit		Interrupt Source Description
9	**Overlap Detect**	Indicates that an Overlap condition occurred, signifying that more than one signal conditioning module accessed the MUX-bus in the same time slot. Refer to the Scan RAM section of this manual for trouble-shooting assistance.
8	**Excitation Alarm**	Indicates that an Excitation Alarm was generated. Read the Channel Alarm register (04h in **A24** space) to determine which channel caused the alarm.

Table 5-2. Sources of Interrupts

Reserved / Logical Address *Bits 7 - 0*

During a read, these bits return all **"1's."** During an interrupt acknowledge cycle, these bits return the Logical Address of this V246.

Interrupt Control Register *1Ch*

The read/write register contains mask bits for each of the two interrupt sources, a bit for disabling of interrupts and three bits that determine interrupt level.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Not Used						Overlap Detect	Excitation Alarm	Interrupt Enable*	1	Interrupt Req. Level			1	1	1
							Interrupt Mask bits									

Not Used *Bits 15 - 10*

These bits are read as "**0**"s.

Interrupt Mask Bits Bits 9 - 8

Writing a "**1**" one of these bits *prevents* the corresponding interrupt source from generating an interrupt request. Writing a **"0"** enables an interrupt source to generate an interrupt request.

Interrupt Enable Bit 7

Writing a "**1**" to this bit disables interrupt generation. Writing a **"0"** enables interrupt generation.

Not Used Bits 6 and 2 – 0

Bits 6 and 2 – 0 are not used and return **"1"**s when read.

Interrupt Request Level Bits 5 - 3

These bits determine the interrupt request level.

Bits			Interrupt Request Level
5	4	3	
0	0	0	IRQ7
0	0	1	IRQ6
0	1	0	IRQ5
0	1	1	IRQ4
1	0	0	IRQ3
1	0	1	IRQ2
1	1	0	IRQ1
1	1	1	Disconnected

Table 5-3. Interrupt Request Levels

Subclass Register 1Eh

This read-only register provides information about the Subclass of the VXIbus device.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
	Extended Device	**Extended Register-based Device**														

Bit 15 indicates that the V246 is a VXIbus-defined Extended Device.
Bits 14 through 0 indicate that the V246 is an Extended Register-based Device.

Suffix Register *20h, 22h*

The Suffix read-only registers (high and low words) hold the ASCII codes for the four characters of the V246's suffix. The suffix defines the optional characteristics of the module.

20h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	1	0	0	x	0	1	x	0	1	0	0	0	x	x	x

ASCII code for B or K = 42h or 4Bh (1st character) **ASCII code for A, B, C, D, E or F = 41h, 42h, 43h, 44h, 45h or 46h (2nd character)**

High Word

22h

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read-only	0	0	1	1	0	0	x	x	0	0	1	1	0	0	x	x

ASCII code for A or B = 41h or 42h (3rd character) **ASCII code for 1, 2 or 3 = 31h, 32h or 33h (4th character)**

Low Word

The suffix options for the V246 are:

1st character: Filter type

"B" indicates that the filters are 6-pole Bessel.
"K" indicates that the filters are 6-pole Chebyshev.

2nd character: Front-end option

	Trifilar transformers	Bridge completion
A	yes	no
B	yes	120-ohm
C	yes	350-ohm
D	no	no
E	no	120-ohm
F	no	350-ohm

3rd character: Simultaneous sampling options

"1" indicates no simultaneous sampling.
"2" indicates simultaneous sampling capability.

4th character: Revision level

The number, **"1," "2" or "3,"** etc., gives the revision level.

User Defined Registers *24h - 3Eh*

Fourteen read/write registers allow you to store any data you wish. The registers are EEPROM, so the data will not disappear until you over-write it.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write																

Note that when a register is written, a minimum of 3 ms must pass before *any* User-Defined register may be read or written.

Operational Registers in A24 Space

The following operational registers are in a block of memory in **A24** space, beginning at the starting address specified by the Offset register in **A16** configuration space. The size of the block of memory is 16 kbytes. The hexadecimal addresses shown are the offset from the starting address. You can access these registers by **D16** transfers only.

The operational registers are:

- Configuration register 00h
- Calibration register 02h
- Channel Alarm register 04h
- Self-test register 08h
- Channel-specific registers
  (for channels n = 1 through 8)
  - Gain 10h – 80h
  - Filter 12h – 82h
  - Bridge Balance 14h – 84h
- Scan RAM 100h – 10FEh

Configuration Register 00h

This read/write register selects the trigger source for simultaneous sample and hold. It also allows the anti-aliasing filters to be switched in or out, puts the module in Setup or Run mode and indicates whether or not a MUX-bus channel overlap condition has occurred.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Not Used				Connector Type (read only)				Not Used	Overlap Ind.	Select/ Run	Filter Enable	Trigger Enable	S/H Trigger Select		

Connector Type Bits 11 – 8

Reading this field allows you to determine the Termination Assembly type and to verify that it is installed correctly.

Not Used Bits 15 - 12, Bit 7

These bits are not used and are read as **"1's."**

Overlap Indicator Bit 6

This bit indicates whether or not a **MUX-bus** overlap condition has occurred that involves this module. To clear this bit, you must write a **"0"** to it.

Run/Setup Bit 5

Write a **"0"** to select Setup mode, **"1"** to select Run. The module must be in Setup mode to load the Scan RAM.

Filter Enable Bit 4

The low-pass anti-aliasing filters can be in-the-circuit (enabled) or bypassed. Write a **"1"** to this bit to enable all eight filters, **"0"** to bypass them.

Trigger Enable *Bit 3*

Writing a **"1"** to this bit enables the selected trigger line. **"0"** disables the trigger.

S & H Trigger Select *Bits 2 - 0*

Bits 2 - 0 select a VXIbus trigger line that, when enabled via Bit 3, can trigger the eight-channel simultaneous sample-and-hold function.

Bits 2	1	0	VXIbus Trigger Line
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Table 5-4. VXIbus Trigger Line Selection

Not Used *Bits 15 – 12 and 7*

These bits are not used and are read as **"1's."**

Calibration Register *02h*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Reference Source	Not Used						Minus	Plus	0.2	0.5	1.0	0.001	0.01	0.1	1.0
								Calibrator Polarity		**Stage-one Multiplier**			**Stage-two Multiplier**			

Reference Source *Bit 15*

A reference source is available on-board or via the **MUX-bus**. Write a **"1"** to bit 15 to select the on-board source, **"0"** to select the **MUX-bus** source.

Not Used *Bits 14 – 9*

These bits are not used and are read as **"1's."**

Calibrator Polarity *Bits 8 – 7*

This field is used to specify calibrator polarity. Write a **"1"** to only one of these two bits. A **"1"** to bit 7 selects positive polarity, **"0"** selects negative polarity.

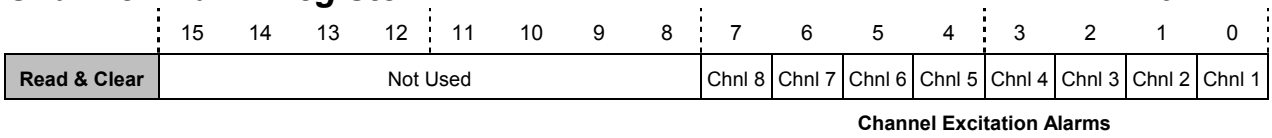
Stage-one Multiplier *Bits 6 – 4*

The on-board calibrator is a precision active attenuator connected to the 10-volt reference source. Write a **"1"** to only one of these three bits. A **"1"** to bit 6 selects a gain of 0.2, bit 5 selects 0.5, and bit 4 selects 1.0.

Stage-two Multiplier *Bits 3 – 0*

Stage 2 is a precision active attenuator connected to the output of stage 1. Write a **"1"** to only one of these four bits. Writing a **"1"** to bit 3 selects a gain of 0.001, to bit 2 selects a gain of 0.01, to bit 1 selects 0.1, and to bit 0 selects 1.0.

Channel Alarm Register *04h*



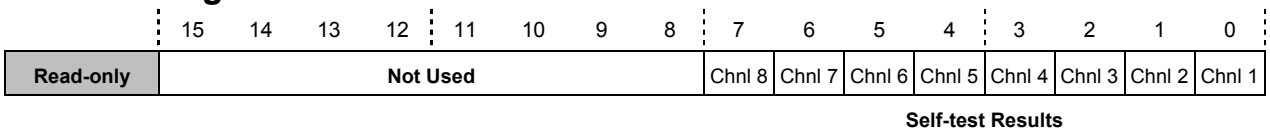
Not Used *Bits 15 – 8*

These bits are not used and are read as **"1's."**

Channel Excitation Alarms *Bits 7 - 0*

These bits indicate the status of each of the channel excitation alarms. **"1's"** indicate alarm conditions. Reading this register clears the alarm bits. *Note that the alarm status information becomes current by reading the Interrupt Status register at 1Ah in* ***A16*** *space.*

Self-test Register *08h*



Not Used *Bits 15 – 8*

These bits are not used and are read as **"1's."**

Self-test Results *Bits 7 - 0*

These bits indicate the status of the self-test for each channel. A **"0"** indicates that the self-test failed. A **"1"** indicates that it passed.

Channel-N Gain Registers (N = 1 – 8) *N0h*

There is one of these registers for each channel. The addresses are N0h, where N = 1 through 8. Note that you must wait 3 ms after writing to this register before attempting to access another register in this module. Writing to the V246 before 3 ms has elapsed may cause the contents of this register to change.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Not Used	Monitor	Local Sense	Bridge Configuration		15	10	5	2.5	x10	x5	x2	x1	x100	x10	x1
						Excitation				**2nd-stage Gain**				**1st-stage Gain**		

Not Used *Bit 15*

This bit is not used and is read as a **"1."**

Monitor *Bit 14*

Write a **"1"** to this bit to connect the monitor lines to the sense lines.

Local Sense *Bit 13*

Write a **"1"** to this bit to select local sense.

Bridge Configuration *Bits 12 – 11*

The bridge configuration can be full bridge, half bridge or quarter bridge. Writing **"00"** to this field selects full, **"01"** selects half, and **"10"** selects quarter bridge.

Excitation *Bits 10 – 7*

Write a **"1"** to no more than one of these bits. Write **"0's"** to all bits in this field to have no excitation voltage. Write a **"1"** to bit 7 to select 2.5 volts excitation, to bit 8 to select 5 volts, to bit 9 to select 10 volts, and to bit 10 to select 15 volts.

2nd-stage Gain *Bits 6 – 3*

Write a **"1"** to one, and only one, of these bits. Write a **"1"** to bit 3 to select a gain of 1, to bit 4 to select a gain of 2, to bit 5 to select a gain of 5, and to bit 6 to select a gain of 10.

1st-stage Gain *Bits 2 - 0*

Write a **"1"** to one, and only one, of these bits. Write a **"1"** to bit 0 to select a gain of 1, to bit 1 to select a gain of 10, and to bit 2 to select a gain of 100.

Channel-N Filter Register (N = 1 – 8) *N2h*

There is one of these registers for each channel. The addresses are N2h, where N = 1 through 8.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Not Used					Line Sense	+E Sense	–E Sense	Not Used		**Input MUX**		2 kHz	1 kHz	200 Hz	20 Hz
						Output MUX									**Filter**	

Not Used *Bits 15 – 11, 7 - 6*

These bits are not used and are read as **"1's."**

Output MUX *Bits 10 – 8*

The three bits in this field allow you to output either the channel (line) voltage or the excitation voltage, allowing you to calibrate the excitation. You can write a **"1"** to one, and only one, bit in this field.

Input MUX *Bits 5 – 4*

The input MUX is used to select the source for calibration. Four sources can be selected via this field: "00" selects Line, "01" selects an internal programmable calibrator voltage, "10" selects a known voltage via the front connector, and "11" selects a ground reference.

Filter *Bits 3 - 0*

Write a **"1"** to one, and only one, of the bits in this field. Note that the use of filters requires that bit 4 in the Configuration register (at address 00h in **A24** space) be set to **"1."** The values listed for filters are the "band-edge" values. Write a **"1"** to bit 0 to select 20 Hz, to bit 1 to select 200 Hz, to bit 2 to select 1 kHz, or to bit 3 to select 2 kHz.

Channel-N Bridge Balance Register (N = 1 – 8) *N4h*

There is one of these registers for each channel. The addresses are N4h, where N = 1 through 8.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	Shunt Calibration		Bridge Balance Polarity		Bridge Balance DAC Value											

Shunt Calibration *Bits 15 – 14*

Bits 14 and 15 control shunt calibration. When neither bit is asserted the bridge is unshunted. Writing a "1" to bit 14 or 15 causes the external shunt calibration resistor to be connected across one arm of the bridge or the other.

Bridge Balance Polarity *Bits 13 – 12*

Polarity is set by writing a "1" to one of the bits in this field. Write a "1" to bit 12 for negative polarity or to bit 13 for positive polarity.

Bridge Balance DAC Value *Bits 11 - 0*

The bridge balance DAC is set via bits 0 - 11.

Scan RAM *100h - 10FEh*

The Scan RAM contains the scan table that must be set up properly on all **MUX-bus** modules. The Scan RAM is 256 words long, and the Scan Table is a subset of the Scan RAM. Each

module scans through its Scan Table sequentially at the ADC clock rate. The currently addressed data on the list specifies which module is to connect a channel to the **MUX-bus**.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read/write	End of List	Module Select	Not Used						Channel Numbers							

End of List *Bit 15*

You set this bit to a "**1**" to signify the end of the list.

Module Select *Bit 14*

This bit is not actually used in the V207. However, you use this bit the in signal-conditioning MUX modules to indicate which module applies its analog channel to the **MUX-bus** in that time slot.

Channel Numbers *Bits 7 - 0*

You use these bits to define the active channels and the order of scanning.
Before you can write the Scan Table into Scan RAM, you must put the V207 in "Setup" mode. The V207 (or any other module receiving the MUX-bus) should be the first device put in "Setup" mode and the last put in "Run" mode. The Scan RAM is organized the same on all modules, with the exception of the Module Select bit. Bits 0 - 7 specify the channel number (0-255). Bits 8 - 14 are not used in the V207 Scan RAM and should be filled with zeroes. Bit 15 is the End-of-List bit. This bit should be set in the last location of the Scan Table (i.e., the last active channel) on all MUX-bus modules.
Scan RAM reflects the list of active channels for a given application. There can be up to 256 ADC time slots for each period of the sample clock. The channels, each representing an ADC time slot, are multiplexed into four paths, with the channels being assigned to the paths as follows (Note that physical Channel 1 is defined as 0000 0000 in Scan RAM.):
MUX-bus Path A -- Channels 1, 5, 9…
MUX-bus Path B -- Channels 2, 6, 10…
MUX-bus Path C -- Channels 3, 7, 11…
MUX-bus Path D -- Channels 4, 8, 12…
This physical mapping of the channels causes certain restrictions on the organization of the Scan RAM to attain maximum system performance. The Scan RAM must be organized to allow acquiring consecutive samples from Path A, Path B, Path C, and Path D respectively. For example, consecutive entries in the Scan RAM should appear as follows:

Address	Data (bits 7 - 0)	Comment
200h	xxxx xx00	These channels are assigned to MUX-bus path A.
202h	xxxx xx01	These channels are assigned to MUX-bus path B.
204h	xxxx xx10	These channels are assigned to MUX-bus path C.
206h	xxxx xx11	These channels are assigned to MUX-bus path D.
208h	xxxx xx00	Repeat back to MUXbus path A, etc.

Appendices

About KineticSystems

KineticSystems Corporation designs, produces and markets high-performance data acquisition and control systems to a broad range of customers in aerospace, defense, automotive, scientific and other industrial markets.

The Leader in the Delivery of High-performance CAMAC-based Products

The company was founded in 1970 to develop and manufacture interface modules and associated products based on the international CAMAC standard. CAMAC, an acronym for Computer Automated Measurement and Control, is a set of specifications developed by a committee of the government-sponsored research laboratories (the NIM Committee). The committee's goal was to provide standardized modular building blocks for configuring a wide range of data acquisition and control systems. CAMAC, the first open-system real-time input/output (I/O) specification, later was accepted as a standard by the Institute of Electrical and Electronic Engineers (IEEE STD 583). We soon became the recognized leader in delivering high-performance CAMAC-based products. We have retained that leadership position.

Innovation with the CAMAC Serial Highway

As the need for large distributed data acquisition and control systems grew, the NIM Committee produced specifications for the CAMAC Serial Highway to allow communication between a host computer and CAMAC I/O chassis over some distance. In 1975, we delivered the first CAMAC Serial Highway computer interface. We soon were recognized as the leader in the delivery of Serial Highway system components. Serial Highway innovations included a block-mode protocol that increased data throughput by a factor of 10 and fiber-optic highway interfaces that allow the CAMAC chassis to be separated by up to 2 kilometers at full data rate. We continue to be an innovator in the field of high-performance data acquisition.

H•TMS, a Turn-key Testing Solution, Added to Our Product Range

In 1991, we purchased the H•TMS (High-performance Test Management System) product line. H•TMS is a modular set of microprocessor-based hardware and software components that delivers functions usually found in several instruments and a computer. H•TMS increases testing productivity and provides solutions to key problems encountered by test engineers and managers. The addition of this product line provides the answer for customers who need a turnkey testing solution.

A Major Player in VXIbus, a Rapidly Growing Interface Standard

VXIbus is a standard (now IEEE STD 1155) developed by the major instrumentation manufacturers to allow customers to move from chassis-type instruments to computer-interfaced modular building blocks. In 1992 we embraced the relatively new VXIbus standard. Using our extensive CAMAC experience, we soon produced 35 VXI modules for data acquisition and control. As the VXI market has grown to several hundred million dollars, we continue our innovations with additional high-performance products. This includes the development of a set of products called the Grand Interconnect™. These products allow VXI chassis to be distributed on a fiber-optic highway. CAMAC and mixed VXI/CAMAC chassis are also supported. We are an active member of the VXI *plug&play* Systems Alliance, an organization that promotes standards that make VXI easier to configure and to use.

KineticSystems Today

Our headquarters and factory facilities in Lockport, Illinois, have grown to 70,000 square feet. We also have an operation in Englewood, Colorado, and six domestic sales offices, including the Lockport facility. We have distributors in 17 other countries. VXI, CAMAC and H•TMS continue to be our major product lines.

Today, an increasing number of customers are demanding the delivery of data acquisition and control solutions, not just products. For many years we have provided software drivers for our products to make them easier to use. We have an active program to develop VXI *plug&play* instrument drivers for our range of VXI modules. We have developed a high-performance software application program called Reality®. Distributed VXI and/or CAMAC systems can be configured using this software. By using UNIX workstations and powerful I/O control computers, a high I/O performance can be achieved that is not available with any other general-purpose software package. Additionally, to achieve more complete solutions, we provide integration services.

KineticSystems is ideally suited to meet customers' needs as we approach the twenty-first century. We have extensive experience in the design, manufacture and delivery of high-performance data acquisition products and systems. Even though the demand for standards-based products has only recently become a high priority, we have the experience with such products since 1970.

Ways to contact us:

KineticSystems Company, LLC
900 N. State Street
Lockport, IL 60441-2200

Phone: 1-800-DATA NOW (1-800-328-2669)
(815) 838-0005
Fax: (815) 838-4424

E-mail: mkt-info@kscorp.com
tech-serv@kscorp.com
sales@kscorp.com
Web: http://www.kscorp.com

Warranty

KineticSystems warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. KineticSystems warrants its software products to conform to the software description applicable at the time of purchase for a period of ninety days from the date of shipment. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty. KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems are prepaid by the purchaser, while charges for returning the repaired product to the purchaser, if located in the United States, are paid by KineticSystems. Return shipments are made by UPS, where available, unless the purchaser requests a premium method of shipment at his expense. The selected carrier is not the agent of KineticSystems, and KineticSystems assumes no liability relating to the services provided by the carrier.

The product warranty may vary outside the United States or Switzerland and does not include shipping, customs clearance or any other charges. Consult your local authorized representative for more information regarding specific warranty coverage and shipping details.

KineticSystems specifically makes no warranty of fitness for a particular purpose or any other warranty either expressed or implied, except as is expressly set forth herein. This warranty does not cover product failures created by unauthorized modifications, product misuse or improper installation.

Products are not accepted for credit or exchange without prior written approval. If it is necessary to return a product for repair replacement or exchange, a Return Authorization (RA) Number must first be obtained from the Repair Service Center before shipping the product to KineticSystems.

Please take the following steps if you are having a problem and feel you may need to return a product for service:

1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include with the product a description of the problem and the name of the technical contact person at your facility.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

   KineticSystems Company, LLC
   Repair Service Center
   900 North State Street
   Lockport, IL 60441

   Telephone: (815) 838-0005
   Fax: (815) 838-4424

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Feedback

The purpose of this manual is to provide you with the information you need to make the V246 as easy as possible to understand and use. It is very important that the information is accurate, understandable and accessible. To help us continue to make this manual as useful as possible to you, we hope you will fill out this form and Fax it back to us at (815) 838 0095. Or mail a copy to Technical Services Dept., KineticSystems Company, LLC, 900 N. State, Lockport, IL 60441. Your input is very valuable.

Please rate each of the following.

The information in this manual is:

	Yes									**No**
Accurate	10	9	8	7	6	5	4	3	2	1
Readable	10	9	8	7	6	5	4	3	2	1
Easy to find	10	9	8	7	6	5	4	3	2	1
Well organized	10	9	8	7	6	5	4	3	2	1
Sufficient	10	9	8	7	6	5	4	3	2	1

We would appreciate receiving any thoughts you have about how we can improve this user's manual:

(Include additional sheets if needed)

Name **Phone**

Company