Model V252-Zxx2
8 or 16-channel, 8-Pole Analog Filter
w/Programmable Gain and
Simultaneous Sampling
INSTRUCTION MANUAL

October 12, 1999

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FIGURES

TABLES

8 or 16-channel, 8-pole Analog Filter

Provides high filter roll-off for excellent anti-alias filtering

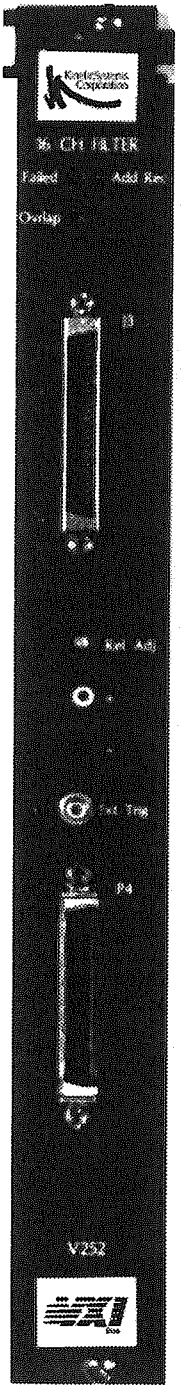
V252

Features

- **8 or 16 differential channels**
- **8-pole low-pass filters with plug-in headers provided by factory option: 10 Hz to 100 kHz in a 1,2,5, .. progression**
- **Optional programmable gain per channel**
- **Optional simultaneous sampling**
- **Output available at front panel or MUX-bus™**

Typical Applications

- **Shock/vibration tests**
- **Rocket engine testing**
- **Wind tunnel data acquisition**



General Description *(Product specifications and descriptions subject to change without notice.)*

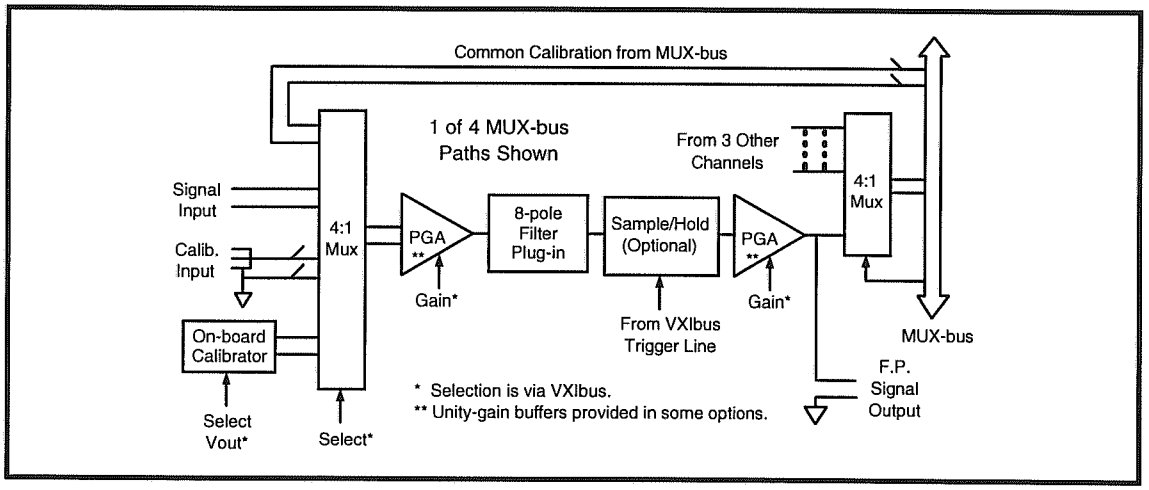
The V252 is a single-width, C-size, register-based, VXIbus module that contains 8 or 16 channels of fixed-frequency, low-pass filtering. Each differential input signal is received by an instrumentation amplifier which provides a high common mode rejection ratio. The V252-ZA12 and -ZC12 options provide filtering at unity gain. Pre-filter gains of 1, 10, and 100 as well as post-filter gains of 0.5, 1, 2, 5, and 10 are provided on the V252-ZB12 and -ZD12 options. The selection of gain is programmable on a channel-by-channel basis.

Eight-pole, low-pass, Bessel, Butterworth, Elliptic, or Constant-delay filters may be selected for each channel. This module is capable of providing filter cutoff frequencies from 10 Hz to 100 kHz. Cutoff frequencies are established by plug-in filter headers. These headers must be ordered separately. Standard headers provide nominal cutoff frequencies from 10 Hz to 100 kHz in a 1, 2, 5, ... progression. Please consult the factory regarding the availability of other cutoff frequencies by special order.

This filter module is also available with an optional sample/hold amplifier per channel. This option provides for simultaneous sampling of all channels by using the VXI trigger lines. Input and output signals appear at the V252 front panel on 68-contact High Density connectors. The differential input signals are brought in via one of these connectors, and the filtered output pairs use a second connector. The output signals are also available as four multiplexed channels on the VXI Local Bus for the V207 or V208 ADC using the KineticSystems MUX-bus™ protocol.

Calibration inputs are provided via a host ADC reference from the VXI Local Bus or from an on-board reference. The calibration signals may be selectively placed on any channel. A Calibration Register is used to select the desired channel.

The V252 supports both static and dynamic configuration. It may by accessed using A24/A16, D16 data transfers.



Item	Specification
General	
Number of channels	8 or 16 differential input
Gain ranges (-ZB12 and -ZD12 options)	0.5, 1, 2, 5, 10, 20, 50, 100, 200, 500, 1000
Standard cutoff frequencies	10 Hz, 20 Hz, 50 Hz, 100 Hz, 200 Hz, 500 Hz, 1 kHz, 2 kHz, 5 kHz, 10 kHz, 20 kHz, 50 kHz, and 100 kHz
Cutoff frequency accuracy	±1%
Gain match	±0.3 dB maximum at f_c
Phase match	±0.2 dB maximum, dc to 0.8 f_c ±3.0° maximum at f_c
Passband ripple (typical)	±2.0° maximum, dc to 0.8 f_c Bessel, Butterworth: 0.0 dB Elliptic: 0.035 dB Constant Delay: 0.15 dB
Input	
Input range	Differential: ±10 V Common mode: ±10 V
Input protection	±35 V continuous
Input impedance	20 MΩ minimum
Transfer Characteristics	
Linearity error	±0.005% FSR maximum
Initial accuracy	After automatic calibration using the on-board reference: G=1 to 5 ±(50 µV + 0.02% of reading) G=10 to 50 ±(50 µV + 0.03% of reading) G=100 to 1000 ±(20 µV + 0.1% of reading)
Offset stability, RTI	2 µV/°C maximum at G=500
Gain stability	20 ppm/°C maximum
Bandwidth	G=1 to 100 200 kHz G=200 to 1000 20 kHz Sample/Hold Options 50 kHz
Common mode rejection	-100 dB typical, -80 dB minimum
Noise, RTI	5 µV RMS maximum at G=500
Channel-to-channel crosstalk	-90 dB minimum at fc
Output	
Output range	±10 V
Output current	5 mA maximum
Output resistance	100 Ω maximum
I/O Connector Type	68P High Density (input), 68S High Density (output)

Power Requirements (with 16 filters)	ZA12	ZB12	ZC12	ZD12	ZA22	ZB22	ZC22	ZD22
+5 V	3.3A	3.3A	3.3A	3.3A	2.9A	2.9A	2.9A	2.9A
+24 V	750mA	750mA	1.1A	1.15A	415mA	440mA	595mA	620mA
-24 V	750mA	780mA	1.1A	1.15A	385mA	410mA	570mA	595mA

Environmental and Mechanical	
Temperature range	
Operational	0°C to 50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to +40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Please note that a complete filter module consists of a V252-Zxy2 main board plus P708-wxyz series filter headers (16 P708s for the 16-channel V252 options or 8 P708s for the 8-channel V252 options)..

Model V252-ZA12 16-channel, 8-pole Analog Filter
Model V252-ZB12 16-channel, 8-pole Analog Filter with Programmable Gain
Model V252-ZC12 16-channel, 8-pole Analog Filter with Simultaneous Sampling
Model V252-ZD12 16-channel, 8-pole Analog Filter with Programmable Gain and Simultaneous Sampling
Model V252-ZA22 8-channel, 8-pole Analog Filter
Model V252-ZB22 8-channel, 8-pole Analog Filter with Programmable Gain
Model V252-ZC22 8-channel, 8-pole Analog Filter with Simultaneous Sampling
Model V252-ZD22 8-channel, 8-pole Analog Filter with Programmable Gain and Simultaneous Sampling

Filter Plug-ins

Model P708-wxyz Filter Plug-in (16 required for V252-Zy12, 8 required for V252-Zy22).

w: Filter type: B = Bessel, T = Butterworth, D = Constant Delay, E = Elliptic

xyz: Cutoff Frequency:

100 = 10 Hz	501 = 500 Hz	203 = 20 kHz
200 = 20 Hz	102 = 1 kHz	503 = 50 kHz
500 = 50 Hz	202 = 2 kHz	104 = 100 kHz
101 = 100 Hz	502 = 5 kHz	
201 = 200 Hz	103 = 10 kHz	

Please consult the factory for additional cutoff frequency options.

Example: A Model V252 16-channel Filter module with programmable gain, no simultaneous sampling and 8-pole, Elliptic filters with a 10 kHz cutoff frequency on all 16 channels would be ordered as:

Quan 1	V252-ZB12
Quan 16	P708-E103

Related Products

Model V207 16-bit, 500,000 Sample/second ADC Subsystem
Model V208 16-bit, 100,000 Sample/second ADC Subsystem
Model 5868-Axyz Cable—68P High Density to Unterminated
Model 5868-Bxyz Cable—68S High Density to Unterminated
Model 5868-Cxyz Cable—68P High Density to 68P High Density (V252 output to V765)
Model 5868-Dxyz Cable—68S High Density to 68P High Density (V765 to V252 input)
Model 5868-Exyz Cable—68S High Density to 68S High Density
Model V752-ZB11 Termination Assembly for V252
Model V765-ZA11 Rack-mount Termination Panel

UNPACKING AND INSTALLATION

At KineticSystems, static precautions are observed from production, test, and packaging of the module. This includes using static proof mats and wrist straps. Please observe these same precautions when unpacking and installing the module whenever possible.

The Model V252 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the logical address switches to the appropriate value.

Configuration

There is one set of user configurable switches on the V252. All eight switches, #1 (msb) to #16 (lsb), are for the logical address. The logical address may be set from 0 to 254 as a statically configured device. If the module is set for logical address 255 (all switches open), then the V252 will be dynamically configured by the resource manager. Logical address 255 is the factory default setting. (See Figure 1, page 5)

Installing Filter Bricks

Eight-pole, low-pass Bessel, Butterworth, Elliptic, or Constant Delay filters may be installed for each channel. Channels 9 through 16 are available on V252-Zx12 options only. If the filters are purchased at the same time as the module, the filters bricks are installed and tested as one unit. If the filter bricks are bought separately, a strap must be removed at that channel before the filter brick may be inserted. (See Figure 1, page 5)

Overlap Enable

Overlap detect is factory set to the enabled position (across pins 1 and 2). Overlap detect may be disabled by moving the strap across pins 2 and 3. (See Figure 1, page 5)

Model V252-Zxx2

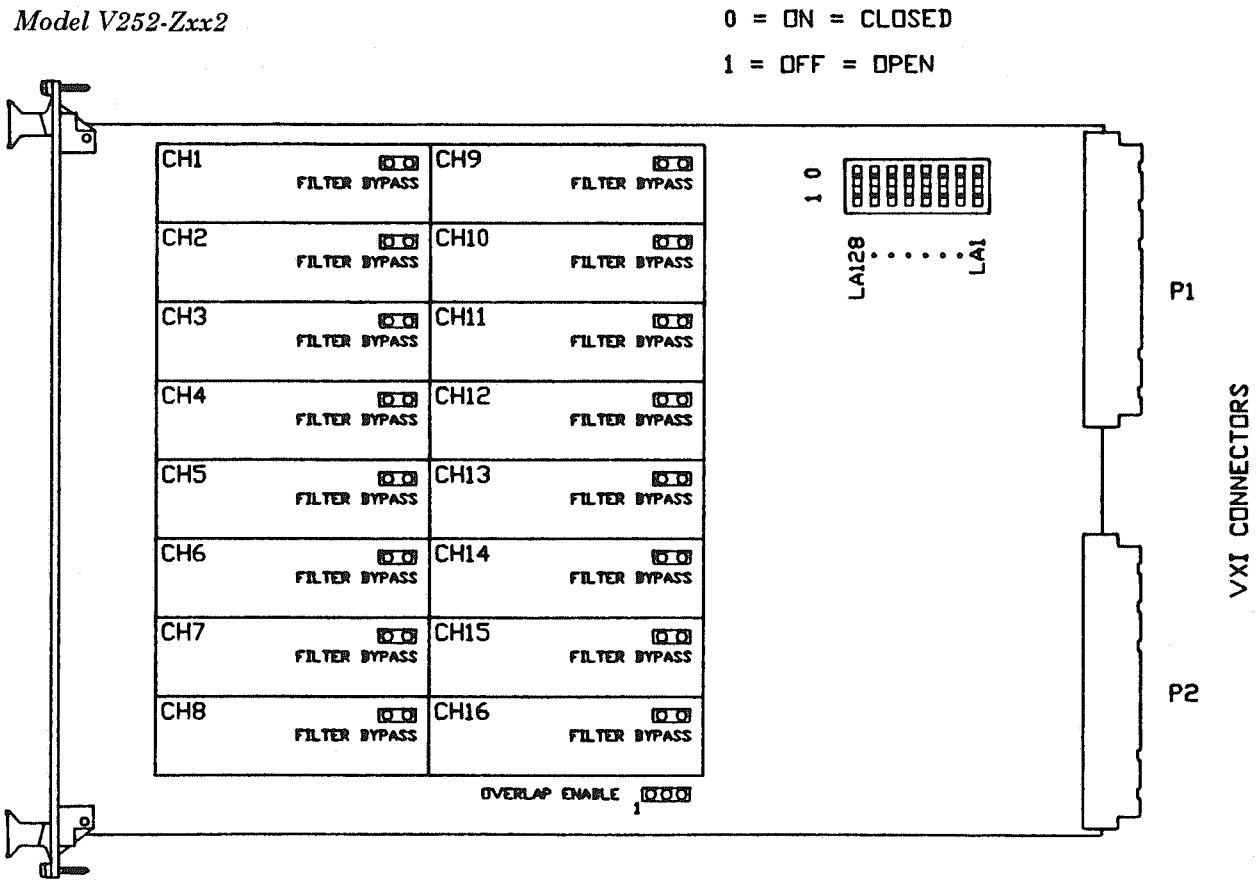


FIGURE 1 - V252 Switch Locations

Module Insertion

The V252 is a C-sized, single width, VXIbus module. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame. Since the V252 is a signal conditioning module that uses MUXbus, this module must be plugged into the crate only to the right of the V207 (or any other ADC module using MUXbus) in order to use MUXbus.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

To insure proper interrupt acknowledge cycles from the V252 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a

slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V252 and the Slot 0 Controller.

FRONT PANEL DESCRIPTION

LEDs

After power up the Failed LED will be on for at most five seconds while self tests are being run. If the Failed LED stays on after five seconds, then the self test failed. When the self test is complete, Add Rec and Overlap LEDs will be off. The Add Rec (address received) LED lights to indicate the V252 is being accessed through VXI. The Overlap (overlap detect) LED will light to indicate that another module tried to output its voltage out on the MUXbus at the same time the V252 did.

Connectors

The V252 has two 68 pin, high density SCSI type connectors. The P4 connector has the differential inputs with an individual guard per channel as well as a front panel calibration input and an external, negative edge, TTL level sample hold signal. The J3 connector has the differential outputs as well as a calibration output. See Figure 2 and TABLE 2 (Page 24) for the precise pinout descriptions. The front panel calibration voltage can be brought in through the P4 connector. The "on board" calibration voltage can be calibrated by adjusting the voltage through the pot labeled Ref Adj (Reference Adjust) on the front panel. The "on board" voltage can be monitored through the connectors labeled "+" and "-".

PROGRAMMING INFO

VXIbus Addressing

The V252 is classified as an extended register device which means it has registers that occupy A16 and A24 space.

The configuration registers are located in A16 space and include the standard registers defined by VXI as well as additional registers to help identify the module. The additional register defined by KineticSystems is the Suffix Register. The Suffix Register includes the model suffix number which indicates the model option. The User Defined Registers at the end of the configuration space can also be used to identify the module (i.e., with an internal identification number). The operational registers are located in A24 space and include the registers specific to V252 modules.

Appendix A includes a C/C++ code example using NI-VXI routines with V252. It includes codes which will use the configuration registers to help identify the specific module and access both configuration and operational registers.

Resetting the V252

The V252 can be put into soft reset by setting the Reset bit of the Status Control Register. Once taken out of soft reset, the module will initiate self test.

Self Tests

During self test, each channel's path is checked at unity gain. If the gain option is available, self tests are performed on options that can be tested using the Self Test and Calibration Register. If the sample hold option is available, a functional test is performed on the sample hold card.

NOTE:	**DURING SELF TEST, SCAN RAM IS OVERWRITTEN. ALL OTHER REGISTERS WILL REMAIN UNCHANGED EXCEPT THE V252 WILL BE TAKEN OUT OF RUN MODE.**

If the Scan RAM passes the self test, it is automatically configured to work with the first 8 or 16 channels of the V207. In the case where one V252 is used with one V207, the ADSEL bit in the Configuration Register need only be set (put in Run Mode). In any case, it may be read in order to see how Scan RAM is used on V252 to work with V207.

Should self test fail, the following registers may be accessed to find where the V252 failed self tests.

1.) Sample Hold and Scan RAM test results are located in the Calibration Register ($ 0x02).

2.) If Scan RAM tests passed, gain results are listed in Scan RAM starting at 0x200. If the value at 0x200 equals 0x4000, Scan RAM is setup for the V207 and gain passed. If the value at 0x200 does not equal 0x4000, Scan RAM includes a list of gain settings that failed in the following order:

   A.) Value in all channels Gain Register when test failed.
   B.) Value in Calibration Register when test failed.
   C.) Value read from Self Test Register.

D.) Value equals 0xFFFF to indicate end of the list or another gain failed and the list is repeated starting at step A.

Channel Setup

The V252-ZBx2 and the V252-ZDx2 has two separate gain stages. The first gain stage is applied before the filter and is controlled by bits 1 and 0 of each channel's Gain Register. First stage gain may be set to 1, 10, or 100. The second stage gain is applied after the filter and is controlled by bits 3-5 of each channel's Gain Register. Second stage gain ranges from .5 to 10.0 with a total of five different choices. All other options are hardwired for unity gain.

Once calibration is completed, the input of each channel can be selected to connect to the 68 pin, high density, SCSI II type connector (P4). It is set by writing zeros to bits 7 and 8 of each channels Gain Register.

MUXbus

The MUXbus makes use of the VXI P2 connector lines LBUSC00 - LBUSC11 on this module. Signal conditioning modules supporting the MUXbus may be plugged into the crate only to the right of the V207 (or any other ADC module using MUXbus).

The MUXbus pin definition (P2) is:

LBUSC00 MUX path A signal hi

LBUSC01 MUX path A signal lo

LBUSC02 MUX path B signal hi

LBUSC03 MUX path B signal lo

LBUSC04 MUX path C signal hi

LBUSC05 MUX path C signal lo

LBUSC06 MUX path D signal hi

LBUSC07 MUX path D signal lo

LBUSC016 Reference Hi

LBUSC09 Reference Lo

LBUSC10 Overlap Detect

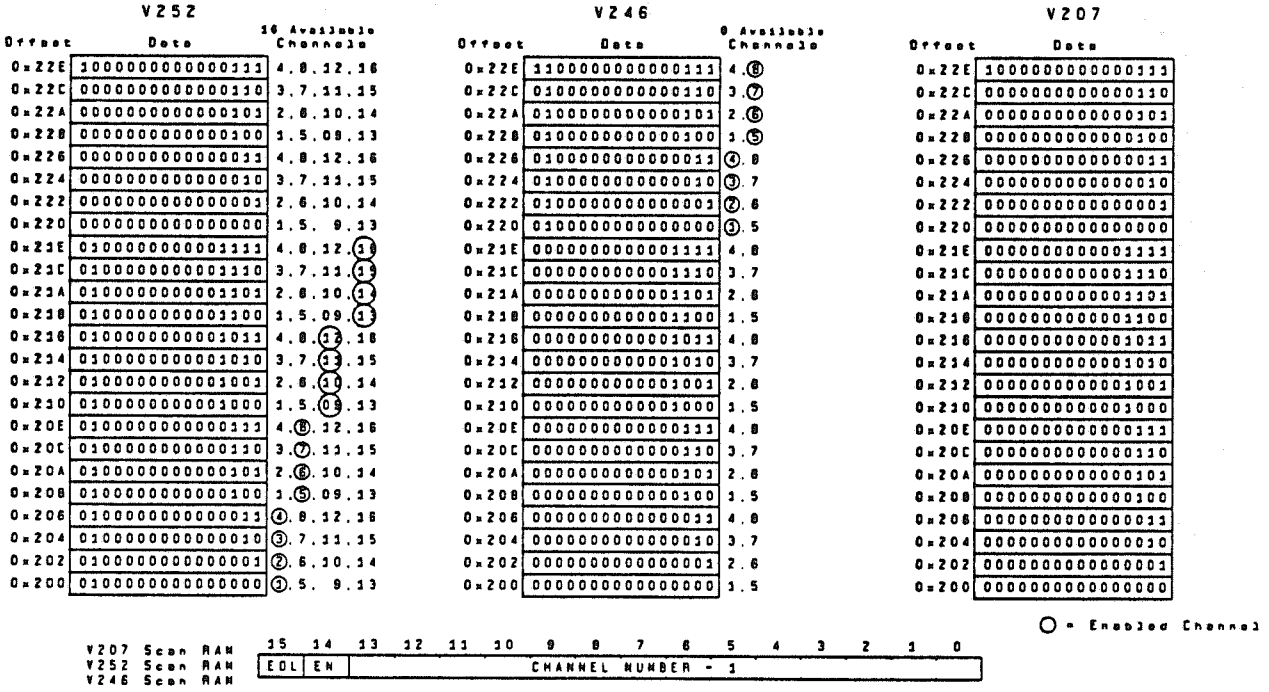
LBUSC11 MUXBUS CLOCK

The MUXbus clock generates the control signal that causes the output multiplexers on the signal conditioning modules to increment to the next channel.

Reference Hi and Reference Lo provide +10 volt differential signal to adjacent signal conditioning modules, allowing all channels to be referenced to a common standard. This greatly simplifies system calibration.

Overlap Detect is used by the signal conditioning modules to detect if two or more modules are attempting to output their voltages at the same time. This helps prevent conflicts caused by an incorrectly programmed Scan RAM.

FIGURE 2 - Scan RAM/Scan Table Example



For this example: (Refer to Figure 2)

ADC clock rate must be less than or equal to 500kHz / 24 channels
Let ADC clock rate = 20kHz, t_{ADC} = 1 / 20kHz = 50 uS.

Every 50 uS:

1.) All modules read Scan RAM location 0x200.
V252 outputs its channel 1 voltage.
V246 waits.
V207 reads its channel 1 voltage.

2.) All modules read Scan RAM location 0x202.
V252 outputs its channel 2 voltage.
V246 waits.
V207 reads its channel 2 voltage.

.
.
.

24.) All modules read Scan RAM location 0x21E.
V252 reads end of list bit, waits for next tick of ADC clock.
V246 outputs its channel 16 voltage, reads end of list bit, waits for next tick of ADC clock.
V207 reads its channel 24 voltage, reads end of list bit, waits for next tick of ADC clock.

Scan RAM

NOTE:	As a general rule, the V207 or any other receiving MUX module, should be the FIRST to be put in "setup" mode and the LAST to be put in "run" mode.

FIGURE 2 (page 10) shows an example of how Scan RAM might be setup in a case using a 16 channel V252, V246, and a V207. In the example, all 16 channels of V252 are assigned to the first 16 channels of V207. The V246 (16 channel strain gage) is then assigned to the next eight channels on the V207 for a total of 24 channels.

The Scan RAM contains the Scan Table which must be setup properly on all MUXbus modules. The Scan RAM is 4096 bytes long, and the Scan Table is a subset of the Scan RAM. This means the Scan Table can be large enough to handle a system with up to 20416 channels. Each module scans through their Scan Table sequentially at the ADC clock rate. At any time, the current data on the list dictates which module is to connect a channel to the MUXbus.

Before the Scan Table can be written into Scan RAM, the V252 and the V207 must be put in "setup" mode by resetting the ADSEL bit in the Configuration Register. As a general rule, the V207 or any other receiving MUXbus module, should be the FIRST to be put in "setup" mode, and the LAST to be put in "run" mode. The Scan RAM is organized the same on all modules whether it sources or receives voltages on the MUXbus. Bit 14 is the enable bit which connects the specified channel to MUXbus. The enable bit must be set on only one sourcing module at any one time in the Scan Table (only one voltage may be out on MUXbus at one time). If two modules attempt to output voltages at the same time overlap will occur.

The source module channel is specified by the first 14 bits of Scan RAM. However, not all 16 channels of the V252 are available at any one time. The MUXbus is comprised of four paths, and the 16 channels of the V252 are distributed evenly among them. For instance, channels 1, 5, 9, and 13 of V252 are accessible only through path A of the MUXbus. On the V207 ADC module, the MUXbus paths A through D are scanned repeatedly in order and without variation. Consequently, although source modules like the V252 may have Scan Tables which address channels out of order, some limitations are imposed by the V207 MUXbus scanning order. For example, since the first MUXbus path to be scanned after entering "run" mode must be path A, the first element in a V252 Scan Table must call out a channel from the series "1, 5, 9, ... 4n+1". Furthermore, since the first hardware channel corresponds to a channel address (Scan Table data) of "0", the actual data to be written to the first element is from the series "0, 4, 8, ... 4n". The second element corresponds to a V207 read of MUXbus path B and must contain a V252 channel from the series "2, 6, 10, ... 4n+2". (Scan Table elements of the series "1, 5, 9, 4n+1"). The fifth element of the V252 Scan Table would once again correspond to a scan of MUXbus path A.

Bit 15 is the end of list bit. This bit must be set on the last location of the Scan Table on all MUXbus modules. Finally, all modules using MUXbus should be put it "run" mode starting with the sourcing (V252, V246, etc.) modules first.

As shown in the example, the simplest way to setup MUXbus is start with the V207 Scan Table. Include the channel address information of every MUXbus source module. The enable bit (bit 14) need not be set on the V207, but the end of list bit (bit 15) must be set at the last channel. Once the Scan Table is written on the V207, all that is necessary is to copy the table over to all MUXbus source modules. The only difference is that the enable bit (bit 14) must be set on the particular module whose channel is to be enabled out on MUXbus.

Overlap Detect

Should the overlap LED turn on, the V252 will stop asserting its voltage out on MUXbus because one of these conditions:

1.) A channel was indicated at the wrong time. Only certain channels are available for each MUXbus path. For example, if channel 2 was requested out on MUXbus path A, C, or D, an overlap would occur.

2.) Two modules attempted to output voltages out on MUXbus at the same time because the enable bit (bit 14) was set in the same location in their Scan Table.

3.) Not all modules had their end of list bit (bit 15) set at the same location in their Scan Tables. The Scan Tables must all be the same length.

TABLE 1 - Calibration Register Values

Cal Voltage	On board Source	MUX bus Source
+10.0	0x8091	0x0091
+5.0	0x80A1	0x00A1
+2.0	0x80C1	0x00C1
+1.0	0x8092	0x0092
+0.5	0x80A2	0x00A2
+0.2	0x80C2	0x00C2
+0.1	0x8094	0x0094
+0.05	0x80A4	0x00A4
+0.02	0x80C4	0x00C4
+0.01	0x8096	0x0096
+0.005	0x80A6	0x00A6
+0.002	0x80C6	0x00C6
-0.002	0x8146	0x0146
-0.005	0x8126	0x0126
-0.01	0x8116	0x0116
-0.02	0x8144	0x0144
-0.05	0x8124	0x0124
-0.1	0x8114	0x0114
-0.2	0x8142	0x0142
-0.5	0x8122	0x0122
-1.0	0x8112	0x0112
-2.0	0x8141	0x0141
-5.0	0x8121	0x0121
-10.0	0x8111	0x0111

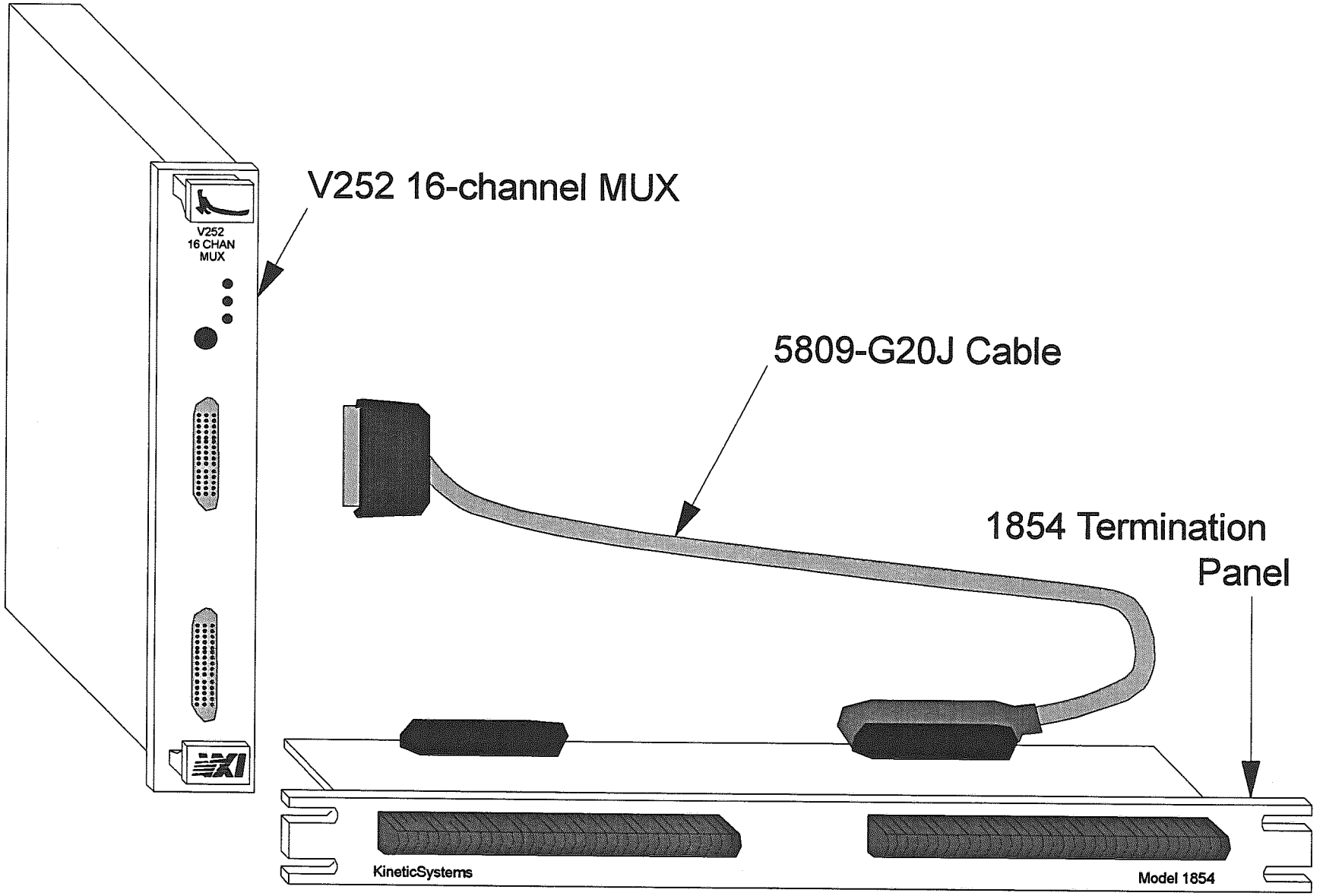
Calibration

The wide range of calibration sources was chosen to easily calibrate V252 at a module or system level whether it be with other KineticSystems MUXbus modules or not.

The V252 can be calibrated at the module level by using the 10 volt precision voltage source and the specialized hybrid calibrator both available on board the V252. The voltage source itself can be calibrated easily by monitoring the voltage from the connectors, "+" and "-", and adjusting the voltage from the pot, "Ref Adj", both accessible from the front panel. When monitoring the calibration voltage through the front panel, a meter accurate to the 16-bit level is highly recommended. The Calibration Register then can be used to generate 24 different voltages anywhere from -10.0 to +10.0 volts. A table of the available voltages with the corresponding value written to the Calibration Register is in Table 1 (page 12).

The V252 can be calibrated at the system level by also using the hybrid calibrator by choosing the MUXbus as the 10 volt precision source. The V207 will output its 10 volt precision voltage source which can then be used by all MUXbus sourcing modules for end to end, system calibration with no external cabling. A table of the available voltages with the corresponding value written to the Calibration Register is in Table 1 (page 12).

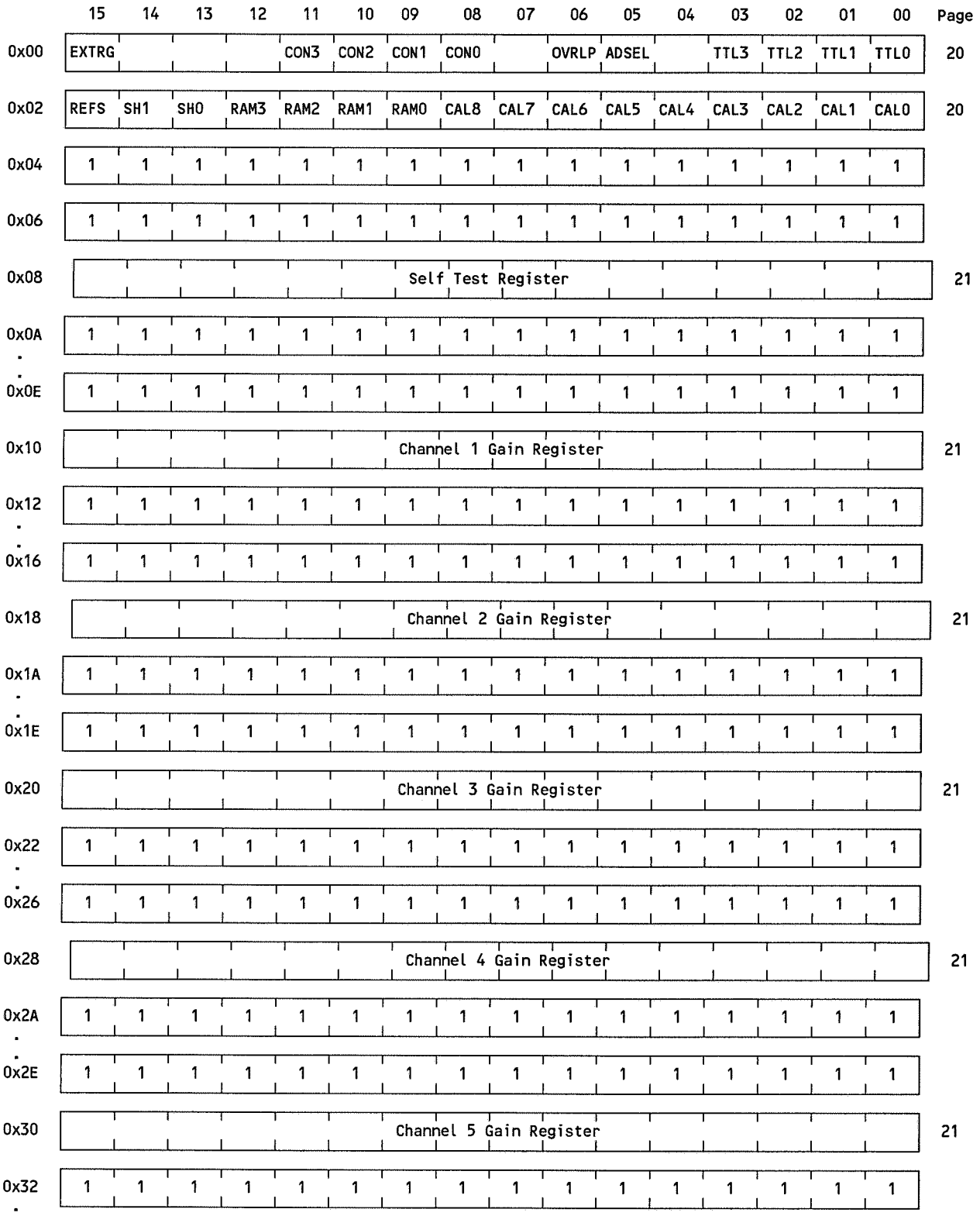
With some external cabling, the V252 can still be calibrated with non KineticSystems MUXbus modules at the system level. A calibration voltage may be brought in through pins 33 and 67 on the P4 connector. This voltage may be switched in on a per-channels basis by writing a 10_2 to bits 8 and 7 on each channel's Gain Register. However, the hybrid calibrator may not be applied to this calibration voltage.


V252 16-channel MUX
V252
16 CHAN
MUX
5809-G20J Cable
1854 Termination
Panel
KineticSystems
Model 1854

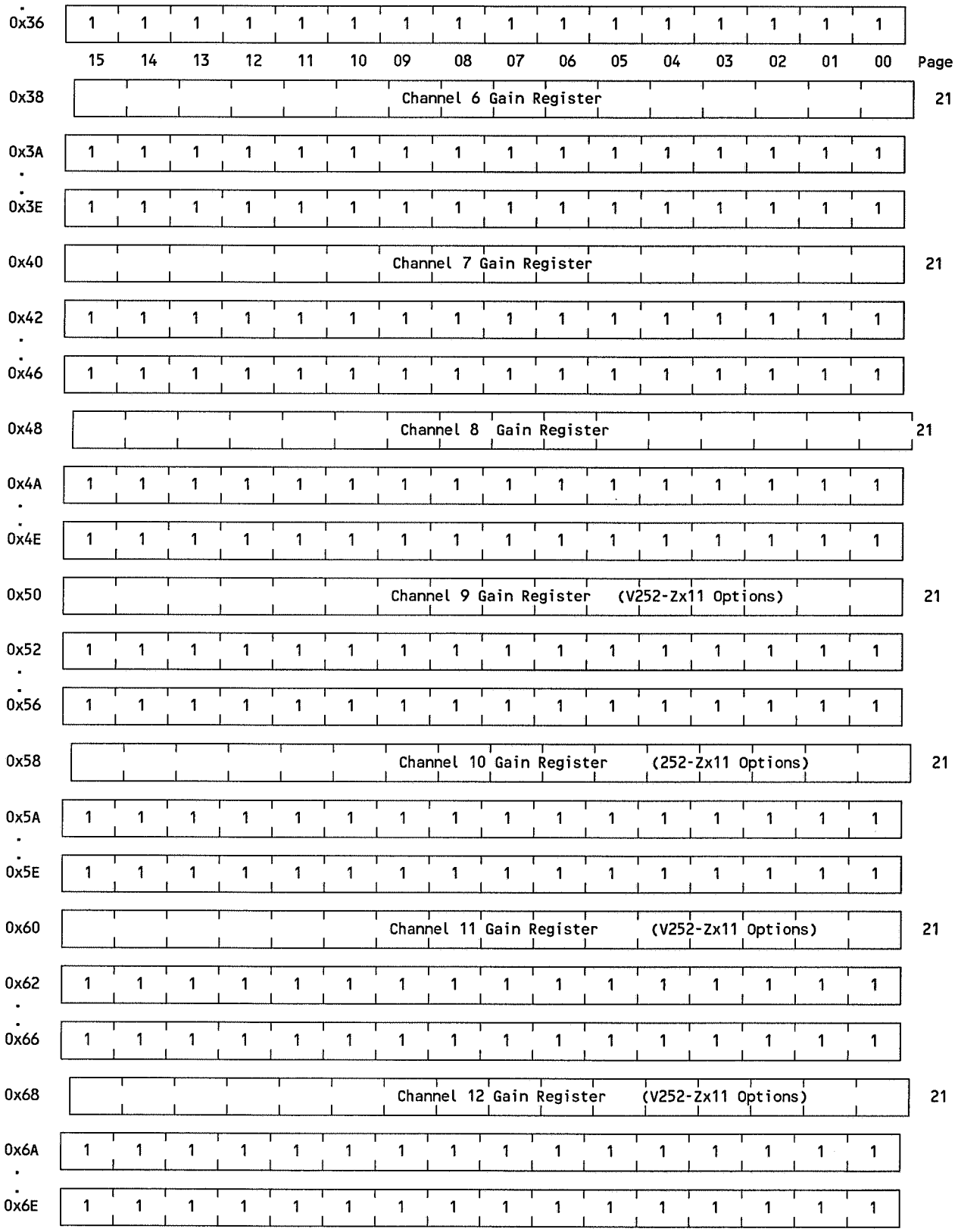
V252 Configuration Registers, A16 Space

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Page
0x00 (R)	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	17
0x00 (W)	Logical Address Register																17
0x02	1	0	0	1	0	0	1	0	0	1	0	1	0	0	1	0	17
0x04	A24	Modid											Ready	Passd	Inhbt	Reset	17
0x06	Offset Register																17
0x08	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	18
0x0A	Serial Number High																18
0x0C	Serial Number Low																18
0x0E	FVER3	FVER2	FVER1	FVER0	FREV3	FREV2	FREV1	FREV0	HVER3	HVER2	HVER1	HVER0	HREV3	HREV2	HREV1	HREV0	18
0x10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
. . 0x18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
0x1A	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	18
0x1C	1	1	1	1	1	1	1	IMASK	*IEN	1	IRQ2	IRQ1	IRQ0	1	1	1	19
0x1E	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	19
0x20	Suffix High Register																19
0x22	Suffix Low Register																19
0x24 . . 0x3E	User Defined Register																19
	User Defined Register																19

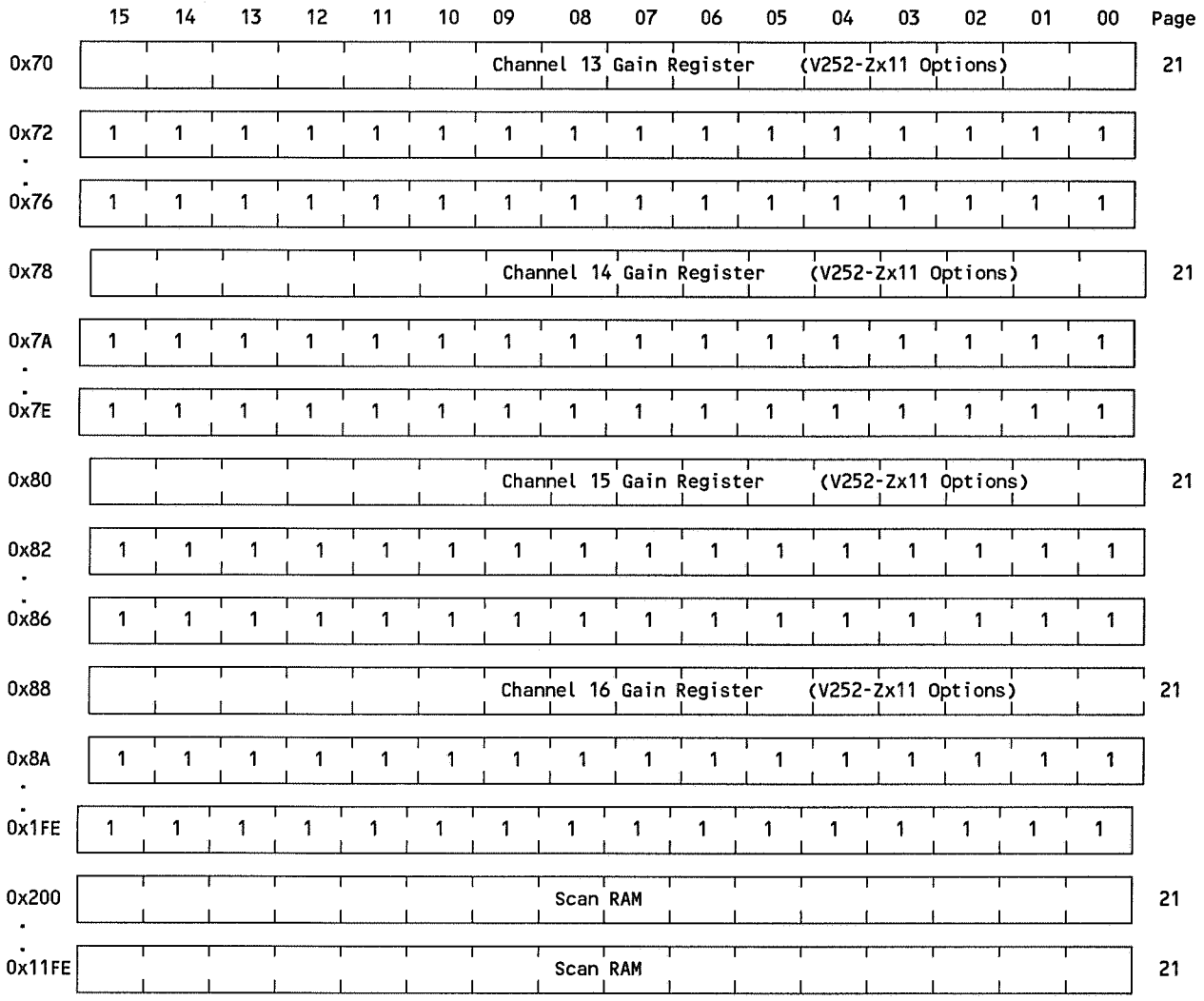
V252 Operational Registers, A24 Space



Model V252-Zxx2



Model V252-Zxx2



V252 Configuration Registers

$ 0x00 - ID Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1

[15:14]	(R)	Class = Extended
[13:12]	(R)	Mode = A16/A24
[11:0]	(R)	ID = F29

$ 0x00 - ID Register (W)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	x	x	x	x	x	x	LAR7	LAR6	LAR5	LAR4	LAR3	LAR2	LAR1	LAR0

LAR[7:0]	(W)	Logical Address Register

$ 0x02 - Device Type Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	1	0	0	1	0	0	1	0	1	0	0	1	0

[15:12]	(R)	Memory = 4096 Bytes
[11:0]	(R)	Model = 252

$ 0x04 - Status Control Register (Mixed)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A24	Modid	1	1	1	1	1	1	1	1	1	1	Ready	Passd	Inhbt	Reset

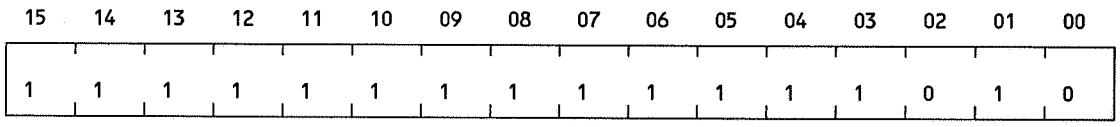
A24	(RW)	A24 Enable
Modid	(R)	Active low Modid line to V252
Ready	(R)	V252 is ready for VXI access
Passd	(R)	V252 passed all of the self tests
Inhbt	(RW)	Inhibits assertion of *Sysfail on VXI bus
Reset	(RW)	Soft reset, run self test after Reset is deserted

$ 0x06 - Offset Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OFF15	OFF14	OFF13	OFF12	OFF11	OFF10	OFF9	OFF8	OFF7	OFF6	OFF5	OFF4	OFF3	OFF2	OFF1	OFF0

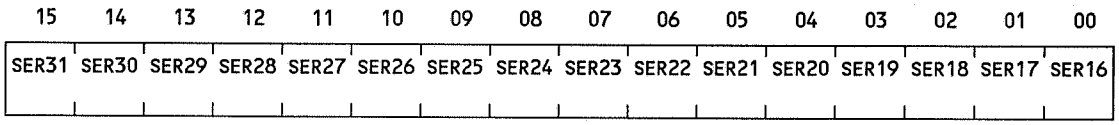
OFF[15:0]	(RW)	Offset Register which points to base address in A24 space

$ 0x016 - Attribute Register (R)

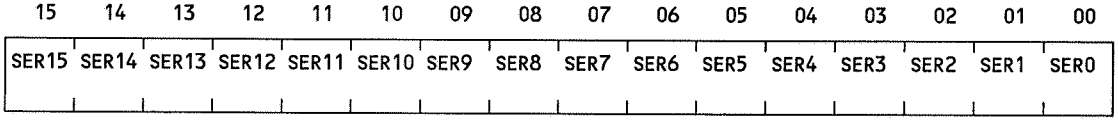


[2]	(R)	Interrupt Control Capability
[1]	(R)	No Interrupt Handler Capability
[0]	(R)	Interrupt Status Capability

$ 0x0A - Serial Number High (R)

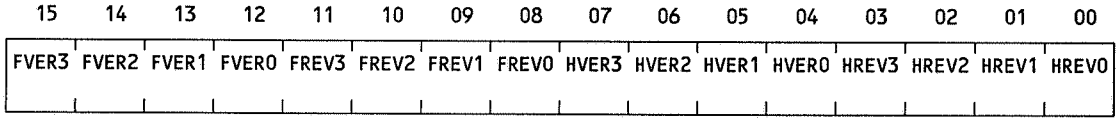


$ 0x0C - Serial Number Low (R)



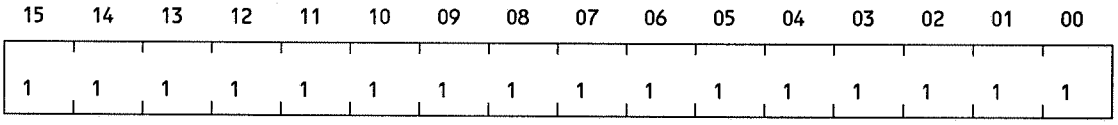
SER[31:0]	(R)	KSC's unique serial number for every module

$ 0x0E - Version Number Register (R)

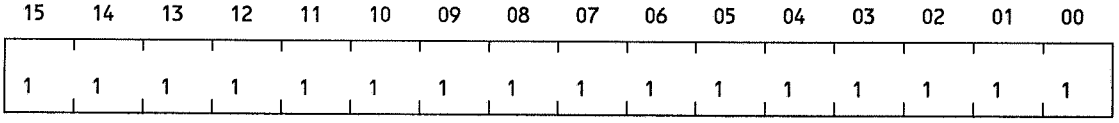


FVER[3:0]	(R)	Firmware Main Version #
FREV[3:0]	(R)	Firmware Revision #
HVER[3:0]	(R)	Hardware Main Version #
HREV[3:0]	(R)	Hardware Revision #

$ 0x10 to 0x116 - Reserved (R)



$ 0x1A - Interrupt Status Register (R)



[15:16]	(R)	Status ID = FF
[7:0]	(R)	Reserved

$ 0x1C - Interrupt Control Register (RW)

Model V252-Zxx2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							IMASK	*IEN		IRQ2	IRQ1	IRQ0			
1	1	1	1	1	1	1			1				1	1	1

IMASK	(RW)	Interrupt Mask
*IEN	(RW)	Interrupt Enable
IRQ[2:0]	(RW)	Interrupt Request Level
		000 IRQ7
		001 IRQ6
		010 IRQ5
		011 IRQ4
		100 IRQ3
		101 IRQ2
		110 IRQ1
		111 Disconnected

$ 0x1E - Subclass Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

[15]	(R)	VXI Extended Device
[14:0]	(R)	7FFE = Extended Register Based Device

$ 0x20 - Suffix High Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SUF31	SUF30	SUF29	SUF28	SUF27	SUF26	SUF25	SUF24	SUF23	SUF22	SUF21	SUF20	SUF19	SUF18	SUF17	SUF16

$ 0x22 - Suffix Low Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SUF15	SUF14	SUF13	SUF12	SUF11	SUF10	SUF9	SUF8	SUF7	SUF6	SUF5	SUF4	SUF3	SUF2	SUF1	SUF0

SUF[31:0]	(R)	4 Character string representing the model's suffix.

$ 0x24 to 0x3F - User Defined Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
USE15	USE14	USE13	USE12	USE11	USE10	USE9	USE8	USE7	USE6	USE5	USE4	USE3	USE2	USE1	USE0

USE[15:0]	(RW)	User defined register stored on EEPROM (non-volatile RAM).

V252 Operational Registers

$ 0x00 - Configuration Register (Mixed)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXTRG				CON3	CON2	CON1	CON0		OVRLP	ADSEL		TTL3	TTL2	TTL1	TTL0
(0)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	(1)	(0)	(0)	(0)	(0)

() power up value

EXTRG	(RW)	When set, the external trigger is enabled.
OVRLP	(R)	Overlap detected by V252 on MUX bus, cleared by a write or a read to scan ram.
CON[3:0]	(R)	Connector Type
		1111 No Termination Housing
ADSEL	(RW)	Address select bit for MUX bus.
		0 Setup Mode
		1 Run Mode
TTL[3:0]	(RW)	TTL Trigger select for sample hold option.
		0000 TTL Trig 0
		0001 TTL Trig 1
		0010 TTL Trig 2
		0011 TTL Trig 3
		0100 TTL Trig 4
		0101 TTL Trig 5
		0110 TTL Trig 6
		0111 TTL Trig 7
		1000 Disable
		. .
		. .
		1111 Disable

$ 0x02 - Calibration Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REFS	SH1	SH0	RAM3	RAM2	RAM1	RAM0	CAL8	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0
(1)	(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

() power up value

REFS	(RW)	Reference Source
		0 MUX bus
		1 On board source
SH1	(RW)	When set, Sample Hold passed for channels 9 to 16.
SH0	(RW)	When set, Sample Hold passed for channels 1 to 16.
RAM3	(RW)	When set, Scan RAM address walking ones test passed.
RAM2	(RW)	When set, Scan RAM address walking zeros test passed.
RAM1	(RW)	When set, Scan RAM data walking ones test passed.
RAM0	(RW)	When set, Scan RAM data walking zeros test passed.
CAL8	(RW)	CAL-
CAL7	(RW)	CAL+
CAL6	(RW)	Selects Reference Source * .2
CAL5	(RW)	Selects Reference Source * .5
CAL4	(RW)	Selects Reference Source * 1
CAL3	(RW)	Scale Reference Source by .001
CAL2	(RW)	Scale Reference Source by .01
CAL1	(RW)	Scale Reference Source by .1
CAL0	(RW)	Scale Reference Source by 1

$ 0x08 - Selftest Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

() power up value

CH[i] (R) Indicates if the voltage for channel I is at 5 volts +- .7 volts. This register is used by the self test micro to check various gains as well as sample hold.

$ 0x10 - Channel 1 Gain Register (RW)
$ 0x18 - Channel 2 Gain Register (RW)
$ 0x20 - Channel 3 Gain Register (RW)
$ 0x28 - Channel 4 Gain Register (RW)
$ 0x30 - Channel 5 Gain Register (RW)
$ 0x38 - Channel 6 Gain Register (RW)
$ 0x40 - Channel 7 Gain Register (RW)
$ 0x48 - Channel 8 Gain Register (RW)
$ 0x50 - Channel 9 Gain Register (RW)
$ 0x58 - Channel 10 Gain Register (RW)
$ 0x60 - Channel 11 Gain Register (RW)
$ 0x68 - Channel 12 Gain Register (RW)
$ 0x70 - Channel 13 Gain Register (RW)
$ 0x78 - Channel 14 Gain Register (RW)
$ 0x80 - Channel 15 Gain Register (RW)
$ 0x88 - Channel 16 Gain Register (RW)

The gain register for channels 9 through 16 are available for V252-Zx11 options only.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
							IMUX1	IMUX0		SGN2	SGN1	SGN0		FGN1	FGN0
(1)	(1)	(1)	(1)	(1)	(1)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)

() power up value

IMUX[1:0] (RW) Input selection
- 00 Line
- 01 Local calibration (voltage set by Calibration Register)
- 10 Front panel calibration (P4 connector)
- 11 Analog ground

SGN[2:0] (RW) Second stage gain selection
- 000 Gain = 0.5 (1)
- 001 Gain = 1.0 (1)
- 100 Gain = 2.0
- 110 Gain = 5.0 (1)
- 111 Gain = 10.0 (1)

FGN[1:0] (RW) First stage gain selection
- 00 Gain = 1.0 (1)
- 01 Gain = 10.0 (1)
- 10 Gain = 100.0 (1)
- 11 Invalid

(1) verified by self test

$ 0x200 to 0x11FE - Scan RAM (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EOL	ENABL											CH3	CH2	CH1	CH0
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

() power up value

EOL	(RW)	End of list.
ENABL	(RW)	Enables CH[3:0].
CH[3:0]	(RW)	Selects channel number on the V252 to be placed out on the MUX bus.

Note: A bus error will occur if a write is attempted while in 'run mode'.

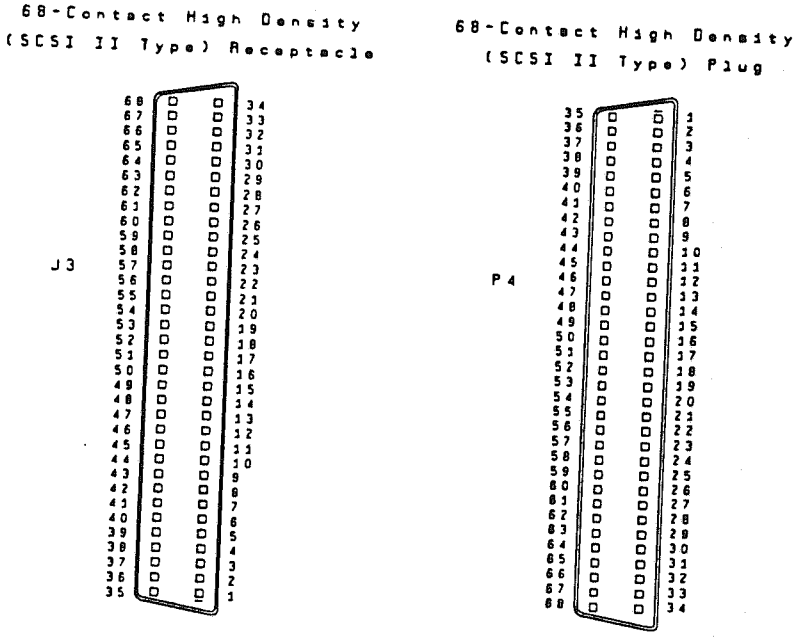


FIGURE 3 - 68 Pin SCSI II Connectors, J3 and P4

TABLE 2 - 68 Pin SCSI II Connectors, J3 and P4 Pinout

Please note that channels 9 through 16 are available on V252-Zx11 options only.

J3		P4	
Pin #	Description	Pin #	Description
1	Channel 1 Out +	1	Channel 1 In +
35	Channel 1 Out -	35	Channel 1 In -
2	Channel 2 Out +	2	Channel 1 Guard
36	Channel 2 Out -	36	Channel 2 Guard
3	Channel 3 Out +	3	Channel 2 In +
37	Channel 3 Out -	37	Channel 2 In -
4	Channel 4 Out +	4	Channel 3 In +
38	Channel 4 Out -	38	Channel 3 In -
5	Channel 5 Out +	5	Channel 3 Guard
39	Channel 5 Out -	39	Channel 4 Guard
6	Channel 6 Out +	6	Channel 4 In +
40	Channel 6 Out -	40	Channel 4 In -
7	Channel 7 Out +	7	Channel 5 In +
41	Channel 7 Out -	41	Channel 5 In -
8	Channel 8 Out +	8	Channel 5 Guard
42	Channel 8 Out -	42	Channel 6 Guard
9	Channel 9 Out +	9	Channel 6 In +
43	Channel 9 Out -	43	Channel 6 In -
10	Channel 10 Out +	10	Channel 7 In +
44	Channel 10 Out -	44	Channel 7 In -
11	Channel 11 Out +	11	Channel 7 Guard
45	Channel 11 Out -	45	Channel 8 Guard
12	Channel 12 Out +	12	Channel 8 In +
46	Channel 12 Out -	46	Channel 8 In -
13	Channel 13 Out +	13	Channel 9 In +
47	Channel 13 Out -	47	Channel 9 In -
14	Channel 14 Out +	14	Channel 9 Guard
48	Channel 14 Out -	48	Channel 10 Guard
15	Channel 15 Out +	15	Channel 10 In +
49	Channel 15 Out -	49	Channel 10 In -
16	Channel 16 Out +	16	Channel 11 In +

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J3		P4	
Pin #	Description	Pin #	Description
50	Channel 16 Out -	50	Channel 11 In -
17		17	Channel 11 Guard
51		51	Channel 12 Guard
18		18	Channel 12 In +
52		52	Channel 12 In -
19		19	Channel 13 In +
53		53	Channel 13 In -
20		20	Channel 13 Guard
54		54	Channel 14 Guard
21		21	Channel 14 In +
55		55	Channel 14 In -
22		22	Channel 15 In +
56		56	Channel 15 In -
23		23	Channel 15 Guard
57		57	Channel 16 Guard
24		24	Channel 16 In +
58		58	Channel 16 In -
25		25	
59		59	
26		26	
60		60	
27		27	
61		61	
28		28	
62		62	
29		29	
63		63	
30		30	
64		64	
31		31	
65		65	
32		32	External Trigger
66		66	Ground

Model V252-Zxx2

J3		P4	
Pin #	Description	Pin #	Description
33	Calibration Out +	33	Front Panel In +
67	Calibration Out -	67	Front Panel In -
34	No Connect	34	No Connect
68	No Connect	68	No Connect

APPENDIX A

```
#include <stdio.h>

typedef unsigned short uint8;
typedef unsigned long uint32;
typedef short int8;

uint8 const A24SuperData = 0x6;
uint8 const A32SuperData = 0x7;
uint32 const V252_serial = 1234;
uint32 const V207_serial = 3456;
uint8 const V252_suf_high = 'ZD';
uint8 const V252_suf_low = '12';
uint8 const V207_suf_high = 'ZB';
uint8 const V207_suf_low = '11';

void reportError() {
    printf("Error: closing VXIlibrary\n");
    CloseVXIlibrary();
    exit(1);
    }

uint8 find_la (
uint8 model,
uint32 serial_numb,
uint8 suf_high_numb,
uint8 suf_low_numb
) {
    int8  i,error;
    uint8 data,id,dev_type,la;
    uint8 serial,suf_high,suf_low;

    la = 0xFF;
    for (I=0; i<0xFF; I++) {
     error = VXIinReg(i,0x0,&id);
     id &= 0xFFF;

     if (error ==0) {
         /* get device type value */
         error = VXIinReg(i,0x2,&dev_type);
         dev_type &= 0xFFF;
         if (error != 0)
          reportError();

         /* get serial number */
         error = VXIinReg(i,0xA,&(uint8)serial);
         if (error != 0)
          reportError();
         error = VXIinReg(i,0xC,&data);
         if (error != 0)
          reportError();
```

```
          serial = (serial << 8) + (uint32)data;

          /* get suffix number */
          error = VXIinReg(i,0x20,&suf_high);
          if (error != 0)
           reportError();
          error = VXIinReg(i,0x22,&suf_low);
          if (error != 0)
           reportError();

          if (id==0xF29 && dev_type==model && serial==serial_numb
          && suf_high==suf_high_numb && suf_low==suf_low_numb) {
           la = I;
           printf("V%x found at logical address 0x%x\n",model,la);
           }
          }
      }
     if (la == 0xFF) {
      printf("V%x not found, search parameters
incorrect\n",model);
      reportError();
      }

     return la;
     }

/*    The main program will assign all 16 channels of the V252 to
      */
/* the first 16 channels of V207.  MUXbus will be enabled after
both */
/* Scan Tables has been written                                  */
main () {
  uint8 V252,V207,data;
  uint32 address;

  error = InitVXIlibrary();
  if (error != 0) {
    printf("Error: opening InitVXIlibrary()\n");
    exit(1);
    }

  V252 = find_la ( 0x252, V252_serial, V252_suf_high,
V252_suf_low);
  error = GetDevInfo(V252,12,&A24_V252);
  if (error != 0)
    reportError();

  V207 = find_la ( 0x207, V207_serial, V207_suf_high,
V207_suf_low);
  error = GetDevInfo(V252,12,&A32_V207);
  if (error != 0)
    reportError();
```

```
address =  A32_V207 + 0x6;  /* V207 in setup mode    /*
data = 0;
error = VXIout(A32SuperData,address,2,data);
if (error != 0)
  reportError();

address =  A24_V207;   /* V252 in setup mode    /*
data = 0;
error = VXIout(A32SuperData,address,2,data);
if (error != 0)
  reportError();

address = A32_V207 + 0x200; /* set V207 for 16 channels   /*
for (I=0; i<15; I++) {
  data = 0x4000 | I;
  error = VXIout(A32SuperData,address,2,data);
  if (error != 0)
    reportError();
  address += 2;
  }
data = 0xC00F;
error = VXIout(A32SuperData,address,2,data);
if (error != 0)
  reportError();

address = A24_V207 + 0x200; /* set V252 for 16 channels   /*
for (I=0; i<15; I++) {
  data = 0x4000 | I;
  error = VXIout(A24SuperData,address,2,data);
  if (error != 0)
    reportError();
  address += 2;
  }
data = 0xC00F;
error = VXIout(A24SuperData,address,2,data);
if (error != 0)
  reportError();

for (I=1; I<=16; I++) { /* set all channels to unity gain */
  address = A24_V252 + (0x8*(I+1));
  data = 0x11;
  error = VXIout(A24SuperData,address,2,data);
  if (error != 0)
    reportError();
  }

address =  A24_V207;   /* V252 in run mode      /*
data = 0x20;
error = VXIout(A32SuperData,address,2,data);
if (error != 0)
  reportError();
```

```
  address =  A32_V207 + 0x6;  /* V207 in run mode      /*
  data = 0x20;
  error = VXIout(A32SuperData,address,2,data);
  if (error != 0)
    reportError();

  CloseVXIlibrary();
  }
```