Model V258

2 or 4-channel Resolver or
Synchro-to-Digital Converter

INSTRUCTION MANUAL

March, 2002

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Resolver- or Synchro-to-Digital Converter

Converts shaft position to digital values

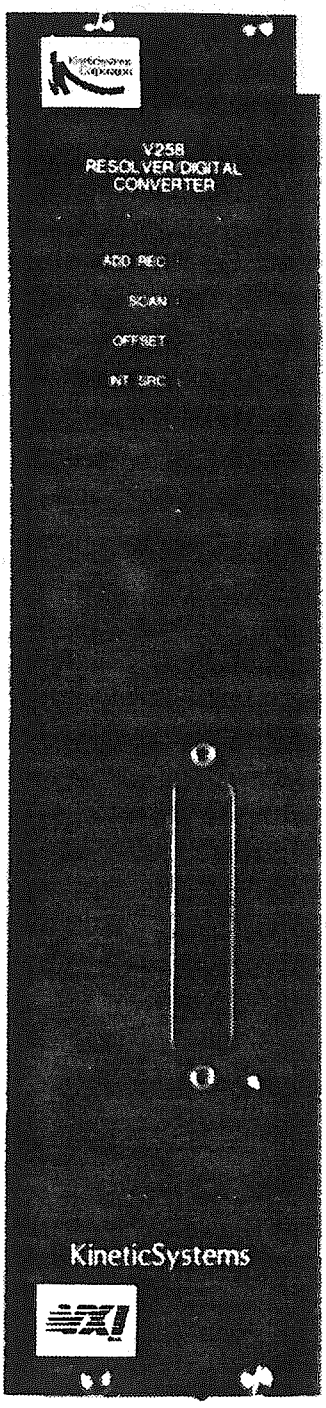
V258

Features

- **Options available for 2 or 4 channels**
- **Programmable bandwidth**
- **Programmable resolution**
- **Accuracy to ±7.3 arc minutes.**
- **Loss-of-signal indication**
- **Angle and turns monitor**
- **Simultaneous channel measurements**
- **Independent preset functions**
- **Available in either 3-wire synchro or 4-wire resolver input configurations**

Typical Applications

- **Engine and powertrain testing**
- **Monitoring high-speed steel rolling mills**



General Description

The V258 is a double-width, C-size, register-based, VXIbus module which functions as a multi-turn resolver-to-digital or synchro-to-digital converter. This module is available in either two-channel or four-channel versions.

Each channel is monitored by a single-speed, tracking resolver-to-digital or synchro-to-digital converter. Separate registers are provided for turn count and angle data. The module can continuously scan all channels and store the data in internal registers. The module can be directed to stop scanning the inputs to allow simultaneous angle measurement of all channels. While scanning is disabled, the turn counters internally track the inputs to prevent loss of data.

The V258 may be operated in absolute angle mode (in which the current angle is stored in the data registers) or in the offset mode. The offset mode is used to specify a reference point to reduce the amount of overhead required to monitor turns correctly. In the offset mode, the user may assign a reference point by setting a channel's angle-and-turns count data to the desired value. The present angle value now becomes the zero degree angle position for calculating angle information.

To further reduce overhead and eliminate the need for polling, the V258 utilizes interrupts to signal when a given angle and turn value have been reached. Each channel has a 32-bit compare register which describes a channel compare point. This register contains a 16-bit angle value and a 16-bit turn value. When a channel input value matches or passes through both values, an interrupt may be generated. This eliminates the need for the host computer to constantly monitor each channel. An interrupt may also be generated when a channel's converter detects a Loss-of-Signal.

Angle resolution is user programmable for 10, 12, 14, or 16 bits. The bandwidth for each channel is also programmable. Each channel's converter may be programmed for higher precision in the higher resolution mode or faster settling in the lower resolution modes. This allows the converter to settle faster for step inputs.

The V258 supports both static and dynamic configuration. Access to the module's operational registers is via memory locations pointed to by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.

Resolver-to-Digital		Bandwidth							
Parameter	Units	High				Low			
Resolution	Bits	10	12	14	16	10	12	14	16
	Degrees	0.35	0.088	0.022	0.0055	0.35	0.088	0.022	0.0055
Input Frequency	kHz	1-6	*	2-6	NR	0.36-6	*	*	2-6
Tracking Rate	RPS†	800	200	50	12.5	200	50	12.5	3.2
Closed Loop Bandwidth	Hz	530	*	*	*	130 k	*	*	*
Acceleration Constant, K_a	$1/s^2$	1.4 M	*	*	*	90 k	*	*	*
Acc-1 LSB Lag	$°/s^2$	512 k	128 k	32 k	8 k	32 k	8 k	2 k	500
Settling Time	ms	10	15	30	75	40	60	120	300
Accuracy	6 minutes max. + 1 LSB of selected resolution (4 LSBs differential linearity) at 14 bits.								
Signal Input	11.8 V L-L								
resolver									
Z_{in} line to line	140 kohm								
Z_{in} each line-ground	80 kohm								
Common mode range	26 V peak								
Max voltage w/o damage	110 V transient, 15 V Continuous								
Power Requirements									
+5 V									
+24 V									
-24 V									
Environmental and Mechanical									
Temperature range									
Operational	0°C to +50°C								
Storage	-25°C to +75°C								
Relative humidity	0 to 85%, non-condensing to 40°C								
Cooling requirements	10 CFM								
Dimensions	340 mm x 233.35 mm x 60.66 mm (C-size VXIbus)								
Front-panel potential	Chassis ground								

* same as to the left
† RPS minimum
NR Not recommended

Synchro-to-Digital		Bandwidth							
Parameter	Units	High				Low			
Resolution	Bits	10	12	14	16	10	12	14	16
	Degrees	0.35	0.088	0.022	0.0055	0.35	0.088	0.022	0.0055
Input Frequency	kHz	0.36-1	*	*	*	0.047-1	*	*	*
Tracking Rate	RPS†	160	40	10	2.5	40	10	2.5	0.62
Closed Loop Bandwidth	Hz	53	*	*	*	13	*	*	*
Acceleration Constant, K_a	$1/s^2$	14.4 k	*	*	*	3.6 k	*	*	*
Acc-1 LSB Lag	$°/s^2$	17 k	4.2 k	1.1 k	260	1.1 k	260	66	17
Settling Time	ms	110	110	200	500	550	600	750	1100
Accuracy	6 minutes max. + 1 LSB of selected resolution (4 LSBs differential linearity) at 14 bits								
Signal Input	90 V L-L (V258-ZB11, -ZB21), 11.8 V L-L (V258-ZC11, -ZC21)								
Synchro									
Z_{in} line to line	123 kohm								
Z_{in} each line-ground	180 kohm								
Common mode range	180 V peak								
Power Requirements									
+5 V									
+24 V									
-24 V									
Environmental and Mechanical									
Temperature range									
Operational	0°C to +50°C								
Storage	-25°C to +75°C								
Relative humidity	0 to 85%, non-condensing to 40°C								
Cooling requirements	10 CFM								
Dimensions	340 mm x 233.35 mm x 60.66 mm (C-size VXIbus)								
Front-panel potential	Chassis ground								

* same as to the left
† RPS minimum

Ordering Information

Model V258-ZA11 2-channel, Resolver-to-Digital Converter
Model V258-ZA21 4-channel, Resolver-to-Digital Converter
Model V258-ZB11 2-channel, Synchro-to-Digital Converter, 90 V Signal
Model V258-ZB21 4-channel, Synchro-to-Digital Converter, 90 V Signal
Model V258-ZC11 2-channel, Synchro-to-Digital Converter, 11.8 V Signal
Model V258-ZC21 4-channel, Synchro-to-Digital Converter, 11.8 V Signal

Related Products

Model 5851-Bxyz Cable—50S "D" to Unterminated
Model 5851-Dxyz Cable—50S "D" to 50S "D"
Model 5851-Exyz Cable—50P "D" to 50S "D"
Model 5934-Z1A Connector—50S "D"
Model 1850-E1D Rack-mount Termination Panel

032602

UNPACKING AND INSTALLATION

The Model V258 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment. Switches and straps not described here should remain in their factory configured position for proper operation.

Logical Address Switches

The V258 is one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot-0 device.) The module is shipped from the factory with its Logical Address switches set for Logical Address 255 (FF_{16}). This address can be shared by multiple devices in a system that supports Dynamic Configuration. If the V258 is to be used in a system that does not support Dynamic Configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating the eight rocker switches located under the access hole in the module's right-side ground shield. Refer to Figure 1 below.

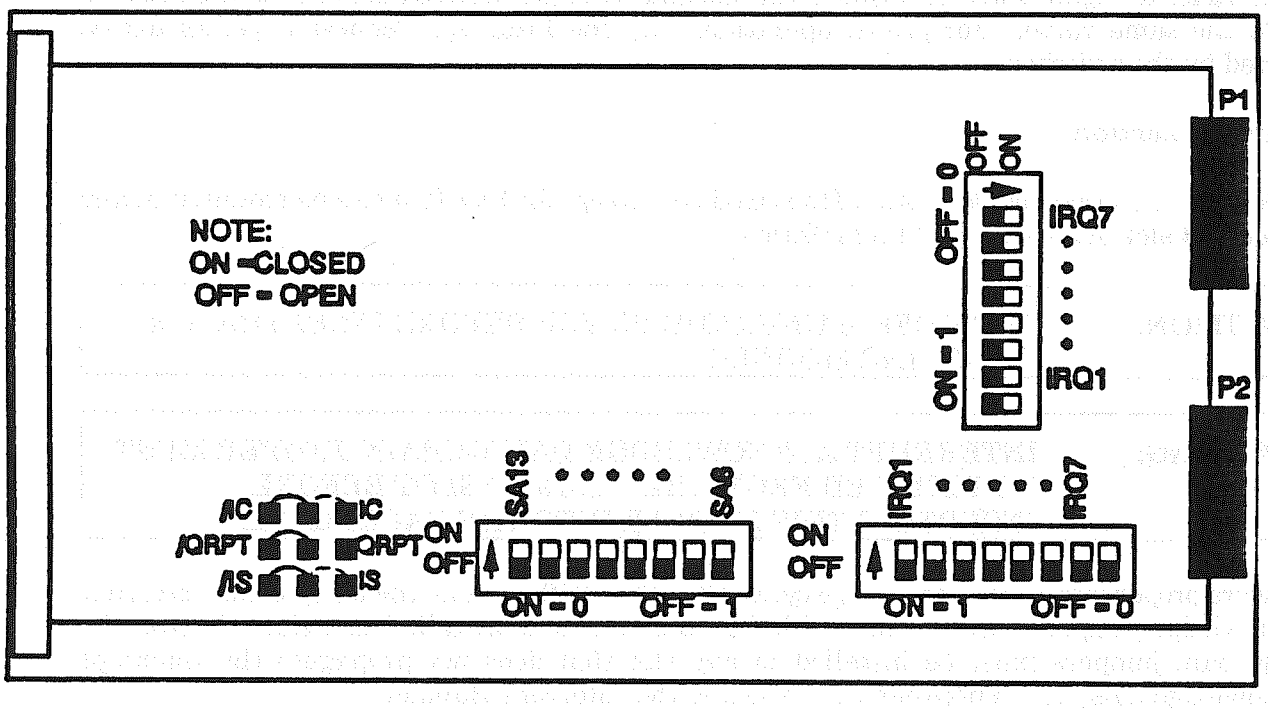


Figure 1 - V258 Switch Locations

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The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value. Closing a switch sets its corresponding bit to a "0", opening a switch sets its bit to a "1". The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (VXIbus defined).

Bits 13-06 are user-selectable via the address switches LA128-LA1 (when the module is statically configured).

Bits 05-00 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V258 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to Figure 1 for the switch locations and settings. Both banks of switches must be set to the same value. For proper operation, only one Interrupt Request Level should be selected by the switches.

Module Insertion

The V258 is a C-sized double-width VXIbus module. Except for Slot-0, it can be mounted in any unoccupied slot in a C-sized VXI mainframe.

CAUTION:	**TURN OFF MAINFRAME POWER BEFORE INSERTING OR REMOVING MODULE.**

WARNING:	**INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPER MUST BE REMOVED FROM THE DESIRED SLOT BEFORE INSERTING THIS MODULE INTO THE BACKPLANE.**

To insure proper interrupt acknowledge cycles from the V258 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any slot that does not propagate the Interrupt Acknowledge daisy chain between the V258 and the Interrupt Handler.

FRONT PANEL INFORMATION

The front panel of the V258 has four LEDs and one 50-position female Amphenol connector. These components are used for signal input and to monitor operating conditions.

LEDs

The four LEDs are used to monitor the present operating conditions of the V258.

LED	Meaning
ADD REC	When lit, this LED indicates that the V258 Operational Registers are presently being addressed. This LED is one-shot extended.
SCAN	When lit, this LED indicates that the V258 is in the scanning mode, and is storing input data in the CVT. When this LED is not lit, the V258 is scanning disabled and will not update the CVT.
OFFSET	When lit, this LED indicates that the V258 has its offset circuitry enabled. When in this mode, the data stored in the channel offset registers is subtracted from the input angle to form the present angle data for the CVT. When this LED is not lit, this indicates that the V258 is operating in the true angle mode, and that the offset circuitry is disabled.
INT SRC	When lit, this LED indicates that the V258 has an Interrupt Request pending.

Connector Information

The V258 uses a 50-position female Amphenol connector. A mating connector number is Amphenol's 157-72500-3.

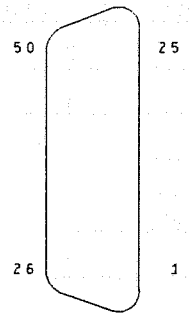

Figure 2 - Front Panel Connector

The following is a V258 front panel pin description:

Table 1. Front Panel Pin Description

50 Channel 3, S4 (Resolver only)	25 Channel 3, S1
49 Channel 3, S2	24 Channel 3, S3
48	23
47 Channel 3, Reference	22 Ground
46	21
45	20
44 Ground	19 Ground
43 Channel 2, S4 (Resolver only)	18 Channel 2, S1
42 Channel 2, S2	17 Channel 2, S3
41	16
40 Channel 2, Reference	15 Ground
39	14
38	13
37 Ground	12 Ground
36 Channel 1, S4 (Resolver only)	11 Channel 1, S1
35 Channel 1, S2	10 Channel 1, S3
34	9
33 Channel 1, Reference	8 Ground
32	7
31	6
30 Ground	5 Ground
29 Channel 0, S4 (Resolver only)	4 Channel 0, S1
28 Channel 0, S2	3 Channel 0, S3
27	2
26 Channel 0, Reference	1 Ground

Note: Channels two and three are not used with V258-Zx11 options (2-Channel version).

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INTRODUCTION

The V258 is a multi-channel Resolver or Synchro-to-Digital Converter. The V258 has independent reference (stator) and signal (rotor) inputs for each channel, making it capable of monitoring up to four channels of isolated resolver/synchro data. The V258-Zx21 is the four channel version; while, the V258-Zx11 is the two channel model.

Convertor Operation

The V258 resolver options utilize the *ILC Data Device Corporation's* **RDC-19201-304** 16-bit resolver-to-digital converter. This device allows connection of 11.8V L-L resolver inputs, and a reference input of 4-50Vrms 360Hz-6KHz. The RDC-19021-304 incorporates a Type II servo-loop ($K_v = \infty$) and a high acceleration constant.

The V258 is dynamically configurable for 10, 12, 14, or 16-bit resolution for each of its channels. The operating bandwidth is also programmable, which allows for a multitude of configurations without the need for straps. Connection to the V258 is made through a 50- position ribbon Amphenol connection located on the module's front panel.

Reference Signal Characteristics

PARAMETER	VALUE
Voltage Range	4-50Vrms
Single Ended Impedance	100k Ohm min 110k Ohm nom
Frequency Range	360Hz-6kHz

Resolver Signal Input Characteristics

PARAMETER	VALUE
Resolver Input Voltage	11.8V L-L
Zin Single Ended	70k Ohm
Zin Differential	140k Ohm
Zin Each Line to Ground	80K Ohm
Common Mode Range	26V peak
Max Voltage Without Damage	100V Transient

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Synchro Converter Operation

The V258 synchro options utilize the *ILC Data Device Corporation* **RDC-19204-304** 16-bit synchro-to-digital converter. This device allows connection of 90V L-L synchro inputs, and a reference input of 4 - 130V rms 47 hz to 1Khz.

The V258 is dynamically configurable for 10, 12, 14 and 16-bit resolution for each of its channels. The operating bandwidth is also programmable, which allows for a multitude of configurations without the need for straps. Connection to the V258 is made through a 50-position connection located on the modules front panel.

Reference Signal Characteristics

PARAMETER	VALUE
Voltage Range	4-130Vrms
Single Ended Impedance	100k Ohm min 110k Ohm nom
Frequency Range	47hz-1Khz

Synchro Signal Input Characteristics

PARAMETER	VALUE
Synchro Input Voltage	90V L-L
Zin Line to Line	123K Ohm
Zin Each Line to Ground	180K Ohm
Common Mode Range	180V max

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V258 implements those required for register-based devices. The V258 also contains a set of Operational registers to monitor and control the functional aspects of the device. Both sets of registers are described in this section.

VXIbus Configuration Registers

Configuration registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. Access to the Configuration registers for all VXIbus modules is available through the VMEbus short (A16) address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ - $FFFF_{16}$). The setting of the Logical Address switches, or the contents of the Logical Address Register are mapped into Address lines A13 through A06, thereby establishing a base address (for the module's Configuration registers) somewhere in the range of $C000_{16}$ to $FFC0_{16}$. For instance, the Logical Address switches are set for Logical Address 128 (80_{16}); the base address for the Configuration registers resides at $E000_{16}$.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Mapping	1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0
Switch Setting			1	0	0	0	0	0	0	0						
A16 Base	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (VXIbus defined).
Bits 05 through 00 are set to zero to indicate a block of 64 bytes.

When Dynamic Configuration is used (Logical Address switches set to 255), the value written to the ID/Logical Address Register defines the A16 base address. For example, a value of 131 (83_{16}) is written to the ID/Logical Address Register. The new base address for the Configuration Registers will be $E0C0_{16}$ as shown below:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Mapping	1	1	LA 128	LA 64	LA 32	LA 16	LA 8	LA 4	LA 2	LA 1	0	0	0	0	0	0
ID/Logical Address Register 07-00			1	0	0	0	0	0	1	1						
A16 Base	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0

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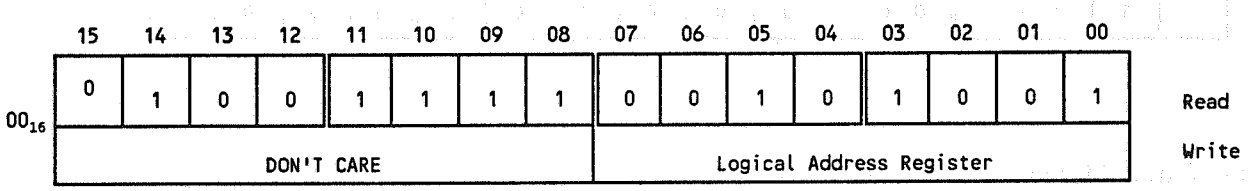
The Configuration registers in the V258 are offset from the base address. Note the V258 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle. Table 2 shows the applicable Configuration Registers present in the V258, their offset from the A16 base address, and their Read/Write capabilities.

Table 2. Configuration Registers - Short (A16) Address Space

A16 Offset (HEX)	Read/Write Capabilities	Register Name
00_{16}	Mixed	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Mixed	Status/Control Register
06_{16}	Mixed	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address register are as follows:

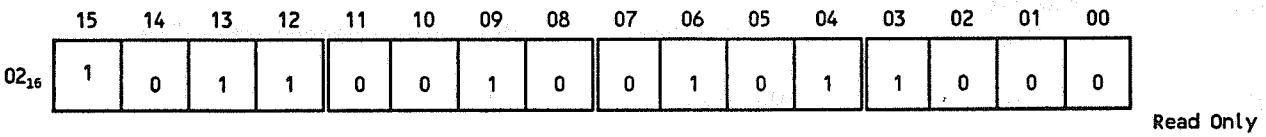


On READ transactions the module returns $4F29_{16}$:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits fifteen through eight are not used. In Dymaically configured systems (i.e., the Logical Address switches are set to a value of 255), bits 07 through 00 are written with the new Logical Address value.

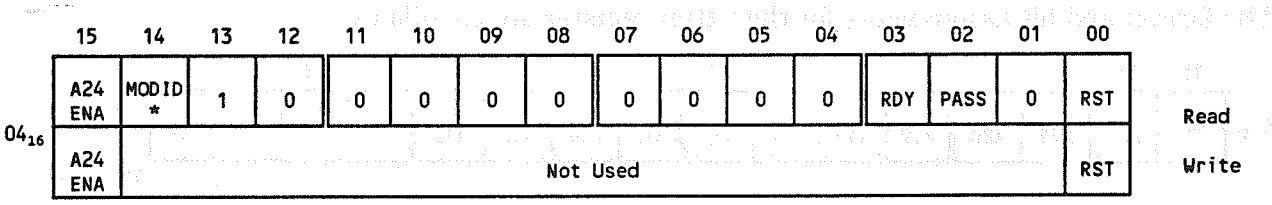
Device Type Register
The format and bit assignments for the Device Type register are as follows:



On READ transactions the module returns $B258_{16}$:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	Requires 4096 bytes of additional memory space.
11 - 0	Model Code	Identifies this device as Model V258 (258_{16}).

Status/Control Register
The format and bit assignments for the Status/Control register are as follows:



Bit(s)	Mnemonic	Meaning
15	A24 Enable (A24 ENA)	This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. This bit must be set to "1" to allow access to the module's OperationalRegisters. Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET* .
14	MODID*	This read only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Not used.	Reads of this bit will always return a "1". Writes to this bit are ignored.
12 - 04	Not used.	When read will return all "0s". These bits are ignored when written.

03	Ready	A "1" indicates the successful completion of register (RDY) initialization.
02	Passed (PASS)	A "1" indicates that the module passed its self-test.
01	Not used.	Not used; read as a "0".
00	Reset (RST)	This Read/Write bit controls the Soft Reset condition within the V258. While the Soft Reset condition is enabled (this bit is written with a "1") any further access to the Operational Registers, except for the Diagnostic and Interrupt Status registers, is inhibited. This bit can be cleared by writing a "0" to this bit location, on power-up, or by the assertion of SYSRESET*.

Offset Register

The format and bit assignments for the Offset register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
06_{16}	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	0	0	0	0

Read/Write

After SYSRESET* and prior to self-test all bits set to "0". Otherwise, a read or write defines the base address of the device's A24 operational registers. Bits 03 through 00 are not used and should always be written with "0s".

Attribute Register

The format and bit assignments for the Attribute register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
08_{16}	Not Used (read as "0s")													1	1	0

Read Only

This Read Only register's lowest bit is read as a "0" to indicate that the V258 has Interrupt Status reporting capability.

Subclass Register

The format and bit assignments for the Subclass register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

Read Only

On READ transactions the module returns $FFFE_{16}$. This indicates that the module is a VXIbus Extended Register Based Device.

Operational Registers

The Operational Registers are the channels through which the various functions of the V258 are controlled. These registers are positioned in VMEbus Standard (A24) Address Space. The base address for these registers is defined by the contents of the Offset Register within the VXIbus Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. Then, using the value in the Offset Register, the A24 base address for the Operational Registers can be calculated. The value held in the Offset Register is mapped onto address lines 23 through 12, as shown below:

Address Lines	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	0
Offset Register	OF 15	OF 14	OF 13	OF 12	OF 11	OF 10	OF 09	OF 08	OF 07	OF 06	OF 05	OF 04	NU	NU	NU	NU								
Operational Register													RO 11	RO 10	RO 09	RO 08	RO 07	RO 06	RO 05	RO 04	RO 03	RO 02	RO 01	RO 00

The four least significant bits in the offset register are not used and assumed to be zero when calculating the A24 Base Address. The upper twelve bits (OF15-OF04) are mapped directly onto the upper twelve address lines (A23-A12) in the VMEbus Standard Address Space. The lower twelve bits of any Operational Register's address are shown as RO11-R00. These bits are the offset of the Operational Register from the base address. For example, the Offset Register contains the value 2040_{16} and it is desirable to access A24 offset $C02_{16}$. The absolute address of the desired register should be at $204C02_{16}$ as shown below:

$$R11\text{-}RO00 = C02_{16}$$
$$OF15\text{-}OF04 = 2040_{16}$$

Address Lines	0	0	1	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0
Offset Register	0	0	1	0	0	0	0	0	0	1	0	0	NU	NU	NU	NU								
Operational Register													1	1	0	0	0	0	0	0	0	0	1	0

Table 3 shows the applicable Operational Registers present in the V258, their offset from the A24 base address, and their Read/Write capabilities.

Table 3. Operational Registers - Standard (A24) Address Space

A24 Offset	Read/Write Mode	Register Description
000_{16}	Mixed	Diagnostic Register
002_{16}	Read Only	Interrupt Status/Identification Register
802_{16} 812	Read Only	Read the Current Value Table (CVT) and increment the Current Value Table Address
812_{16} 816	Read Only	Read Channel 0 Angle Offset Register
816_{16} 81A	Read Only	Read Channel 1 Angle Offset Register
$81A_{16}$ 81E	Read Only	Read Channel 2 Angle Offset Register
$81E_{16}$ 822	Read Only	Read Channel 3 Angle Offset Register
842_{16} 826	Read Only	Read the Current Value Table Address
846_{16} 82A	Read Only	Read the Resolver/Synchro to Digital Configuration Register
872_{16} 82E	Read Only	Read the Interrupt Status Register
876_{16} 832	Read Only	Read the Interrupt Mask Register
$87A_{16}$ 836	Read Only	Read the Interrupt Request Register
$A3E_{16}$ 83A	Read Only	Test for Interrupt Request
$A82_{16}$ 842	Read Only	Clear Interrupt Status Register
$AC2_{16}$ 846	Read Only	Clear the Current Value Table Address
$C02_{16}$ 84A	Write Only	Write Channel 0 Turn Count Register
$C06_{16}$ 84E	Write Only	Write Channel 1 Turn Count Register
$C0A_{16}$ 852	Write Only	Write Channel 2 Turn Count Register
$C0E_{16}$ 856	Write Only	Write Channel 3 Turn Count Register
$C12_{16}$ 85A	Write Only	Write Channel 0 Angle Offset Register
$C16_{16}$ 85E	Write Only	Write Channel 1 Angle Offset Register

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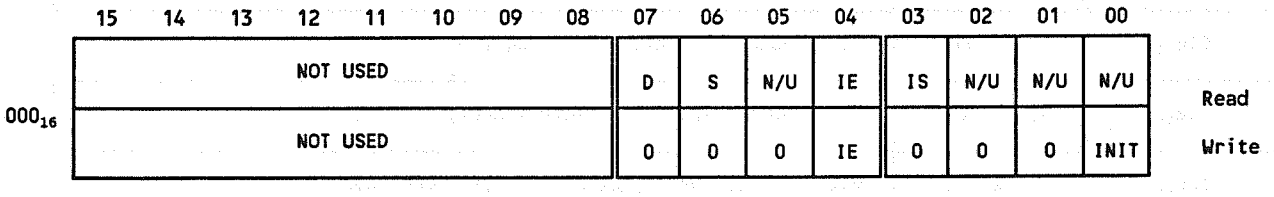
A24 Offset	Read/Write Mode	Register Description
$C1A_{16}$ 862	Write Only	Write Channel 2 Angle Offset Register
$C1E_{16}$ 866	Write Only	Write Channel 3 Angle Offset Register
$C42_{16}$ 86A	Write Only	Write the Current Value Table Address Register
$C46_{16}$ 86E	Write Only	Write the Resolver/Synchro to Digital Configuration Register
$C76_{16}$ 872	Write Only	Write the Interrupt Mask Register
$C82_{16}$ 876	Write Only	Write Channel 0 Turn Count Compare Register
$C86_{16}$ 87A	Write Only	Write Channel 1 Turn Count Compare Register
$C8A_{16}$ 87E	Write Only	Write Channel 2 Turn Count Compare Register
$C8E_{16}$ 882	Write Only	Write Channel 3 Turn Count Compare Register
$C92_{16}$ 886	Write Only	Write Channel 0 Angle Compare Register
$C96_{16}$ 88A	Write Only	Write Channel 1 Angle Compare Register
$C9A_{16}$ 88E	Write Only	Write Channel 2 Angle Compare Register
$C9E_{16}$ 892	Write Only	Write Channel 3 Angle Compare Register
$D82_{16}$ 896	Write Only	Selectively Clear Interrupt Status Register
$E02_{16}$	Read Only	Disable Scanning 89A
$E06_{16}$	Read Only	Disable Offset 89E
$E82_{16}$	Read Only	Enable Scanning 8A2
$E86_{16}$	Read Only	Enable Offset 8A6
$EC2_{16}$	Read Only	Test for Interrupt Source 8AA
$EC6_{16}$	Read Only	Test for Scanning Active 8AE

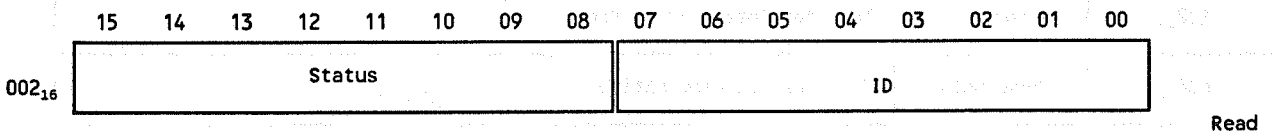
The V258 will only respond to these addresses if the Standard Nonpriviledged Data Access (39_{16}), Standard Nonpriviledged Program Access (3A), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for bus cycles.

Diagnostic Register
The format and bit assignments for the Diagnostic Register are as follows:



Bit(s)	Mnemonic	Meaning
15-08	NOT USED	These bits are not used and read as "0".
07	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (offsets 802_{16} through $EC6_{16}$) was valid.
06	Status	When this bit is set to a "1", the last register access to the Operational Registers (offsets 802_{16} through $EC6_{16}$) was accepted.
05	NOT USED	This bit is not used and read as "0".
04	IE	This bit must be set to a "1" to enable the V258 to generate interrupts.
03	IS	This bit is read as a "1" when the V258 has an Interrupt Request pending.
02-01	NOT USED	This bit is not used and is read as a "0".
00	INIT	Setting this bit will reset the Operational Registers (802_{16} through $EC6_{16}$). The Configuration and the Diagnostic registers are unaffected.

Interrupt Status/Identification Register
The format and bit assignments for the Interrupt Status/ID Register are as follows:



During an interrupt acknowledge cycle, this READ-only register will output a Status/ID value.

Bit(s)	Mnemonic	Meaning
15-08	Status	These bits will indicate a Request True or Request False.

Request True = FD_{16}
Request False = FC_{16}

07-00 ID These bits return the Logical Address of the V258.

Current Value Table

The Current Value Table (CVT) is composed of the Current Value Table Status Word (CVTSW) and eight information words, two for each channel. Each channel's information words contain a value for angle data and turn count data. Together these two entries indicate the shaft position and number of revolutions that the shaft has completed. The following table shows the location of the four channels' data words:

Table 4. Current Value Table Description

Address	Current Value Table Data
0	Status Word
1	Channel 0 Angle Data
2	Channel 0 Turn Count Data
3	Channel 1 Angle Data
4	Channel 1 Turn Count Data
5	Channel 2 Angle Data
6	Channel 2 Turn Count Data
7	Channel 3 Angle Data
8	Channel 3 Turn Count Data

The Current Value Table is read by reading offset 802_{16}. The data returned from this command is dependent on the CVT Address Register. This register points to the CVT entry to be read. After a read to location 802_{16} is executed, the CVT Address Register is automatically incremented, pointing to the next entry in the CVT. After a read from address 8 of the CVT, the CVT Address Register is reset to 0.

The value in the CVT Address Register can be specified by writing to offset $C42_{16}$. Legal data values are from 0 through 8. A read of offset $AC2_{16}$ will reset the CVT Address Register to zero. The current value contained in the CVT Address register may be obtained by reading offset 842_{16}.

Circuitry on the V258 prevents a channel's entry from being updated while data is in the process of being read. For example, if channel 2's angle data has been read, the V258 will not update channel 2's turn count or angle data until the present turn data has been read. This prevents erroneous data readouts from the CVT.

The first element in the CVT is the CVT Status Word. This word contains two bits which define the current operating conditions of the V258. This word also has two bits per channel indicating the individual channel's status.

Current Value Table Status Word

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
SA	OFF ENA	N/U	N/U	N/U	N/U	N/U	N/U	LOS 3	LOS 2	LOS 1	LOS 0	STL 3	STL 2	STL 1	STL 0

Bit	Mnemonic	Function
16	SA	SCAN ACTIVE. When set, this bit indicates that the V258 is in the scanning mode and is capable of updating the CVT.
15	OFF ENA	OFFSET ENABLE. When set, this bit indicates that the channel offset function has been enabled, and the angle data stored reflects the shaft position in relation to the offset angle stored in the channel's Angle Offset register.
14 - 9	N/U	NOT USED. These bits are not used and are read as zero.
8	LOS3	LOSS OF SIGNAL CHANNEL 3. When set, this bit indicates that channel 3 has both inputs disconnected. When both inputs are disconnected, unpredictable convertor performance occurs.
7	LOS2	LOSS OF SIGNAL CHANNEL 2. When set, this bit indicates that channel 2 has both inputs disconnected. When both inputs are disconnected, unpredictable convertor performance occurs.
6	LOS1	LOSS OF SIGNAL CHANNEL 1. When set, this bit indicates that channel 1 has both inputs disconnected. When both inputs are disconnected, unpredictable convertor performance occurs.
5	LOS0	LOSS OF SIGNAL CHANNEL 0. When set, this bit indicates that channel 0 has both nputs disconnected. When both inputs are disconnected, unpredictable convertor performance occurs.
4	STL3	STALE DATA FOR CHANNEL 3. When set, this bit indicates that channel 3 is experiencing a stale data condition. Stale data is defined as having read

		the angle data for the channel, but have not yet read the turn count data for the channel. Data for this channel will not be updated until the stale data condition is removed, either by a reset or reading the turn count data for the channel.
3	STL2	STALE DATA FOR CHANNEL 2. When set, this bit indicates that channel 3 is experiencing a stale data condition. Stale data is defined as having read the angle data for the channel, but have not yet read the turn count data for the channel. Data for this channel will not be updated until the stale data condition is removed, either by a reset or reading the turn count data for the channel.
2	STL1	STALE DATA FOR CHANNEL 1. When set, this bit indicates that channel 3 is experiencing a stale data condition. Stale data is defined as having read the angle data for the channel, but have not yet read the turn count data for the channel. Data for this channel will not be updated until the stale data condition is removed, either by a reset or reading the turn count data for the channel.
1	STL0	STALE DATA FOR CHANNEL 0. When set, this bit indicates that channel 3 is experiencing a stale data condition. Stale data is defined as having read the angle data for the channel, but have not yet read the turn count data for the channel. Data for this channel will not be updated until the stale data condition is removed, either by a reset or reading the turn count data for the channel.

Angle Data

The CVT stores the current angle data for each channel. The V258 is dynamically configurable for angle data size. Refer to the Configuration Register section of this manual for further information on channel configuration. The following table contains the bit weight information for angle data.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1

Table 5. Angle Data Registers' Bit Description

Bit	Degree(s)/Bit	Minute(s)/Bit
16 (MSB All Modes)	180	10,800
15	90	5,400
14	45	2,700
13	22.5	1,350
12	11.25	675
11	5.625	387.5
10	2.813	168.5
9	1.405	84.38
8	.7031	42.19
7 (LSB 10 Bit Mode)	.3516	21.09
6	.1758	10.55
5 (LSB 12 Bit Mode)	.0879	5.27
4	.0439	2.64
3 (LSB 14 Bit Mode)	.0220	1.32
2	.0110	.66
1 (LSB 16 Bit Mode)	.0055	.33

Note: All bits below the LSB for the mode in use (i.e., bits 1 and 2 for the 14-Bit mode) are read as zero.

Turn Count Data

The CVT stores each channel's turn count data. These bits represent the number of turns a shaft makes. Each turn count register is sixteen bits in length. These bits are binary weighted enabling counts from 0 to 65535.

Turns are incremented when the shaft angle passes from the fourth quadrant (the angle is greater than, or equal to, 270 degrees) to the first quadrant (the angle is less than, or equal to, 90 degrees).

Turns are decremented when the shaft angle passes from the first quadrant to the fourth quadrant.

The turn count values can be preset to a predetermined value by writing to offsets $C02_{16}$ through $C0E_{16}$. Offset $C02_{16}$ corresponds to channel 0's turn count, offset $C06_{16}$ corresponds to channel 1's turn count, etc. By presetting the turn count, the user is given the flexibility of generating a true ± counter. By setting the MSB of the register, and using this position as the zero point, the MSB can be used as a sign bit. This allows the V258 to count ± 32767 turns.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1

Current Value Table Address Register

The Current Value Table Address Register is used to set the address of the CVT which is to be read (refer to the Current Value Table section of this manual for a description of the data locations). This register is written by accessing offset $C42_{16}$ and is through offset 842_{16}. Legal data values for this register are from 0 through 8. The Address register can be reset to zero by reading offset $AC2_{16}$.

Note: Care should be taken when changing the values of the address register to avoid a stale data condition for one of the V258's input channels.

The CVTAR is automatically incremented after each read of the Current Value Table (offset 802_{16}). After a CVT read of address 8, the address is automatically reset to 0.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	AD4	AD3	AD2	AD1

Bit	Mnemonic	Function
16:5	N/U	Not Used. These bits are not used and are read as zeros.
4:1	AD4:AD1	Address 4 through 1. These bits are used to specify the CVT address that is to be read. The data written to these bits must be less than or equal to 8. Values greater than 8 can cause erratic readout of the CVT.

Configuration Register

The V258 has a 16-bit configuration register which is used for dynamic configuration of the individual channel converters. The configurable parameters are for converter bandwidth, and converter resolution. This register is modified by writting offset $C46_{16}$, and is read by reading offset 846_{16}. Refer to Table 6 for a description of the resolution control bits; and, Table 7 for more on the bandwidth selection.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
N/U	BW3	B3	A3	N/U	BW2	B2	A2	N/U	BW1	B1	A1	N/U	BW0	B0	A0

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Bit	Mnemonic	Function
16	N/U	Not Used. This bit is not used and is read as zero.
15	BW3	Bandwidth Channel 3. This bit is used to select the operating bandwidth of channel three's converter. A "1" in this position selects the high bandwidth for channel 3.
14	B3	Channel 3 Resolution bit B. This bit is used, in conjunction with resolution bit A, to select the channel converter's data resolution.
13	A3	Channel 3 Resolution bit A. This bit is used, in conjunction with resolution bit B, to select the channel converter's data resolution.
12	N/U	Not Used. This bit is not used and is read as zero.
11	BW2	Bandwidth Channel 2. This bit is used to select the operating bandwidth of channel three's converter. A "1" in this position selects the high bandwidth for channel 2.
10	B2	Channel 2 Resolution bit B. This bit is used, in conjunction with resolution bit A, to select the channel converter's data resolution.
9	A2	Channel 2 Resolution bit A. This bit is used, in conjunction with resolution bit B, to select the channel converter's data resolution.
8	N/U	Not Used. This bit is not used and is read as zero.
7	BW1	Bandwidth Channel 1. This bit is used to select the operating bandwidth of channel three's converter. A "1" in this position selects the high bandwidth for channel 1.
6	B1	Channel 1 Resolution bit B. This bit is used, in conjunction with resolution bit A, to select the channel converter's data resolution.
5	A1	Channel 1 Resolution bit A. This bit is used, in conjunction with resolution bit B, to select the channel converter's data resolution.
4	N/U	Not Used. This bit is not used and is read as zero.

3	BW0	Bandwidth Channel 0. This bit is used to select the operating bandwidth of channel three's converter. A "1" in this position selects the high bandwidth for channel 0.
2	B0	Channel 0 Resolution bit B. This bit is used, in conjunction with resolution bit A, to select the channel converter's data resolution.
1	A0	Channel 0 Resolution bit A. This bit is used, in conjunction with resolution bit B, to select the channel converter's data resolution.

Note: All unused data bits are read as zero.

Table 6. Resolution Control Bits

B	A	Resolution
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Table 7a. Resolver Bandwidth Parameter Table

Parameter	Units	Bandwidth							
		High				Low			
Resolution	Bits	10	12	14	16	10	12	14	16
	Degrees	0.35	0.088	0.022	0.0055	0.35	0.088	0.022	0.0055
Input frequency	kHz	1-6	*	2-6	NR	.36-6	*	*	2-6
Tracking rate	RPS.	800	200	50	12.5	200	50	12.5	3.2
Closed loop bandwidth, CL	Hz	530	*	*	*	130	*	*	*
Acceleration constant, K_a	$1/sec^2$	1.4M	*	*	*	90K	*	*	*
acc-1 LSB lag	$°/sec^2$	512K	128K	32K	8K	32K	8K	2K	500
Settling Time	msec	10	15	30	75	40	60	120	300

* Same as value to the left. . RPS minimum. NR Not recommended

Table 7b. Synchro Bandwidth Parameter Table

Parameter	Units	Bandwidth							
		High				Low			
Resolution	Bits	10	12	14	16	10	12	14	16
	Degrees	0.35	0.088	0.022	0.0055	0.35	0.088	0.022	0.0055
Input frequency	kHz	.36-1	*	*	*	.047-1	*	*	*
Tracking rate	RPS.	160	40	10	2.5	40	10	2.5	0.62
Closed loop bandwidth, CL	Hz	53	*	*	*	13	*	*	*
Acceleration constant, K_a	$1/sec^2$	14.4K	*	*	*	3.6K	*	*	*
acc-1 LSB lag	$°/sec^2$	17K	4.2K	1.1K	260	1.1K	260	66	17
Settling Time	msec	110	110	200	500	550	600	750	1100

* Same as value to the left. . RPS minimum. NR Not recommended

Angle Offset Registers

The V258 has the capability of generating an arbitrary zero angle reference point. This is accomplished by means of an angle offset register, and an angle offset enable/disable function. These registers are written by accessing locations $C12_{16}$ through $C1E_{16}$. They are read through offsets 812_{16} through $81E_{16}$.

V258 angle offsets are enabled by reading offset $E86_{16}$. This command enables the offset registers for all channels on the V258. The offset function can be disabled by reading offset $E06_{16}$.

Each channel has its own register. These registers may be written with a value which is equal to the desired zero degree reference point.

With the V258 in the Offset Enable mode, the value in the angle offset register is subtracted from the current input angle for a given channel. The difference of these two angles is stored as the channel's angle data position in the CVT, thus generating a new zero reference point for the channel. This value is also used to increment or decrement the channel's turn count value.

With the V258 in the Offset Disable mode, the value in the channel's angle offset register is ignored and the input angle position is stored.

The following diagram shows the angle offset register data format for each channel. Notice that the data format is the same as the stored CVT angle data.

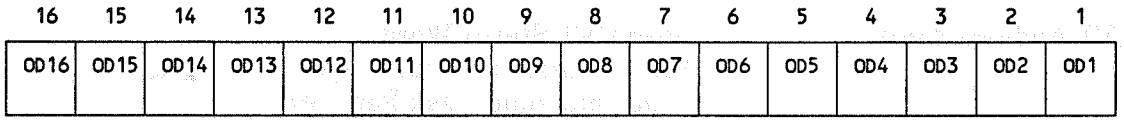

Table 8. Angle Offset Register Data Format

Bit	Degree(s)/Bit	Minute(s)/Bit
16	180	10,800
15	90	5,400
14	45	2,700
13	22.5	1,350
12	11.25	675
11	5.625	387.5
10	2.813	168.5
9	1.405	84.38
8	.7031	42.19
7 (LSB 10-bit Mode)	.3516	21.09
6	.1758	10.55
5 (LSB 12-bit Mode)	.0879	5.27

4	.0439	2.64
3 (LSB 14-bit Mode)	.0220	1.32
2	.0110	.66
1 (LSB 16-bit Mode)	.0055	.33

Note: All bits below the LSB for the mode in use (i.e., bits 1 and 2 for the 14 Bit mode) should be written as zero.

Interrupt Structure

The V258 can generate an interrupt from one of eight sources. Each channel can generate an interrupt if its channel experiences as an LOS (Loss Of Signal) condition. This condition occurs when the channel's converter detects an open on both channel signal inputs. These interrupts should be considered a drastic failure in the system and appropriate action should be taken to restore the input signals to the V258.

Each channel has the capability of setting an interrupt by reaching its compare value. The V258 contains four channel compare registers. These may be used for generating an interrupt when the input angle and turn count matches, or passes through, the user defined value contained in the channel's compare register.

The following is a list of offsets in A24 space which are used to monitor and control interrupts.

802_{16} (At CVT Address Zero)	Read CVT Status Word
872_{16}	Read Interrupt Status Register
876_{16}	Read Interrupt Mask Register
$87A_{16}$	Read Interrupt Request Register
$A3E_{16}$	Test for Interrupt Request
$A82_{16}$	Clear Interrupt Status Bits
$C76_{16}$	Write Interrupt Mask Register
$C82_{16}$ through $C8E_{16}$	Write Channel Turn Count Compare Registers
$C92_{16}$ through $C9E_{16}$	Write Channel Angle Compare Registers
$DB2_{16}$	Selectively Clear Interrupt Status Bits
$EC2_{16}$	Test for Interrupt Source

Channel Compare Register

The V258 contains a compare register for each channel. These write-only registers contain a 32-bit value which describes a channel's compare point. This value is a 16-bit angle value and a 16-bit turn value.

The turn count compare value for these registers is written by accessing offsets $C82_{16}$ through $C8E_{16}$. A24 offset $C82_{16}$ corresponds to channel 0's turn count compare register, C86 corresponds to channel 1's turn count compare register, etc.

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The angle compare value for these registers is written by accessing offsets $C92_{16}$ through $C9E_{16}$. $C92_{16}$ corresponds to channel 0's angle compare register, $C96_{16}$ corresponds to channel 1's angle compare register, etc.

When a channel input value matches or passes through (goes from less than to greater than, or greater than to less than) its compare value (both angle and turn count), the V258 sets a latch in the Interrupt Status register. This can be used to generate an interrupt to notify the user that the channel has reached its compare point, allowing the user to take appropriate action.

By utilizing the interrupt facilities, the host computer does not need to constantly read the V258's CVT to determine when a given angle and turn value has been reached.

Note: A compare value of 00000000_{16} is not recommended. Due to the nature of the comparators, this value must be matched or a pass through will not be possible.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
TD16	TD15	TD14	TD13	TD12	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4	TD3	TD2	TD1

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
CD32	CD31	CD30	CD29	CD28	CD27	CD26	CD25	CD24	CD23	CD22	CD21	CD20	CD19	CD18	CD17

BIT	DEG/BIT	MIN/BIT
16	180	10,800
15	90	5,400
14	45	2,700
13	22.5	1,350
12	11.25	675
11	5.625	387.5
10	2.813	168.5
9	1.405	84.38
8	.7031	42.19
7	.3516	21.09
6	.1758	10.55
5	.0879	5.27
4	.0439	2.64
3	.0220	1.32
2	.0110	.66
1	.0055	.33

Note: All bits below the LSB for the mode in use (i.e., bits 1 and 2 for the 14-Bit mode) should be written as zero.

Interrupt Status Register

The Interrupt Status Register is a 16-bit read only register which provides access to the four LOS and four compare bits. The Interrupt Status bits may also be read in the CVT Status Word. Refer to the Current Value Table section of this manual for additional information.

For bits 1 through 4, a bit which is read as a one indicates that the corresponding channel has, at some time, experienced a Loss Of Signal (all signal inputs have opened) at some time. For bits 5 through 8, a bit read which is read as a one indicates that the corresponding channel has met its compare value, as described in the Channel Compare Registers section of this manual.

All Interrupt Status bits are cleared on power-up, after setting the INIT bit in the Diagnostic Register, a Clear Interrupt Status command, or a Selective Clear Interrupt Status command.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	CMP3	CMP2	CMP1	CMP0	LOS3	LOS2	LOS1	LOS0

Bit	Mnemonic	Function
16:9	N/U	Not Used. These bits are not used and are read as zero.
8:5	CMP3-CMP0	Compare 3 through 0. These bits represent the compare bits for the individual channels.
4:1	LOS3-LOS0	Loss Of Signal 3 through 0. These bits represent the Loss of Signal bits for the individual channels.

Interrupt Mask Register

The Interrupt Mask Register is used to specify which of the interrupt status bits are to generate an Interrupt Request. If an Interrupt Status bit is to assert an interupt, it must first be masked on by writing a one to the corresponding bit in the Interrupt Mask register. The Interrupt Mask register is written by accessing offset $C76_{16}$, and is read by accessing offset 876_{16}. The Interrupt Mask register is reset to zero on power-up or by setting the INIT bit in the Diagnostic Register.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	IM8	IM7	IM6	IM5	IM4	IM3	IM2	IM1

Bit	Mnemonic	Function
16:9	N/U	Not Used. These bits are not used and are read as zero
8:1	IM8:IM1	Interrupt Mask 8 through 1. These bits are written to enable/disable a generation of an Interrupt Request by the corresponding Interrupt Status bits (see Table 9) .

Interrupt Request Register

The Interrupt Request Register is used to determine the source of an interrupt generated by the V258. An interrupt is asserted when an Interrupt Status bit is true AND its corresponding Interrupt Mask bit is enabled (set to one).

The Interrupt Request register is a read-only register which is accessed by reading offset $87A_{16}$. The Interrupt Request register is cleared on power-up, setting the INIT bit in the Diagnostic Register, clearing the Interrupt Status bits, or clearing the Interrupt Mask bits.

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
N/U	N/U	N/U	N/U	N/U	N/U	N/U	N/U	IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1

Bit	Mnemonic	Function
16:9	N/U	Not Used. These bits are not used and are read as zero.
8:1	IR8:IR1	Interupt Request 8 through 1. These read-only bits indicate which conditions have occurred in the V258 to cause an interrupt to be generated. For these bits to be set to a one, the corresponding Interrupt Status bit and Interrupt Mask bit (see Table 9) must be set to a one.

Table 9. Interrupt Mask/Request/Source Mapping

Interrupt Mask Bit	Interrupt Request Bit	Interrupt Source
IM8	IR8	CPM3
IM7	IR7	CPM2
IM6	IR6	CPM1
IM5	IR5	CPM0
IM4	IR4	LOS3
IM3	IR3	LOS2
IM2	IR2	LOS1
IM1	IR1	LOS0

Operational Register Overview

802_{16} - Read the Current Value Table and Increment the Address

This is used to read the data contained in the Current Value Table (CVT). After the data at the addressed location is read, the CVT address is incremented.

The first entry in the CVT (address 0) contains the Status Word. Refer to the Current Value Table section of this manual for further information on the Status Word. The next eight entries in the CVT contain the angle and turn count values for each of the four channels. Refer to the Current Value Table section of this manual for a detailed description of the CVT. After the turn count data of channel four is read, the address returns to zero thus pointing to the Status Word.

812_{16} - $81E_{16}$ - Read Channel Offset Registers

These offsets, 812_{16} - $81E_{16}$, read channel 0 through channel 3 (respectively) offset register data. Refer to the Offset Register section of this manual for a detailed description of the Offset register function and contents.

842_{16} - Read the CVT Address Register

This offset is used to read the contents of the CVT address register. Refer to the Current Value Table section of this manual for further information on the register contents.

846_{16} - Read the Configuration Register

A read of this offset returns the value of the V258 Resolver to Digital Configuration register. The data in this register contains set-up information for the individual channels of the V258. Refer to the Configuration Register section of this manual for a detailed description of the register's contents.

872_{16} - Read the Interrupt Status Register

This offset is used to read the contents of the Iterrupt Status register. Refer to the Interrupt Structure section of this manual for a detailed description of this register.

876_{16} - Read the Interrupt Mask Register

The data in this register indicates which conditions are masked on and are capable of setting a interrupt condition. Refer to the Interrupt Structure section of this manual for further information.

$87A_{16}$ - Read the Interrupt Request Register

This offset is used to read the contents of the Interrupt Request register. The data in this register indicates which conditions caused an interrupt to be generated. Refer to the Interrupt Structure section of this manual for further information on this command.

$A3E_{16}$ - Test for Interrupt Request

This offset is used to determine if the V258 is generating an Interrupt Request. If true, the Status bit in the Diagnostic Register will be set after a read of this offset. If false, this bit will be read as a "0". Refer to the Interrupt Structure section of this manual for further information on this command.

$A82_{16}$ - Clear Interrupt Status Register

Reading this register will clear all the bits in the Interrupt Status register. Refer to the Interrupt Structure section of this manual for further information on interrupt operations.

$AC2_{16}$ - Clear the CVT Address Register

A read of this register is used to reset the CVT address to zero. Refer to the Current Value Table section of this manual for details on the operation of this command.

$C02_{16}$ - $C0E_{16}$ - Write Channel Turn Count Registers

Writes to offsets $C02_{16}$ - $C0E_{16}$ are used to specify channels 0 - 3 Turn Count Registers, respectively. The Turn Count values for each channel can be preset to a given value by utilizing these commands. Accesses to these locations will set the Status bit in the Diagnostic Register if the V258 is not in the busy state. This bit will be read as a "0" if the V258 is in the busy state. Busy is set when a command which affects angle or turn data is issued. The busy state is exited when the V258 has updated the angle and turn data for the channel affected.

$C12_{16}$- $C1E_{16}$ - Write Channel 0 - 3 Angle Offset Registers

Offsets $C12_{16}$ - $C1E_{16}$ are used to write channels 0 - 3 angle offset registers, respectively. The Status bit in the Diagnostic Register will be read as a "1" if the V258 is in the not busy state. This bit will be read as a "0" if the V258 is in the busy state. The Angle Offset register function is described in the Convertor Operation section of this manual.

$C42_{16}$ - Write the CVT Address Register

This offset is used to write the CVT Address register. The valid data range is from 0 through 8. Refer to the Current Value Table section of this manual for further detail on the CVT operation.

$C46_{16}$ - Write the Resolver to Digital Configuration Register

Thi offset is used to write the V258's Resolver to Digital Configuration Register. This register is used for configuring the individual channel operation parameters. Refer to the Configuration Register section of this manual for further details on the function of this register.

$C76_{16}$ - Write the Interrupt Mask Register

A write to this register is used to enable/disable specific interrupt sources. Refer to the Interrput Structure section of this manual for a complete description of the interrupt functions of the V258.

$C82_{16}$ - $C8E_{16}$ - Write channel 0 - 3 Turn Count Compare Registers

These write-only registers are used to specify turn count value(s) that the inputs are to be compared with. Refer to the Channel Compare Register section of this manual for a complete description of the compare registers.

$C92_{16}$ - $C9E_{16}$ - Write channel 0 - 3 Angle Compare Registers

These write-only registers specify he Angle Compare value(s) that inputs are to be compared with. Refer to the Channel Compare Register section of this manual for a complete description of the compare registers.

$D82_{16}$ - Selectively Clear the Interrupt Status Register

This offset is used to selectively clear the individual bits of the Interruupt Status register. Refer to the Interrupt Structure section of this manual for a complete description of this command.

$E02_{16}$ - Disable Scanning

Reading this offset disables the V258 from scanning the channel data registers and updating the CVT. With scanning disabled, the V258 will not update the CVT. The internal channel operation continues to function. This allows the V258 to continue tracking the signal inputs.

$E06_{16}$ - Disable Offset

A read of this offset will disable the offset function of the V258. This access will be valid when the V258 is in the not busy state. Refer to the decription of Channel Turn Count Registers section of this manual for a definition of busy. The offset function is fully described in the Convertor Operation section of this manual.

$E82_{16}$ - Enable Scanning

Reading this offset will enable the scanning function of the V258. With scanning enabled, the V258 CVT is updated with the individual channel's data. Refer to the Current Value Table section of this manual for a complete description of the CVT operation.

$E86_{16}$ - Enable Offset

A read of this register will enable the offset function of the V258. Accesses to this location will be successful when the V258 is in the not busy state. Refer to the decription of Channel Turn Count Registers section of this manual for a definition of busy. The offset function is fully described in the Convertor Operation section of this manual.

$EC2_{16}$ - Test for Interrupt Source

A read of this register will return a response that is used to determine if any bits in the Interrupt Status register are set. After a read to this offset, the Status bit in the Diagnostic Register will be set to a "1" if any of the bits in the Interrupt Status Register are set. Else, the Status bit will be read as a "0". Refer to the Interrupt Structure section of this manual for further information on the interrupt functions of the V258.

$EC6_{16}$ - Test for Scan Active

A read of this register will test for scanning active and set the Status bit in the Diagnostic register if true. If scanning is not enabled, the Status bit will be read as a "0". Refer to the Current Value Table section of this manual for the effects of scan enabling/disabling.

APPENDIX A

RESOLVER RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES

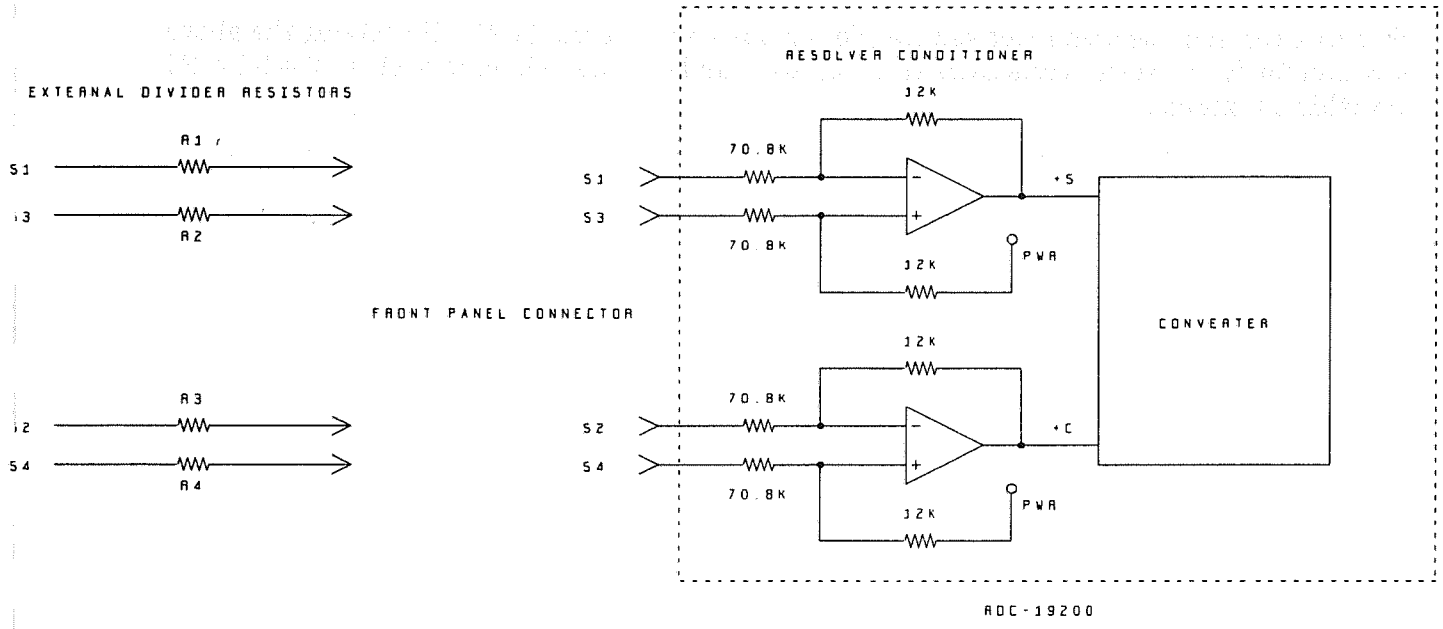


Figure 3 - Non -Standard Voltage Configuration

Model V258

As shown in Figure 3, to accommodate non-standard input voltages, a simple voltage divider can be used to attenuate both the sine and cosine inputs. This is accomplished by using four external resistors, one in series with each input line, ahead of the resolver conditioner to scale down the voltage.

$$\frac{R+70.8k\Omega}{70.8k\Omega} = \frac{Voltage}{11.8V}$$

Note that the input desired input voltage (Voltage) is greater than 11.8V. By solving the above equation for R, the series resistance value needed can be found. Note: R = R1 = R2 = R3 = R4 to within 1% match.

APPENDIX B

The following is a procedure used to configure the V258. Each reading describes a general function followed by the steps needed to accomplish the function. For a more detailed description of each operation, refer to the Operational Registers section of this manual.

Initialization

1.) Enable Operational Registers
2.) Establish A24 Base Address

Resetting Device

1.) Initialization
2.) Initialize A24 Registers (Diagnostic Register)

Configuring Resolver-to-Digital Converter

1.) Initialization
2.) Write Desired Configuration (Resolver/Synchro-to-Digital Configuration Register)
3.) Read Configuration (Resolver-to-Digital Configuration Register)

Reading All Channel Angle and Turn Count Values

1.) Reset Device
2.) Configure Resolver-to-Digital Converter
3.) Enable Scanning
4.) Clear Current Value Table Address
5.) Read Current Value Table and Increment Address (Status Word)
6.) Read Current Value Table and Increment Address (CH 0 Angle Data)
7.) Read Current Value Table and Increment Address (CH 0 Turn Count Data)
8.) Read Current Value Table and Increment Address (CH 1 Angle Data)
9.) Read Current Value Table and Increment Address (CH 1 Turn Count Data)
10.) Read Current Value Table and Increment Address (CH 2 Angle Data)

11.) Read Current Value Table and Increment Address (CH 2 Turn Count Data)
12.) Read Current Value Table and Increment Address (CH 3 Angle Data)
13.) Read Current Value Table and Increment Address (CH 3 Turn Count Data)

Reading Specific Channel Angle and Turn Count Values

1.) Reset Device
2.) Configure Resolver-to-Digital Converter
3.) Enable Scanning
4.) Clear Current Value Table Address
5.) Read Current Value Table and Increment Address (Status Word)
6.) Write Current Value Table Address Register (?)
7.) Read Current Value Table and Increment Address (CH ? Angle Data)
8.) Read Current Value Table and Increment Address (CH ? Turn Count Data)

Establishing Channel Reference Points

1.) Read Channel Angle and Turn Count Values
2.) Disable Scanning
3.) Claculate Reference Point
4.) Write Angle Offset Registers
5.) Enable Scanning
6.) Enable Offset

Using Channel Compare Registers

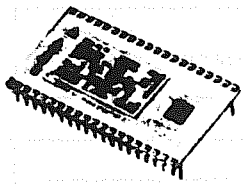
1.) Read Channel Angle and Turn Count Values
2.) Disable Scanning
3.) Disable Offset
4.) Calculate Compare Values
5.) Write Channel Angle and Turn Count Compare Registers
6.) Enable Scanning
7.) Enable Ofset (if used)
8.) Poll or test wait for Interrupt

APPENDIX C

Resolver-to-Digital Converter Data Sheet

DDC
ILC DATA DEVICE CORPORATION

RDC-19200® MONOBRID® SERIES



10, 12, 14, OR 16 BIT INDUSTRIAL RESOLVER TO DIGITAL CONVERTERS

DESCRIPTION

The RDC-19200 Monobrid Series are versatile state-of-the-art resolver to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes + 1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

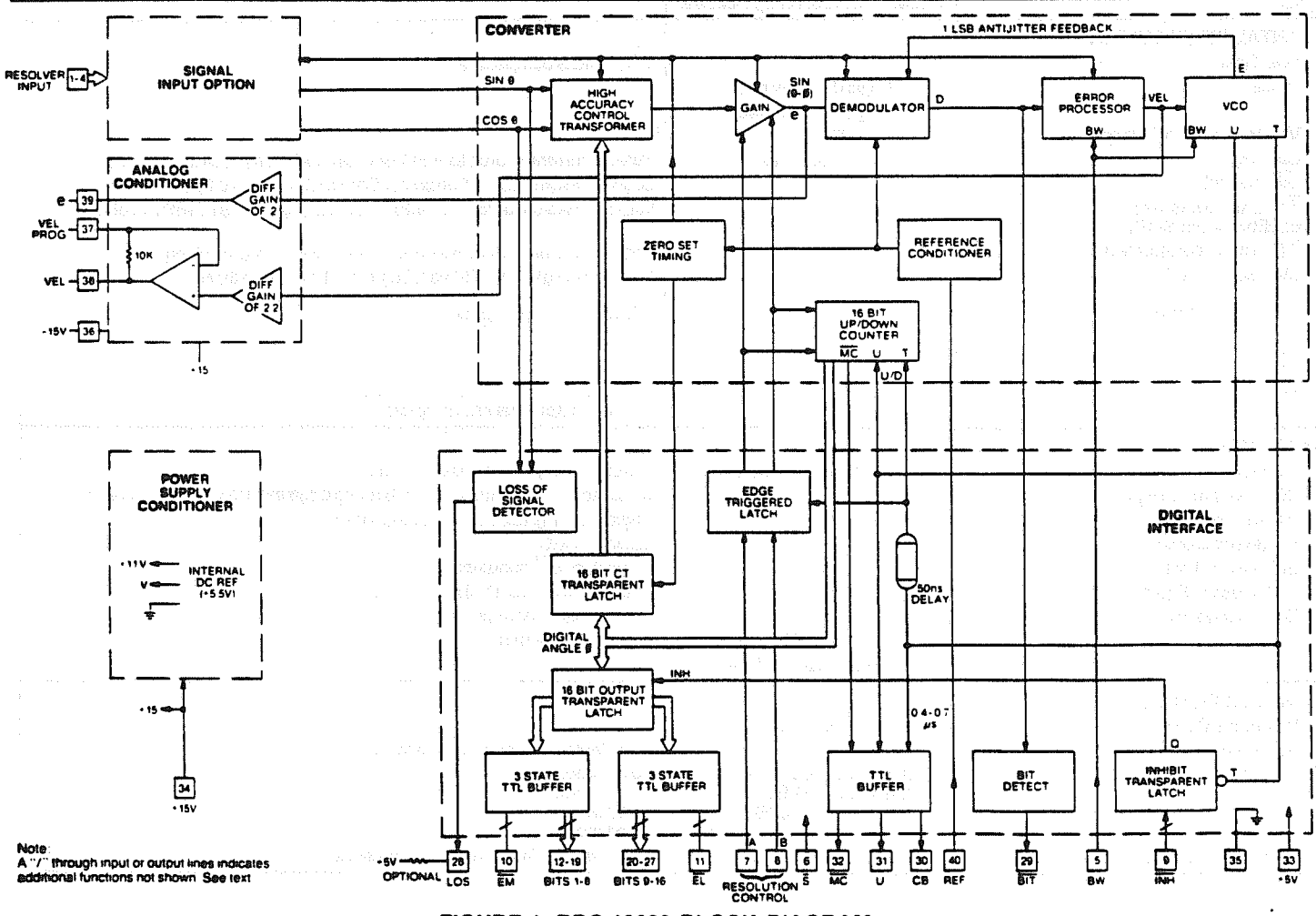
The velocity output (VEL) from the RDC-19200 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0% or 0.7%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The RDC-19200 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the RDC-19200 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST (BIT) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*



Note:
A "/" through input or output lines indicates additional functions not shown. See text.

FIGURE 1. RDC-19200 BLOCK DIAGRAM

TABLE 1. RDC-19200 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency and amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	10, 8, 4, 3, 2 minutes	Max +1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-50Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	360Hz to 6KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Resolver	11.8V L-L	
Z_{in} Single Ended	70K Ohm	
Z_{in} Differential	140K Ohm	
Z_{in} Each line-ground	80K Ohm	
Common Mode Range	26V peak	
Max Voltage w/o damage	100V transient	
Direct	2.0V L-L	
Input Signal Type		Sin and Cos resolver signal referenced to converter's internal DC ref voltage of +5.5V.
Sin/Cos Voltage Range	2V nom, 2.3V max	
Max Voltage w/o Damage	15V continuous, 110V peak transient	
Z_{in}	>20M ohm//10pf voltage follower	
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	−0.3 to 11V	
Loading	−10 μA max	Pull-up current source to +5V//5pf max CMOS transient protected.
$\overline{INH}$ (Inhibit)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3μs
$\overline{EM}$ (Enable bits 1-8) $\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
BW (Bandwidth)		Logic 1 = High BW (530 Hz); Logic 0 = Low BW (130 Hz)
Resolution Control 10 Bit 12 Bit 14 Bit 16 Bit		B (pin8) / A (pin 7) 0 / 0 0 / 1 1 / 0 1 / 1 Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 μs to 0.7 μs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3μA pull-up to +5V).
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10μA/5pf max	−1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

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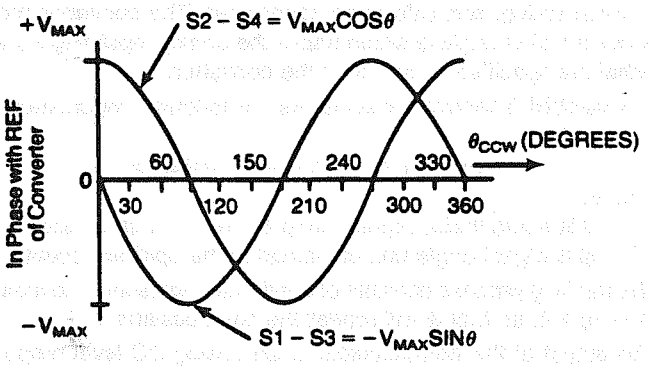
TABLE 1. RDC-19200 SPECIFICATIONS (Continued)

PARAMETER	VALUE			DESCRIPTION
POWER SUPPLY CHARACTERISTICS				
Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	−15VDC ±5%	Note: When analog outputs are not required, ground −15V (pin 36).
Max Voltage w/o Damage	+18V	+8V	−18V	
Max Current	25mA	10mA	15mA	
TEMPERATURE RANGES				
Operating	0°C to +70°C			
Storage	−40°C to +120°C			
PHYSICAL CHARACTERISTICS				
Size	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm)			40 pin TDIP
Weight	0.46 oz (13 gm)			

TECHNICAL INFORMATION

INTRODUCTION

The RDC-19200 Series are small, 40 pin TDIP resolver to digital hybrid converters. As shown in the block diagram (figure 1), the RDC-19200 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. RESOLVER SIGNALS

SIGNAL INPUT OPTIONS

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The converter internal to the RDC-19200 operates with signals in resolver format, $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 shows the resolver signals as a function of the angle θ. The RDC-19200 accepts solid state resolver (11.8Vrms) and direct (2Vrms) inputs. The reference is a single ended input with 100K ohm impedance.

2V DIRECT INPUT OPTION. The direct inputs are transient protected voltage followers which accept 2Vrms resolver inputs, as shown in figure 3. A 2V input from a resolver allows use of a lower reference voltage. This lowers oscillator cost and allows a lower power reference oscillator.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

11.8V RESOLVER INPUT OPTION. The 11.8V resolver inputs are true differential inputs with high AC and DC common mode rejection (see figure 4). Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed 26V peak; maximum transient peak voltage should not exceed 100V.

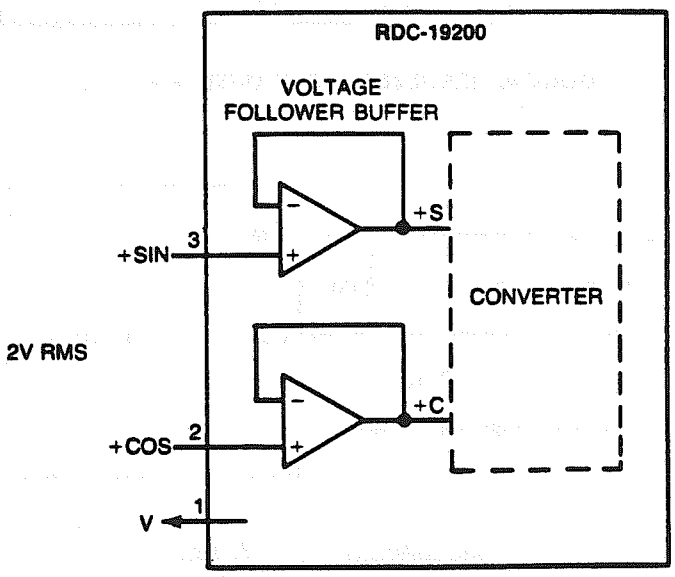


FIGURE 3. DIRECT INPUT OPTION - 2V

RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES. When applying voltages greater than 2Vrms, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers, there will be no loading on the resistor dividers (see figure 5).

The 11.8V resolver input conditioner consists of two differential amplifiers. The 11.8V input is scaled down to 2V. When applying resolver inputs greater than 11.8V, four resistors, one in series with each input line, can be used to scale down the voltage (see figure 6).

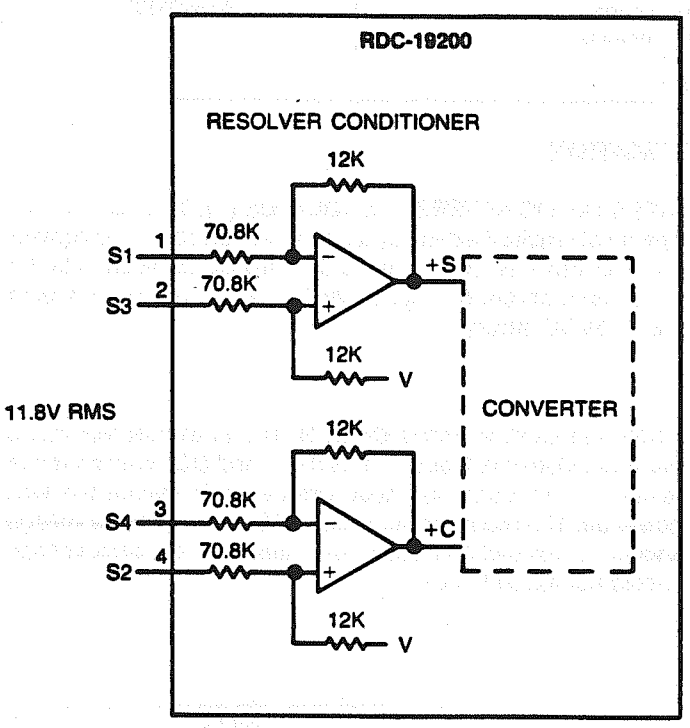
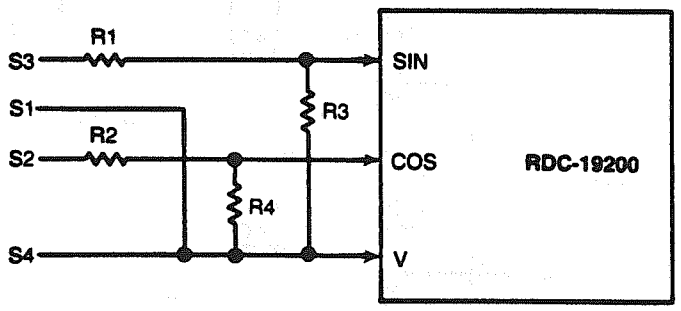


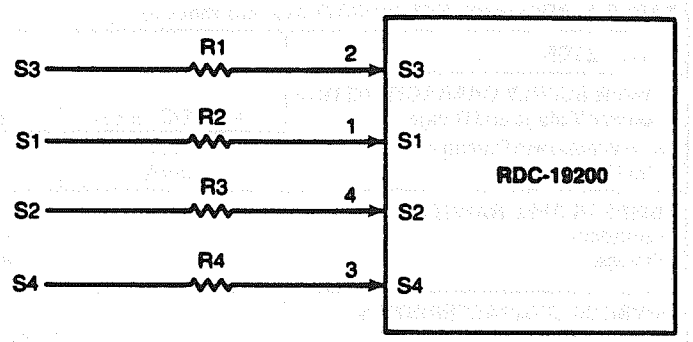
FIGURE 4. RESOLVER INPUT OPTION – 11.8V



$$\frac{\text{Input Voltage L-L}}{2V} = \frac{R1 + R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 5. INPUT RESISTOR SCALING – 2V



$$\frac{R + 70.8K}{70.8K} = \frac{\text{Input Voltage L-L}}{11.8V}$$

Notes:
(1) Input Voltage L-L is greater than 11.8V.
(2) R = R1 = R2 = R3 = R4 to 0.1% match.

FIGURE 6. INPUT RESISTOR SCALING – 11.8V

CONVERTER OPERATION

As shown in figure 1, the converter section of the RDC-19200 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \Phi 0$, so that ϕ will repeat the shaft position θ.

The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The RDC-19200 has unique **zero-set timing** circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

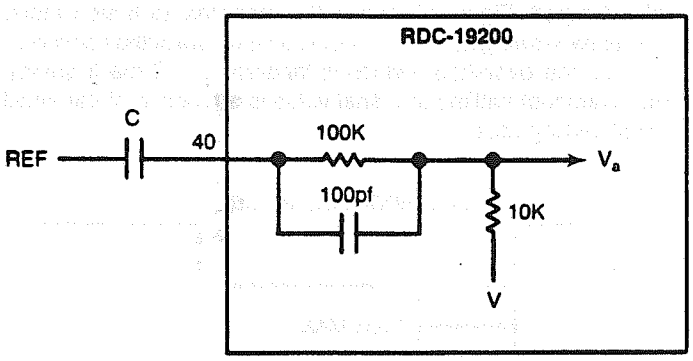
The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical

E

performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive.

MINIMIZING ERRORS DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the resolver input. To determine the capacitor's value, see figure 7.



Note:
Choose C such that the V_a to REF phase lead is equal to the resolver to REF phase lead plus 9μs.

FIGURE 7. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min ≃ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the RDC-19200.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the RDC-19200, applying an Inhibit ($\overline{INH}$) command will lock the data in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by −10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS		
BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.5
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.879	5.27
13	0.439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33
Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.		

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 8). The angle is determined by the sum of the bits at logic 1.

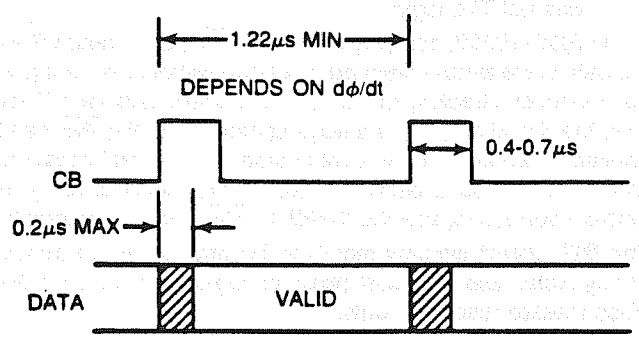


FIGURE 8. CB TIMING

INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the RDC-19200, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 9). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 10 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

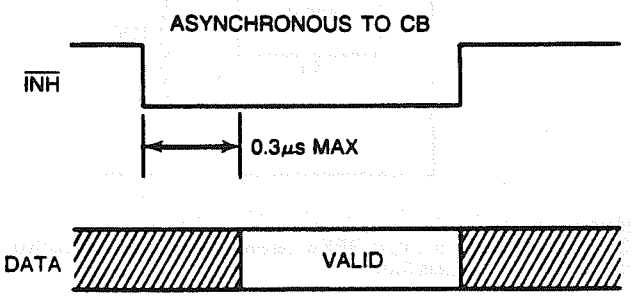


FIGURE 9. INHIBIT TIMING

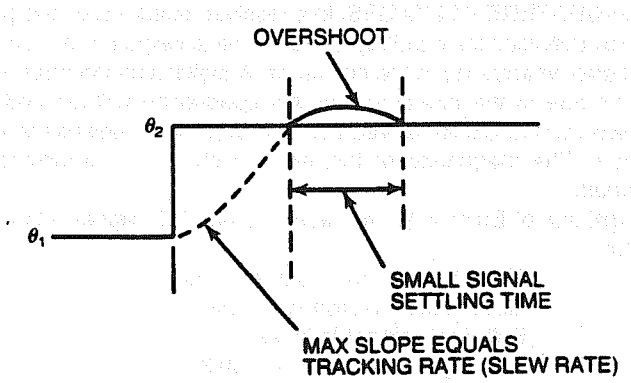


FIGURE 10. RESPONSE TO A STEP INPUT

DATA TRANSFERS

Digital output data from the RDC-19200 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially (see figures 11 and 12). For 16 bit systems, all bits are transferred at the same time (see figures 13 and 14).

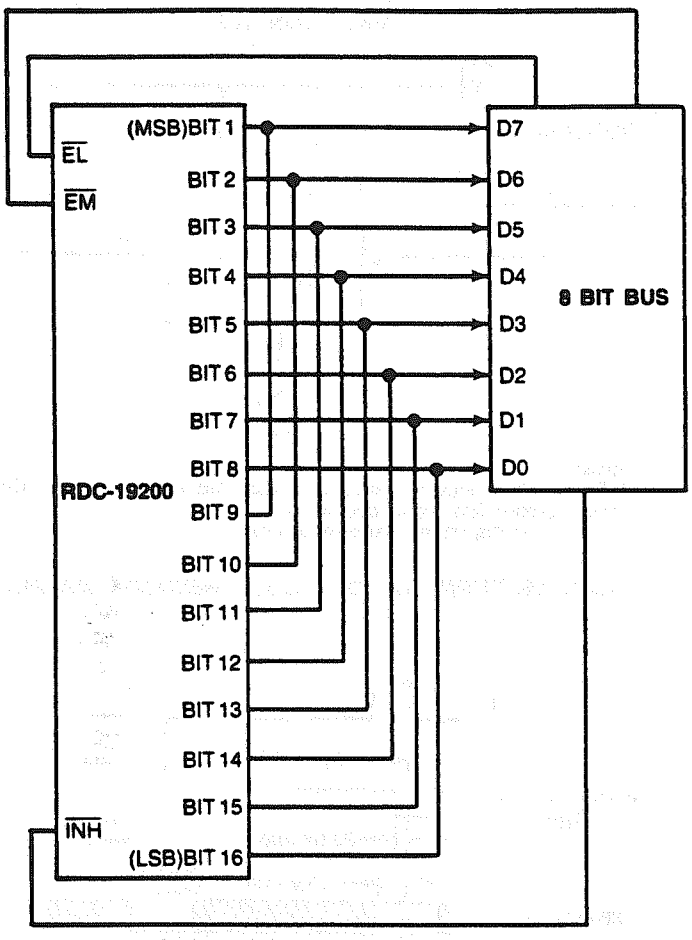


FIGURE 11. DATA TRANSFER TO 8 BIT BUS

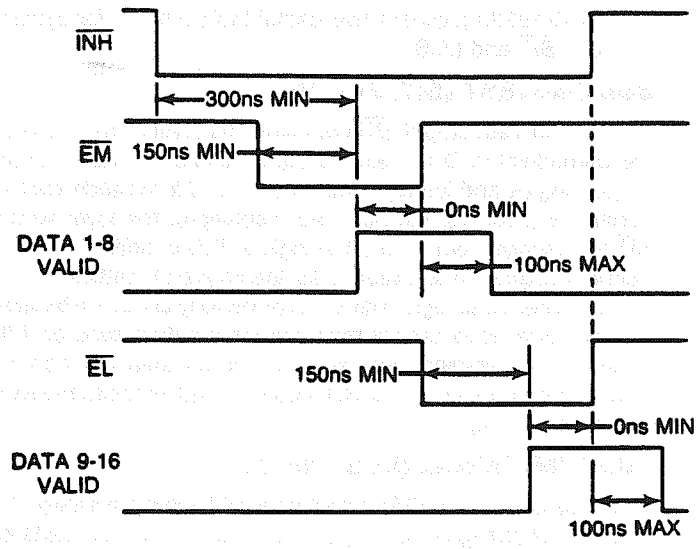


FIGURE 12. DATA TRANSFER TO 8 BIT BUS TIMING

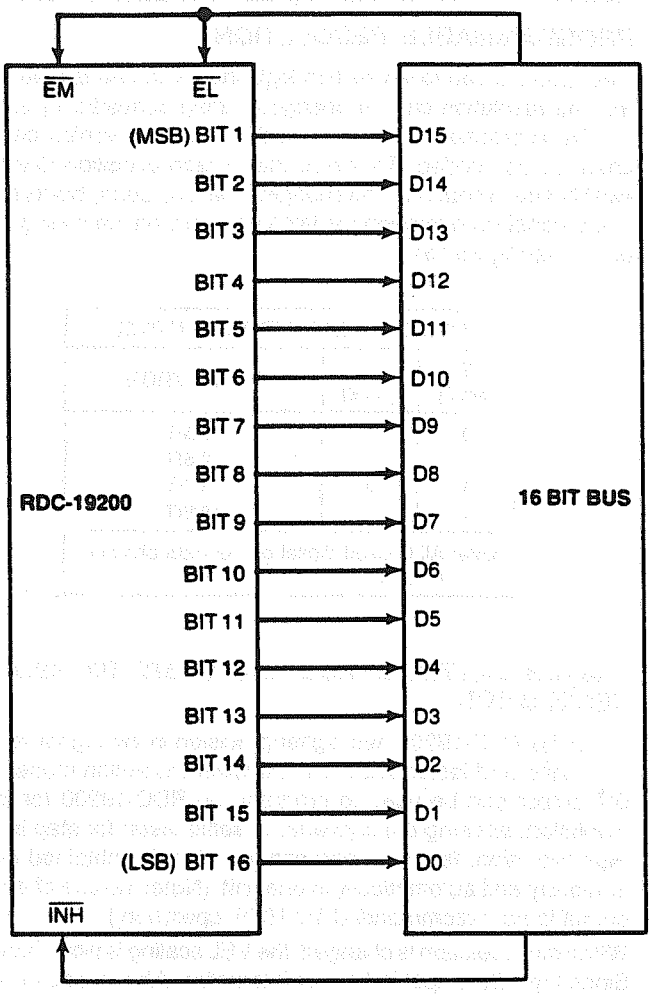


FIGURE 13. 16 BIT DATA TRANSFER

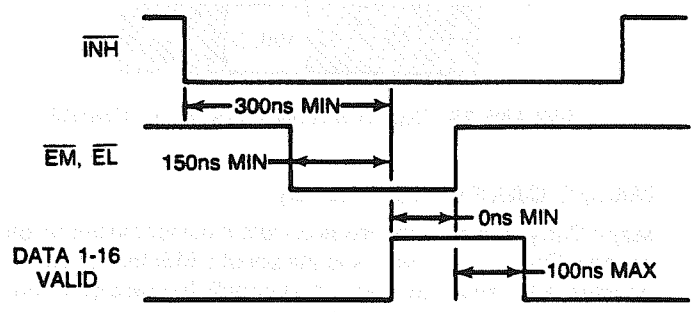


FIGURE 14. 16 BIT DATA TRANSFER TIMING

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 15).

TABLE 3. RESOLUTION CONTROL

B (pin 7)	A (pin 8)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0.

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the RDC-19200 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the RDC-19200 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth (see figure 22).

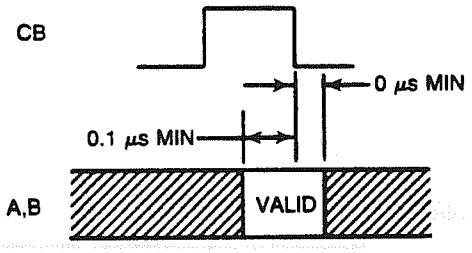


FIGURE 15. RESOLUTION CONTROL TIMING

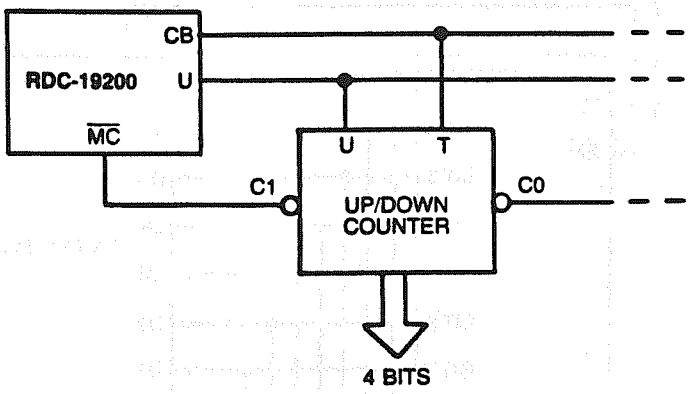
MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 16 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 17. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5µs before and at least 20ns after the leading edge of CB.

TURNS COUNTING



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

FIGURE 16. TURNS COUNTING CONNECTION DIAGRAM

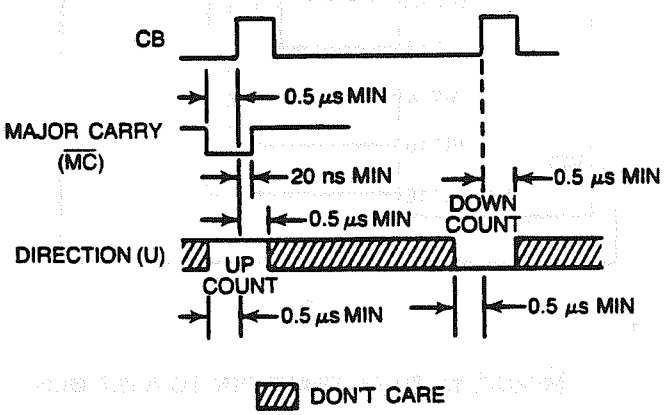


FIGURE 17. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The RDC-19200 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

If the LOS signal is used with the 2V Direct Input option, connect a 10M ohm resistor from +S to V and from +C to V. This will insure that if the input resolver signal opens, the input pin will go to V volts.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (130 Hz nom), while a logic 1 selects high bandwidth (530 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\,A/\pi$$

$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figures 23 and 24 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

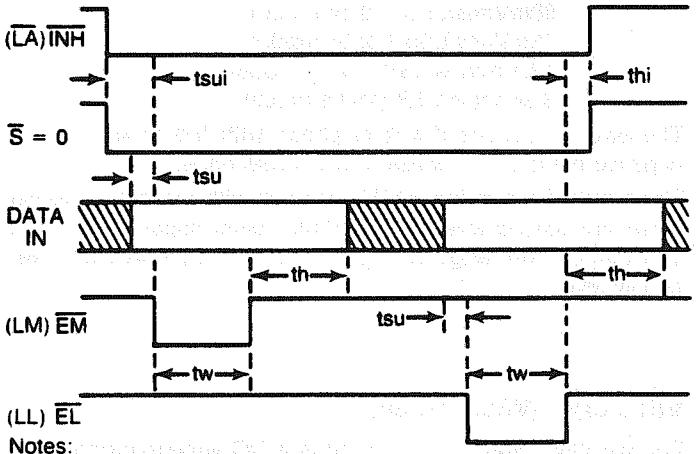
PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	1-6	*	2-6	NR	.36-6	*	*	2-6
Tracking Rate	RPS†	800	200	50	12.5	200	50	12.5	3.2
Bandwidth, CL	Hz	530	*	*	*	130	*	*	*
K_a	1/sec²	1.4M	*	*	*	90K	*	*	*
A1**	1/sec	8	*	*	*	2	*	*	*
A2**	1/sec	178	*	*	*	45K	*	*	*
A**	1/sec	1200	*	*	*	300	*	*	*
B**	1/sec	600	*	*	*	150	*	*	*
acc-1 LSB lag	°/sec²	512K	128K	32K	8K	32K	8K	2K	500
Settling time	msec	10	15	30	75	40	60	120	300

†RPS minimum
*Same as value to left
**See figure 24 for definitions of A1, A2, A, and B.

CONTROL TRANSFORMER MODE ($\overline{S}$, PIN 6)

The converter will function as a Control Transformer (CT) by placing $\overline{S}$ (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered, $\overline{EM}$ is redefined as LM, $\overline{EL}$ is redefined as LL and $\overline{INH}$ becomes LA (see figures 19 and 27). Figure 18 shows CT mode timing for a two byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.



Notes:
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thui = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsui = 300 ns min (setup inhibit)
(2) When $\overline{S}$ is low:
(LM) $\overline{EM}$ is latch control for MSB byte,
(LL) $\overline{EL}$ is latch control for LSB byte,
1 – data held in latch,
0 – latch is transparent.
(3) (LA) $\overline{INH}$ is latch control for CT latch,
1 – latch is transparent,
0 – data held in latch.

FIGURE 18. CT MODE TIMING – TWO BYTE TRANSFER, DOUBLE BUFFERED

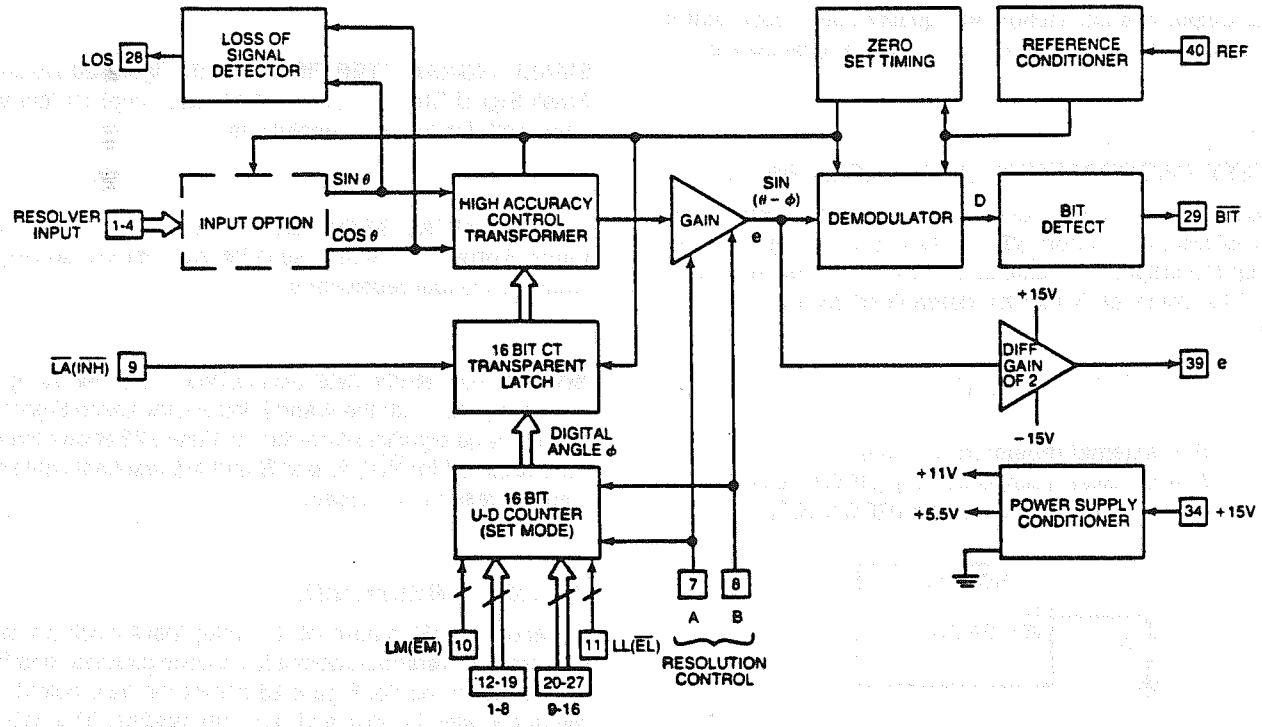


FIGURE 19. CONTROL TRANSFORMER BLOCK DIAGRAM

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground −15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

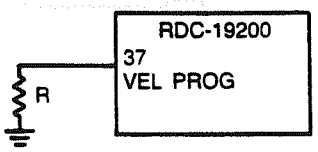
VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \times B/A}{1 - B/A}$$

Where:

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	RDC-19200/19202		RDC-19201/19203	
		TYP	MAX	TYP	MAX
Polarity		(positive for increasing angle)			
Voltage scaling	RPS/V	See Voltage Scaling Table 6			
Scale Factor	%	5	10	5	10
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	%	1	2	0.5	0.7 overtemp
Linearity	% output	1	2	0.5	0.7 overtemp
Zero Offset	mV	15	40	15	40
Zero Offset TC	µV/°C	25	50	25	50
Load	KOhms	–	3	–	3
Output Voltage	V	±13	±10 min	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	80	20	5	1.25
LOW	20	5	1.25	0.32

E

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the RDC-19200 superior dynamic performance as listed in table 1.

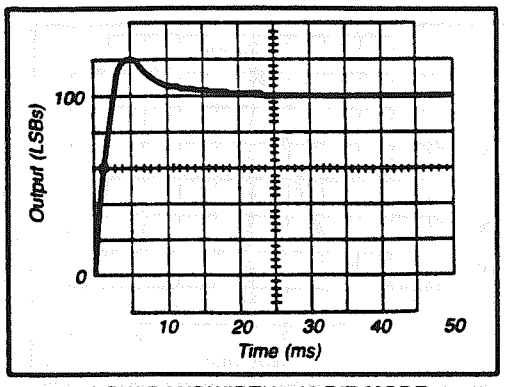
SMALL SIGNAL STEP RESPONSE. Figure 20 illustrates the Small Signal Step Response (100 LSB step) for low and high bandwidth for the four resolutions.

LARGE SIGNAL STEP RESPONSE. Figure 21 illustrates the Large Signal Step Response (179° step) for low and high bandwidth for the four resolutions.

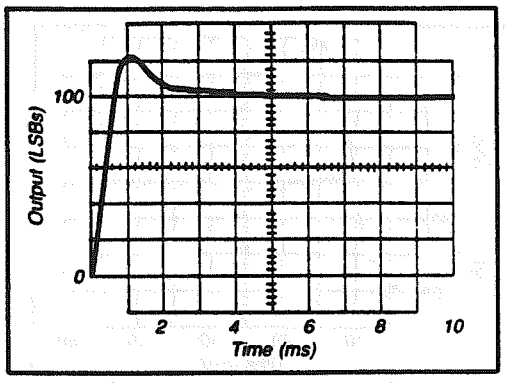
BIT OUTPUT REDUCES SETTLING TIME. By using the $\overline{BIT}$ output together with the A and B inputs, the Large Signal Settling Time may be significantly reduced. Figure 22 shows the connections required for $\overline{BIT}$, A, and B and the resultant settling for the different resolution modes.

VELOCITY RESPONSE

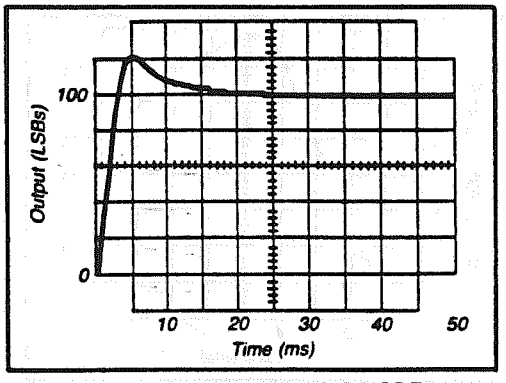
A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. Figure 23 shows the VEL output with and without a filter for low and high bandwidths. The VEL filter is shown in figure 24.



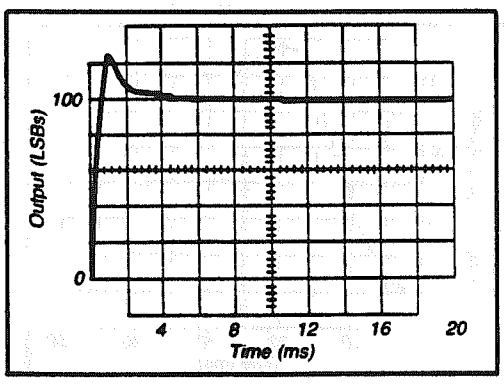
LOW BANDWIDTH – 10 BIT MODE



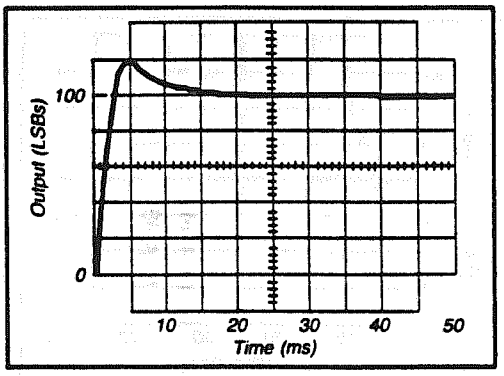
HIGH BANDWIDTH – 10 BIT MODE



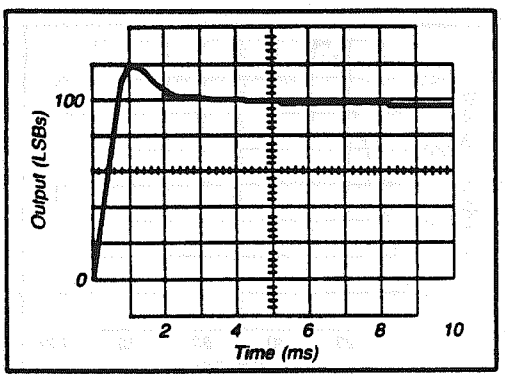
LOW BANDWIDTH – 12 BIT MODE



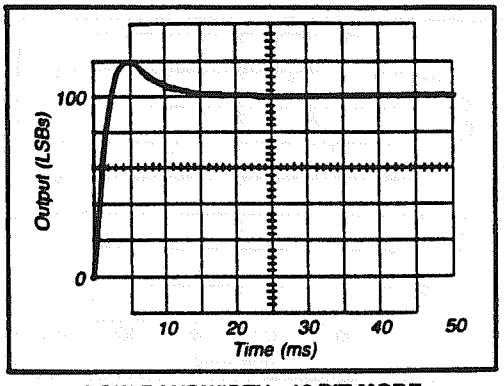
HIGH BANDWIDTH – 12 BIT MODE



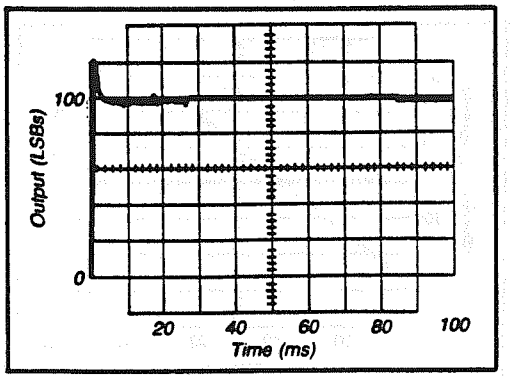
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

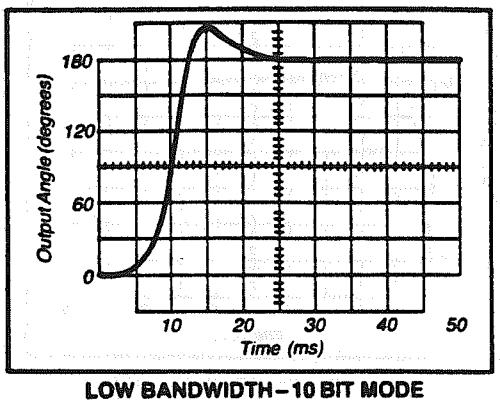


LOW BANDWIDTH – 16 BIT MODE

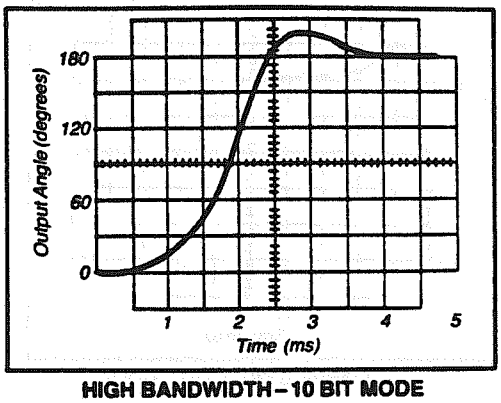


HIGH BANDWIDTH – 16 BIT MODE

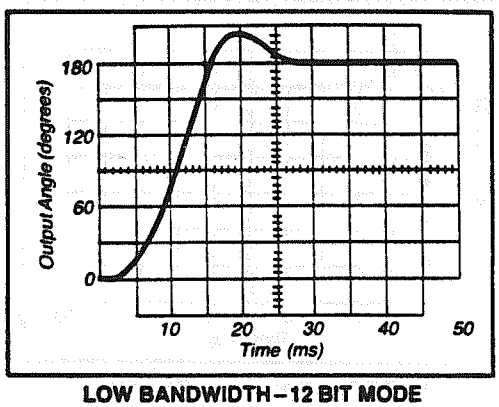
FIGURE 20. SMALL SIGNAL STEP RESPONSE (100 LSB STEP)



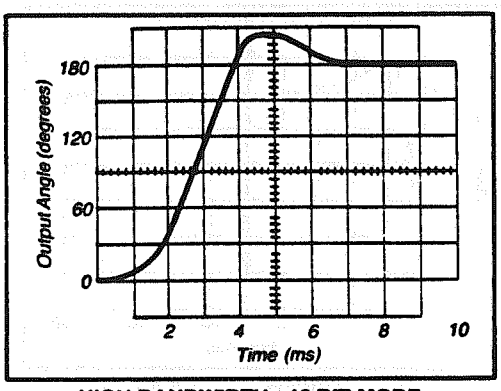
LOW BANDWIDTH – 10 BIT MODE



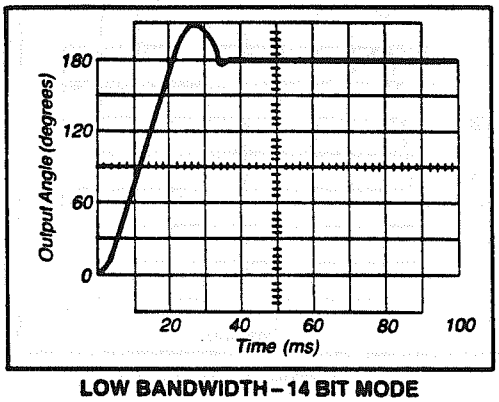
HIGH BANDWIDTH – 10 BIT MODE



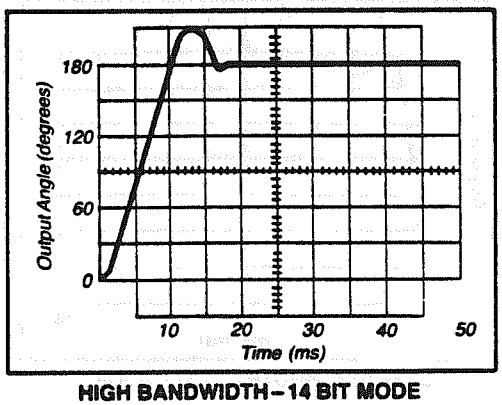
LOW BANDWIDTH – 12 BIT MODE



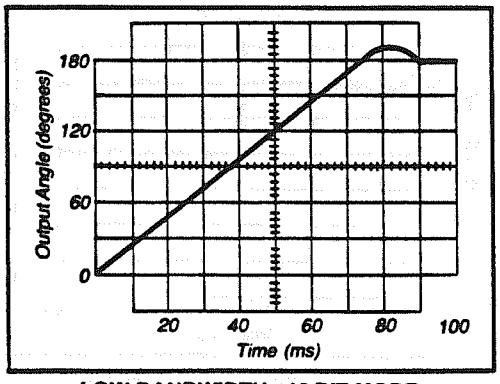
HIGH BANDWIDTH – 12 BIT MODE



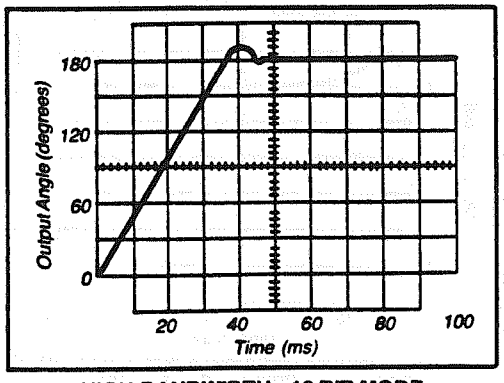
LOW BANDWIDTH – 14 BIT MODE



HIGH BANDWIDTH – 14 BIT MODE

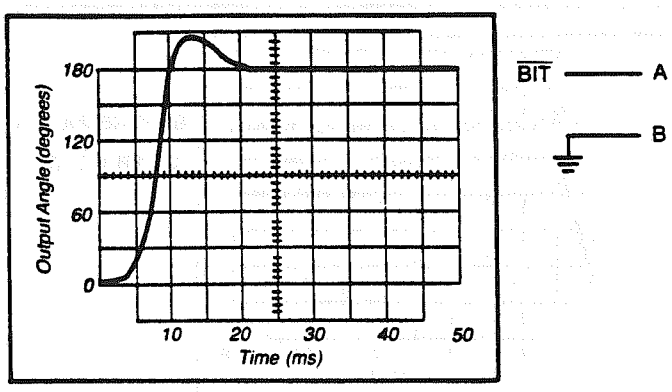


LOW BANDWIDTH – 16 BIT MODE

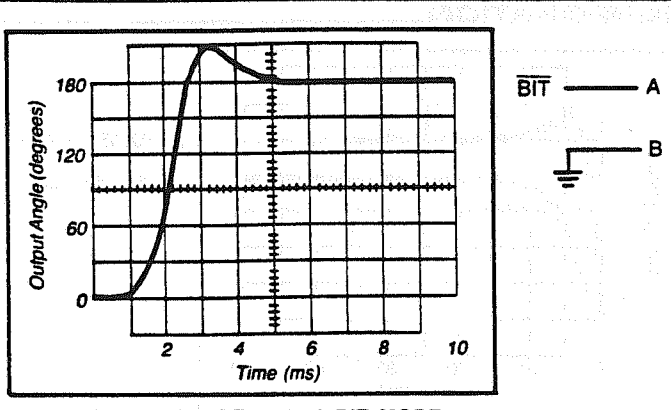


HIGH BANDWIDTH – 16 BIT MODE

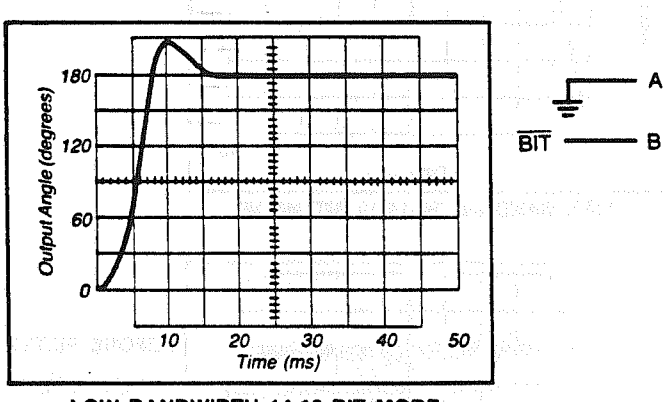
FIGURE 21. LARGE SIGNAL STEP RESPONSE (179° STEP)



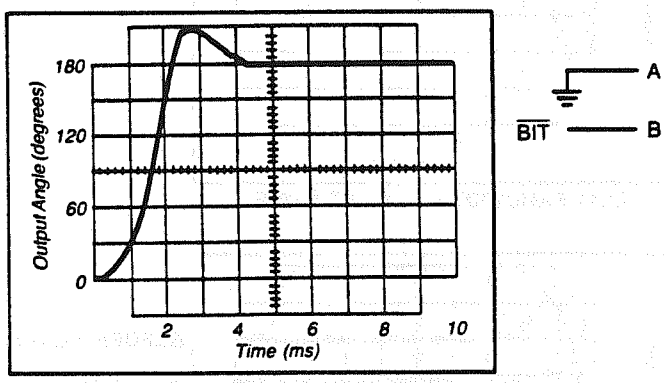
LOW BANDWIDTH 12-10 BIT MODE



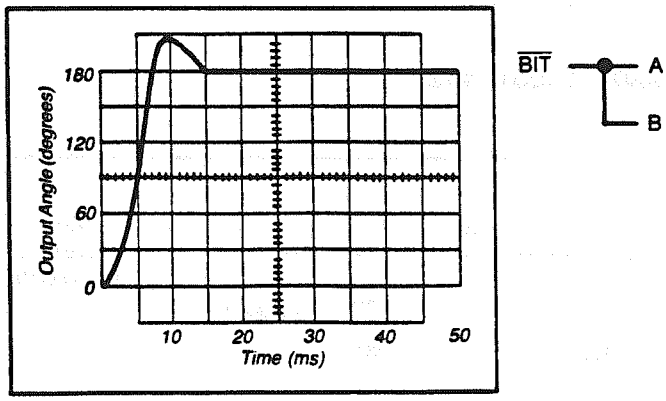
HIGH BANDWIDTH 12-10 BIT MODE



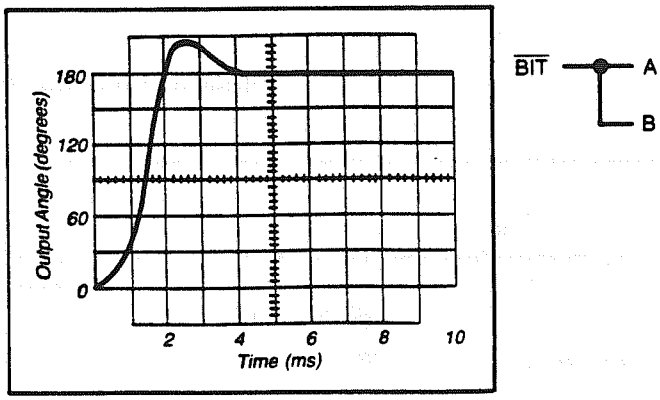
LOW BANDWIDTH 14-10 BIT MODE



HIGH BANDWIDTH 14-10 BIT MODE

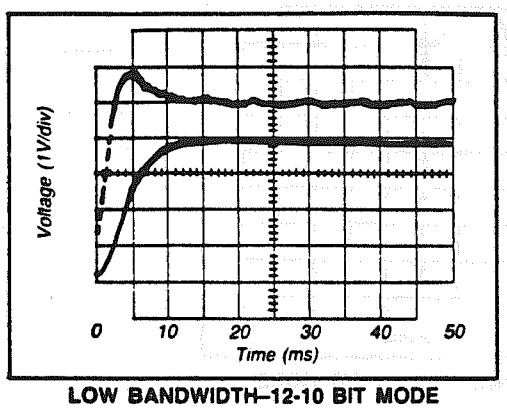


LOW BANDWIDTH 16-10 BIT MODE

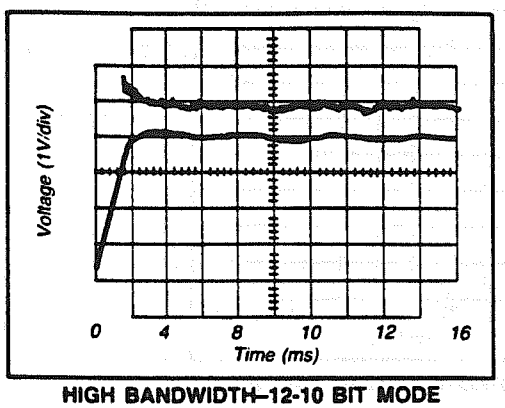


HIGH BANDWIDTH 16-10 BIT MODE

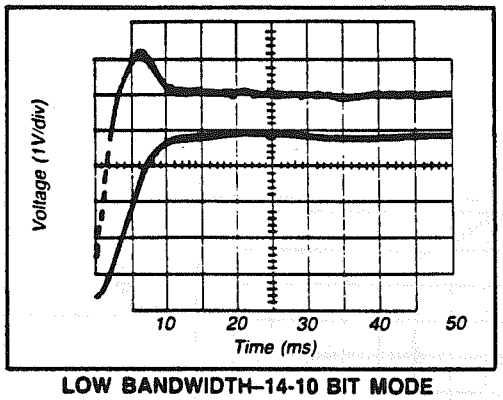
FIGURE 22. USING BIT TO REDUCE SETTLING TIME (179° STEP)



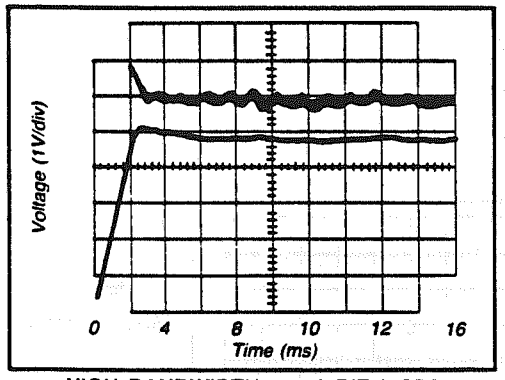
LOW BANDWIDTH–12-10 BIT MODE



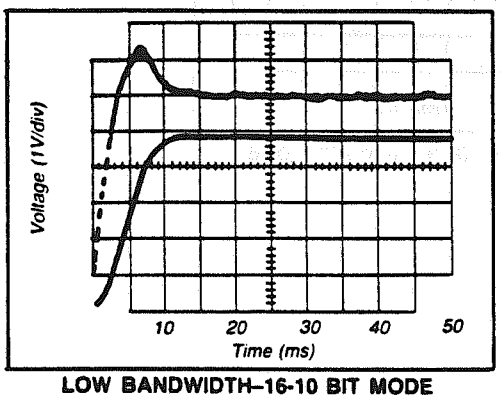
HIGH BANDWIDTH–12-10 BIT MODE



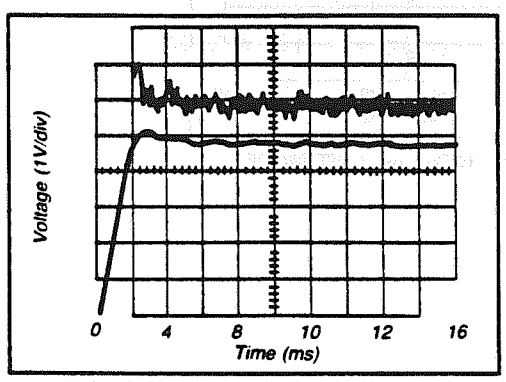
LOW BANDWIDTH–14-10 BIT MODE



HIGH BANDWIDTH–14-10 BIT MODE

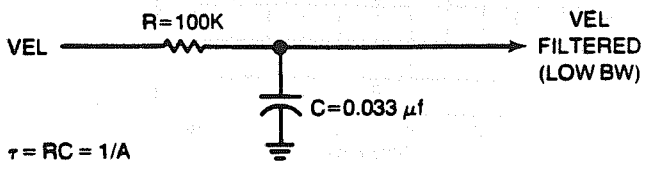


LOW BANDWIDTH–16-10 BIT MODE



HIGH BANDWIDTH–16-10 BIT MODE

FIGURE 23. VEL OUTPUT WITH AND WITHOUT FILTER



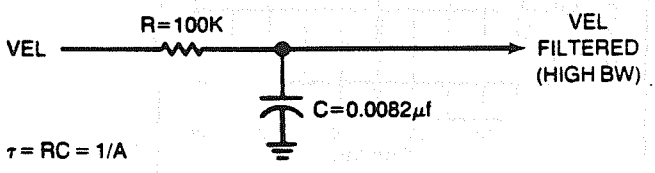
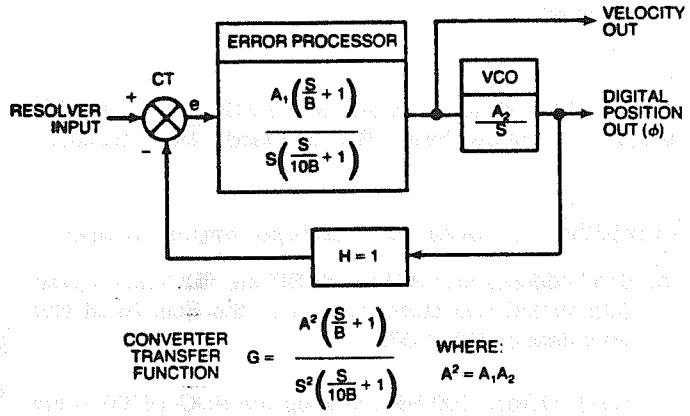


FIGURE 24. VEL OUTPUT FILTERS

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 25) and open and closed loop Bode plots (figures 26 and 27). Table 4 lists the parameters relating to the RDC-19200's dynamic characteristics for different resolution and bandwidth modes.



Note: See table 4 for values of A1, A2, and B.

FIGURE 25. TRANSFER FUNCTION BLOCK DIAGRAM

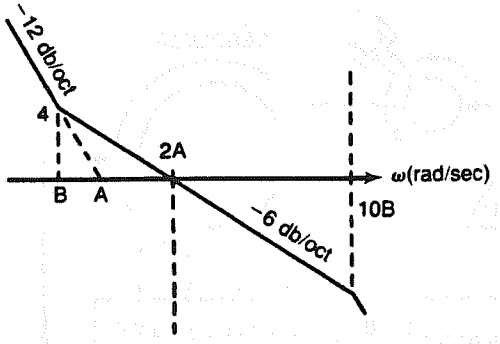


FIGURE 26. OPEN LOOP BODE PLOT

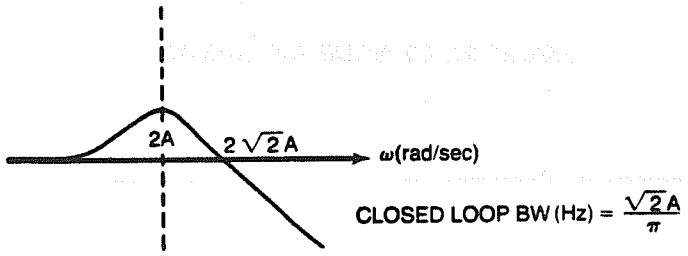


FIGURE 27. CLOSED LOOP BODE PLOT

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

RDC-19200 SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
RDC-1920X-304	2'+1 LSB	23.1	7.3	3.3	2.3
RDC-1920X-303	3'+1 LSB	24.1	8.3	4.3	3.3
RDC-1920X-302	4'+1 LSB	25.1	9.3	5.3	4.3
RDC-1920X-301	8'+1 LSB	29.1	13.3	9.3	8.3

RDC-19200 APPLICATIONS

USING THE RDC-19200 IN THE CT MODE

The CT mode can be applied in servo systems, as shown in figure 28. In this application, changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

MULTI-TURN APPLICATIONS–USE OF MAJOR CARRY (MC, PIN 32)

Refer to Major Carry paragraph on page 8 for details.

USING THE RDC-19200 AS AN R/D WITH VEL TO STABILIZE POSITION LOOP

Figure 29 illustrates a typical use of a RDC-19200 connected as an R/D using the VEL output to stabilize the position loop.

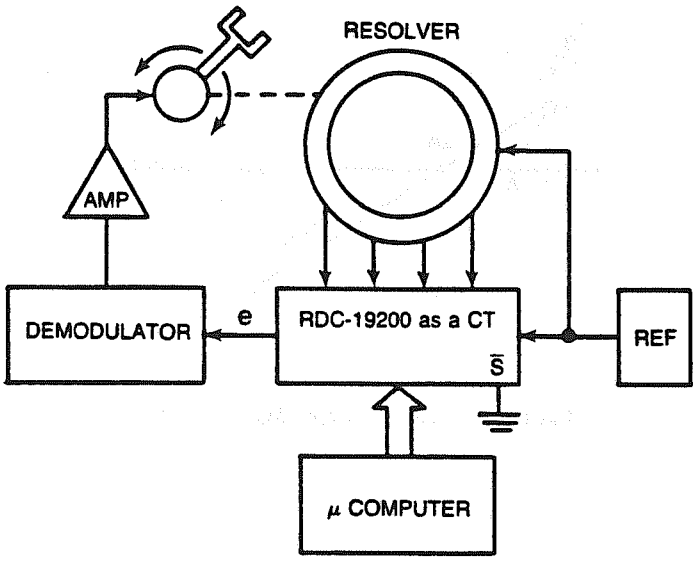


FIGURE 28. CT MODE APPLICATION

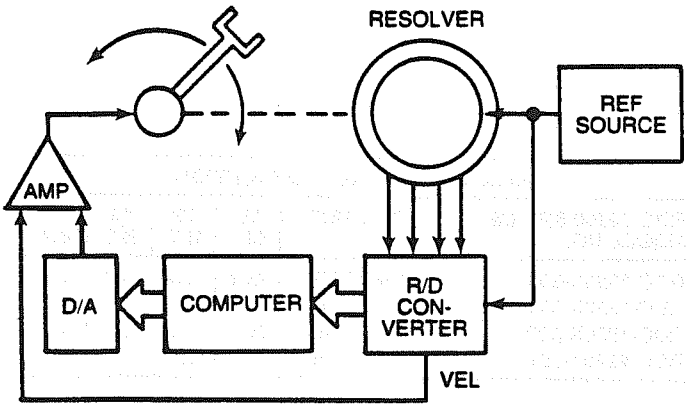


FIGURE 29. R/D WITH VEL TO STABILIZE POSITION

INTERFACING THE RDC-19200 WITH AN IBM PC/XT/AT®

The RDC-19200 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. Figure 31 illustrates the connection to the IBM PC Bus; figure 30 illustrates the timing considerations for the interface.

RDC-19200 TO IBM PC/XT/AT THEORY OF OPERATION

1. The port address where the RDC-19200 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the RDC-19200 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the RDC-19200 INHIBIT line. When A0 is low, the INHIBIT command ($\overline{INH}$) is invoked.

4. To read the output of the RDC-19200, perform the following:

   a. Send address HEX 302 to INHIBIT the RDC-19200 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.

   b. Send address 300 HEX to keep the RDC-19200 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.

   c. Read address 301 HEX or 303 HEX to release the RDC-19200 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5μs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

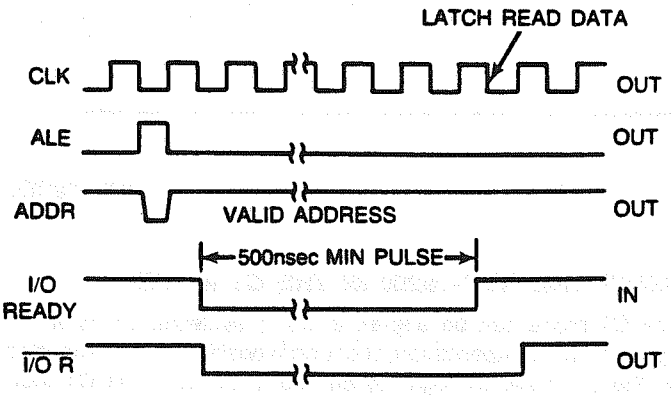


FIGURE 30. PC APPLICATION – I/O READ CYCLE TIMING

E

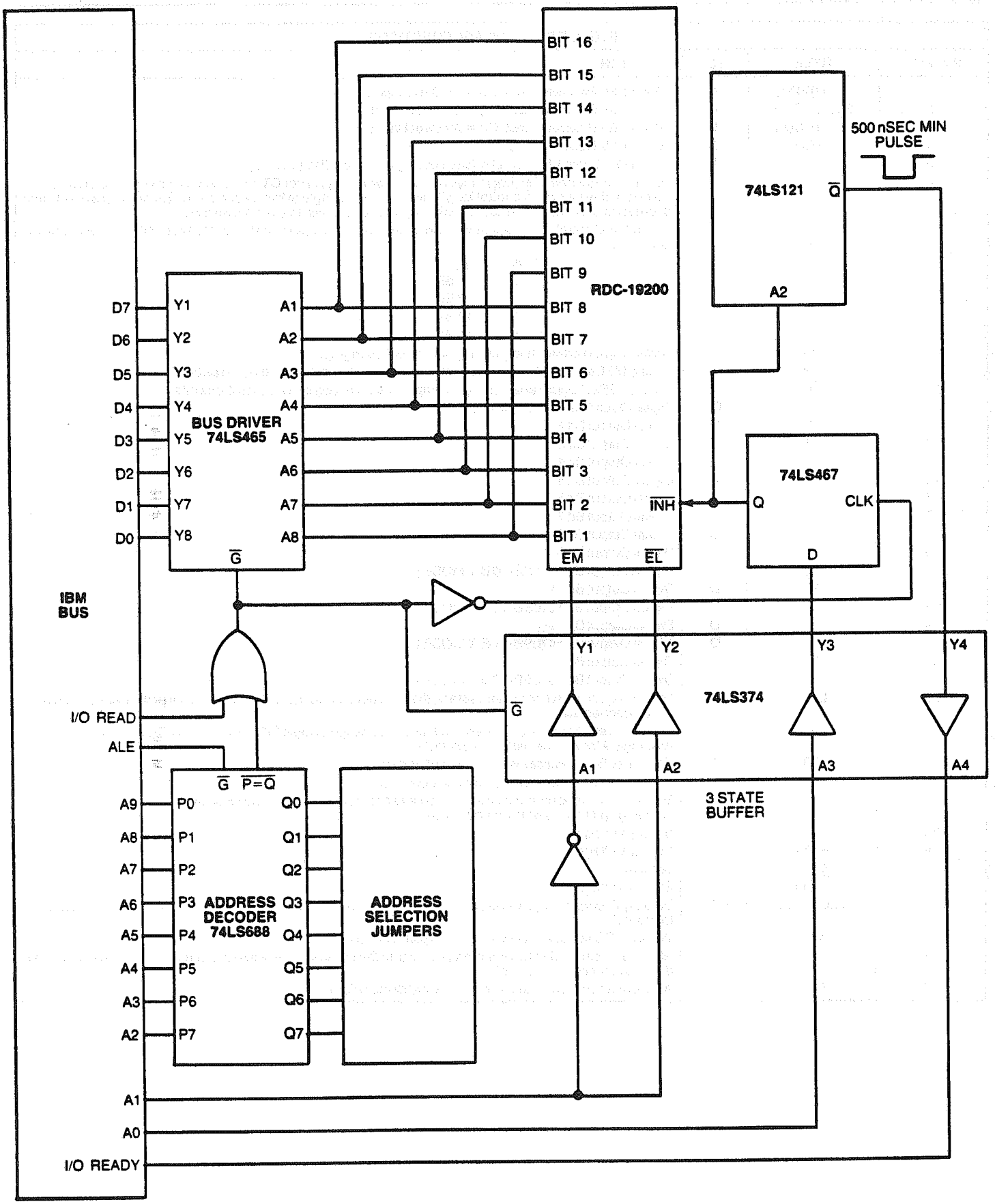


FIGURE 31. RDC-19200 TO PC CONNECTION DIAGRAM

TABLE 8. RDC-19200 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1(R)V(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
2	S2(R)+C(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
3	S3(R)+S(X)	I	(R) = 11.8V Resolver input; (X) = 2V Direct input.
4	S4(R)−	I	(R) = 11.8V Resolver input.
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz); logic 0 for low BW (130 Hz).
6	$\overline{S}$	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7 8	A B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level. B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{INH}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety, the LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up; logic 0 to count down.
32	$\overline{MC}$	O	Major Carry. Used for turns counting applications; normally high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	−	Ground
36	−15V	I	Supply Voltage.
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG, pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity
39	e	O	AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ ($\theta - \phi$).
40	REF	I	AC Reference Input. Used to drive internal demodulator.

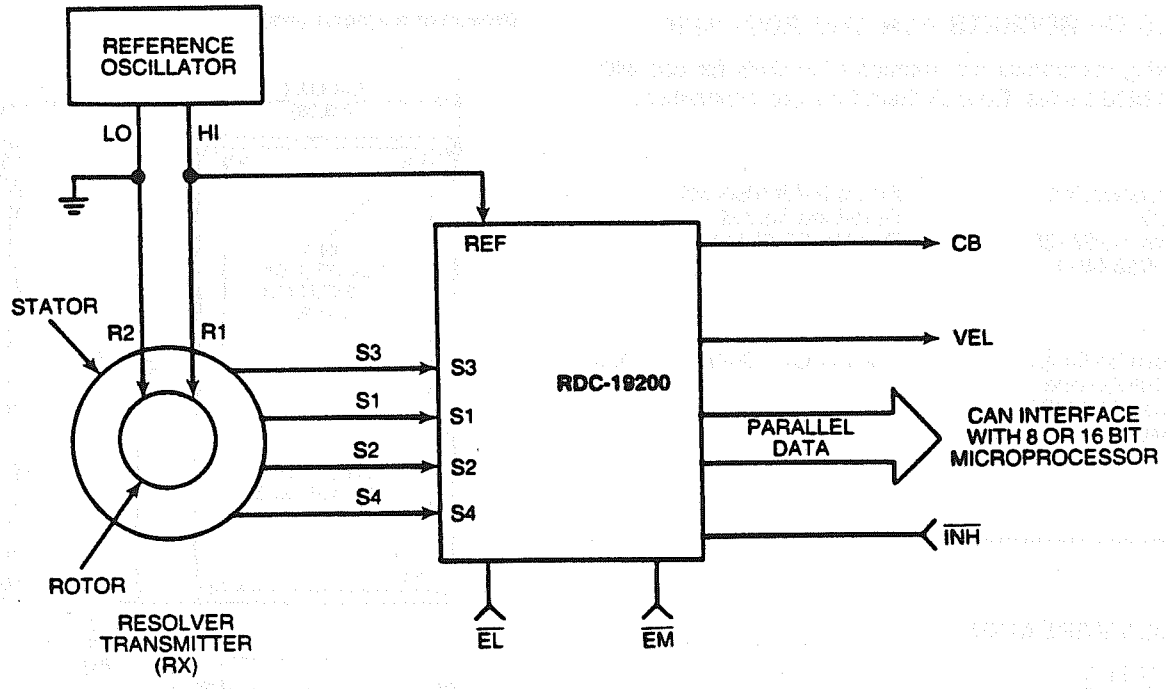


FIGURE 32. RESOLVER CONNECTION – 11.8V

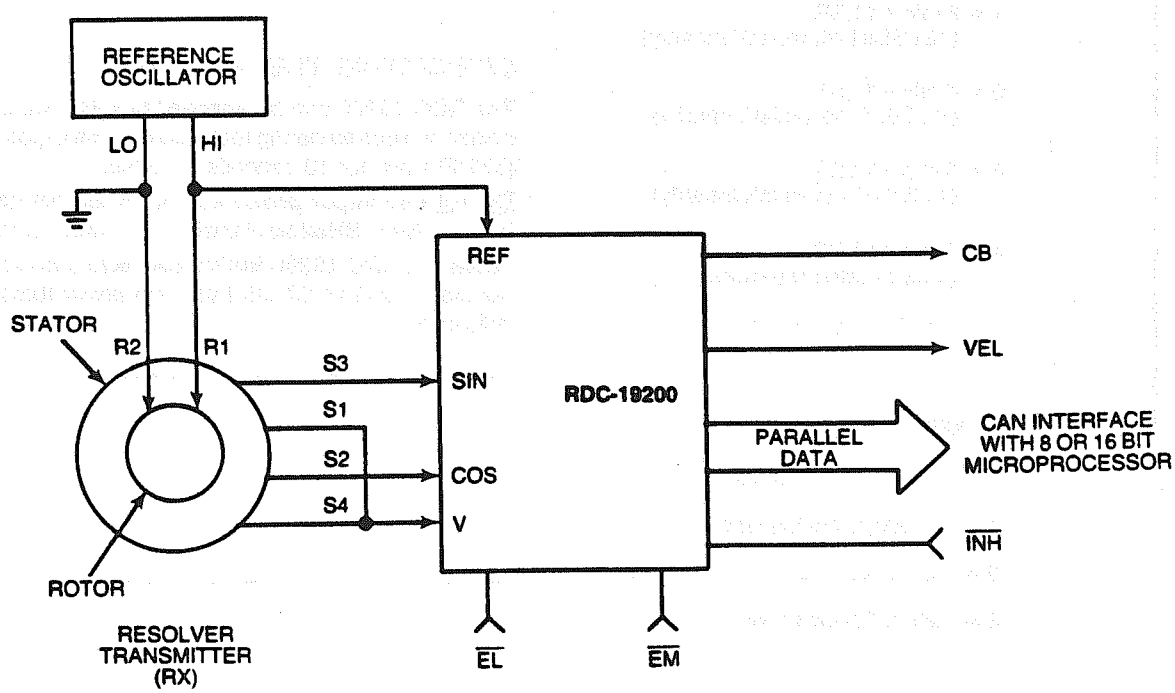


FIGURE 33. RESOLVER CONNECTION – 2V

SOURCES OF SOCKETS FOR THE RDC-19200

The following companies are sources of sockets for use with the RDC-19200 Series. Consult them for more information.

Aries Electronics, Inc.
P.O. Box 30
Frenchtown, NJ 08825
Tel: 1-201-996-6841

Single In-Line Socket
Strip-Line Socket
Part No. 20-05511-11

Circuit Assembly Corp.
3169 Red Hill Avenue
Costa Mesa, CA 92626
Tel: 714-540-5490

Part No. CA-20-STL-XX XX-X

ORDERING INFORMATION

RDC-1920X-3 0 X

Accuracy

0 = 10 min + 1 LSB (1)
(16 LSBs Differential Linearity, RDC-19200 and RDC-19202 only)

1 = 8 min + 1 LSB
(12 LSBs Differential Linearity)

2 = 4 min + 1 LSB
(8 LSBs Differential Linearity)

3 = 3 min + 1 LSB
(4 LSBs Differential Linearity)

4 = 2 min + 1 LSB
(4 LSBs Differential Linearity)

Configuration:

0 = 11.8V, 2% Linearity

1 = 11.8V, 0.7% Linearity

2 = 2V, 2% Linearity

3 = 2V, 0.7% Linearity

Notes:
(1) Vel and e not characterized on models RDC-19200-300 and RDC-19202-300.
(2) Differential Linearity is x LSB in the 16th bit.

Dimensions are inches (mm).

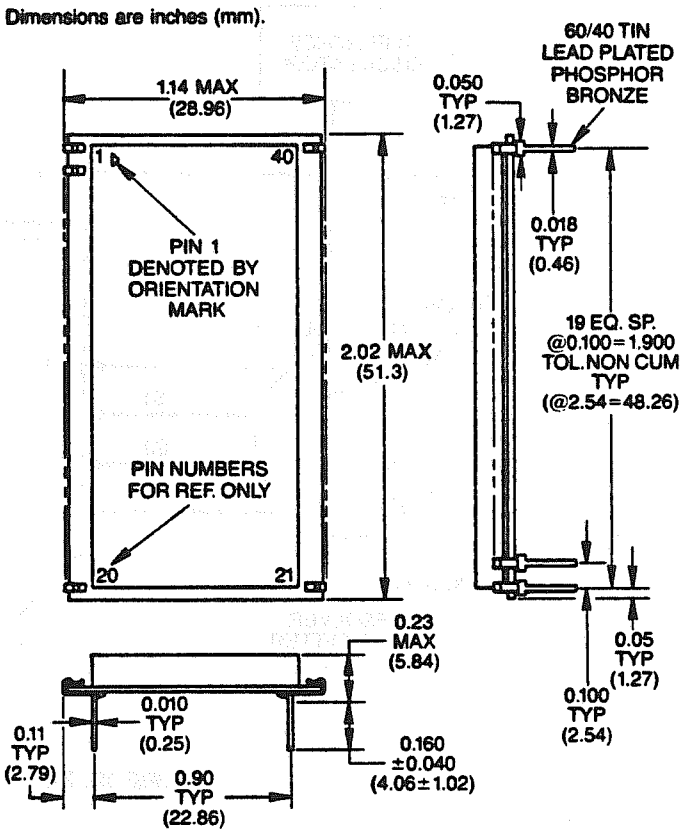


FIGURE 34. RDC-19200 MECHANICAL OUTLINE

CONNECTING THE RDC-19200

The RDC-19200 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

Since the RDC-19200 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

APPENDIX D

Synchro-to-Digital Converter Data Sheet

DDC
ILC DATA DEVICE CORPORATION

SDC-19204® MONOBRID® SERIES

NEW

10, 12, 14, OR 16 BIT INDUSTRIAL SYNCHRO TO DIGITAL CONVERTERS

PRELIMINARY

DESCRIPTION

The SDC-19204 Monobrid Series are versatile state-of-the-art synchro to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes +1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

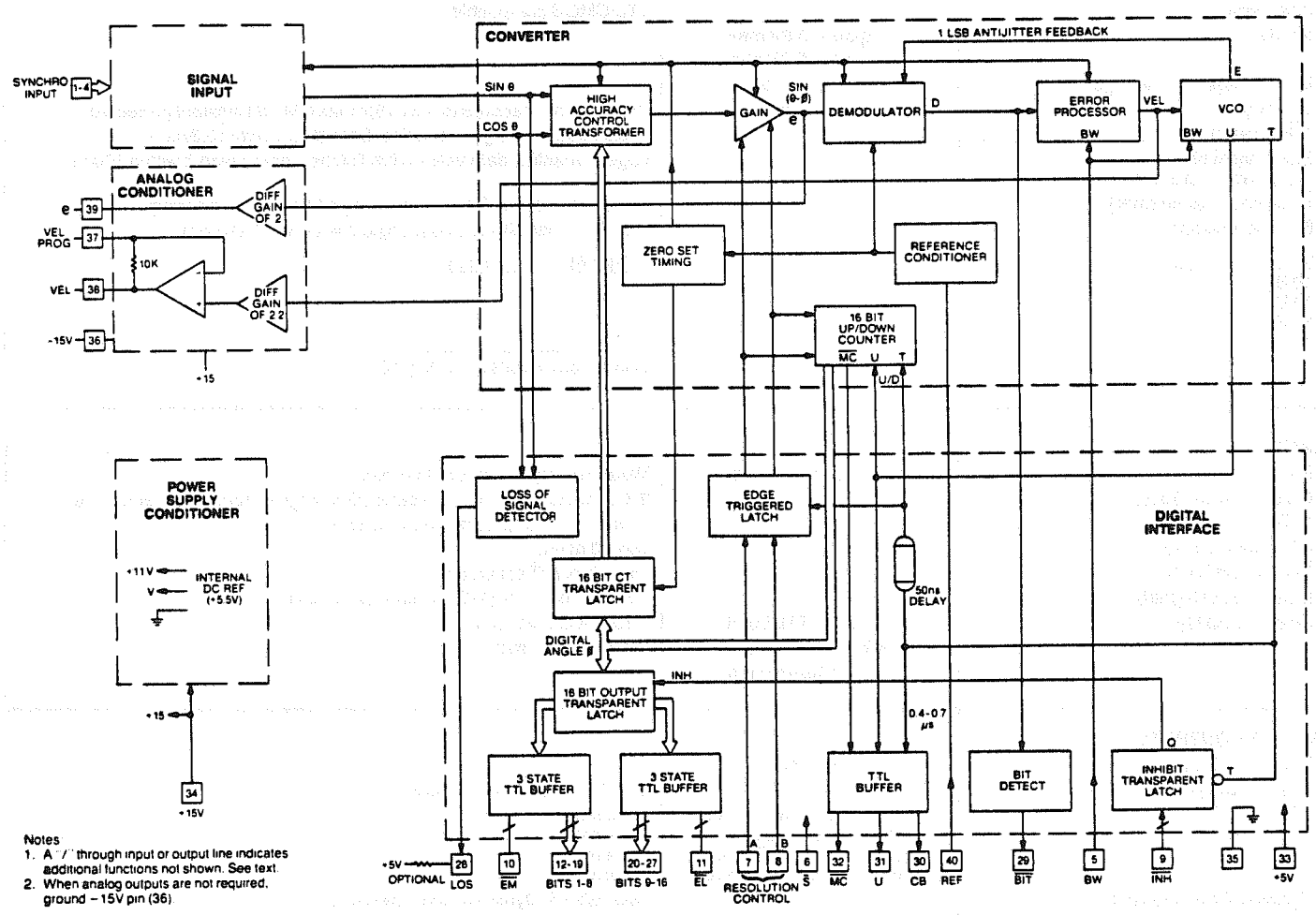
The velocity output (VEL) from the SDC-19204 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The SDC-19204 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the SDC-19204 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST (BIT) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*



Notes
1. A "/" through input or output line indicates additional functions not shown. See text.
2. When analog outputs are not required, ground – 15V pin (36).

FIGURE 1. SDC-19204 BLOCK DIAGRAM

TABLE 1. SDC-19204 SPECIFICATIONS

These specifications apply over temperature range, power supply range, reference frequency and amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	8, 4, 3, 2 minutes	Max + 1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-130 Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	47 Hz to 1 KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Synchro	11.8VL-L / 90VL-L	
Zin Line to Line	52K Ohm / 123K Ohm	
Zin Each Line to Ground	70K Ohm / 180K Ohm	
Common Mode Range	25V max / 180V max	
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	−0.3 to 11V	
Loading	−10 μA max	
$\overline{INH}$ (Inhibit)		Pull-up current source to +5V//5pf max CMOS transient protected.
$\overline{EM}$ (Enable bits 1-8)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3μs
$\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
BW (Bandwidth)		Logic 1 = High BW (53 Hz); Logic 0 = Low BW (13 Hz)
Resolution Control		B (pin8) / A (pin 7)
10 Bit		0 / 0
12 Bit		0 / 1
14 Bit		1 / 0
16 Bit		1 / 1
		Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 μs to 0.7 μs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3μA pull-up to +5V).
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10μA/5pf max	−1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

E

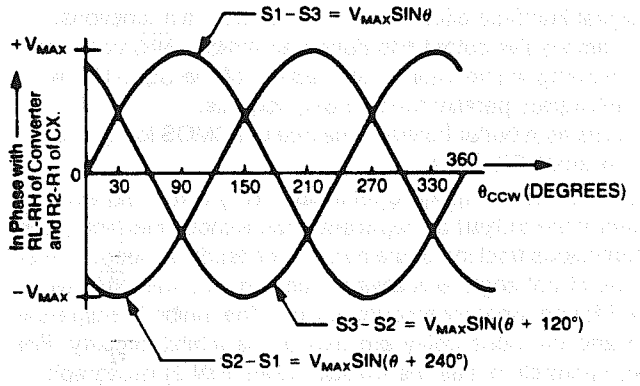
TABLE 1. SDC-19204 SPECIFICATIONS (Continued)

PARAMETER	VALUE			DESCRIPTION
POWER SUPPLY CHARACTERISTICS				
Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	−15VDC ±5%	Note: When analog outputs are not required, ground −15V (pin 36).
Max Voltage w/o Damage	+18V	+8V	−18V	
Max Current	25mA	10mA	15mA	
TEMPERATURE RANGES				
Operating	0°C to +70°C			
Storage	−40°C to +120°C			
PHYSICAL CHARACTERISTICS				
Size	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm)			40 pin TDIP
Weight	0.46 oz (13 gm)			

TECHNICAL INFORMATION

INTRODUCTION

The SDC-19204 Series are small, 40 pin TDIP synchro to digital hybrid converters. As shown in the block diagram (figure 1), the SDC-19204 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

FIGURE 2. SYNCHRO SIGNALS

SIGNAL INPUT

In a synchro, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form $\sin\theta\cos\omega t$, $\sin(\theta+120^\circ)\cos\omega t$ and $\sin(\theta+240^\circ)\cos\omega t$ are internally converted to resolver format: $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 illustrates synchro signals as a function of the angle θ.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

CONVERTER OPERATION

As shown in figure 1, the converter section of the SDC-19204 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \Phi 0$, so that ϕ will repeat the shaft position θ.

The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

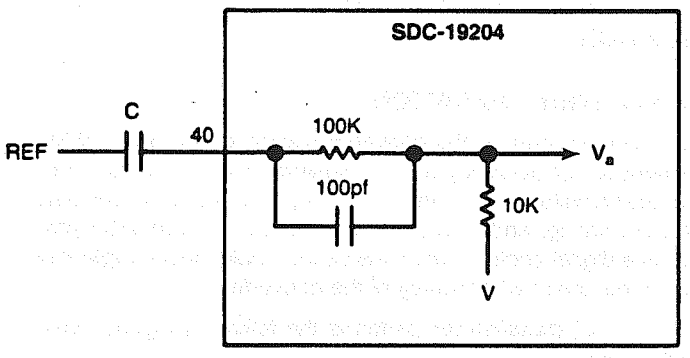
The SDC-19204 has unique **zero-set timing** circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical

performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive.

MINIMIZE ERROR DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the synchro input. To determine the capacitor's value, see figure 3.



Note:
Choose C such that the V_a to REF phase lead is equal to the synchro to REF phase lead plus 9μs.

FIGURE 3. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min ≃ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

E

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the SDC-19204.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the SDC-19204, applying an Inhibit ($\overline{INH}$) command will lock the data in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by −10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS		
BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.5
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.879	5.27
13	0.439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33
Note: $\overline{EM}$ enables the 8 MSBs and $\overline{EL}$ enables the LSBs.		

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 4). The angle is determined by the sum of the bits at logic 1.

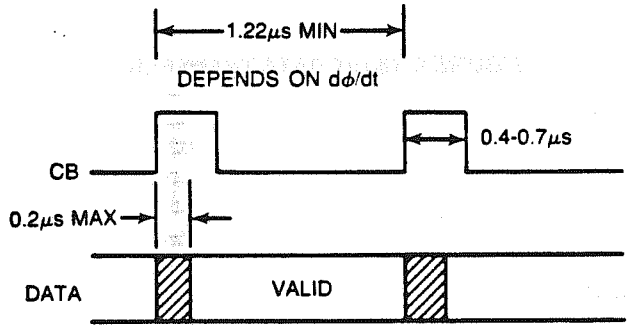


FIGURE 4. CB TIMING

INHIBIT ($\overline{INH}$, PIN 9)

When an Inhibit ($\overline{INH}$) input is applied to the SDC-19204, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 5). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{INH}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{INH}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{INH}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 6 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

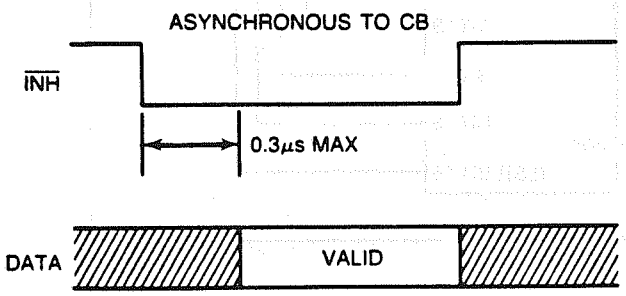


FIGURE 5. INHIBIT TIMING

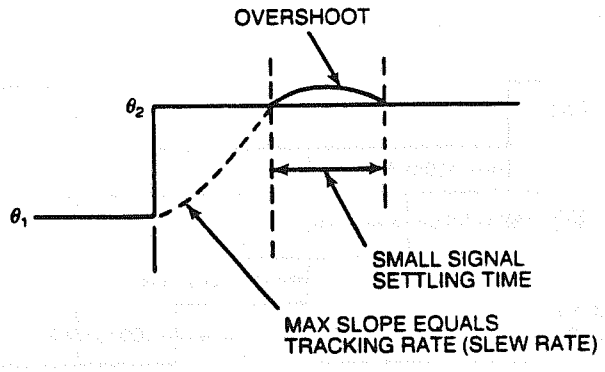


FIGURE 6. RESPONSE TO A STEP INPUT

DATA TRANSFERS

Digital output data from the SDC-19204 can be transferred to 8 bit and 16 bit bus systems. For 8 bit systems, the MSB and LSB bytes are transferred sequentially (see figures 7 and 8). For 16 bit systems, all bits are transferred at the same time (see figures 9 and 10).

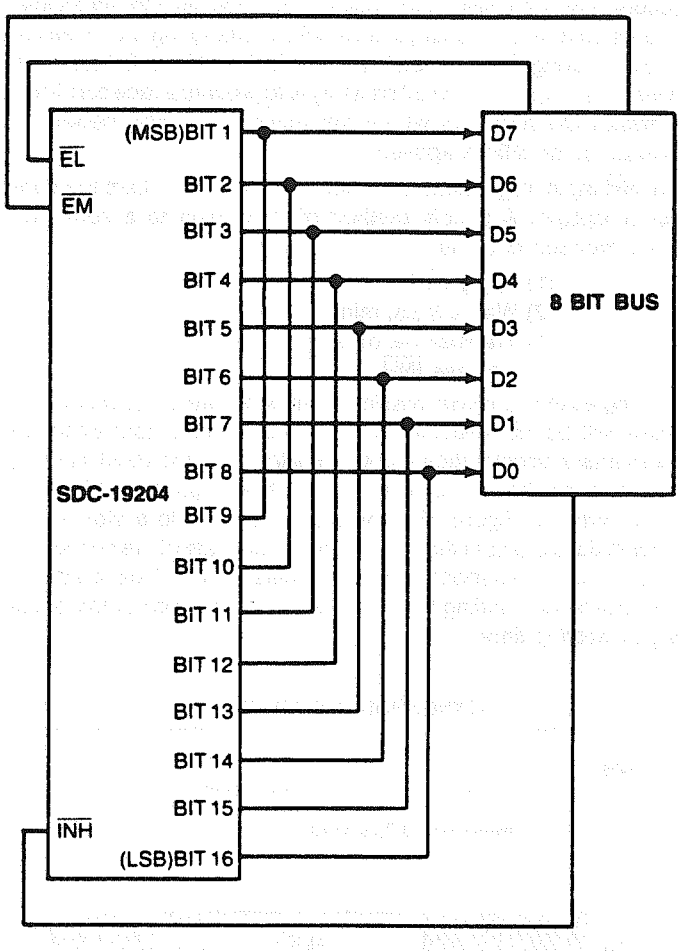


FIGURE 7. DATA TRANSFER TO 8 BIT BUS

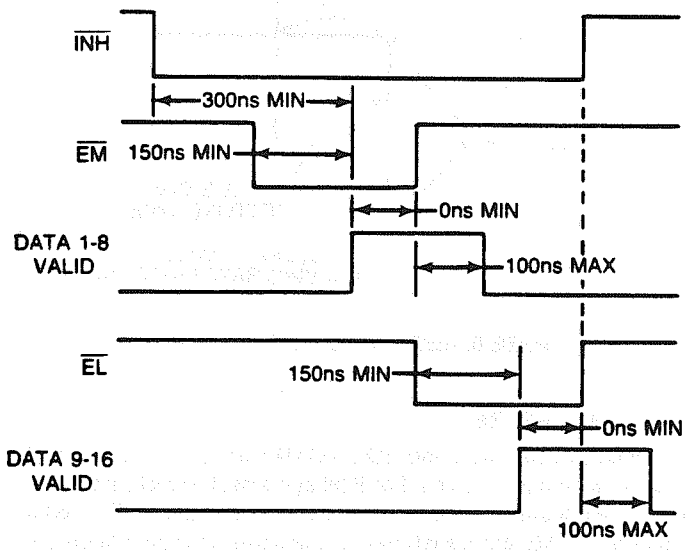


FIGURE 8. DATA TRANSFER TO 8 BIT BUS TIMING

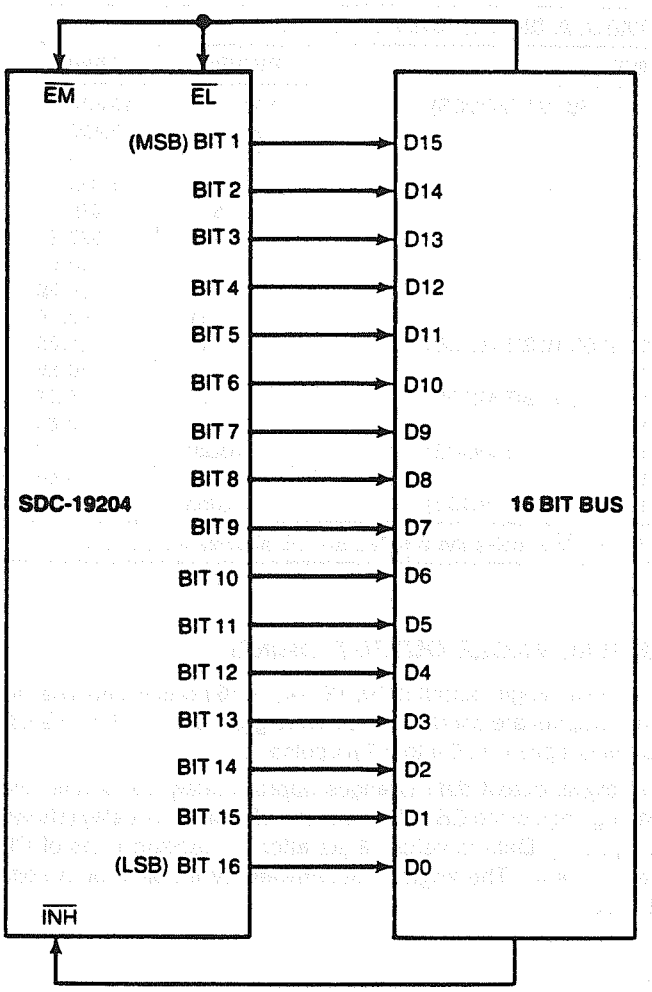


FIGURE 9. 16 BIT DATA TRANSFER

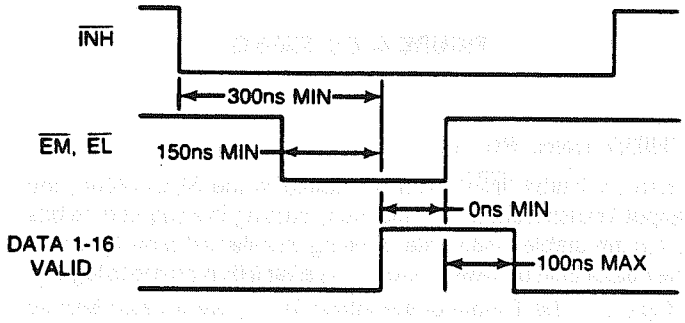


FIGURE 10. 16 BIT DATA TRANSFER TIMING

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 11).

TABLE 3. RESOLUTION CONTROL

B (pin 7)	A (pin 8)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0.

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the SDC-19204 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the SDC-19204 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth.

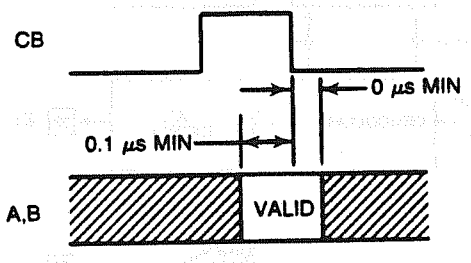


FIGURE 11. RESOLUTION CONTROL TIMING

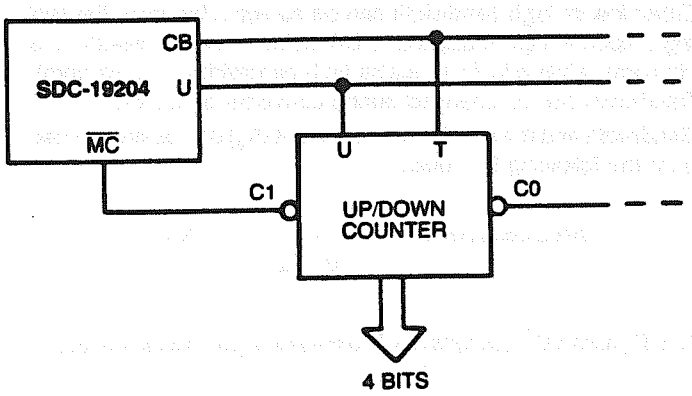
MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 12 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 13. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5μs before and at least 20ns after the leading edge of CB.

TURNS COUNTING



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

FIGURE 12. TURNS COUNTING CONNECTION DIAGRAM

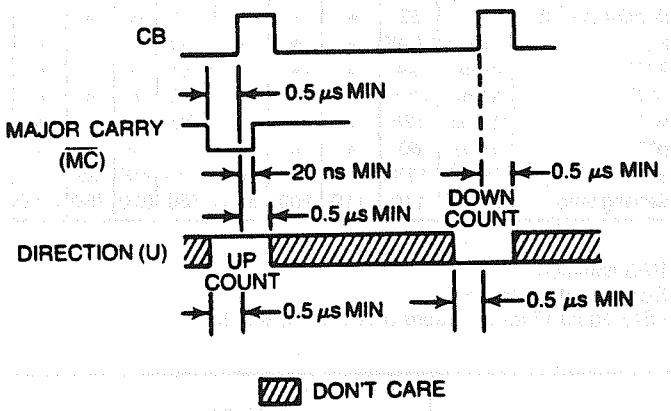


FIGURE 13. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The SDC-19204 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (13 Hz nom), while a logic 1 selects high bandwidth (53 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\,A/\pi$$
$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figure 16 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

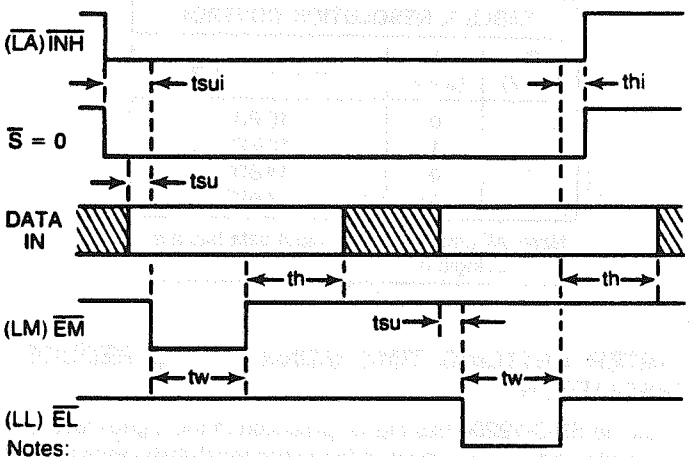
PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	.36-1	*	*	*	.047-1	*	*	*
Tracking Rate	RPS†	160	40	10	2.5	40	10	2.5	0.62
Bandwidth, CL	Hz	53	*	*	*	13	*	*	*
K_a	1/sec²	14.4K	*	*	*	3.6K	*	*	*
A1**	1/sec	0.4	*	*	*	0.1	*	*	*
A2**	1/sec	36K	*	*	*	9K	*	*	*
A**	1/sec	120	*	*	*	30	*	*	*
B**	1/sec	60	*	*	*	15	*	*	*
acc-1 LSB lag	°/sec²	17K	4.2K	1.1K	260	1.1K	260	66	17
Settling time	msec	110	110	200	500	550	600	750	1100

†RPS minimum
*Same as value to left
**See figure 17 for definitions of A1, A2, A, and B.

CONTROL TRANSFORMER MODE ($\overline{S}$, PIN 6)

The converter will function as a Control Transformer (CT) by placing $\overline{S}$ (pin 6) to logic 0. In the CT mode, the digital inputs are double buffered, $\overline{EM}$ is redefined as LM, $\overline{EL}$ is redefined as LL and $\overline{INH}$ becomes LA (see figures 15 and 20). Figure 14 shows CT mode timing for a two byte transfer.

The CT mode is used when the AC error (e) is needed to drive an external control loop by the difference angle of the resolver input and the digital input. It is also used for presetting the converter to a specific angle to reduce the step response time.



Notes:
(1) tw = 100 ns min (pulse width)
th = 50 ns min (hold time)
thui = 0 ns min (hold time inhibit)
tsu = 0 ns min (setup time)
tsui = 300 ns min (setup inhibit)
(2) When $\overline{S}$ is low:
(LM) $\overline{EM}$ is latch control for MSB byte,
(LL) $\overline{EL}$ is latch control for LSB byte,
1 – data held in latch,
0 – latch is transparent.
(3) (LA) $\overline{INH}$ is latch control for CT latch:
1 – latch is transparent,
0 – data held in latch.

FIGURE 14. CT MODE TIMING – TWO BYTE TRANSFER, DOUBLE BUFFERED

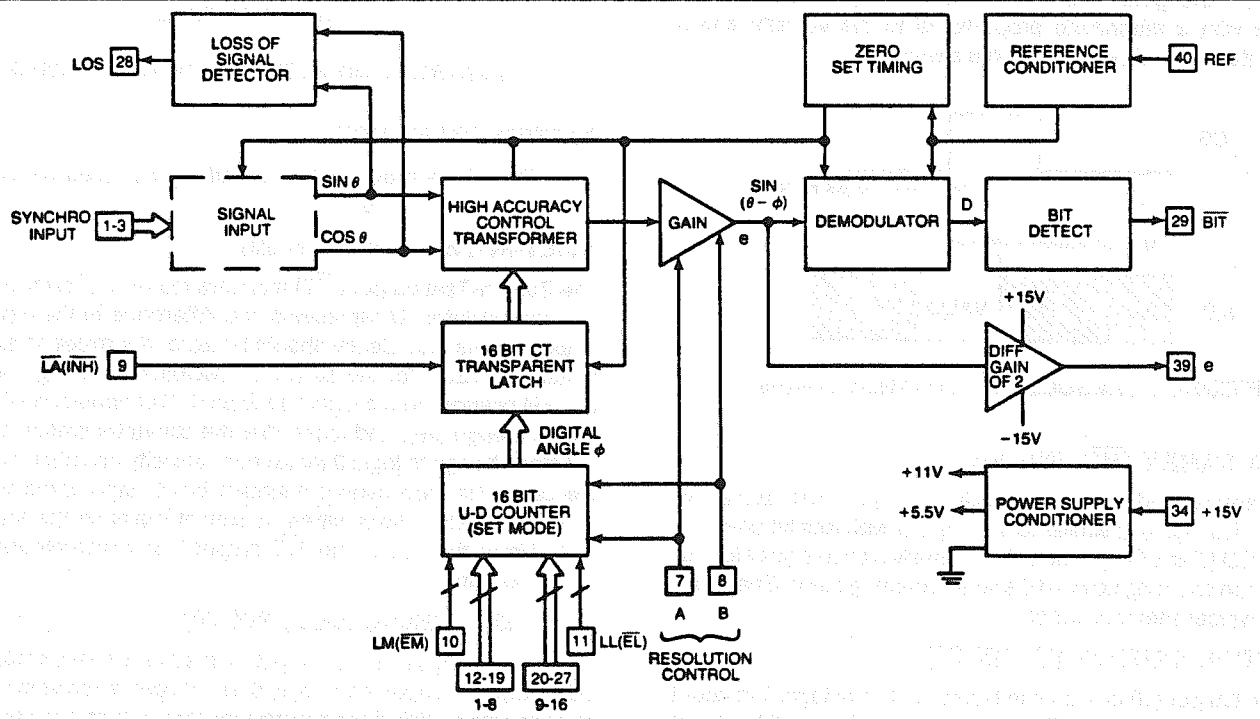


FIGURE 15. CONTROL TRANSFORMER BLOCK DIAGRAM

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground −15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

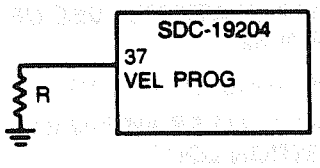
VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

$$R = \frac{10 \times B/A}{1 - B/A}$$

Where:

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	SDC-19204/SDC-19206	
		TYP	MAX
Polarity		(positive for increasing angle)	
Voltage scaling	RPS/V	See Voltage Scaling Table 6	
Scale Factor	%	5	10
Scale Factor TC	PPM/°C	100	200
Reversal Error	%	1	2
Linearity	% output	1	2
Zero Offset	mV	15	40
Zero Offset TC	µV/°C	25	50
Load	KOhms	–	3
Output Voltage	V	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	16	4	1	0.25
LOW	4	1	0.25	0.062

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the SDC-19204 superior dynamic performance as listed in table 1.

VELOCITY RESPONSE

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. The VEL filter is shown in figure 16.

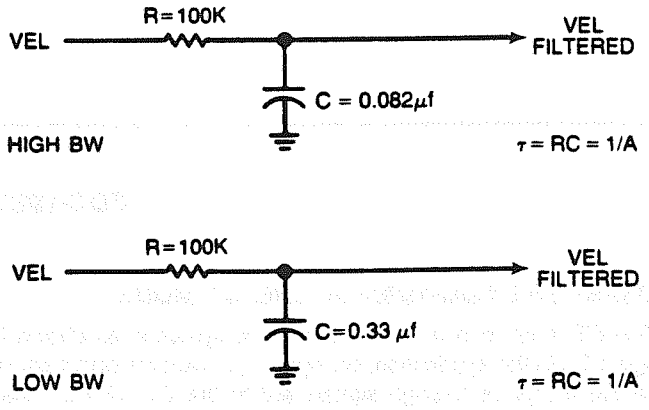
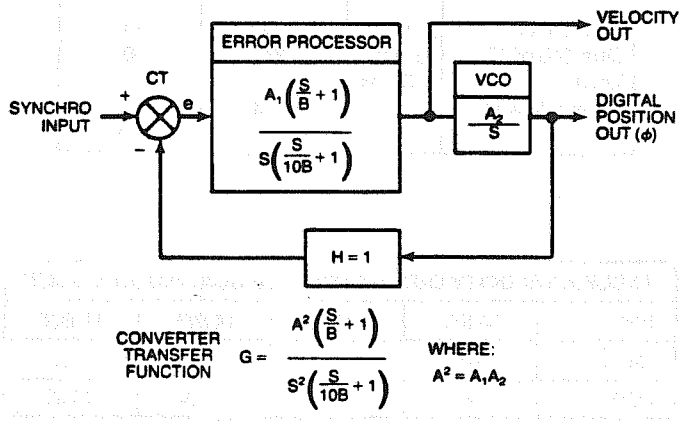


FIGURE 16. VEL OUTPUT FILTER

TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 17) and open and closed loop Bode plots (figures 18 and 19). Table 4 lists the parameters relating to the SDC-19204's dynamic characteristics for different resolution and bandwidth modes.



Note: See table 4 for values of A1, A2, and B.

FIGURE 17. TRANSFER FUNCTION BLOCK DIAGRAM

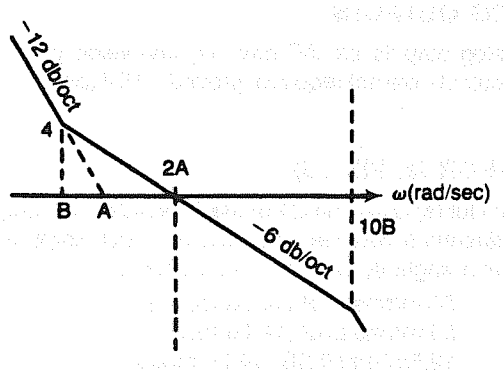


FIGURE 18. OPEN LOOP BODE PLOT

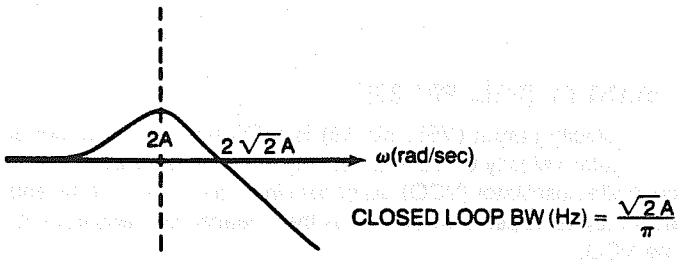


FIGURE 19. CLOSED LOOP BODE PLOT

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

SDC-1920X SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
SDC-1920X-304	2'+1 LSB	23.1	7.3	3.3	2.3
SDC-1920X-303	3'+1 LSB	24.1	8.3	4.3	3.3
SDC-1920X-302	4'+1 LSB	25.1	9.3	5.3	4.3
SDC-1920X-301	8'+1 LSB	29.1	13.3	9.3	8.3

SDC-19204 APPLICATIONS

USING THE SDC-19204 IN THE CT MODE

The CT mode can be applied in servo systems, as shown in figure 20. In this application, changes in position are commanded by the computer through signals fed to the CT. The CT then drives the motors through DC power amplifiers.

MULTI-TURN APPLICATIONS – USE OF MAJOR CARRY (MC, PIN 32)

Refer to Major Carry paragraph for details.

USING THE SDC-19204 AS AN S/D WITH VEL TO STABILIZE POSITION LOOP

Figure 21 illustrates a typical use of a SDC-19204 connected as an S/D using the VEL output to stabilize the position loop.

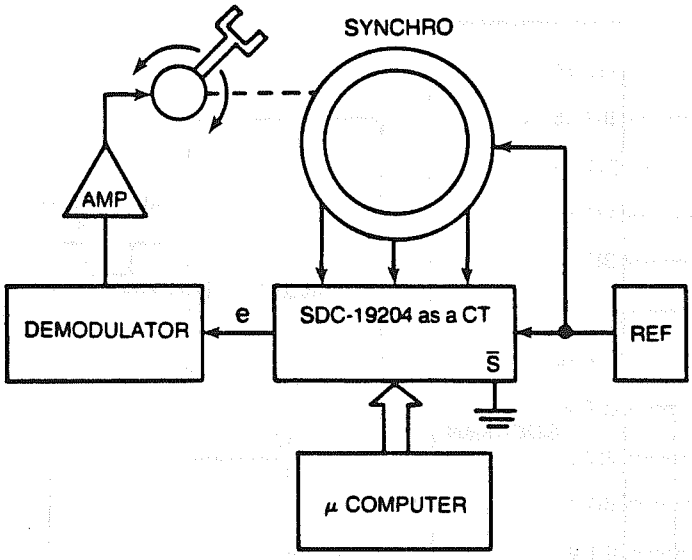


FIGURE 20. CT MODE APPLICATION

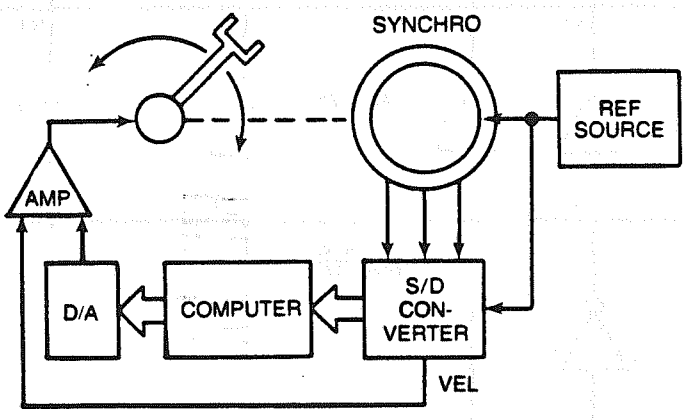


FIGURE 21. S/D WITH VEL TO STABILIZE POSITION

INTERFACING THE SDC-19204 WITH AN IBM PC/XT/AT®

The SDC-19204 can be connected to an IBM PC/XT/AT through the IBM PC Bus located at address HEX 300 through 303. This location is reserved by the PC for prototype cards. Figure 23 illustrates the connection to the IBM PC Bus; figure 22 illustrates the timing considerations for the interface.

SDC-19204 TO IBM PC/XT/AT THEORY OF OPERATION

1. The port address where the SDC-19204 is located is hard wired with jumpers into the 74LS688 address decoder. This address is HEX 300 through 303 and is reserved for prototype cards.

2. Address line A1 selects the upper or lower 8 bits of the SDC-19204 to be placed on the Bus. When A1 is high, bits 1-8 are selected.

3. Address line A0 sets and resets the SDC-19204 INHIBIT line. When A0 is low, the INHIBIT command ($\overline{INH}$) is invoked.

4. To read the output of the SDC-19204, perform the following:
   a. Send address HEX 302 to INHIBIT the SDC-19204 (hold data stable) and place bits 1-8 on the Bus. Read and store data on D0 to D7.
   b. Send address 300 HEX to keep the SDC-19204 in the INHIBIT mode and place bits 9-14 on the Bus. Read and store data on D0 to D7.
   c. Read address 301 HEX or 303 HEX to release the SDC-19204 from the INHIBIT mode and prepare for the next measurement. No valid data will be on the bus during this command.

5. Since the output data is not valid until 0.5μs after the INHIBIT command is invoked, the I/O READY line is held low for this period of time. When I/O READY returns to the high level, the data on the bus reads on the next negative clock edge.

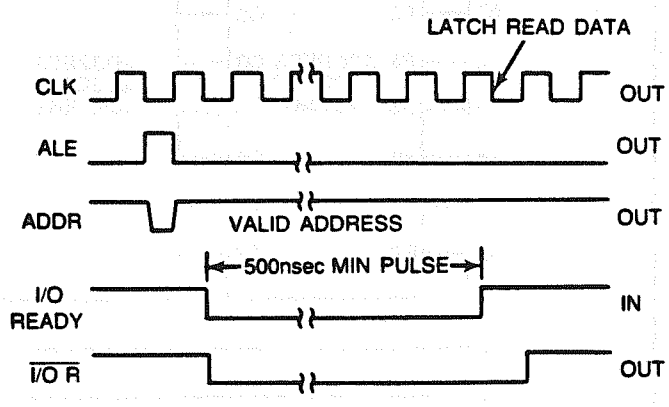


FIGURE 22. PC APPLICATION – I/O READ CYCLE TIMING

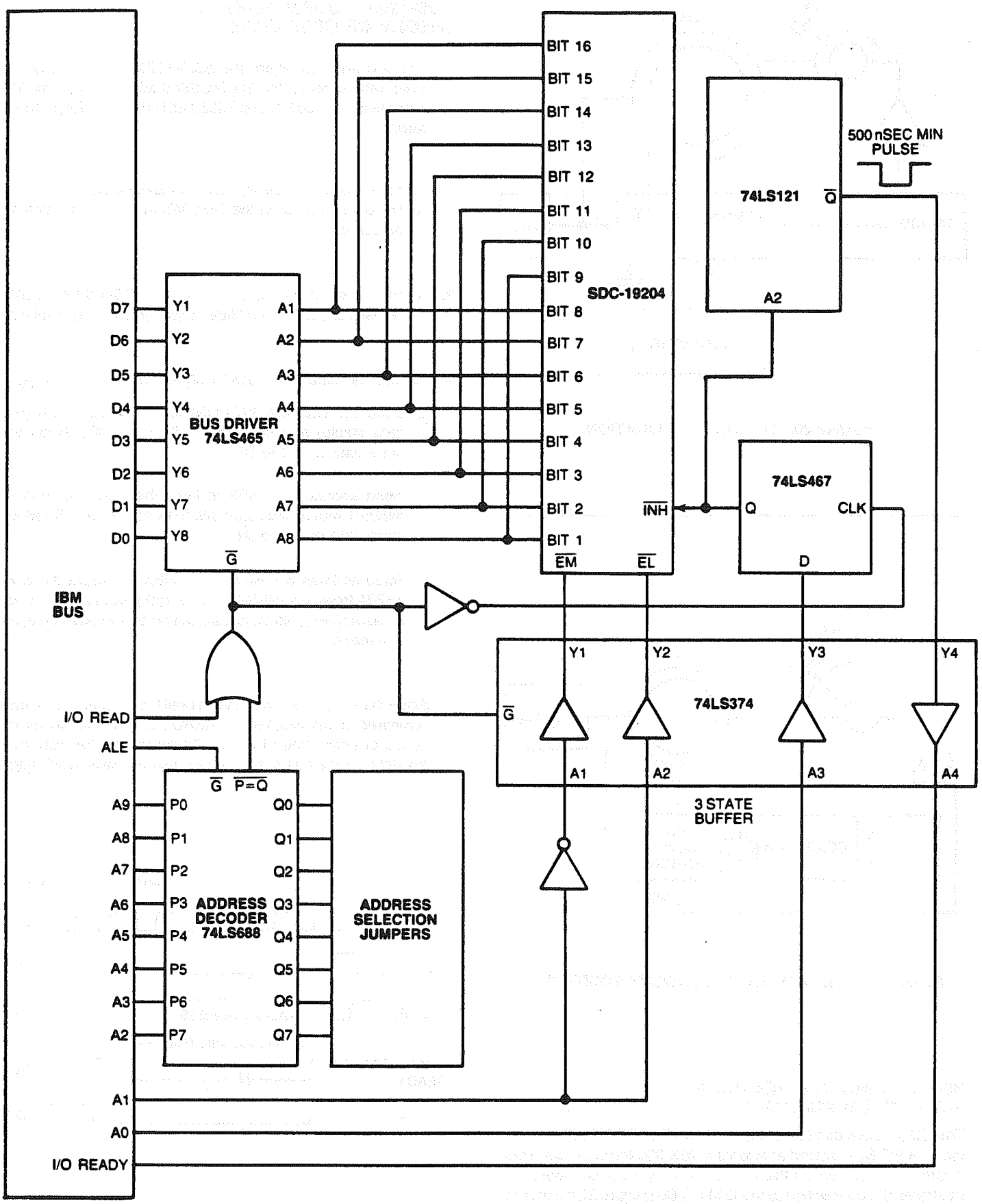


FIGURE 23. SDC-19204 TO PC CONNECTION DIAGRAM

TABLE 8. SDC-19204 PIN FUNCTIONS

PIN NO.	TITLE	I/O	FUNCTION
1	S1	I	Synchro Input.
2	S2	I	Synchro Input.
3	S3	I	Synchro Input.
4	NC	I	No connection
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz); logic 0 for low BW (130 Hz).
6	$\overline{S}$	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7 8	A B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level. B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{INH}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{EM}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{EL}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety, the LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	$\overline{BIT}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up; logic 0 to count down.
32	$\overline{MC}$	O	Major Carry. Used for turns counting applications; normally high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	–	Ground
36	−15V	I	Supply Voltage.
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG, pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity
39	e	O	AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ ($\theta - \phi$).
40	REF	I	AC Reference Input. Used to drive internal demodulator.

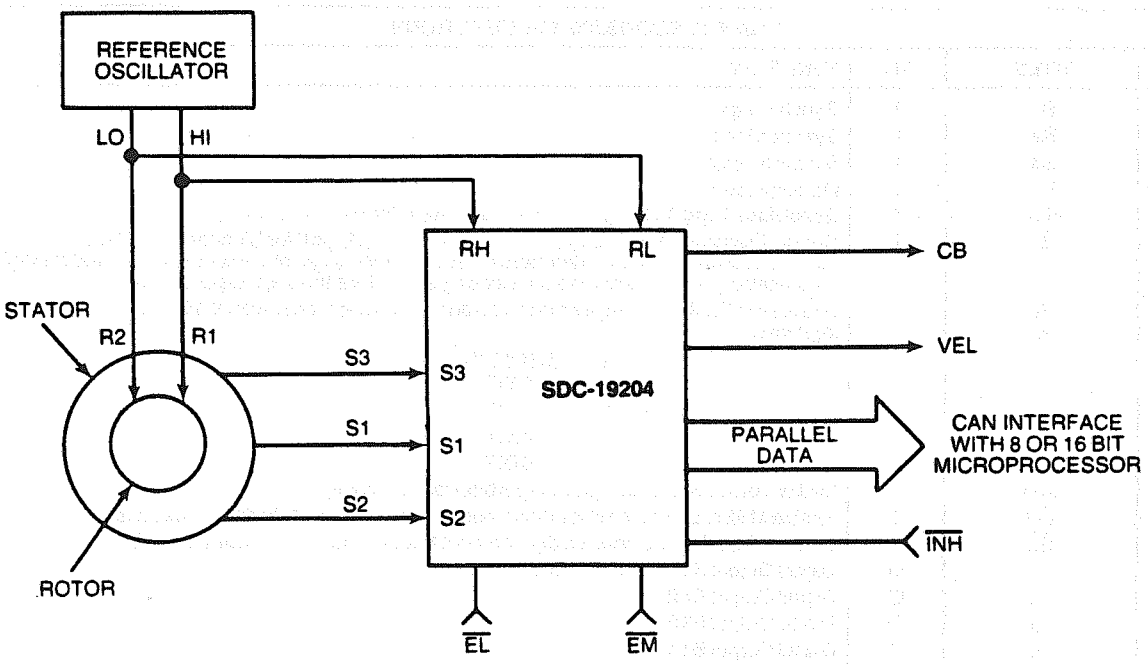


FIGURE 24. SYNCHRO CONNECTION

SOURCES OF SOCKETS FOR THE SDC-19204

The following companies are sources of sockets for use with the SDC-19204 Series. Consult them for more information.

Aries Electronics, Inc.
P.O. Box 30
Frenchtown, NJ 08825
Tel: 1-201-996-6841

Single In-Line Socket
Strip-Line Socket
Part No. 20-05511-11

Circuit Assembly Corp.
3169 Red Hill Avenue
Costa Mesa, CA 92626
Tel: 714-540-5490

Part No. CA-20-STL-XX XX-X

CONNECTING THE SDC-19204

The SDC-19204 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

Since the SDC-19204 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.

Dimensions are inches (mm).

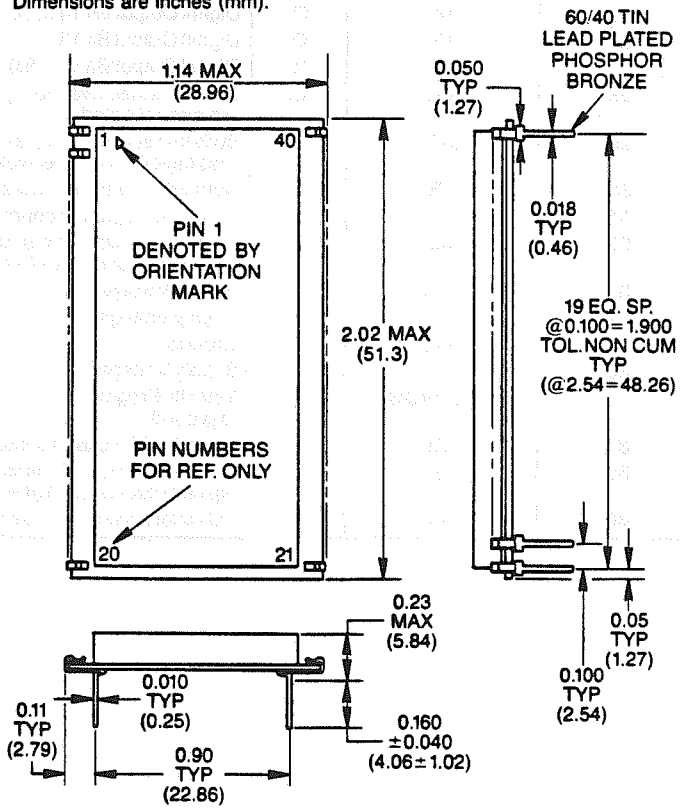
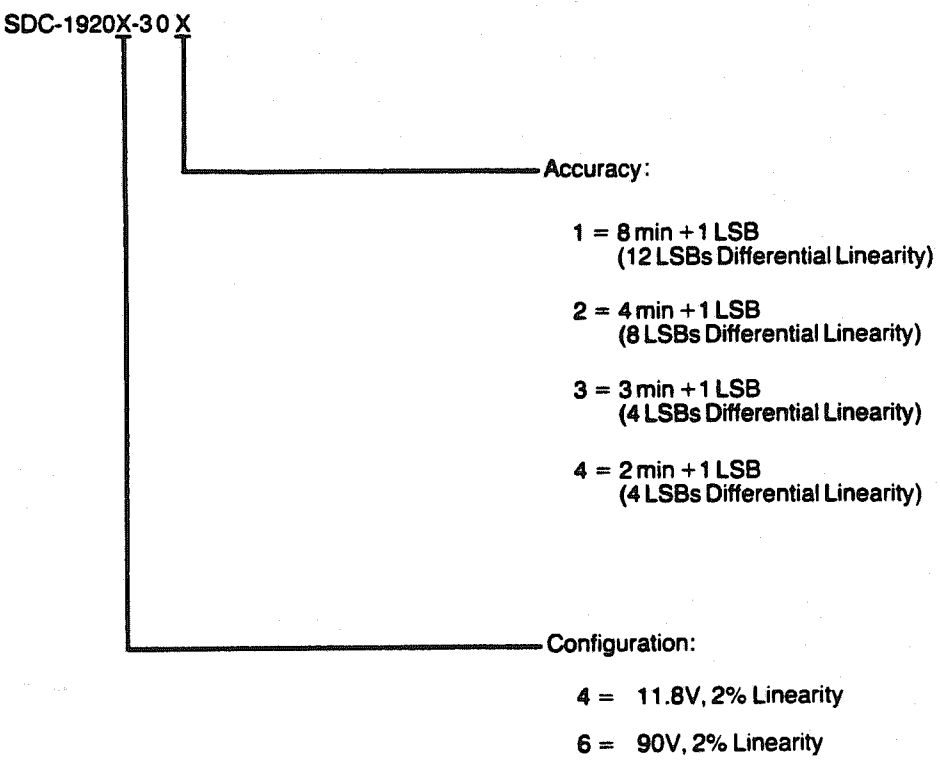


FIGURE 25. SDC-19204 MECHANICAL OUTLINE

ORDERING INFORMATION



Note:
Differential Linearity is x LSB in the 16th bit.