Model V266

16/32/64-channel, 16-bit DAC

INSTRUCTION MANUAL

February, 1997

CONTENTS

FIGURES

TABLES

WARRANTY
PTS

UNPACKING AND INSTALLATION

The Model V266 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the operating environment.

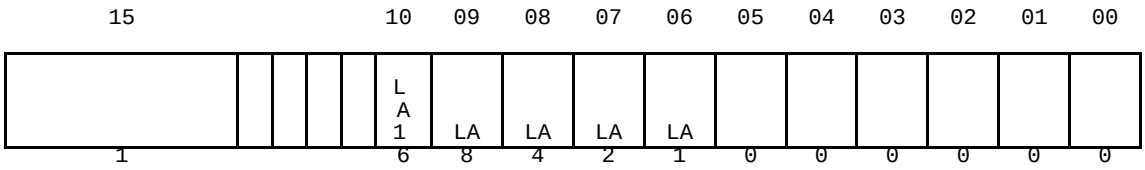
Logical Address Switches

The V266 represents one of the 255 devices permitted in a VXI*bus* system. (Logical Address 0 is reserved for the Slot 0 device.) The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V266 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to Figure 1.)

FIGURE 1 - V266 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the A16 base address is shown below:



Bits 15 and 14 are set to one (VXI defined).

Bits 13 through 6 are user selectable via the address switches LA128-LA1.

Bits 5 through zero are set to "0" to indicate a block of 64 words.

Module Insertion

The V266 is a C-sized, single width VXI*bus* module. It requires 1850 milliamperes of +5, 850 milliamperes of +24, and -24 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-sized VXI*bus* mainframe.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE THE INTERRUPT ACKNOWLEDGE DAISYCHAIN JUMPERS P IN BACKPLANE

To insure proper interrupt acknowledge cycles through the V266 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot.

FRONT PANEL INFORMATION

LEDs

Add Rec This LED turns on when any of the V266's registers are being accessed.

Failed This LED turns on when the V266 has failed or is executing its self-test.

Front Panel Connections

The front panel connections depend upon the option of the V266. The V266-ZA11 and the V266-ZD11 have one connector on the front panel (J3). All other options have two output connectors (J3 and J4). These output connectors are 68-position SCSI-II type receptacle connectors. The connector pinouts are shown on page 7. Additionally, two test points are provided. The test points labeled "+" and "-" provide an auxiliary point to connect to the voltage output of Channel 1.

Note that for the V266-ZB11, 4-20 mA output option, 32- 0v to +10v voltage outputs are available at front panel connector J3 while 32- 4-20 mA outputs are available at connector J4. For a given channel you may use either the 0v to +10v J3 connector output or the 4-20 mA J4 connector output, but not both at the same time. The 0v to +10v outputs serve as the voltage inputs to the 4-20 mA current transmitters. Access to these outputs at connector J3 provides some flexibility when both voltage and current outputs are required.

For the V266-ZC11, +/-16 volt output option, 32- +/-10 volt voltage outputs are available at front panel connector J3 while 32- +/-16 volt voltage outputs are available at connector J4. For a given channel you may use either the +/-10 volt J3 connector output or the +/-16 volt J4 connector output, but not both at the same time. The +/-10 volt outputs are passed through a gain stage to provide the +/-16 volt outputs. Access to the +/-10 volt outputs at connector J3 provides flexibility if the higher resolution and accuracy of the +/-10 volt outputs is required in lieu of the greater output range available at connector J4.

V266-ZA11, ZA21, ZD11 ±10v Output Connector Pinouts

V266 Output Signals - Connector J3				V266 Output Signals - Connector J4			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	CH-1 Signal	35	CH-1 Return	1	CH-33 Signal	35	CH-33 Return
2	CH-2 Signal	36	CH-2 Return	2	CH-34 Signal	36	CH-34 Return
3	CH-3 Signal	37	CH-3 Return	3	CH-35 Signal	37	CH-35 Return
4	CH-4 Signal	38	CH-4 Return	4	CH-36 Signal	38	CH-36 Return
5	CH-5 Signal	39	CH-5 Return	5	CH-37 Signal	39	CH-37 Return
6	CH-6 Signal	40	CH-6 Return	6	CH-38 Signal	40	CH-38 Return
7	CH-7 Signal	41	CH-7 Return	7	CH-39 Signal	41	CH-39 Return
8	CH-8 Signal	42	CH-8 Return	8	CH-40 Signal	42	CH-40 Return
9	CH-9 Signal	43	CH-9 Return	9	CH-41 Signal	43	CH-41 Return
10	CH-10 Signal	44	CH-10 Return	10	CH-42 Signal	44	CH-42 Return
11	CH-11 Signal	45	CH-11 Return	11	CH-43 Signal	45	CH-43 Return
12	CH-12 Signal	46	CH-12 Return	12	CH-44 Signal	46	CH-44 Return
13	CH-13 Signal	47	CH-13 Return	13	CH-45 Signal	47	CH-45 Return
14	CH-14 Signal	48	CH-14 Return	14	CH-46 Signal	48	CH-46 Return
15	CH-15 Signal	49	CH-15 Return	15	CH-47 Signal	49	CH-47 Return
16	CH-16 Signal	50	CH-16 Return	16	CH-48 Signal	50	CH-48 Return
17	CH-17 Signal	51	CH-17 Return	17	CH-49 Signal	51	CH-49 Return
18	CH-18 Signal	52	CH-18 Return	18	CH-50 Signal	52	CH-50 Return
19	CH-19 Signal	53	CH-19 Return	19	CH-51 Signal	53	CH-51 Return
20	CH-20 Signal	54	CH-20 Return	20	CH-52 Signal	54	CH-52 Return
21	CH-21 Signal	55	CH-21 Return	21	CH-53 Signal	55	CH-53 Return
22	CH-22 Signal	56	CH-22 Return	22	CH-54 Signal	56	CH-54 Return
23	CH-23 Signal	57	CH-23 Return	23	CH-55 Signal	57	CH-55 Return
24	CH-24 Signal	58	CH-24 Return	24	CH-56 Signal	58	CH-56 Return
25	CH-25 Signal	59	CH-25 Return	25	CH-57 Signal	59	CH-57 Return
26	CH-26 Signal	60	CH-26 Return	26	CH-58 Signal	60	CH-58 Return
27	CH-27 Signal	61	CH-27 Return	27	CH-59 Signal	61	CH-59 Return
28	CH-28 Signal	62	CH-28 Return	28	CH-60 Signal	62	CH-60 Return
29	CH-29 Signal	63	CH-29 Return	29	CH-61 Signal	63	CH-61 Return
30	CH-30 Signal	64	CH-30 Return	30	CH-62 Signal	64	CH-62 Return
31	CH-31 Signal	65	CH-31 Return	31	CH-63 Signal	65	CH-63 Return
32	CH-32 Signal	66	CH-32 Return	32	CH-64 Signal	66	CH-64 Return
33	Ground	67	Ground	33	Ground	67	Ground
34	Reserved	68	Reserved	34	Reserved	68	Reserved

V266-ZB11 0v to +10v and 4-20 mA Output Connector Pinouts

V266 Output Signals - Connector J3 (0v to +10v)				V266 Output Signals - Connector J4 (4-20 mA)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	CH-1 Signal	35	CH-1 Return	1	CH- 1 Signal	35	CH- 1 Return
2	CH-2 Signal	36	CH-2 Return	2	CH- 2 Signal	36	CH- 2 Return
3	CH-3 Signal	37	CH-3 Return	3	CH- 3 Signal	37	CH- 3 Return
4	CH-4 Signal	38	CH-4 Return	4	CH- 4 Signal	38	CH- 4 Return
5	CH-5 Signal	39	CH-5 Return	5	CH- 5 Signal	39	CH- 5 Return
6	CH-6 Signal	40	CH-6 Return	6	CH- 6 Signal	40	CH- 6 Return
7	CH-7 Signal	41	CH-7 Return	7	CH- 7 Signal	41	CH- 7 Return
8	CH-8 Signal	42	CH-8 Return	8	CH- 8 Signal	42	CH- 8 Return
9	CH-9 Signal	43	CH-9 Return	9	CH- 9 Signal	43	CH- 9 Return
10	CH-10 Signal	44	CH-10 Return	10	CH-10 Signal	44	CH-10 Return
11	CH-11 Signal	45	CH-11 Return	11	CH-11 Signal	45	CH-11 Return
12	CH-12 Signal	46	CH-12 Return	12	CH-12 Signal	46	CH-12 Return
13	CH-13 Signal	47	CH-13 Return	13	CH-13 Signal	47	CH-13 Return
14	CH-14 Signal	48	CH-14 Return	14	CH-14 Signal	48	CH-14 Return
15	CH-15 Signal	49	CH-15 Return	15	CH-15 Signal	49	CH-15 Return
16	CH-16 Signal	50	CH-16 Return	16	CH-16 Signal	50	CH-16 Return
17	CH-17 Signal	51	CH-17 Return	17	CH-17 Signal	51	CH-17 Return
18	CH-18 Signal	52	CH-18 Return	18	CH-18 Signal	52	CH-18 Return
19	CH-19 Signal	53	CH-19 Return	19	CH-19 Signal	53	CH-19 Return
20	CH-20 Signal	54	CH-20 Return	20	CH-20 Signal	54	CH-20 Return
21	CH-21 Signal	55	CH-21 Return	21	CH-21 Signal	55	CH-21 Return
22	CH-22 Signal	56	CH-22 Return	22	CH-22 Signal	56	CH-22 Return
23	CH-23 Signal	57	CH-23 Return	23	CH-23 Signal	57	CH-23 Return
24	CH-24 Signal	58	CH-24 Return	24	CH-24 Signal	58	CH-24 Return
25	CH-25 Signal	59	CH-25 Return	25	CH-25 Signal	59	CH-25 Return
26	CH-26 Signal	60	CH-26 Return	26	CH-26 Signal	60	CH-26 Return
27	CH-27 Signal	61	CH-27 Return	27	CH-27 Signal	61	CH-27 Return
28	CH-28 Signal	62	CH-28 Return	28	CH-28 Signal	62	CH-28 Return
29	CH-29 Signal	63	CH-29 Return	29	CH-29 Signal	63	CH-29 Return
30	CH-30 Signal	64	CH-30 Return	30	CH-30 Signal	64	CH-30 Return
31	CH-31 Signal	65	CH-31 Return	31	CH-31 Signal	65	CH-31 Return
32	CH-32 Signal	66	CH-32 Return	32	CH-32 Signal	66	CH-32 Return
33	Ground	67	Ground	33	Ground	67	Ground

V266 Output Signals - Connector J3 (0v to +10v)				V266 Output Signals - Connector J4 (4-20 mA)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
34	Reserved	68	Reserved	34	Reserved	68	Reserved

V266-ZC11 +/-10v and +/-16v Output Connector Pinouts

V266 Output Signals - Connector J3 (+/-10v)				V266 Output Signals - Connector J4 (+/-16v)			
Pin	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**
1	CH-1 Signal	35	CH-1 Return	1	CH- 1 Signal	35	CH- 1 Return
2	CH-2 Signal	36	CH-2 Return	2	CH- 2 Signal	36	CH- 2 Return
3	CH-3 Signal	37	CH-3 Return	3	CH- 3 Signal	37	CH- 3 Return
4	CH-4 Signal	38	CH-4 Return	4	CH- 4 Signal	38	CH- 4 Return
5	CH-5 Signal	39	CH-5 Return	5	CH- 5 Signal	39	CH- 5 Return
6	CH-6 Signal	40	CH-6 Return	6	CH- 6 Signal	40	CH- 6 Return
7	CH-7 Signal	41	CH-7 Return	7	CH- 7 Signal	41	CH- 7 Return
8	CH-8 Signal	42	CH-8 Return	8	CH- 8 Signal	42	CH- 8 Return
9	CH-9 Signal	43	CH-9 Return	9	CH- 9 Signal	43	CH- 9 Return
10	CH-10 Signal	44	CH-10 Return	10	CH-10 Signal	44	CH-10 Return
11	CH-11 Signal	45	CH-11 Return	11	CH-11 Signal	45	CH-11 Return
12	CH-12 Signal	46	CH-12 Return	12	CH-12 Signal	46	CH-12 Return
13	CH-13 Signal	47	CH-13 Return	13	CH-13 Signal	47	CH-13 Return
14	CH-14 Signal	48	CH-14 Return	14	CH-14 Signal	48	CH-14 Return
15	CH-15 Signal	49	CH-15 Return	15	CH-15 Signal	49	CH-15 Return
16	CH-16 Signal	50	CH-16 Return	16	CH-16 Signal	50	CH-16 Return
17	CH-17 Signal	51	CH-17 Return	17	CH-17 Signal	51	CH-17 Return
18	CH-18 Signal	52	CH-18 Return	18	CH-18 Signal	52	CH-18 Return
19	CH-19 Signal	53	CH-19 Return	19	CH-19 Signal	53	CH-19 Return
20	CH-20 Signal	54	CH-20 Return	20	CH-20 Signal	54	CH-20 Return
21	CH-21 Signal	55	CH-21 Return	21	CH-21 Signal	55	CH-21 Return
22	CH-22 Signal	56	CH-22 Return	22	CH-22 Signal	56	CH-22 Return
23	CH-23 Signal	57	CH-23 Return	23	CH-23 Signal	57	CH-23 Return
24	CH-24 Signal	58	CH-24 Return	24	CH-24 Signal	58	CH-24 Return
25	CH-25 Signal	59	CH-25 Return	25	CH-25 Signal	59	CH-25 Return
26	CH-26 Signal	60	CH-26 Return	26	CH-26 Signal	60	CH-26 Return
27	CH-27 Signal	61	CH-27 Return	27	CH-27 Signal	61	CH-27 Return
28	CH-28 Signal	62	CH-28 Return	28	CH-28 Signal	62	CH-28 Return
29	CH-29 Signal	63	CH-29 Return	29	CH-29 Signal	63	CH-29 Return
30	CH-30 Signal	64	CH-30 Return	30	CH-30 Signal	64	CH-30 Return
31	CH-31 Signal	65	CH-31 Return	31	CH-31 Signal	65	CH-31 Return
32	CH-32 Signal	66	CH-32 Return	32	CH-32 Signal	66	CH-32 Return
33	Ground	67	Ground	33	Ground	67	Ground
34	Reserved	68	Reserved	34	Reserved	68	Reserved

FIGURE 2 - 68-Contact High Density (SCSI II Type) Receptacle

All straps on the V266 are for testing purposes only. They should remain in their factory configured position for proper operation.

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXI*bus* Configuration Registers, The V266 implements those required for extended register-based devices. The V266 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXI*bus* modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see page 10) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

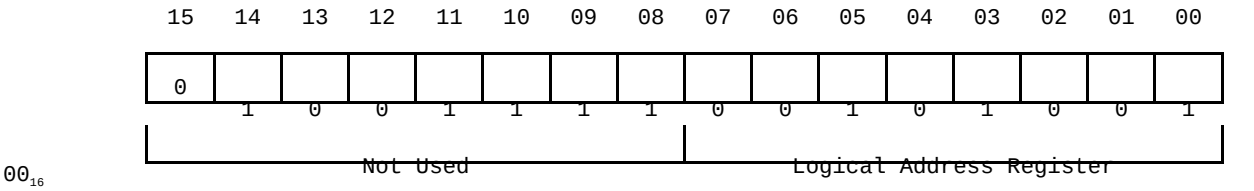
Configuration Registers are required by the VXI*bus* specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V266 are offset from the base address. **Note: the V266 only responds to these addresses if the Short Nonpriviledged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers present in the V266, their offset from the base (Logical) address, and their Read/Write capabilities.

Table 1. Configuration Registers Short Address (A16) Space

A16 Offset	Read/Write Capability	Register Name
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$0A_{16}$	Read Only	Serial Number High Register
$0C_{16}$	Read Only	Serial Number Low Register
$0E_{16}$	Read Only	Version Number Register
10_{16} - 19_{16}	Read Only	Reserved
$1A_{16}$	Read Only	Interrupt Status Register
$1C_{16}$	Read/Write	Interrupt Control Register
$1E_{16}$	Read Only	Subclass Register
20_{16}	Read Only	Suffix Register High
22_{16}	Read Only	Suffix Register Low
24_{16} - $3F_{16}$	Read/Write	User Defined

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address register are as follows:



00_{16}

Read

Write

On READ transactions:

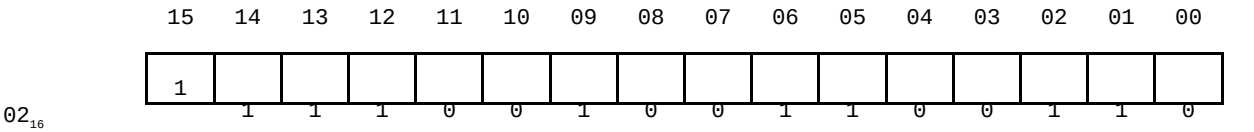
Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is an Extended Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.

11 - 00 Manufacturer's ID3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits fifteen through eight are not used. A write to these bits has no effect on the V266. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

The format and bit assignments for the Device Type register are as follows:



02_{16}

Read

On READ transactions:

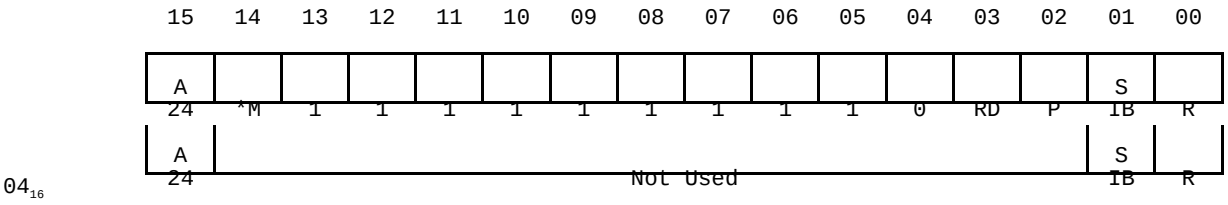
Bit(s)	Mnemonic	Meaning

15 - 12 Required MemoryThe V266 requires 256 bytes of additional memory space.

11 - 0	Model code	Identifies this device as Model V266 (266_{16}).

Status/Control Register

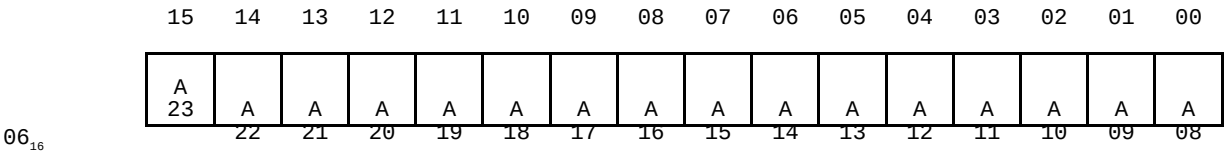
The format and bit assignments for the Status/Control register are as follows:



Bit(s)	Mnemonic	Meaning
15	A24	This bit is written with a "1" enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers**. Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*
14	Modid*	This read only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13 - 04	Not used.	When read will return all "1s". These bits are ignored when written.
03	Ready	A "1" indicates the successful completion of register initialization. This bit is read only.
02	Pass	A "0" indicates that the V266 has failed or is executing its self-test. This bit is read only.
01	Sysfail Inhbit	Writing a "1" to this bit disables the device from driving the SYSFAIL* line. Reads of this bit indicate its current state.
00	Reset	Writing a "1" to this bit forces the device into the Soft Reset condition. While in the Soft Reset state, the module will only allow accesses to Configuration Registers. Writing a "0" to this bit will then force the module to begin its Self Test. This bit must be cleared along with the Passed and Ready bits set before any access to the Operational Registers is allowed.

Offset Register

The format and bit assignments for the Offset Type register are as follows:



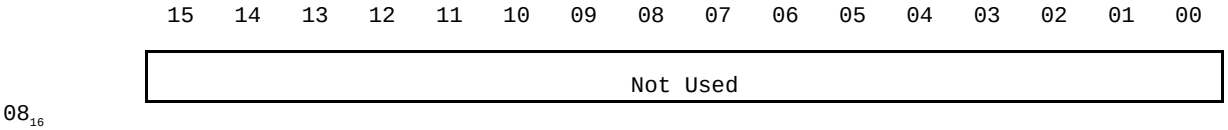
06_{16}

Read

After SYSRESET* and prior to self-test all bits set to "0". Otherwise, a read or write defines the base address of the device's A24 operational registers.

Attribute Register

The format and bit assignments for the Attribute register are as follows:



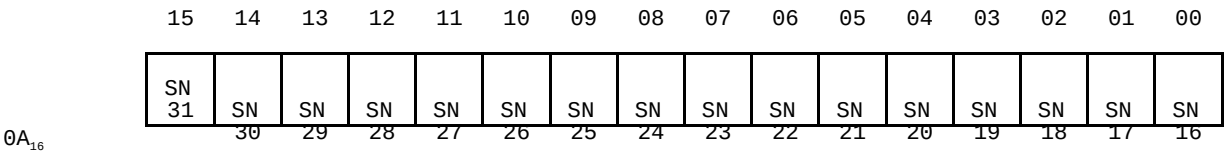
08_{16}

Read

Bit(s)	Mnemonic	Meaning
15 - 00	Not used	A write to these bits has no effect. A read of these bits will return all "1s".

Serial Number High Register

The format and bit assignments for the Serial Number High register are as follows:



$0A_{16}$

Read

This read only register contains the upper code of the module's serial number.

Serial Number Low Register

The format and bit assignments for the Serial Number Low register are as follows:

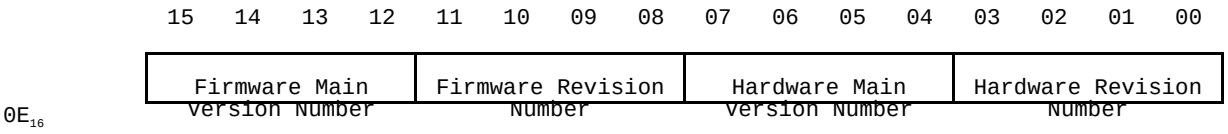
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
$0C_{16}$	SN 15	SN 14	SN 13	SN 12	SN 11	SN 10	SN 09	SN 08	SN 07	SN 06	SN 05	SN 04	SN 03	SN 02	SN 01	SN 0

Read

This read only register contains the lower code of the module's serial number.

Version Number Register

The format and bit assignments for the Version Number register are as follows:



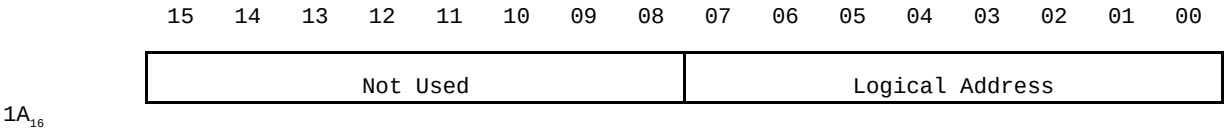
The following patterns are given as an example. The values read will reflect the current revision of the module.

Bit(s)	Mnemonic	Meaning
15 - 12	Firmware Main Version Number	1_{16}
11 - 08	Firmware Revision Number	0_{16}
07 - 04	Hardware Main Version Number	1_{16}
03 - 00	Hardware Revision Number	0_{16}

10_{16} - 19_{16} Reserved

Interrupt Status Register

The format and bit assignments for the Interrupt Status register are as follows:



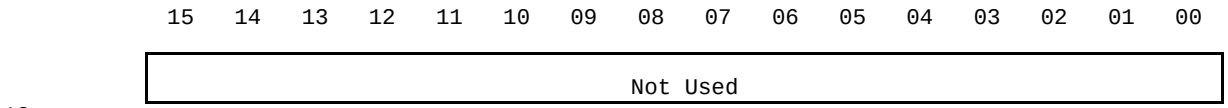
This following bit patterns will be returned during a read of this register.

Bit(s)	Mnemonic	Meaning
15 - 08	Not Used	These bits are read as "1s".

07 - 00	Logical Address	Logical address of the device.

Interrupt Control Register

The format and bit assignments for the Interrupt Control register are as follows:



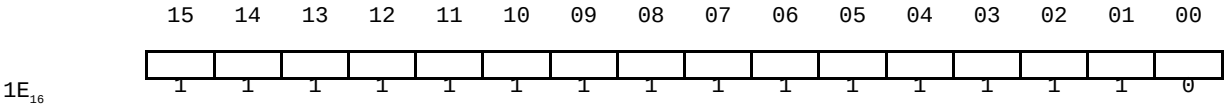
$1C_{16}$

Read

Note: The V266 does not support any interrupt capabilities. For compatibility with other KineticSystems modules, this register is retained. This register should be written with all "1s".

Subclass Register

The format and bit assignments for the Subclass register are as follows:



$1E_{16}$

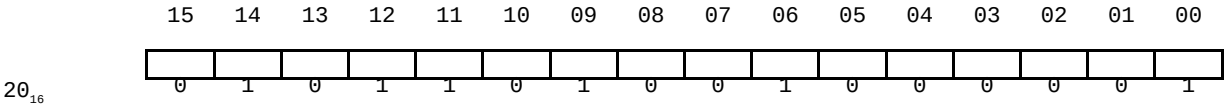
Read

Bit(s)	Meaning
15	VXIbus extended device
14 - 0	$7FFE_{16}$ - Extended Register Based Device

The following two registers contain the ASCII equivalent of the module suffix. This suffix contains the information needed to determine the option of the module. The examples given below are for a V266-ZA11 (32-channel ±10 volt output option). Refer to the Ordering Information to determine the option and its corresponding suffix.

Suffix Register High

The format and bit assignments for the Suffix Register High are as follows:



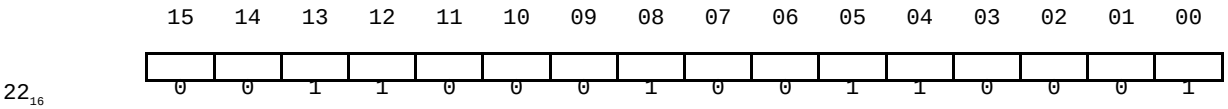
20_{16}

Read

This read only register contains the upper code of the module's suffix (ZA = $5A41_{16}$).

Suffix Register Low

The format and bit assignments for the Suffix Register Low are as follows:



This read only register contains the upper code of the module's suffix (11 = 3131_{16}).

24_{16}-$3F_{16}$ User Defined

These Write/Read registers are contained in non-volatile EEPROM and may be used to store user defined data. Allow 10 milliseconds for writes to these registers.

Operational Registers

The operational registers are the channels through which the various functions of the V266 are controlled. For compatibility with other KineticSystems VXI*bus* modules in this series, these registers are positioned in VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset register within the Configuration Register set.

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V266 will only respond to these addresses if the Standard Address Modifier Codes (3F - $3D_{16}$ or 3B - 39_{16}) are set for the bus cycles.**

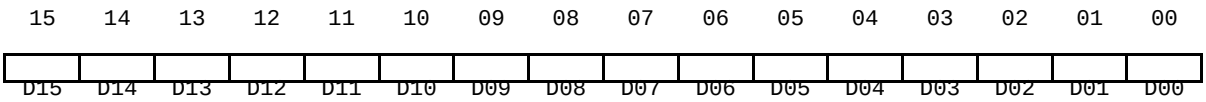
Of the 256 bytes requested by setting bit 15 of the Device Type Register in the Configuration Register set, only 138 bytes are used. (256 bytes is the minimum number of bytes that may be requested through the Device Type register in A24 space.) Table 2 shows the applicable Operational Registers present in the V266, their offset from the base A24 address, and their Read/Write capabilities. **Note: Offsets not listed are not used. Accesses to these locations will return all "1s".**

Table 2. Operational Registers - Standard Address (A24) Space

A24 Offset	Read/Write Capability	Register Name
00_{16}-$7E_{16}$	Read/Write	DAC Registers(64)
80_{16}	Read/Write	DAC Configuration Register
82_{16}- 88_{16}	Read/Write	Self-test Registers(4)

DAC Registers(64 - A24 Offset 00_{16} - $7E_{16}$)

The format and bit assignments for the DAC Registers are as follows:



Each of these output registers contain data for one of the 64 possible channels.

On READ/WRITE transactions:

Bit(s)	Mnemonic	Meaning
15-00	D15-D00	These bits are read and written in offset/straight binary form.

Note: See Table 3 for a description of example digital input codes(D15-D00) and their affect on the analog output for various options.

Channel	A24 Offset	Channel	A24 Offset	Channel	A24 Offset	Channel	A24 Offset
1	00_{16}	17	20_{16}	33	40_{16}	49	60_{16}
2	02_{16}	18	22_{16}	34	42_{16}	50	62_{16}
3	04_{16}	19	24_{16}	35	44_{16}	51	64_{16}
4	06_{16}	20	26_{16}	36	46_{16}	52	66_{16}
5	08_{16}	21	28_{16}	37	48_{16}	53	68_{16}
6	$0A_{16}$	22	22_{16}	38	$4A_{16}$	54	$6A_{16}$
7	$0C_{16}$	23	$2C_{16}$	39	$4C_{16}$	55	$6C_{16}$
8	$0E_{16}$	24	$2E_{16}$	40	$4E_{16}$	56	$6E_{16}$
9	10_{16}	25	30_{16}	41	50_{16}	57	70_{16}
10	12_{16}	26	32_{16}	42	52_{16}	58	72_{16}
11	14_{16}	27	34_{16}	43	54_{16}	59	74_{16}
12	16_{16}	28	36_{16}	44	56_{16}	60	76_{16}
13	18_{16}	29	38_{16}	45	58_{16}	61	78_{16}
14	$1A_{16}$	30	$3A_{16}$	46	$5A_{16}$	62	$7A_{16}$
15	$1C_{16}$	31	$3C_{16}$	47	$5C_{16}$	63	$7C_{16}$
16	$1E_{16}$	32	$3E_{16}$	48	$5E_{16}$	64	$7E_{16}$

Note: Locations 40_{16} - $7F_{16}$ used only on the V266-ZA21 (64-channel ±10 volt output) option.

Table 3. Digital Input Codes

Digital Input Codes	Analog Output (DAC Type)		
	Straight Binary (Unipolar)	Offset Binary (Bipolar)	Two's Complement (Bipolar)
0000_{16}	Zero	- Full Scale	Bipolar Zero
$7FFF_{16}$	+ 2 Full Scale	-1 LSB	+ Full Scale
8000_{16}	- 2 Full Scale	Bipolar Zero	- Full Scale
$FFFF_{16}$	+ Full Scale	+ Full Scale	-1LSB

Note: The unipolar DAC is only used on V266-ZB11(4-20 milliampere current loop option).

DAC Configuration Register

The format and bit assignments for the DAC Configuration Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
														*EN	*EN	2's
80_{16}	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	NU	C	64	/B

On READ/WRITE transactions:

Bit(s)	Mnemonic	Meaning
15-03	NU	These bits not used and read as "1".
02	*EN C	A "0" in this read only bit indicates the presence of a 4-20mA current output card.
01	*EN 64	A "0" in this read only bit indicates the presence of the 64-channel voltage output option.
00	2's/B	This WRITE/READ bit is used to select 2's complement("1") or binary ("0") form. This bit is cleared by writing a "0", or during any Hard/Soft Reset condition. **Binary ("0") form should be selected at all times for the V266-ZB11, 4-20 mA output option.**

Self Test Registers(4 - A24 Offset 82_{16} - $8A_{16}$)

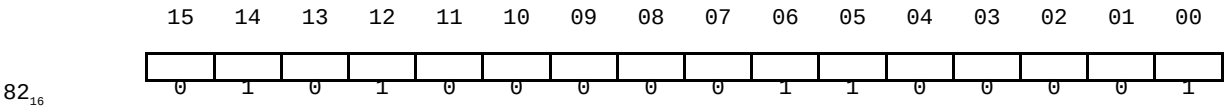
The following registers contain information regarding the module's status. Offset $8A_{16}$ is only used internally by the on-board microprocessor. Writes to this register will be ignored and reads should always return all "0s". Upon successful completion of a self-test, registers 82_{16} - 88_{16} should contain the ASCII equivalent of 'Pass' and 'NoEr'. The Passed and Ready bits contained in the Status/Control Register should also be set to "1s". **Note: Locations 82_{16} - 88_{16} should not be written to if a problem is encountered. The information contained in these registers will be helpful in diagnosing the problem. Otherwise, these registers may be written with any data pattern and should return the last value written.** Similarly, if the module fails its self-test, registers 82_{16} - 86_{16} should contain 'Fail', and 'Er'. Offset 88_{16} should also contain a 16-bit error code as shown below:

Table 4. Self-Test Error Codes

Bit	Error Code: Error indicated by bit(s) set to "1" . Any reserved bits should return "0s".
15	Reserved.
14	Reserved.
13	Reserved.
12	Reserved.
11	Reserved.
10	Reserved.
9	Reserved.
8	Reserved.
7	Reserved.
6	Reserved.
5	Error setting all channels to 0 volts.
4	Error checking DAC output.
3	Error clearing all bit locations.
2	Error setting all bit locations.
1	Error addressing memory.
0	Error testing powerup-zero of memory.

Pass Register High

The format and bit assignments for the Pass Register High are as follows:

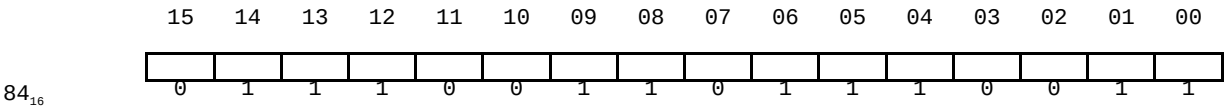


Read

This read/write register contains the upper pass code - 'Pa' = 5061_{16} (or 'Fa' = 4661_{16} if the module fails its self test).

Pass Register Low

The format and bit assignments for the Pass Register Low are as follows:

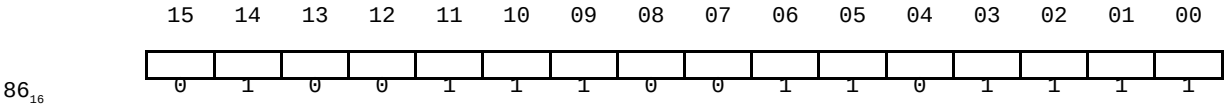


Read

This read/write register contains the lower pass code - 'ss' = 7373_{16} (or 'il' = $696C_{16}$ if the module fails its self test).

Error Register High

The format and bit assignments for the Error Register High are as follows:

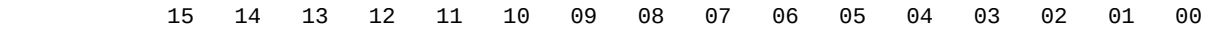


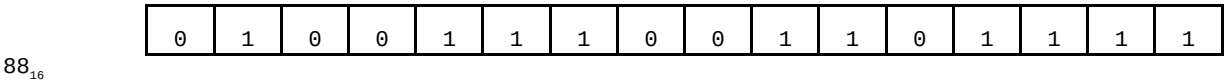
Read

This read/write register contains the upper error code - 'No' = $4E6F_{16}$ (or 'Er' = 4572_{16} if the module fails its self test).

Error Register Low

The format and bit assignments for the Error Register Low are as follows:





88_{16}

Read

This read/write register contains the lower error code - 'Er' = 4572_{16} (or error codes, as listed in Table 4, if the module fails its self test).

OPTION DESCRIPTIONS

Model V266-ZA11 - 32-channel, 16-bit DAC, ±10 volt output

Basic 32-channel model factory upgradeable to all other models.

Model V266-ZA21 - 64-channel, 16-bit DAC, ±10 volt output

Provides a total of 64 channels ±10 volt output.

Model V266-ZB11 - 32-channel, 16-bit DAC, 4-20mA output

Provides 32 channels that may be independently used for either 4-20mA or 0 volt to +10 volt output.

Model V266-ZC11 - 32-channel, 16-bit DAC, ±16 volt output

Provides 32 channels that may be independently used for either ±10 or ±16 volt output.

Model V266-ZD11 - 16-channel, 16-bit DAC, ±10 volt output

Basic 16-channel model factory upgradeable to all other models.

APPENDIX A - BASIC OPERATIONS

CALIBRATION

The V266 is shipped from the factory calibrated for an output range of ±10 volts for the ZA11, ZA21 and ZD11, 0v to +10v (4-20 mA) for the ZB11 and ±10v/±16v for the ZC11. If for any reason it becomes necessary to recalibrate the module, the procedure for D/A offset and gain adjustments is as follows:

Offset Adjustment

The offset adjustment should be made prior to adjusting gain. Set channel one data memory contents to negative full scale (i.e., data of 8000_{16} or 0_{16} when in two's complement or offset binary modes, respectively). Set the data memory contents of the remaining channels for an output of zero volts. (Data of zero or 8000_{16} for two's complement or offset binary modes, respectively.) Adjust the offset potentiometer (PT2) (see Figure 1, page 3) for exactly -10.00000 Volts at channel one's output. Note: Channel one's output is available at both output connector J3 and the two test points located on the front panel. For the ZB11 option, set channel one data memory contents for an output of 4 mA (0 volts at front panel test points or connector J3) i.e., data of 0_{16} for straight binary mode. Adjust the offset potentiometer (PT2) for exactly 4 mA (or 0 volts) at channel one's output.

Gain Adjustment

Set channel one data memory contents to positive full scale (i.e., data of $7FFF_{16}$ or $FFFF_{16}$ when in two's complement or offset binary modes, respectively). Set the data memory contents of the remaining channels for an output of zero volts. (Data of zero or 8000_{16} for two's complement or offset binary modes, respectively.) Adjust the gain potentiometer (PT1) (See Figure 1, page 3) for exactly +9.99969 Volts at channel one's output. Changes in gain may affect the offset; therefore, it is advisable to recheck the calibration for both offset and gain. For the ZB11 option, set channel one data memory contents to full scale output of 20 mA (+9.99969 volts at front panel test points or connector J3) i.e., data of $FFFF_{16}$ for straight binary mode. Adjust the gain potentiometer (PT1) for 20 mA (or +9.99969 volts) at channel one's output.

For the ZC11 ±16v output option, the ±10v outputs available at connector J3 can be calibrated as outlined above. It is recommended that the module be returned to the factory for calibration of the ±16v outputs available at connector J4.

POWER-UP ZERO

During power-up or during a hard or soft reset, the module goes into a sequence of zeroing the memory contents. This sequence and completion of a self test, lasts approximately one second, and any attempts to access the module during this period will be ignored.

INDEX