Model V275-MA11, -MB11, -MC11, -MD11, -ME11

8-channel, 12-bit D/A Converter

INSTRUCTION MANUAL

August, 1992

CONTENTS

FIGURES

TABLES

8-channel, 12-bit DAC

An economical choice for low-channel-count applications

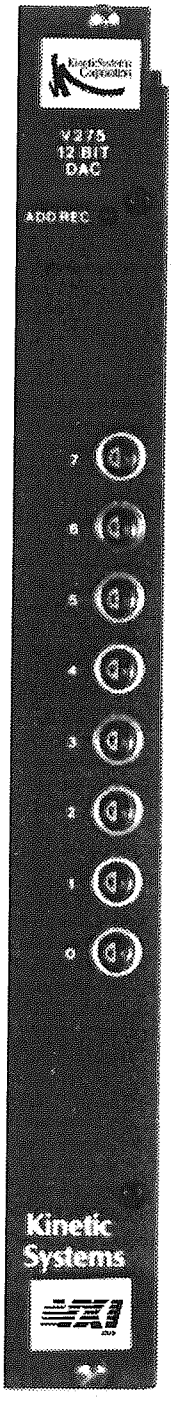
V275

Features

- **8 independent analog outputs**
- **5 output voltage options**
- **12-bit resolution (one part in 4096)**
- **5 mA drive capability**
- **Low drift**
- **4 µs settling time**
- **Outputs reset to 0 V at power-on**

Typical Applications

- **Industrial control**
- **Automatic Test Equipment (ATE)**
- **General-purpose control applications**



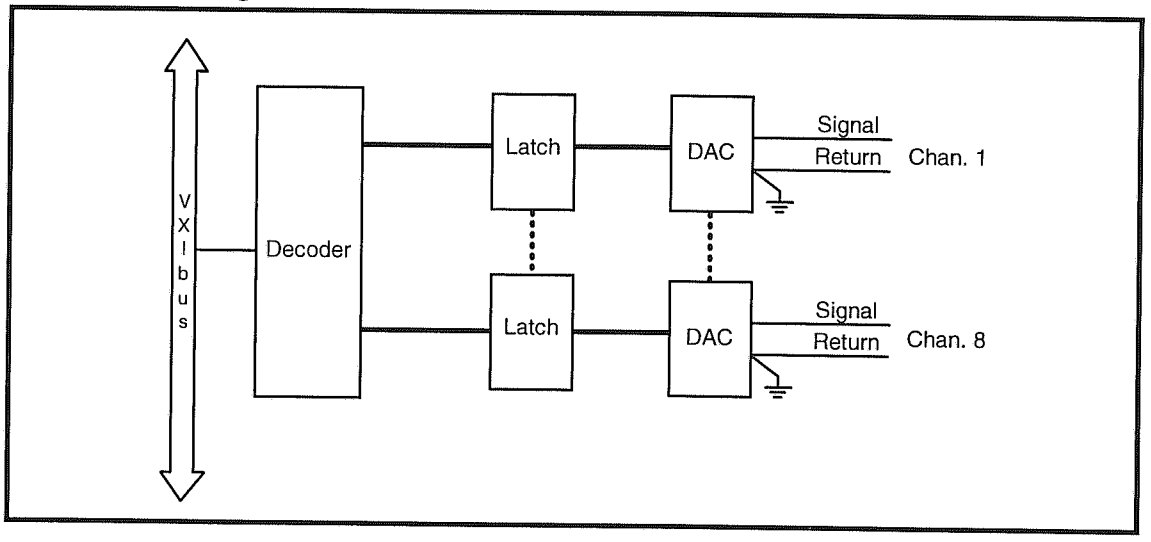
General Description *(Product specifications and descriptions subject to change without notice.)*

The V275 is a single-width, C-size, register-based, VXIbus module for generating eight output voltages. The standard output is 0 to +10 V with a maximum load of 5 mA. Options of the module are available with output ranges of 0 to +5 V, ±2.5 V, ±5 V, and ±10 V. A 12-bit register is provided for each channel. The data is written in two's complement format, and is right-justified (i.e., the LSB is written to D00). Settling time of the output to within 1/2 LSB is less than 4 µs. The output impedance is less than 100 mΩ. The outputs of the V275 will withstand an indefinite short circuit to ground.

The V275 is calibrated at the factory for zero offset and accurate gain. All outputs are referenced to a common ground (module ground). In critical applications, these signals should be received by differential input circuits.

The V275 supports both static and dynamic configuration. Access to the dual-ported memory is via memory locations pointed to by the Offset Register within the VXIbus Configuration Register set, using A24/16, D16 data transfers. All eight channels are accessed using the same VXIbus address.

V275 Block Diagram



Item	Specification
Number of Channels	8
Full-scale Output	0 to +10 V, 0 to +5 V, ±2.5 V, ±5 V, and ±10 V (by order option)
Resolution	12 bits (one part in 4096)
Linearity Error	±½ LSB
Monotonicity	Monotonic to 12 bits
Output Impedance	Less than 0.1 Ω
Output Current	±5 mA
Output Protection	Can withstand short circuit to ground
Settling Time	4 µs, maximum to within ½ LSB for a 20 V change
Output Connector Type	2-contact LEMO connectors
Mating Connector	KineticSystems Model 5911-Z1A
Power Requirements	
+5 V	1.6 A, typical
+24 V	100 mA, typical
-24 V	200 mA, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to +40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V275-MA11 8-channel, 12-bit D/A converter; 0 to +5 V output
Model V275-MB11 8-channel, 12-bit D/A converter; 0 to +10 V output
Model V275-MC11 8-channel, 12-bit D/A converter, ± 2.5 V output
Model V275-MD11 8-channel, 12-bit D/A converter; ± 5 V output
Model V275-ME11 8-channel, 12-bit D/A converter; ± 10 V output

Related Products

Model 5857-Cxyz Cable—2-contact LEMO to Unterminated
Model 5857-Dxyz Cable—2-contact LEMO to 2-contact LEMO
Model 5857-Gxyz Cable—1-contact LEMO to BNC shielded
Model 5911-Z1A Connector—2-contact LEMO

UNPACKING AND INSTALLATION

The Model V275 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V275 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V275 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. Refer to FIGURE 1 below.

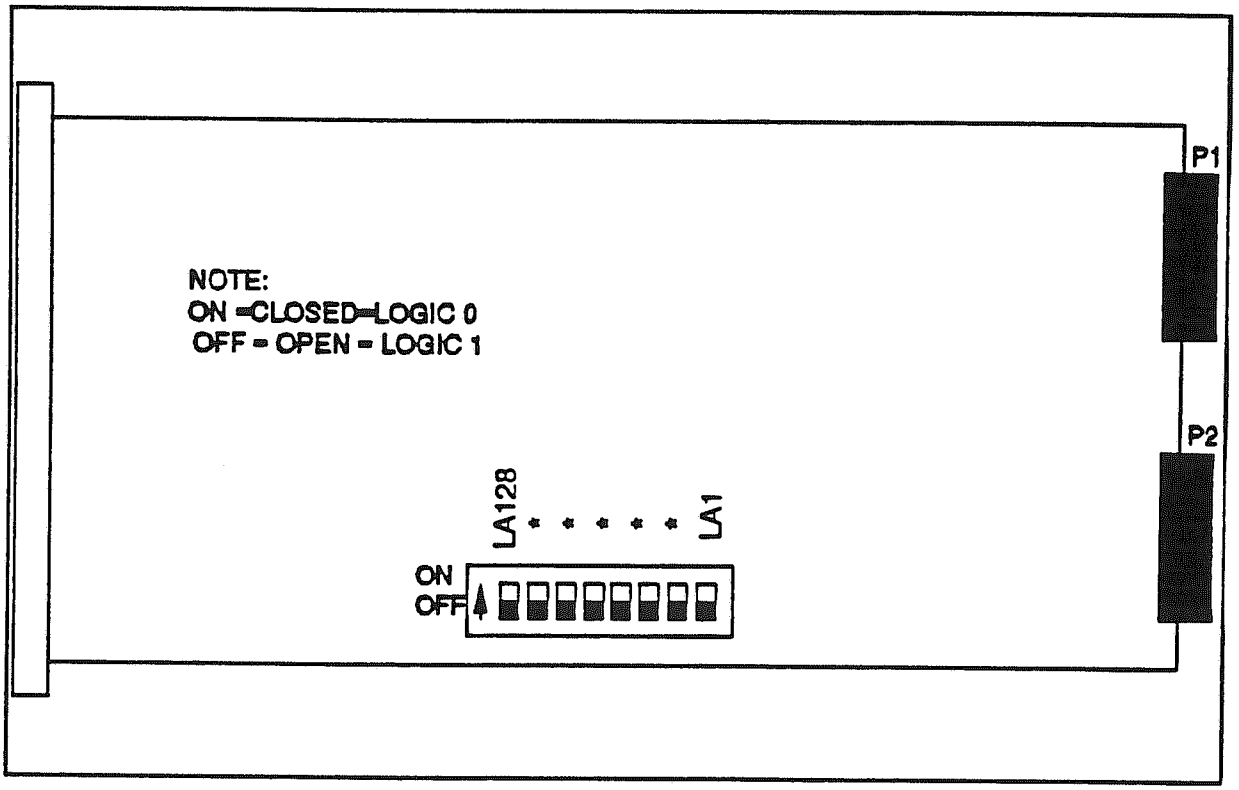


FIGURE 1 - V275 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe, pencil point, or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (VXI defined).
Bits 13 through 6 are user-selectable via the address switches LA128-LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupts

The V275 does not generate interrupts. No switches are provided for setting the interrupt request level.

Module Insertion

The V275 is a C-sized, single width VXIbus module. It requires 1600 milliamperes of +5 volt power, 100 milliamperes of +24 volt power, 200 milliamperes of -24 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus mainframe.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING THIS MODULE IN THE BACKPLANE

Even though the V275 does not generate interrupts, it does maintain the Interrupt Acknowledge continuity through the slot in which it is positioned. The daisy-chain jumpers must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V275 and the Slot 0 Controller.

Connectors

A two-contact LEMO connector is provided for each of the eight output signals. The analog output signal is on the pin portion of the connector, and the return signal is on the socket portion.

OUTPUT VOLTAGE INFORMATION

The V275 has five ordering options, conforming to the five output signal ranges available.

TABLE 1
V275 VOLTAGE OUTPUT OPTIONS

V275 OPTION	VOLTAGE OUTPUT
-MA11	0 to +5 volts
-MB11	0 to +10 volts
-MC11	±2.5 volts
-MD11	±5 volts
-ME11	±10 volts

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V275 implements those required for register-based devices. The V275 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see next page) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIBUS Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V275 are offset from the base address. **Note: The V275 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address**

Modifier Codes are set for the backplane bus cycle. Table 1 shows the applicable Configuration Registers present in the V275, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 2
CONFIGURATION REGISTERS - SHORT I/O ADDRESS SPACE

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

The other 52 byte addresses within the Configuration Register address space are either dedicated to VXIbus Message-Based devices or are reserved for future use by the VXIbus specification, and are not used in the V275.

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	R
	NOT USED								LOGICAL ADDRESS REGISTER								W

On READ transactions,

Bit(s)	Label	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space	This module requires the use of the A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V275. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

The format and bit assignments for the Device Type Register are as follows:

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	0	0	1	1	1	0	1	0	1	R

On READ transactions:

Bit(s)	Label	Meaning
15 - 12	Required Memory	The V275 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V275 (275_{16}).

Status/Control Register

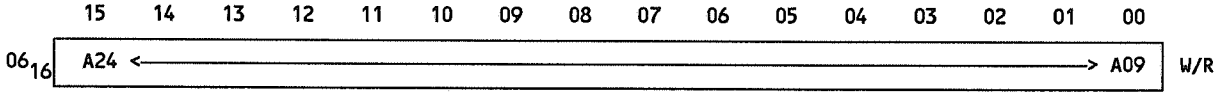
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	ZEROS								RDY	PASS	0	RST	R
	A24 ENA	N/U	N/U	1	NOT USED											RST	W

Bit(s)	Label	Meaning
15	A24 Enable	This bit is written with a "1" to enable A24 addressing, and reset (to "0") to disable A24 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V275. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1".

11 - 04	Not Used	When read, will return all "0"s. These bits are ignored when written.
03	Ready	Along with Bit 02 (Passed), this Read-only bit will appear as a "1" to indicate its readiness to accept operational commands.
02	Passed	See the Ready bit description.
01	Not Used	Read as "0" and ignored on write transactions.
00	Reset	This Read/Write bit controls the Soft Reset condition within the V275. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up, or the assertion of SYSRESET*.

Offset Register

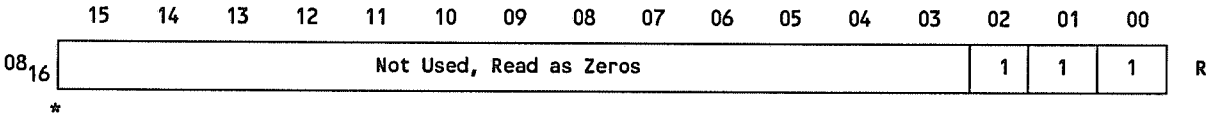
The format and bit assignments for the Offset Register are as follows:



This Read/Write register defines the base address of the V275's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Interrupt Attribute Register

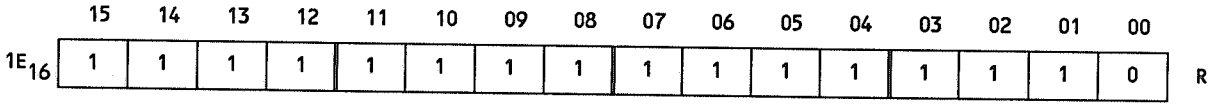
The format and bit assignments for the Interrupt Attribute Register are as follows:



Bit(s)	Label	Meaning
15 - 03	Not Used	These bits are not used by the V275, and are read as zeros.

02	Intr Control	The V275 does not have Interrupt Control capabilities.
01	Intr Handler	The V275 does not have Interrupt Handler capabilities.
00	Intr Status	The V275 does not have an Interrupt Status register.

Subclass Register



Bit(s)	Label	Meaning
15	Extended Device	"1" indicates that this is a VXIbus defined Extended Device.
14 - 00	Register-Based	$7FFE_{16}$ indicates that this is an Extended register-based Device.

Operational Registers

The Operational Registers are the channels through which the outputs of the V275 are set. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in the VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set (see above).

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register. **Note: The V275 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

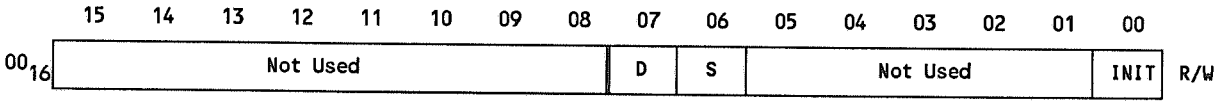
Of the 256 bytes requested by the setting of the Device Type Register in the Configuration Register set, only 18 bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V275, their offset from the base (A24) address, and their Read/Write capabilities.

TABLE 3
V275 OPERATIONAL REGISTERS - STANDARD ADDRESS SPACE

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	Diagnostic Register
12_{16}	Write Only	Channel #1 Output
16_{16}	Write Only	Channel #2 Output
$1A_{16}$	Write Only	Channel #3 Output
$1E_{16}$	Write Only	Channel #4 Output
22_{16}	Write Only	Channel #5 Output
26_{16}	Write Only	Channel #6 Output
$2A_{16}$	Write Only	Channel #7 Output
$2E_{16}$	Write Only	Channel #8 Output

Diagnostic Register

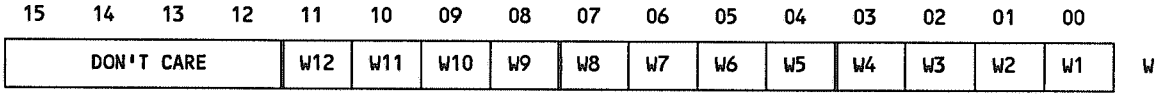
This register is included for diagnostic purposes, and is not accessed as part of a normal output operation. The format and bit assignments for the Diagnostic Register are as follows:



Bit(s)	Label	Meaning
15 - 08	Not Used	On Read transactions, these bits return an all "0" pattern. On Write transactions, they are ignored by the module.
07	Diagnostic	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $2E_{16}$) was valid.
06	Status	When this bit is set to a "1", the last register access to the Operational Registers (offsets 12_{16} through $2E_{16}$) was accepted.
05 - 01	Not Used	On read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module.
00	Initialize	Setting this bit to a "1" will only reset the Operational Registers (offsets 12_{16} through $2E_{16}$). The Configuration and Diagnostic registers are unaffected.

Output Registers

The ouput registers for each channel are written in 2's-complement form. The status bit in the Diagnostic register should always equal "1". Each channel's offset value (from the base value written into the Offset Register) is given in table 3. The data format for these registers is as shown here.



V275 REGISTER LAYOUT

CONFIGURATION REGISTERS

ID/Logical Address Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	R
	DON'T CARE								LOGICAL ADDRESS REGISTER								W

Device Type

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	0	0	1	0	0	0	1	1	1	R

Status/Control Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	ZEROS								RDY	PASS	0	RST	R
	A24 ENA	N/U	N/U	1	NOT USED											RST	W

Offset Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A24 <—															A9	W/R

Attribute Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	NOT USED													1	0	1	R

Subclass Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	R

OPERATIONAL REGISTERS

Diagnostic Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Don't Care								D	S	0	0	0	0	0	0	R
	Don't Care								0	0	0	0	0	0	0	INIT	W

Output Registers (Offsets 12_{16}, 16_{16}, $1A_{16}$, $1E_{16}$, 22_{16}, 26_{16}, $2A_{16}$, and $2E_{16}$)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
DON'T CARE				W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W