Model V285

8/16-Channel, 16 Bit, 500kHz
DAC/Waveform Generator

INSTRUCTION MANUAL

February 16, 1998

KINETICSYSTEMS COMPANY, LLC

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FIGURES

8 or 16-channel, 16-bit, 500 kHz DAC/Waveform Generator

A high-resolution multichannel arbitrary waveform generator

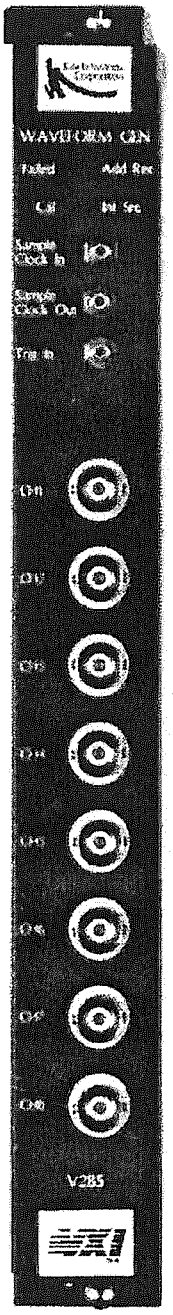
V285

Features

- 16-bit DAC per channel
- Built-in calibration and self-test
- 10 kHz or 100 kHz programmable,4-pole, Bessel filter per channel
- 1 or 4 Mbyte waveform memory option with single shot or continuous modes
- Simultaneous update of all channels
- Programmable clock from 100 Hz to 500 kHz in 1, 2, 5, … progression
- Arbitrary waveform generation capability using LabVIEW

Typical Applications

- Satellite testing
- Missile target simulation
- Hardware-in-the-loop simulation
- Signal synthesis



General Description (*Product specifications and descriptions subject to change without notice)*

The V285 is a single width, C-size, register-based, VXIbus module that is a 16-bit, precision, arbitrary waveform generator. It includes a DAC per channel and is capable of update rates to 500 kHz per channel. Each analog channel includes a 4-pole, Bessel filter with programmable cutoff frequencies of 10 kHz and 100 kHz. A 16-bit ADC/multiplexer allows all channels to be automatically tested and calibrated.

The V285 Waveform Generator optionally includes either a 1 Mbyte or 4 Mbyte RAM memory. This memory may be configured either for multibuffer operation, in which data is continuously updated via the VXIbus, or it may be preloaded with waveforms. These waveforms may be continuously output (in recirculate mode) or output once per trigger (in one-shot mode).

The waveform generator can also be loaded one sample at a time via a set of addressable VIXbus registers (one per DAC channel). The register contents are clocked into the DAC synchronously with the sample clock.

Alternatively, the waveform generator can accept the waveform data over Digi-bus™. Digi-bus data is selected from a "data frame" and stored in a set of holding registers, one for each DAC channel. At the next sample clock or start of Digi-bus frame, the data is strobed from the registers into the respective DACs. This allows the V285 data to be accepted directly from a DSP module such as the V165.

The waveform generator employs a sample clock to simultaneously update all channels. This clock can be selected to be an internals, crystal-controlled clock; a VXI trigger line; a Digi-bus start-of-frame; or an external, front-panel, user-supplied clock.

The V285 supports static and dynamic configuration. It may be accessed using A32/A16, D32/D16 data transfers.

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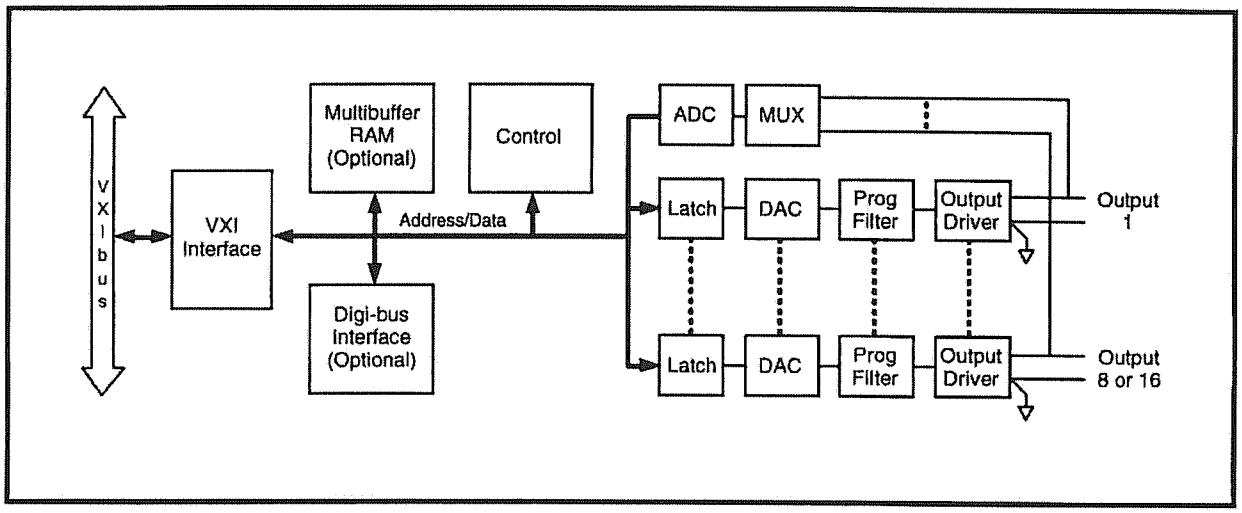
V285 (continued)
V285 Block Diagram



Item	Specification
Number of Channels	8 or 16
Output Signal Range	±10,24 V @ 25 mA (with calibration)
Resolution	16 bits
Linearity Error	±0.003% FSR, typical; ±0.006% FSR, max (with calibration)
DC Gain Error	±0.075% FSR, typical; ±0.2% FSR, max (with calibration)
DC Offset Error	±0.05% FSR, typical; ±0.1% FSR, max (with calibration)
Distortion	-96 dB max. THD
Output Impedance	0.1 Ω
Output Protection	Current limiting for short circuit to ground
Output Connector Type	BNC for 8-channel option 50S High Density for 16-channel option
Maximum Transfer Rates Digi-bus option Multibuffer option	 10 Mbyte/s 6.4 Mbyte/s
Power Requirements +5 V -5.2 V +24 V -24 V	ZA11 ZB11 ZC11 ZD11 ZA21 ZB21 ZC21 ZD21 5.0A 6.0A 6.0A 6.0 6.0A 7.0A 7.0A 7.0A 215mA 215mA 215mA 215mA 420mA 420mA 420mA 420mA 280mA 280mA 280mA 280mA 550mA 550mA 550mA 550mA 240mA 240mA 240mA 240mA 475mA 475mA 475mA 475mA
Environmental & Mechanical Temperature range Operational Storage Relative humidity Cooling requirements Dimensions Front-panel potential	 0° to 50°C -25°C to +75°C 0 to 85%, non-condensing to 40°C 10 CFM 340 mm x 233.35 mm x 30.48 mm (C-size VXIbus) Chassis ground

Ordering Information

Model V285-ZA11	8-channel, 16-bit, 500 kHz DAC/Waveform Generator
Model V285-ZD11	8-channel, 16-bit, 500 kHz DAC/Waveform Generator w/4 Mbyte RAM
Model V285-ZA21	16-channel, 16-bit, 500 kHz DAC/Waveform Generator
Model V285-ZB21	16-channel, 16-bit, 500 kHz DAC/Waveform Generator w/1 Mbyte RAM
Model V285-ZD21	16-channel, 16-bit, 500 kHz DAC/Waveform Generator w/4 Mbyte RAM
Model V285-0001	Digi-bus Factory Upgrade
Model V285-0002	1 Mbyte Buffer Factory Upgrade
Model V285-0004	4 Mbyte Bufer Factory Upgrade

Related Products

Model 5819-Axyz	Cable – 50P High Density to Unterminated
Model 5819-Cxyz	Cable – 50P High Density to 50S Amphenol Ribbon
Model 5819-Exyz	Cable – 50P High Density to 50P High Density (V285 to V765)
Model 5819-Fxyz	Cable – 50S High Density to 50P High Density
Model V754-ZA11	Termination Assembly for V285
Model V765-ZA11	Rack-mount Termination Panel

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UNPACKING AND INSTALLATION

The Model V285 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V285 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V285 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to Figure 1.)

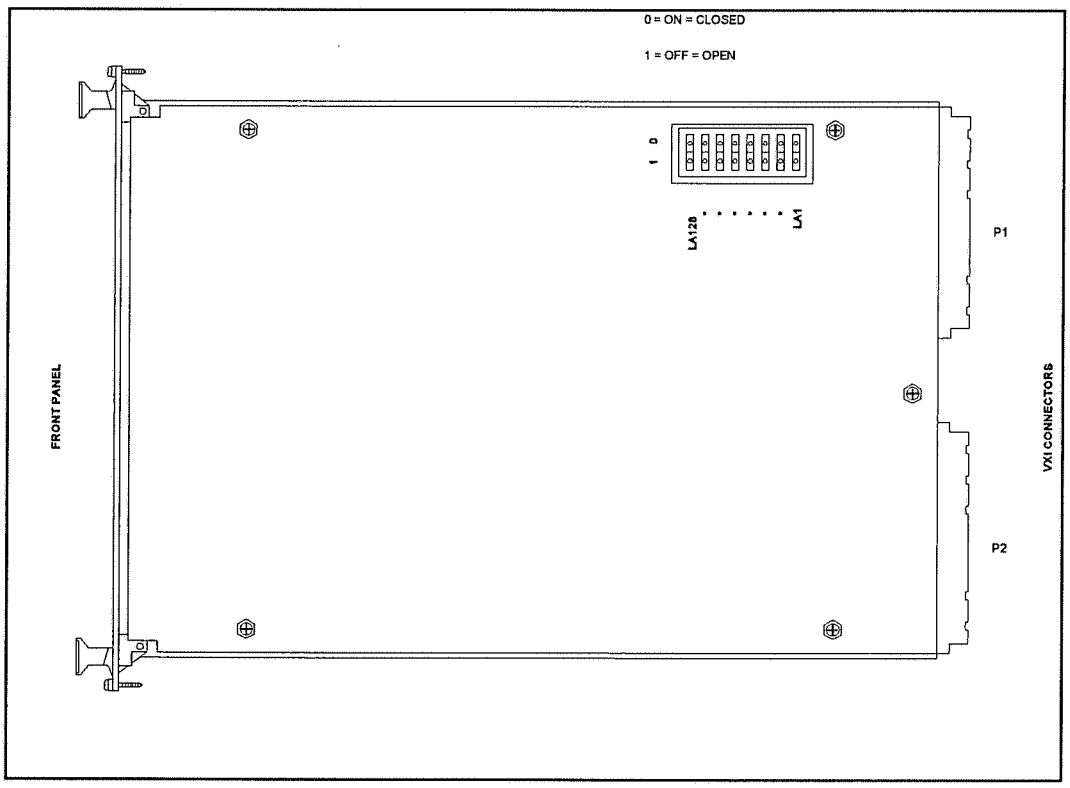

Figure 1 - V285 Switch Locations

Model V285

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 and 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 words.

Module Insertion

The V285 is a C-sized, single width VXIbus module. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame. For MUX-bus operation, the module must be to the right of an ADC module.

CAUTION:	TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING:	REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V285 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V285 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC - The Addressed Received LED is illuminated when the registers are being accessed.

FAILED - The Failed LED is illuminated when the V285 has failed its self-test.

INT SRC - The Interrupt Source LED is illuminated as long as the V285 has an interrupt source pending. The interrupt source indicates that a condition exists for generating an interrupt.

CONNECTORS

(8 Channel Option)

There are three SMB connectors on the front panel:

Sample Clock In - Allows an external sample clock to be used for conversion, if selected by the software. (TTL rising edge)

Sample Clock Out - Allows a Sample clock output. (TTL rising edge)

Trig In - Allows an external trigger to be input which may generate an event, if enabled. (TTL falling edge)

Channel Ouputs - Eight isolated BNC connectors on the front panel.

(16 Channel Option)

There are two high density 50 pin SCSI II type connectors mounted on the front panel. For a definition of the pins on these connectors, see Figure 3.

GENERAL DESCRIPTION

This single width C-size module conforms both electrically and mechanically to the VXI specification.

The V285 8/16 Channel DAC/Waveform Generator is a 16-bit precision arbitrary waveform generator. It includes a D/A per channel and is capable of update rates to 500kHz per channel. Each analog channel includes a 4-pole Bessel filter with programmable corner frequencies of 10kHz and 100kHz to minimize harmonics in the output waveform. A 16 bit ADC/multiplexer allows all channels to be tested and calibrated.

The Arbitrary Waveform Generator optionally includes a 1M byte or 4M byte multibuffer RAM memory which can be either loaded with waveform segments as data is clocked out or it can be loaded once with a waveform and placed in "trigger" mode. The output waveform generation can also be synchronized by an external or VXI "trigger". In single shot mode each "trigger" will cause the waveform generator to generate the waveform stored in RAM. In continuous mode the "trigger" will cause the waveform generator to generate one segment of a waveform repetitively.

The waveform generator can also be loaded a sample at a time via a set of addressable VXI bus registers (one per DAC channel). Synchronous with the "sample clock" the registers are clocked into the DAC and the output channels are simultaneously updated.

Alternatively the waveform generator can accept the waveform data over Digi-bus. Digi-bus data is selected from a "data frame" and stored in a set of holding registers, one for each DAC channel. At the next "sample clock" or start of Digi-bus frame, the data is strobed from the registers into the respective DAC's.

The waveform generator employs a "sample clock" to simultaneously update all channels. This clock can be selected, on a channel-by-channel basis, to be an internal crystal controlled clock, a VXI trigger line, a Digi-bus start-of-frame, or an external front-panel user-supplied clock.

This module contains a microcontroller and 16 bit Sigma-Delta ADC which together provide the ability to perform sophisticated self-test and calibration functions. In self-test mode a sequence of codes are fed to each channels Digital to Analog Converter, while the output is monitored by the ADC. This value is then compared against predetermined test limits to verify proper operation. In calibrate mode the ADC first calibrates itself and then the transfer function of each channel is measured and the M and B values stored in EEPROM.

The outputs are disconnected from the front panel connectors via relays while self test and calibration occurs, after which the outputs can be explicitly enabled.

FUNCTIONAL DESCRIPTION

Sample Clock Selection

One of four sources may be selected to provide the sample clock for the Digital to Analog Converters. The Sample Clock Register (0x00) must be programmed to provide the appropriate source.

Data Source

One of three data sources may be used to drive the Digital to Analog Converters (DAC).

VXIbus Interface

The base module allows data to be written directly from the VXIbus. To do this, select the VXIbus Data Source in the Data Source Register (0x04). The data is written to the appropriate register (0x10 - 0x2E) for that channel. On the next clock edge of the sample clock, the dataword will be presented to the DAC. All channels will be loaded synchronously on this clock edge. The loading sequence for the DACs consists of shifting out a serial bit stream (clocked at a 20MHz. rate) to the DACs. On the 24th clock edge the DAC output will be updated. This means that there will always be a fixed delay of 1.2 microseconds from the clock edge until the DAC output changes.

MultiBuffer Option

If the Multibuffer option is installed, one of several operating modes are possible.The MBUF Scan List controls the routing of the contents of MultiBuffer memory to the appropriate channel.

If MultiBuffer mode is selected in the MBUF_Mode Register (0x220), the data will be buffered from the VXIbus. In this mode, data may be written asynchronously from the VXIbus into MultiBuffer memory, and will be clocked out to the DACs by the Sample Clock. Up to four MultiBuffer partitions may be selected, providing considerable protection against latency in the data source.

If Recirculation Mode is selected, a waveform which has been preloaded into the MBUF RAM (0x400000 - 0x7FFFFF) will be output continuously. The MBUF Scan List (0x200 -0x21E) will contain the channel list to route the MBUF data to the

appropriate channel. The Total_MBUF_Size registers (0x222, 0x224) are used to specify the size of the waveform buffer.

One-shot Mode is similar to the re-circulate mode except that the stored waveform will be output once each time an event trigger occurs. The trigger source is specified in the Trigger Line Register (0x02).

NOTE: The composite rate of 3.2 Mwords/Sec may not be exceeded when transferring data from the multi-buffer RAM to the DAC data registers. The following equation will aid in determining the maximum sample clock frequency for a given number of channels:

$$\text{Sample Clock Freq} \leq \frac{(3.2 \times 10^6)}{\#\text{ channels}}$$

Digi-Bus Option

The V285 has an optional Digi-bus interface. If this option is installed, the V285 may be configured to accept Digi-bus data from one of KineticSystems' Digi-bus Source modules (ie. V165, V207, V208 etc.). A single Digi-bus frame can consist of up to 2048 samples. The V285 can be configured to select any one of these data samples by programming enabling the appropriate bits in Digi-bus Selection Bit Array (0x80 - 0x17E).

The Word Destination Registers (0x182 - 0x186) determine the channel destination for the data samples received by the V285. The Digi-bus Frame Count register (0x180) contains the ENA CAP bit which must be set to allow acceptance of Digi-bus data as well as the Frame Count Interval bits determining which frames will be accepted by the V285.

Output Filtering

Each DAC has a programmable 4 pole Bessel filter at its output, to filter out the steps created as each sample is updated. The filter corner frequency can be selected to be either 10kHz. or 100kHz. by writing to the Sample Clock Register (0x00). Upon initialization the 00kHz. corner will be selected.

Interrupt Sources

The V285 has seven potential sources of interrupts. These sources are as follows:

Interrupt Source 0 -- External Trigger from TTL Trigger Lines
Interrupt Source 1 -- External Trigger from Front Panel Trig In
Interrupt Source 2 -- Multibuffer Empty Flag #1
Interrupt Source 3 -- Multibuffer Empty Flag #2
Interrupt Source 4 -- Multibuffer Empty Flag #3
Interrupt Source 5 -- Multibuffer Empty Flag #4
Interrupt Source 6 -- Multibuffer Underrun

These Interrupt Sources have individual "Mask Bits" as specified in the Interrupt Control register (0x1C -- A16 Space). Programming a "1" for the Mask Bits disables Interrupt generation for the corresponding Interrupt Source. Programming a "0" for the Mask Bits enables Interrupt generation for the corresponding Interrupt Source. In addition to an interrupt being generated on the VXI Backplane, the INT SRC LED on the front panel will be illuminated whenever the V285 has an interrupt pending.

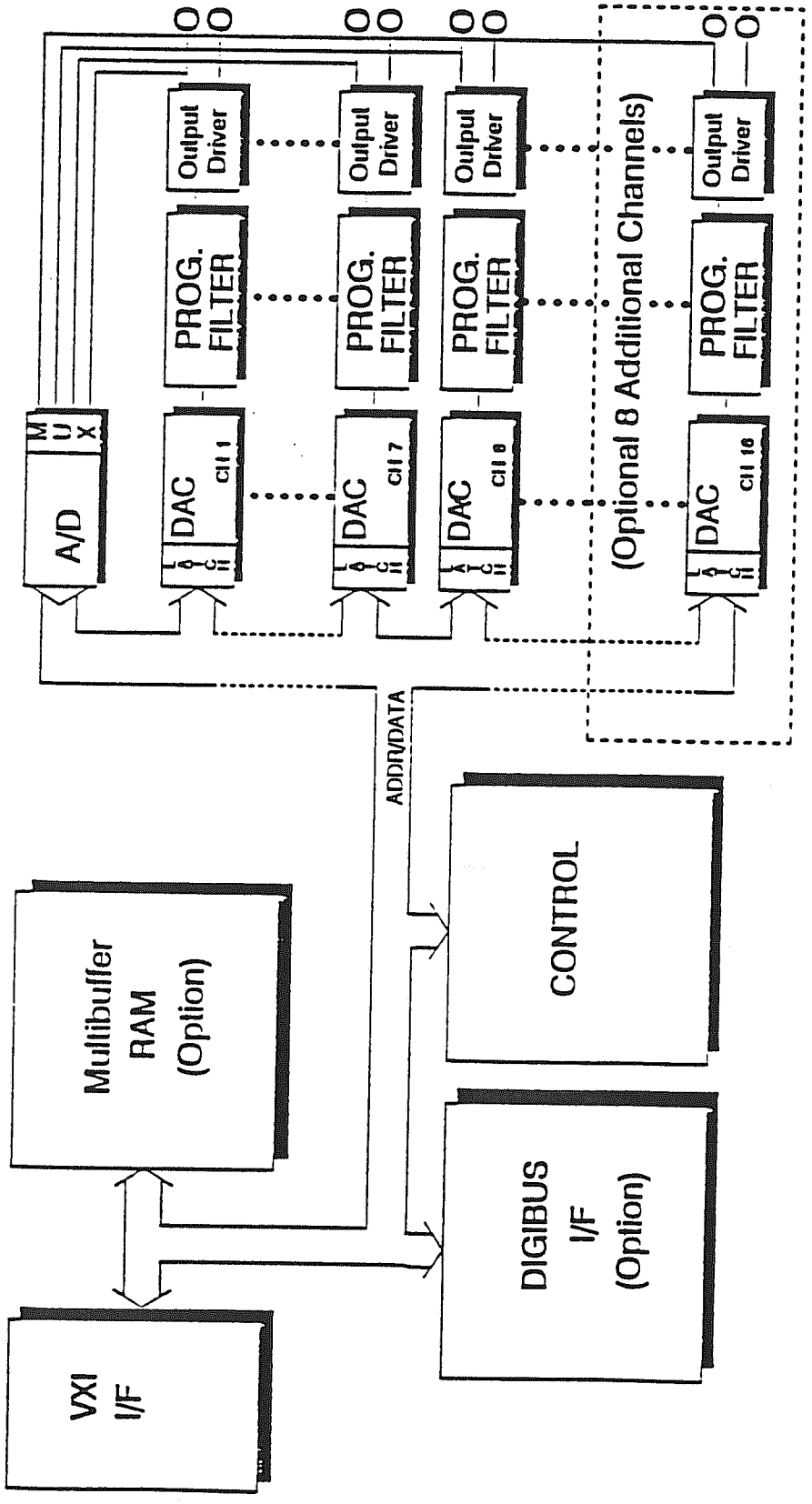

Figure 2 - V285 8/16 Channel, 16-Bit, 500 kHz DAC/Waveform Generator

PROGRAMMING INFORMATION

Address Map

A16 Space -- VXI Configuration Registers

$ 0x00 - ID Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	1	1	1	1	1	0	0	1	0	1	0	0	1

[15:14] (R) Class = Extended
[13:12] (R) Mode = A16/A32
[11:0] (R) ID = F29

$ 0x00 - ID Register (W)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
x	x	x	x	x	x	x	x	LAR7	LAR6	LAR5	LAR4	LAR3	LAR2	LAR1	LAR0

LAR[7:0] (W) Logical Address Register

$ 0x02 - Device Type Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	1

[15:12] (R) Memory = 8 MBytes
[11:0] (R) Model = 285

$ 0x04 - Status Control Register (Mixed)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A32	Modid	1	1	1	1	1	1	1	1	1	1	Ready	Passd	Inhbt	Reset

A32 (RW) A32 Enable
Modid (R) Active low Modid line to V285
Ready (R) V285 is ready for VXI access
Passd (R) V285 passed all of the self tests
Inhbt (RW) Inhibits assertion of *Sysfail on VXI bus
Reset (RW) Soft reset, run self test after Reset is deserted

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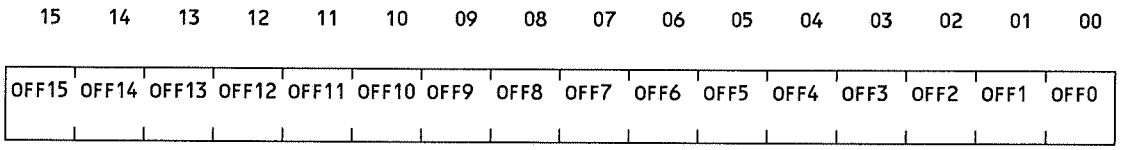
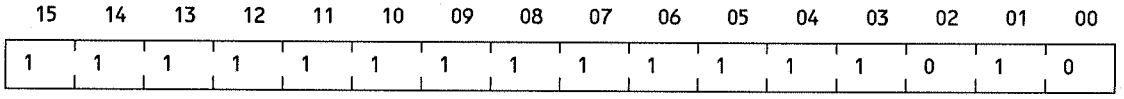
$ 0x06 - Offset Register (RW)



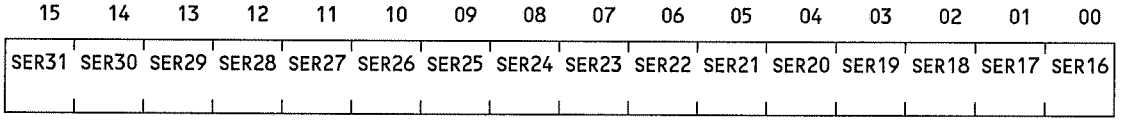
OFF[15:0] (RW) Offset Register which points to base address of module in A32 space

$ 0x08 - Attribute Register (R)

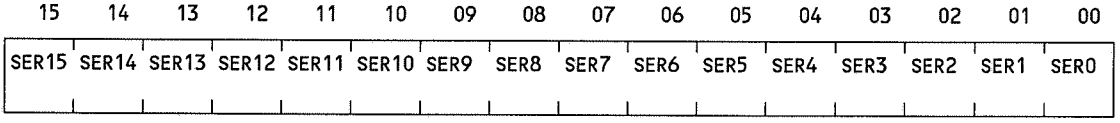


[2] (R) Interrupt Control Capability
[1] (R) No Interrupt Handler Capability
[0] (R) Interrupt Status Capability

$ 0x0A - Serial Number High (R)

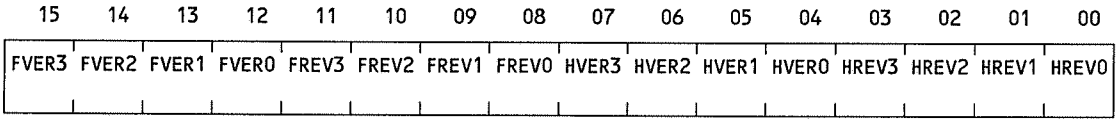


$ 0x0C - Serial Number Low (R)



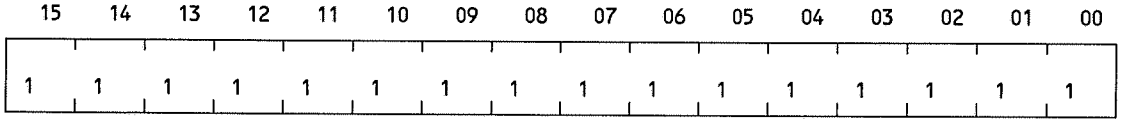
SER[31:0] (R) KSC's unique serial number for every module

$ 0x0E - Version Number Register (R)

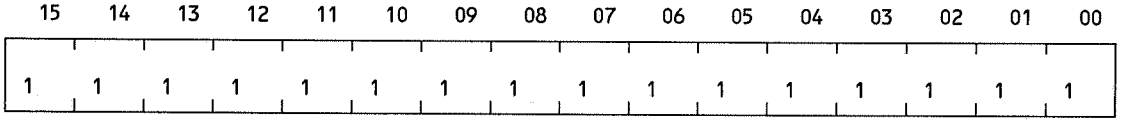


FVER[3:0] (R) Firmware Main Version #
FREV[3:0] (R) Firmware Revision #
HVER[3:0] (R) Hardware Main Version #
HREV[3:0] (R) Hardware Revision #

$ 0x10 to 0x18 - Reserved (R)

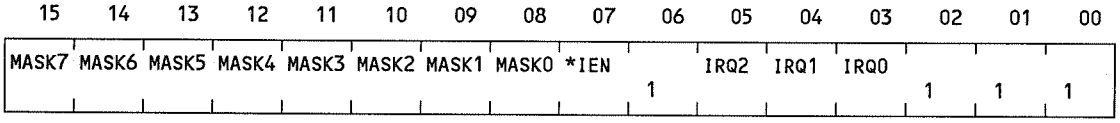


$ 0x1A - Interrupt Status Register (R)



[15:8] (R) Status ID = FF
[7:0] (R) Reserved

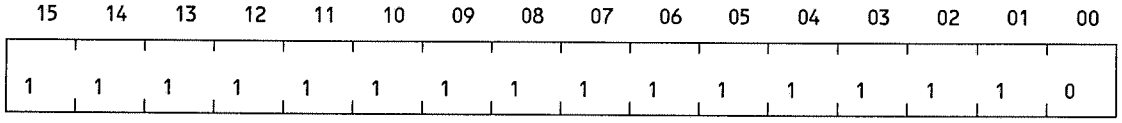
$ 0x1C - Interrupt Control Register (RW)



MASK7 (RW) Interrupt Mask Bit for Interrupt Source #7
MASK6 (RW) Interrupt Mask Bit for Interrupt Source #6
MASK5 (RW) Interrupt Mask Bit for Interrupt Source #5
MASK4 (RW) Interrupt Mask Bit for Interrupt Source #4
MASK3 (RW) Interrupt Mask Bit for Interrupt Source #3
MASK2 (RW) Interrupt Mask Bit for Interrupt Source #2
MASK1 (RW) Interrupt Mask Bit for Interrupt Source #1
MASK0 (RW) Interrupt Mask Bit for Interrupt Source #0
*IEN (RW) Interrupt Enable
IRQ[2:0] (RW) Interrupt Request Level

000 IRQ7
001 IRQ6
010 IRQ5
011 IRQ4
100 IRQ3
101 IRQ2
110 IRQ1
111 Disconnected

$ 0x1E - Subclass Register (R)



[15] (R) VXI Extended Device
[14:0] (R) 7FFE = Extended Register Based Device

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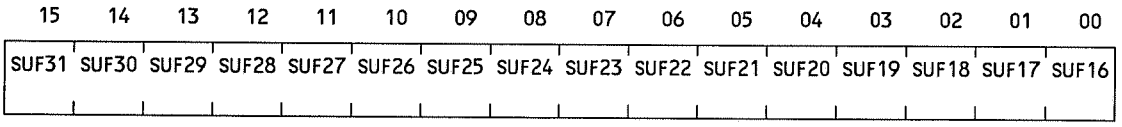
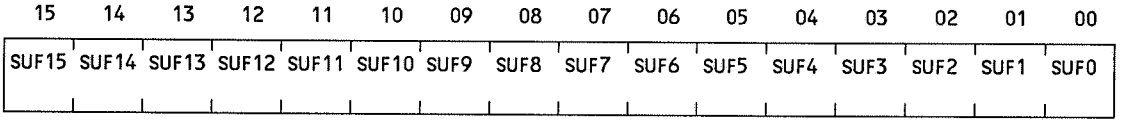
$ 0x20 - Suffix High Register (R)

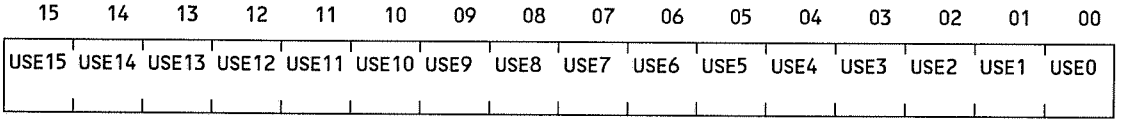


$ 0x22 - Suffix Low Register (R)



SUF[31:0] (R) 4 Character string representing the model's suffix.

$ 0x24 to 0x3F - User Defined Register (RW)



USE[15:0] (RW) User defined register stored on EEPROM (non-volatile RAM).

A32 Space -- V285 Operational Registers

NOTE: Setting a bit in the following registers corresponds to programming a "1" and resetting a bit corresponds to programming a "0".

$ 0x00 - Sample Clock Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
	CAL START	OUTPUT ENBL	FILT SEL	CON3	CON2	CON1	CON0		CLK ENBL	SRC1	SRC0	FREQ3	FREQ2	FREQ1	FREQ0
(0)	(0)	(0)	(0)	(?)	(?)	(?)	(?)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

( ) Power up value

CAL START (W) When set, a calibration cycle will be initiated.

OUTPUT ENBL (RW) When set, all DAC outputs will be enabled.

FILT SEL (RW) Filter Selection

0 - 100kHz Bandedge
1 - 10kHz Bandedge

CON [3:0] (R) Connector Status Lines

1111 - No termination housing installed.
1110 - V285 Termination housing installed.

CLK ENBL (RW) When set, the sample clock is enabled.

SRC[1:0] (RW) Sample Clock Source Selection
00 - Internal Clock Source
01 - Clock Source from Trigger Lines
10 - External Clock Source (Front Panel)
11 - Digi-Bus Frame Clock

FREQ[3:0] (RW) Sample Clock Frequency Selection (Internal Clock Source)

0000 - 500kHz
0001 - 200kHz
0010 - 100kHz
0011 - 50kHz
0100 - 20kHz
0101 - 10kHz
0110 - 5kHz
0111 - 2kHz
1000 - 1kHz
1001 - 500Hz
1010 - 200Hz
1011 - 100Hz

The Sample Clock may be generated from any of the four sources listed -- Internal Clock Source, TTL Trigger Lines, an External Clock supplied through the Front Panel SMB connector, or the Digi-bus Frame Clock. If the internal sample clock is selected as the clock source the lower four bits in this register will determine the clock frequency. If the trigger line source is selected, the contents of Trigger Line Register 1 will determine which trigger line will be used. The Front Panel Clock Input is TTL Compatible. The enable bit is used to enable/disable whichever source is selected.

$ 0x02 - Trigger Line Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TIENB (0)	TI2 (0)	TI1 (0)	TI0 (0)	TOENB (0)	TO2 (0)	TO1 (0)	TO0 (0)	CIENB (0)	CI2 (0)	CI1 (0)	CI0 (0)	COENB (0)	CO2 (0)	CO1 (0)	CO0 (0)

( ) Power up value

TIENB (RW) When set, enables an "Event Trigger In" from the VXI bus TTL Trigger Lines.

TI[2:0] (RW) TTL Trigger Line Selection for the "Event Trigger In".

000 TTL Trigger Line 0
001 TTL Trigger Line 1
010 TTL Trigger Line 2
011 TTL Trigger Line 3
100 TTL Trigger Line 4
101 TTL Trigger Line 5
110 TTL Trigger Line 6
111 TTL Trigger Line 7

TOENB (RW) When set, enables an "Event Trigger Out" onto the VXI bus TTL Trigger Lines.

TO[2:0] (RW) TTL Trigger Line Selection for the "Event Trigger Out".

000 TTL Trigger Line 0
001 TTL Trigger Line 1
010 TTL Trigger Line 2
011 TTL Trigger Line 3
100 TTL Trigger Line 4
101 TTL Trigger Line 5
110 TTL Trigger Line 6
111 TTL Trigger Line 7

CIENB (RW) When set, enables a "Sample Clock In" from the VXI bus TTL Trigger Lines.

CI[2:0] (RW) TTL Trigger Line Selection for the "Sample Clock In".

000 TTL Trigger Line 0
001 TTL Trigger Line 1
010 TTL Trigger Line 2
011 TTL Trigger Line 3
100 TTL Trigger Line 4
101 TTL Trigger Line 5
110 TTL Trigger Line 6
111 TTL Trigger Line 7

COENB (RW) When set, enables the Sample Clock to be output on the VXI bus TTL Trigger Lines.

CO[2:0] (RW) TTL Trigger Line Selection for the "Sample Clock Out".

000 TTL Trigger Line 0
001 TTL Trigger Line 1
010 TTL Trigger Line 2
011 TTL Trigger Line 3
100 TTL Trigger Line 4
101 TTL Trigger Line 5
110 TTL Trigger Line 6
111 TTL Trigger Line 7

This register allows configuration of the VXI bus TTL trigger lines. "Sample clock out" routes the Sample Clock source (specified in the Sample Clock Register) to the appropriate TTL trigger line. This mode is very useful when configuring a synchronous system requiring one clock source. A single master clock source can be selected and routed over the TTL Trigger Lines to the other system elements requiring this master clock. "Sample Clock In" allows a TTL trigger line to be used for the sample clock, if selected in the Sample Clock Register.

"Event Trigger Out" allows an event from this module (such as front panel trigger) to be output onto the selected TTL trigger line. This mode can be used when it is desirable to trigger several VXI modules with an event occurring on a single module. "Event Trigger In" allows an event occurring on a TTL trigger line to generate an interrupt trigger on this module.

$ 0x04 - Data Source Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CH16 (1)	CH15 (1)	CH14 (1)	CH13 (1)	CH12 (1)	CH11 (1)	CH10 (1)	CH9 (1)	CH8 (1)	CH7 (1)	CH6 (1)	CH5 (1)	CH4 (1)	CH3 (1)	CH2 (1)	CH1 (1)

( ) Power up value

CH[16:1] (RW) Channel Data Source Selection

0 - Digi-Bus or MBUF Data Source
(Depends on which option is installed)
1 - VXIbus Data Source

$ 0x06 - $ 0x0E NOT USED

$ 0x10 - CH 1_VXI_DATA (RW)
$ 0x12 - CH 2_VXI.DATA (RW)
$ 0x14 - CH 3_VXI.DATA (RW)
$ 0x16 - CH 4_VXI.DATA (RW)
$ 0x18 - CH 5_VXI_DATA (RW)
$ 0x1A - CH 6_VXI.DATA (RW)
$ 0x1C - CH 7_VXI.DATA (RW)
$ 0x1E - CH 8_VXI.DATA (RW)
$ 0x20 - CH 9_VXI_DATA (RW)
$ 0x22 - CH 10_VXI.DATA (RW)
$ 0x24 - CH 11_VXI.DATA (RW)
$ 0x26 - CH 12_VXI.DATA (RW)
$ 0x28 - CH 13_VXI_DATA (RW)
$ 0x2A - CH 14_VXI.DATA (RW)
$ 0x2C - CH 15_VXI.DATA (RW)
$ 0x2E - CH 16_VXI.DATA (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
D15 (?)	D14 (?)	D13 (?)	D12 (?)	D11 (?)	D10 (?)	D9 (?)	D8 (?)	D7 (?)	D6 (?)	D5 (?)	D4 (?)	D3 (?)	D2 (?)	D1 (?)	D0 (?)

( ) Power up value

D[15:0] (RW) If the channel selection bit for the associated channel is set for the VXI bus Data Source, this register specifies the data word to be presented to the DAC on the next asserted edge of the sample clock. This value is to be loaded from the VXI bus.

$ 0x30 - CH 1_DIGI_DATA (R)
$ 0x32 - CH 2_DIGI_DATA (R)
$ 0x34 - CH 3_DIGI.DATA (R)
$ 0x36 - CH 4_DIGI.DATA (R)
$ 0x38 - CH 5_DIGI_DATA (R)
$ 0x3A - CH 6_DIGI.DATA (R)
$ 0x3C - CH 7_DIGI.DATA (R)
$ 0x3E - CH 8_DIGI.DATA (R)
$ 0x40 - CH 9_DIGI_DATA (R)
$ 0x42 - CH 10_DIGI_DATA (R)
$ 0x44 - CH 11_DIGI.DATA (R)
$ 0x46 - CH 12_DIGI.DATA (R)
$ 0x48 - CH 13_DIGI_DATA (R)
$ 0x4A - CH 14_DIGI.DATA (R)
$ 0x4C - CH 15_DIGI.DATA (R)
$ 0x4E - CH 16_DIGI.DATA (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

( ) Power up value

D[15:0] (R) If the channel selection bit for the associated channel is set for the Digi-bus or MBUF Data Source, this register specifies the data word to be presented to the DAC on the next asserted edge of the sample clock.

$ 0x50 - $ 0x7E NOT USED

$ 0x80 - 0x17E - Digi-Bus Select Bit (RW) (2048 Channels)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

( ) Power up value

These read/write registers contain 2048 bits which enable (1) or disable (0) the reception of the corresponding sample in a given frame.

$ 0x180 - Digi-Bus Frame Count (W)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ENA CAP	(1)	(1)	(1)	(1)	(1)	FC9 (0)	FC8 (0)	FC7 (0)	FC6 (0)	FC5 (0)	FC4 (0)	FC3 (0)	FC2 (0)	FC1 (0)	FC0 (0)

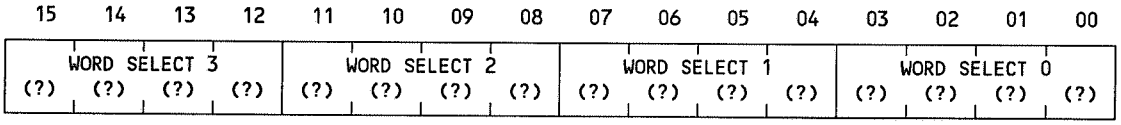
( ) Power up value

ENA CAP (W) Must be set to a "1" to allow acceptance of data from the Digi-bus.

FC[9:0] (W) Specifies the frame count interval. If data equals zero, the V285 stores data from every frame. If data equals one, the V285 stores data from every other frame, etc. This field should only be modified if the ENA CAP bit is RESET.

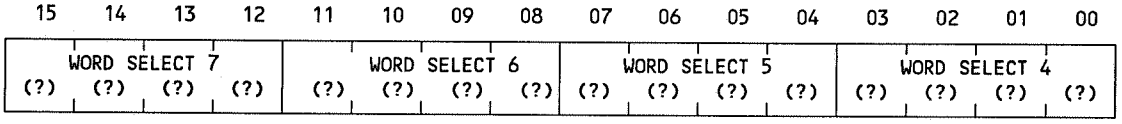
NOTE: The ENA CAP bit should only be RESET after the Digi-Bus source has been disabled (i.e., Digi-Bus transfers have been terminated).

$ 0x182 - Digi-Bus Word Dest 1 (RW) (Digi-Bus Option)



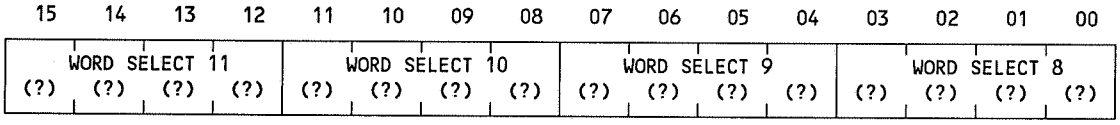
( ) Power up value

$ 0x184 - Digi-Bus Word Dest 2 (RW) (Digi-Bus Option)



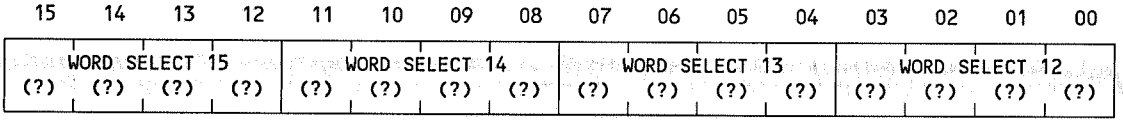
( ) Power up value

$ 0x186 - Digi-Bus Word Dest 3 (RW) (Digi-Bus Option)



( ) Power up value

$ 0x188 - Digi-Bus Word Dest 4 (RW) (Digi-Bus Option)

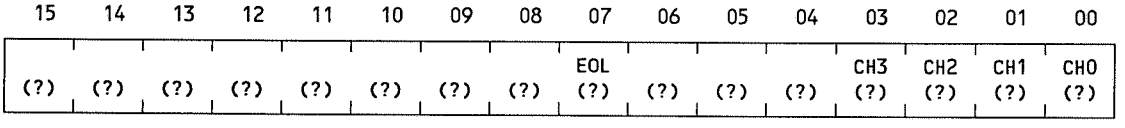


( ) Power up value

Registers 0x182-0x188 each contain the space for four 4-bit channel numbers. Word select 0 corresponds to the first word received from the Digi-bus by the V285. Word Select 1 corresponds to the second word and so on. The channel number specified in the word selection field is the DAC channel (1-16), to be updated with the associated Digi-bus data word. For example, if DAC CH 2 is to be updated with the fourth Digi-bus word received by the V285, then the user would program bits [15:12] of 0x182 with the value of "0001".

Note: Physical DAC channels (1-16) should be mapped as channels 0-15 when programming the Digi-Bus word Destination registers or the MBUF Scan List.

$ 0x200 - 0x21E - MBUF Scan List (RW) (MBUF Option)



( ) Power up value

EOL (RW) End of List. Set for the last active multi buffer channel.

CH[3:0] (RW) These bits indicate the list of active channels using the multi buffer as their data source.

EX. To configure the V285 to use the Multi Buffer as the data source for Channels 1,2, and 3, program the following:

Address:	0x200	Data:	0x0000
Address:	0x202	Data:	0x0001
Address:	0x204	Data:	0x0082

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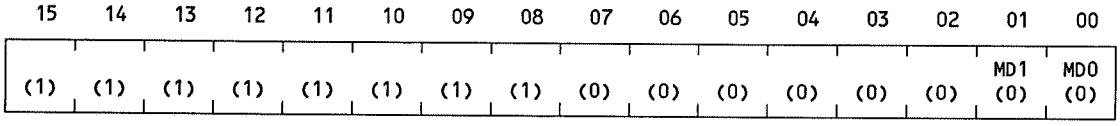
$ 0x220 - MBUF_Mode (RW) (MBUF Option)



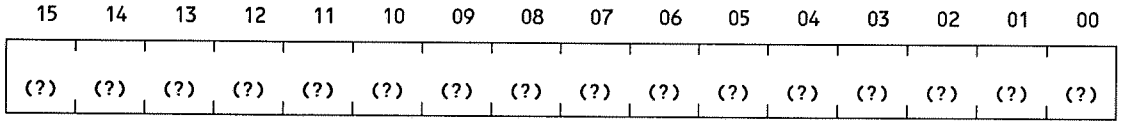
( ) Power up value

MD[1:0] (RW) Multi Buffer Mode

00 - Setup Mode
01 - Recirculation/Multi-Buffer Mode
10 - One-shot Mode
11 - Invalid

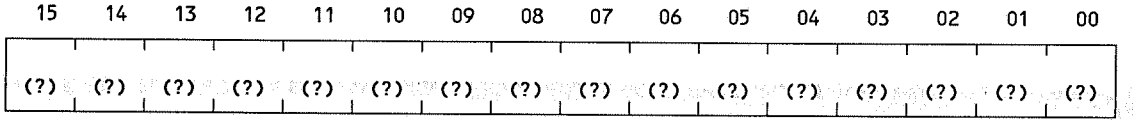
The Multi Buffer mode register must be programmed to "Setup Mode" while configuring all MBUF option registers except the Buffer Empty Flag Register at 0x22A.

$ 0x222 - Total_MBUF_Size_H (RW) (MBUF Option)



( ) Power up value

$ 0x224 - Total_MBUF_Size_L (RW) (MBUF Option)



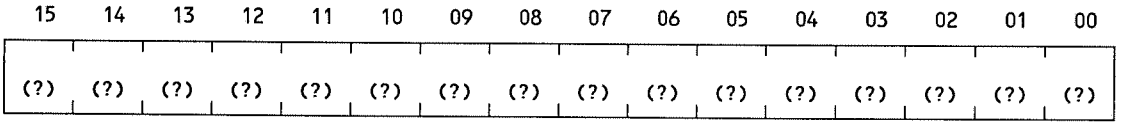
( ) Power up value

The Total Buffer Size Registers (High word and Low word) are to be programmed with a 32-bit value representing the total amount of Multi-Buffer memory required for the application. The following equation can be used in determining the appropriate value to be written:

[(Individual Buffer Size) X (# of Desired Buffers)] - 1

Note: The Individual Buffer Size noted above is the 32 bit value written to the individual Buffer Size Registers (High word and Low word) (0x226, 0x228 -- A32 Space).

$ 0x226 - Indiv_MBUF_Size_H (RW) (MBUF Option)



( ) Power up value

$ 0x228 - Indiv_MBUF_Size_L (RW) (MBUF Option)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

( ) Power up value

The Individual Buffer Size Registers (High word and Low word) are to be programmed with a 32 bit value (16 bits in each register) representing the number of 32 bit words (i.e., 2 Data Samples) desired in each buffer of the Multi-Buffer memory.

$ 0x22A - Buffer Empty Flag (RW) (MBUF) Option

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
											UNDRN	FLAG4	FLAG3	FLAG2	FLAG1
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

( ) Power up value

This register contains status bits which indicate when the associated buffer is empty. These flag bits must be cleared by writing an "1" when updating the associated buffer with new data. Clearing the empty flag for the buffer indicates new data has been written to the register. Failure to do so will result in the underrun bit being set. The underrun bit indicates a buffer's contents have not been updated with new data before the buffer's read cycle begins.

$ 0x2000 - 0x21FE A32 EEPROM (RW)

$ 0x400000 - 0x4FFFFF MBUF RAM (1M byte Version) (RW)

$ 0x400000 - 0x7FFFFF MBUF RAM (4M byte Version) (RW)

The Multi-Buffer RAM is an array of memory intended to be used to contain predetermined waveforms. These waveforms can be transferred to the Multi-Buffer RAM in a couple of different ways to support the available operating modes (i.e., Recirculation, Multi-Buffer and One-Shot modes). In both the Recirculation and One-Shot modes, the data should be stored before the module is activated. Data output can be accomplished by enabling the Sample Clock in Recirculation mode or by supplying a Trigger in One-Shot mode. Multi-Buffer mode allows the user to transfer new data to the RAM in Real-Time, thus allowing continuous waveforms to be output on the V285.

The data in the Multi-Buffer RAM is multiplexed data dependent upon the number of active channels listed in the MBUF Scan List (0x200 - 0x21FE - A32 Space).

For Example:

Assume 3 Active Channels (CH1-3) are specified in the MBUF Scan List. The data for each channel will appear in the Multi-Buffer RAM as shown below:

```
Channel 1  Sample 1        resides in 0x20400000
Channel 2  Sample 1        resides in 0x20400002
Channel 3  Sample 1        resides in 0x20400004
Channel 1  Sample 2        resides in 0x20400006
Channel 2  Sample 2        resides in 0x20400008
   .
   .
   .
```

50-Contact High Density
(SCSI II Type) Receptacle

50-Contact High Density
(SCSI II Type) Receptacle

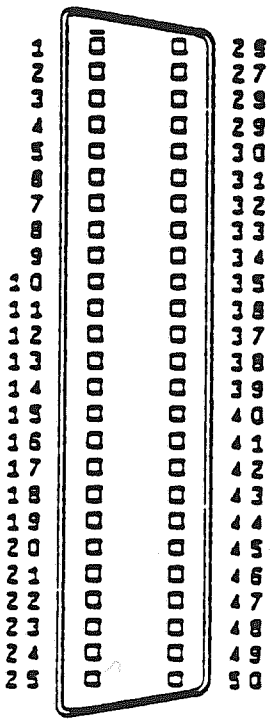


FIGURE 3 - 50 Pin SCSI II Connectors, J3 and J4 (Mating Connector)

FIGURE 4 - 50 Pin SCSI II Connectors, J3 and J4 Pin Connection

J3 Pin #	J3 Description	J4 Pin #	J4 Description
1		1	Channel 1 Out +
26		26	Channel 1 Out –
2		2	Channel 2 Out +
27		27	Channel 2 Out -
3		3	Channel 3 Out +
28		28	Channel 3 OUT –
4		4	Channel 4 Out +
29		29	Channel 4 Out –
5		5	Channel 5 Out +
30		30	Channel 5 Out -
6		6	Channel 6 Out +
31		31	Channel 6 Out –
7		7	Channel 7 Out +
32		32	Channel 7 Out –
8		8	Channel 8 Out +
33		33	Channel 8 Out -
9		9	Channel 9 Out +
34		34	Channel 9 Out -
10		10	Channel 10 Out +
35		35	Channel 10 Out –
11		11	Channel 11 Out +
36		36	Channel 11 Out -
12		12	Channel 12 Out +
37		37	Channel 12 Out –
13		13	Channel 13 Out +
38		38	Channel 13 Out –
14		14	Channel 14 Out +
39		39	Channel 14 Out -

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J3 Pin #	J3 Description	J4 Pin #	J4 Description
15		15	Channel 15 Out +
40		40	Channel 15 Out –
16		16	Channel 16 Out +
41		41	Channel 16 Out –
17		17	
42		42	
18		18	
43		43	
19		19	
44		44	
20		20	
45		45	
21		21	
46		46	
22		22	Sample Clock Out
47		47	Dgnd
23		23	Trigger In
48		48	Dgnd
24		24	Sample Clock In
49		49	Dgnd
25	Constat 0	25	Constat 2
50	Constat 1	50	Dgnd

J3 and J4 Front Panel Connector is AMP 2-174341-5 50 Pins SCSI II type connector

V285 TERMINATION HOUSING ASSEMBLY

Description

The 16 Channel VXI Termination Housing contains 32 screw terminal blocks for connecting outputs to users equipment. This termination housing is intended to be used with the V285. See the signal conditioning specifications located separately in this manual for technical specifications.

APPENDIX A

VIEWING SELF TEST RESULTS

The V285 will perform a self test upon power-up or after the assertion and negation of the reset bit. The on board CPU will perform tests on each of the channels.

First each channel is tested at 85% of the positive full scale. After each channel is written it is compared via an internal ADC and compared to be within the limits of 0xE1EC and 0xF7AC. If the selected channel is between these limits the converted value is written to EEProm and the next channel is selected and the process is continued until the all 16 channels are tested.

Next , each channel is tested at 85% of the negative full scale. After each channel is written it is compared via an internal ADC and compared to be within the limits of 0x0854 and 0x1E14. If the selected channel is between these limits the converted value is written to EEProm and the next channel is selected and the process is continued until the all 16 channels are tested.

The memory addresses used for this test are as follows.

Channel # Address	Ch. Data	+ 85% FS Address	* Value A Data	-85% FS Address	* Value B Data
0x2050	0x 0	0x2052	see below	0x2054	see below
0x2056	0x 1	0x2058	. .	0x205A	. .
0x205C	0x 2	0x205E	. .	0x2060	. .
0x2062	0x 3	0x2064	. .	0x2066	. .
0x2068	0x 4	0x206A	. .	0x206C	. .
0x206E	0x 5	0x2070	. .	0x2072	. .
0x2074	0x 6	0x2076	. .	0x2078	. .
0x207A	0x 7	0x207C	. .	0x207E	. .
0x2080	0x 8	0x2082	. .	0x2084	. .
0x2086	0x 9	0x2088	. .	0x208A	. .
0x208C	0x A	0x208E	. .	0x2090	. .
0x2092	0x B	0x2094	. .	0x2096	. .
0x2098	0x C	0x209A	. .	0x209C	. .
0x209E	0x D	0x20A0	. .	0x20A2	. .
0x20A4	0x E	0x20A6	. .	0x20A8	. .
0x20AA	0x F	0x20AC	. .	0x20AE	. .

*Value A is between 0xE1Ec & 0xF7AC
*Value B is between 0x0854 & 0x1E14

APPENDIX B

USING CALIBRATION WITH THE V285

The V285 is capable of performing an internal calibration of each Digital-to-Analog Converter (DAC) channel. The results of this calibration are stored in the on-board EEPROM, and may be retrieved via VXI-bus accesses to correct the count being applied to a channel.

The nominal transfer function of a channel is given below:-

10.24 volts = 0xFFFF

0.00 volts = 0x7FFF

-10.24 volts = 0x0000

Prior to performing a channel calibration the ADC must perform a self-calibration (after the warm-up period). This self-calibration is initiated by performing a software reset (toggle the reset bit high, then low by writing to offset 0x04 in A16 Space).

To initiate a channel calibration cycle, toggle bit 14 (high then low) in the Sample Clock Register (offset 0x00 in A32 Space).

This operation will take approximately 10 seconds for eight channels. During this time, VXI accesses are not allowed.

Channel calibration is performed by sequencing through a series of DAC counts (plus and minus 85% of full scale and zero) for each channel while monitoring the output voltage with the on-board 16 bit Delta-Sigma Analog to Digital Converter. Gain and offset corrections are then calculated and stored in EEPROM.

The EEPROM space begins at VXI address 0x2000 (A32 Address Space). Beginning at offset 0x2010, each channel occupies two locations, as shown below. The first location contains a 16 bit unsigned integer value containing the results of the gain calibration, while the second location contains the 16 bit count corresponding to the zero reading.

OFFSET CONTENTS

0x2010 ch 1 Mcorr
0x2012 ch 1 Bcorr
0x2014 ch 2 Mcorr
0x2016 ch 2 Bcorr
.
.
.
.
0x204A ch 16 Bcorr

Mcorr is the difference in count measured by the on-board ADC for the + and - 85% points. The nominal value is 57042.

Bcorr is the ADC count corresponding to a mid-scale value and is nominally 32767.

To correct the DAC value being written to the module (NominalCount), use the following equations to calculate the corrected count (CorrectedCount):-

Merror = (57042.0 - Mcorr) / 57042.0 + 1.0;

Berror = Bcorr - 32767.0;

CorrectedCount = (32767.0 + ((NominalCount - 32767.0) *

WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

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1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com