Model V305

24-channel Isolated Digital Input

INSTRUCTION MANUAL

March, 1998

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FIGURES

TABLES

Warranty
NPD:rem(WP)

24-channel Isolated Digital Input

Provides ground-isolated digital monitoring of voltage signals

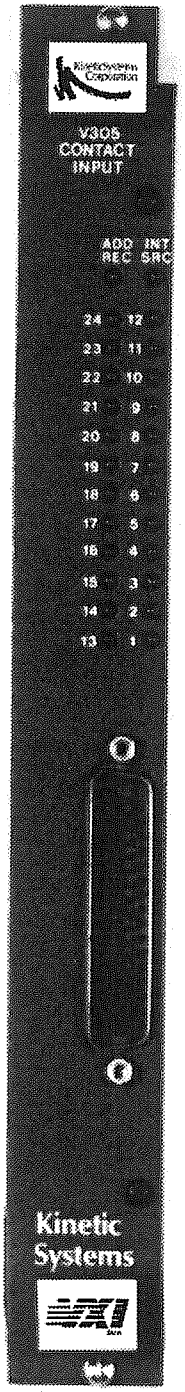
V305

Features

- **12, 24, and 48 V dc or 120 V ac input isolated and TTL non-isolated options**
- **24-channel voltage sense option**
- **Change-of-state indications**
- **Optical isolation**
- **100 ms input filter**

Typical Applications

- **Test cells**
- **Isolated monitoring of relay contacts, "on-off" voltage signals and switches**



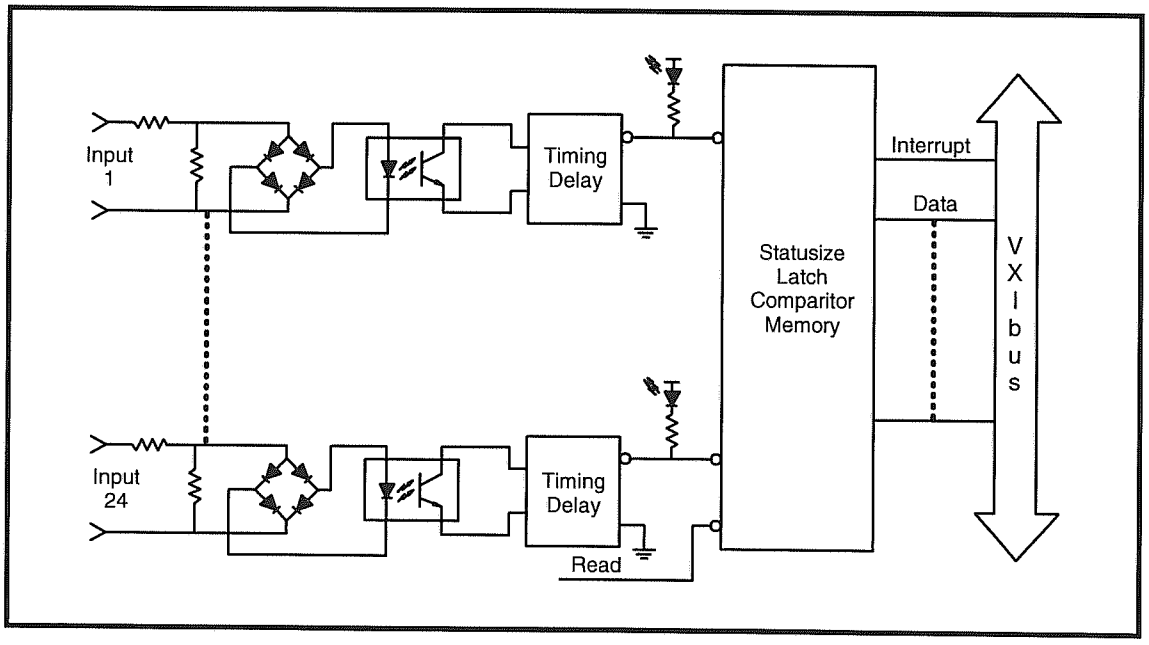
General Description *(Product specifications and descriptions subject to change without notice.)*

The V305 is a single-width, C-size, register-based, VXIbus module that provides 24 individually isolated, contact sense circuits and a global change-of-state indication. Each sense circuit detects the presence or absence of voltage at its terminals and is suitable for sensing such remote process contact closures as limit switches, machine tool relay contacts, pressure switches, manual switches, and mercury-wetted contacts. Five voltage options are available (TTL , 12 V dc, 24 V dc, 48 V dc, and 120 V ac) as well as a contact input option.

Input isolation is achieved by using LED/photo-transistor optical isolators. Each circuit (except the TTL version) is a floating, two-wire circuit with common-mode voltage isolation greater than 500 V. Each option has 24 circuits with identical input voltage ratings, and the switching threshold is approximately one half of the rated input voltage. Each input circuit draws more than 5 mA but less than 10 mA. The logic convention is such that a contact closure (input voltage present) is interpreted as a logical "1." Each input is conditioned by filtering after the optical isolator. The filter time constant is 100 ms. Other time constants are available by special order.

The V305 contains a 24-bit memory register and a 24-bit comparator. If one or more of the inputs has changed state (1-to-0 or 0-to-1) since the last time the memory register was updated, a common interrupt source is set. This can produce an Interrupt Request directing the computer to read the current state of the inputs.

The V305 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specifications
Inputs	
Number of inputs	24 two-wire, floating inputs (except TTL and contact-input options)
Input signal options	12 V dc, 24 V dc or 48 V dc; 120 V ac; TTL; or Contact input
Input switching threshold	30% to 70% of nominal voltage
Input isolation	500 V (isolated options)
Input current	greater than 5 mA, less than 10 mA at nominal voltage
Input Filtering	
Time constant	100 ms
Input Connector type	50P "D"
Mating Connector	KineticSystems Model 5934-Z1A
Power Requirements:	
+5 V	1.7 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to +50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to +40°C
Cooling requirements	10 CFM
Dimensions	340 mm X 233.35 mm X 30.48 mm (C-sized VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V305-EA11 24-channel Isolated Digital Input; 120 V ac
Model V305-EB11 24-channel Isolated Digital Input; 48 V dc
Model V305-EC11 24-channel Isolated Digital Input; 24 V dc
Model V305-ED11 24-channel Isolated Digital Input; 12 V dc
Model V305-EE11 24-channel Isolated Digital Input; Contact Input
Model V305-EF11 24-channel Isolated Digital Input; 5 V dc (TTL level)

Related Products

Model 5851-Bxyz Cable—50S "D" to Unterminated
Model 5851-Dxyz Cable—50S "D" to 50S "D"
Model 5851-Exyz Cable—50P "D" to 50S "D"
Model 5934-Z1A Connector—50S "D"

UNPACKING AND INSTALLATION

The Model V305 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment.

Logical Address Switches

The V305 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V305 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to FIGURE 1 below.)

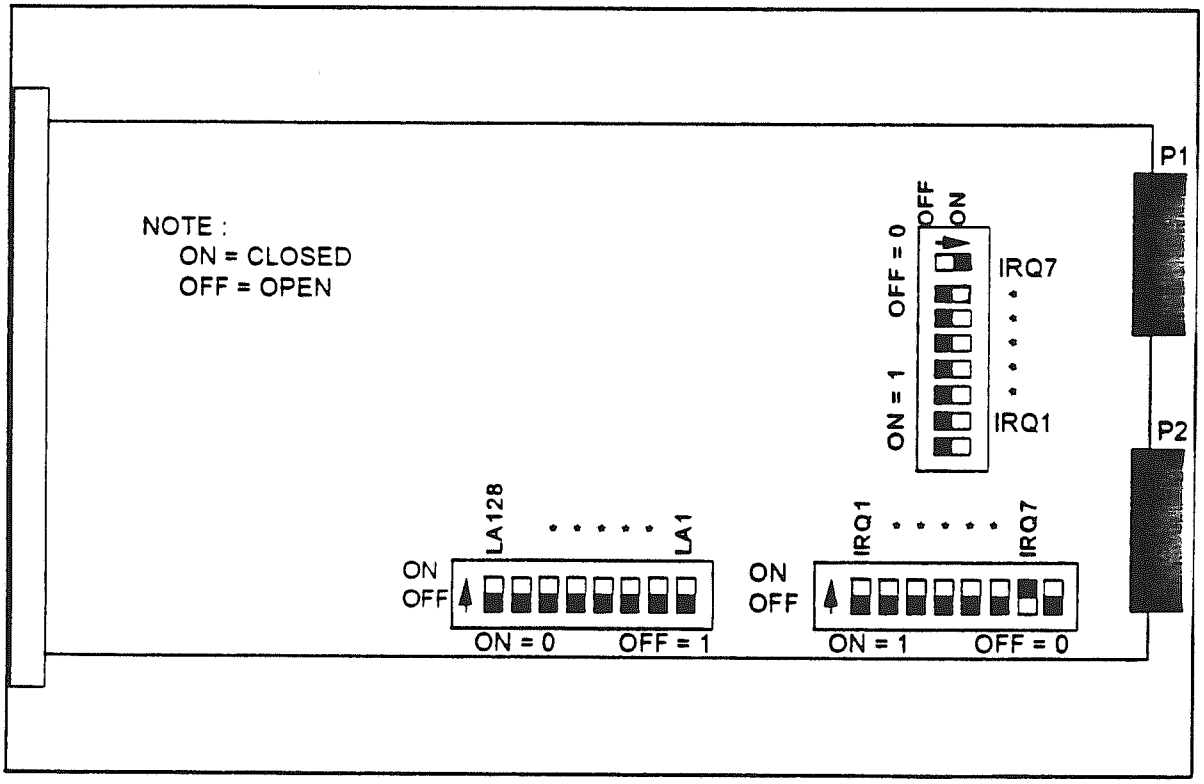


FIGURE 1 - V305 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value. The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).

Bits 13 through 6 are user-selectable via the address switches LA128-LA1.

Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Interrupt Switches

The V305 has two banks of eight-position switches to select one of seven Interrupt Request levels. Refer to FIGURE 1 (page 3) for the switch locations and switch settings. Both banks of eight-position switches must be set to the same position. As shown in FIGURE 1, IRQ 7 is set to the same position in both banks.

Module Insertion

The V305 is a C-sized, single width VXIbus module. It requires 1650 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame.

```
CAUTION:    TURN MAINFRAME POWER OFF WHEN
            INSERTING OR REMOVING MODULE
```

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WARNING:    REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN
            JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE
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To insure proper interrupt acknowledge cycles from the V305 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V350 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED turns on when the V305's Operational Registers are being accessed.

INT SRC — This LED turns on when scanning has stopped and DONE INT request is enabled.

1 - 24 — These 24 LEDs, when on, indicate that the corresponding input has a voltage present.

Connectors

P1 — The front panel P1 connector is used to connect the 24 inputs to be monitored for a change of state. (Refer to FIGURE 3, page 17.)

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V305 implements those required for register-based devices. The V305 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (page 6) are mapped into Address lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

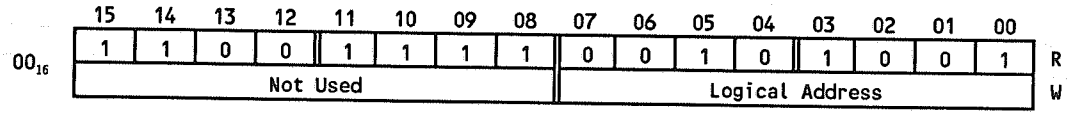
VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V305 are offset from the base address. **Note: the V305 only responds to these addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle.** Table 1 shows the applicable Configuration Registers present in the V305, their offset from the base (Logical) address, and their Read/Write capabilities.

TABLE 1 - Configuration Registers - Short I/O Address Space

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

ID/Logical Address Register

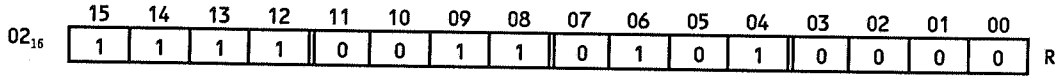


On READ transactions:

Bit(s)	Mnemonic	Description
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

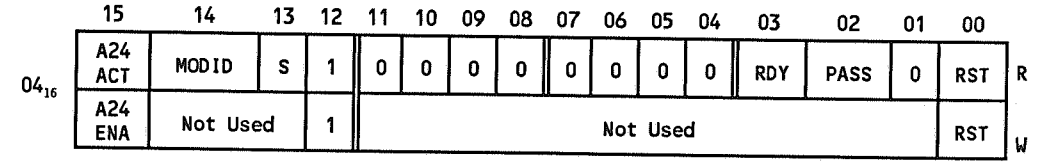
For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V305. In Dynamically configured systems (i.e., the Logical Address switches are set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register



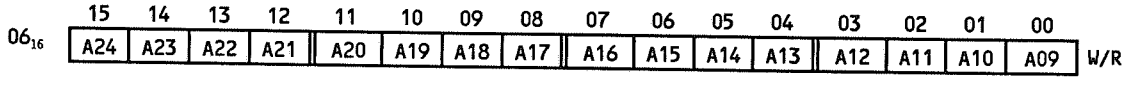
Bit(s)	Mnemonic	Description
15 - 12	Required Memory	The V305 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V305 (305_{16}).

Status/Control Register



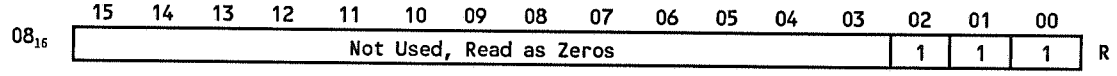
Bit(s)	Mnemonic	Description
15	A24 Enable	This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit <u>must</u> be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is <u>not</u> selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V305. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems' VXIbus modules. It should always be written with a "1."
11 - 04	Not Used	When read, will return all "0"s. These bits, when written to, are ignored.
03	Ready	Along with Bit 02 (Passed), this Read-Only bit will appear as a "1" to indicate its readiness to accept operational commands.
02	Passed	See the Ready bit description.
01	Not Used	Read as "0" and ignored on write transactions.
00	Reset	This Read/Write bit controls the Soft Reset condition within the V305. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) is inhibited. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register



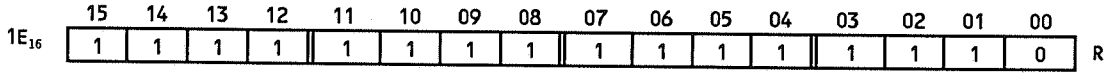
This Read/Write register defines the base address of the V305's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Interrupt Attribute Register



Bit(s)	Mnemonic	Meaning
15 - 03	Not Used	These bits are not used by the V305, and are read as zeros.
02	Intr Control	Indicates Interrupt Control capability.
01	Intr Handler	No Interrupt Handler capabilities.
00	Intr Status	Indicates Interrupt Status capability.

Subclass Register



Bit(s)	Mnemonic	Meaning
15	Extended Device	"1" indicates that this is a VXIbus defined Extended Device.
14-00	Register-Based	$7FFE_{16}$ indicates that this is an Extended register-based Device.

Operational Registers

The Operational Registers are the channels through which the input data patterns of the V305 are read. For compatibility with other KineticSystems' VXIbus modules in this series, these registers are positioned in VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set (see page 7).

Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register (see page 6). **Note: The V305 will only respond to**

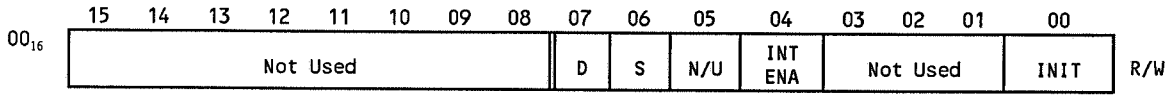
these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).

Of the 256 bytes requested by the setting of the Device Type register in the Configuration Register set, only ten bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 2 shows the applicable Operational Registers present in the V305, their offset from the base A24 address, and their Read/Write capabilities.

TABLE 2 - Operational Registers - Standard Address Space

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	Diagnostic Register
02_{16}	Read/Write	Interrupt Status/ID Register
12_{16}	Read	Input Register Low
14_{16}	Read	Input Register High
16_{16}	Read	Memory Register Low
18_{16}	Read	Memory Register High
$1A_{16}$	Read	Read Input Low / Update Memory / Clear COS Status
$1C_{16}$	Read	Read Input High (Read Register $1A_{16}$ first)
22_{16}	Read	Enable COS INT Request
26_{16}	Read	Disable COS INT Request
$2A_{16}$	Read	Clear COS Status
$2E_{16}$	Read	Test COS Status

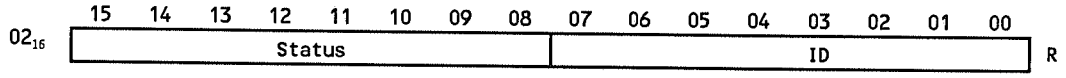
Diagnostic Register



Bit(s)	Mnemonic	Description
15 - 08	Not Used	On Read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module.

07	Diagnostic	When this bit is set to a one, the last register access to the Operational Register (offsets 12_{16} through $2E_{16}$) was valid.
06	Status	When this bit is set to a one, the last register access to the Operational Register (offsets 12_{16} through $2E_{16}$) was accepted.
05	Not Used	Read as "0".
04	INT ENA	Interrupt Enable: setting this bit to a one will enable interrupts.
03 - 01	Not Used	Read as "0".
00	Initialize	Setting this bit to a one will only reset the Operational Register (offsets 12_{16} through $2E_{16}$). The Configuration and Dagnostic registers are unaffected.

Interrupt Status/ID Register



This is a read-only 16-bit Interrupt Vector Register. During an interrupt acknowledge cycle, this register will output a Status/ID value during a D8, D16, or a D32 data transfer. In a D32 data transfer, the upper 16-bits will be pulled up to logic "1" by the backplane termination networks. A read from this register will show the current Status/ID value.

Bit(s)	Mnemonic	Description
15 - 08	STATUS	These eight bits will indicate Request True or Request False. Request True = FD_{16} Request False = FC_{16}
07 - 00	ID	These eight bits represent the Logical Address of the V305 Configuration Registers.

Read Input Register Low
Read Input Register High

To read all 24 bits of the input register, a read to the LOW register must be executed before a read from the HIGH register is executed. The Low register will read the input

state for bits one through 16, while the High register will indicate the state for bits 17 through 24. The Status bit in the Diagnostic Register should be a "1".

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
12_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
14_{16}	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

Read Memory Register Low
Read Memory Register High

To read all 24 bits of the memory register, a read to the LOW register must be executed first before a read from the HIGH register is executed. The Low register will read the memory state for bits one through 16, while the High register will indicate the state for bits 17 through 24. The Status bit in the Diagnostic Register should be a "1".

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
16_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
18_{16}	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

Read Input Low/Update Memory/Clear Change-Of-State Status
Read Input High

This register is used to read all 24 inputs, update the memory register and clear the Change-of-State status bit. To determine the input state before the recent change, a read from the memory register (16_{16} and 14_{16}) should be performed before registers $1A_{16}$ and $1C_{16}$ are read. To read all 24-bits from register $1A_{16}$ and $1C_{16}$, a read to the LOW register ($1A_{16}$) must be executed first before a read from the HIGH register ($1C_{16}$) can be executed. The Low register will read the input state for bits one through 16, while the High register will indicate the state for bits 17 through 24. The Status bit in the Diagnostic Register should be a "1".

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1A_{16}$	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
$1C_{16}$	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

Control Registers

The V305 has four Control Registers at offsets $1E_{16}$ through $2E_{16}$. These registers are read-only and return a one bit status code. This bit is the same as Bit 6 in the Diagnostic Register. This status code will indicate the command was accepted or a test condition is true when equal to "1". These four Control Registers are described below:

Enable Change-of-State INT Request (offset 22_{16})
Disable Change-of-State INT Request (offset 26_{16})

A read from either register will enable or disable Change-of-State INT Request. The Change-of-State INT Request must be enabled if the V305 is going to generate an interrupt. Both registers will return a data value of "1".

Clear Change-of-State Status (offset $2A_{16}$)

A read from this register will clear the Change-of-State status bit. A data value of "1" will be returned to indicate the command was accepted.

Test Change-of-State Status (offset $2E_{16}$)

A read from this register will test whether the SCAN DONE status is set or not. If read data bit 1 equals "1", then COS Status is set.

Unbalanced Contact Monitor

The V305-EA11 through V305-ED11 modules provide isolated inputs (as shown in the block diagram on page 1). This requires an external voltage source (generally in series with an external contact) for the input circuits. This has the advantage of providing ground isolation between the external inputs and the module.

The V305-EE11 is arranged for monitoring unbalanced contacts (one side of each contact is connected to ground at the module). One side of each contact input is connected to +24 volts within the module. This has the advantage of not requiring an external voltage source for the inputs. The "common" sides of the contacts are connected to the even-numbered contacts on the connector. Connections are shown on the connector chart on page 18, except that all return inputs are connected to ground within the module.

This version of the module introduces a current drain of 190 milliamperes from the +24 volts when all inputs are ON.

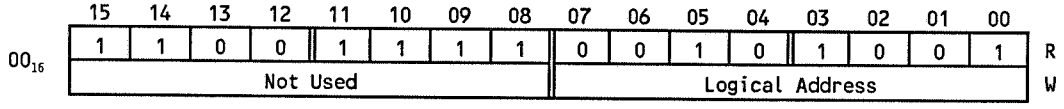
V305 REGISTER LAYOUTS

Configuration Registers - Short I/O Address Space

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

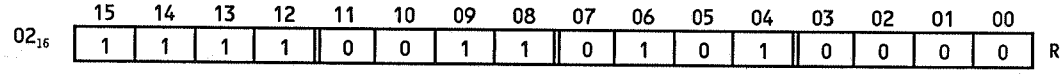
Configuration Register Formats

ID/LOGICAL ADDRESS REGISTER



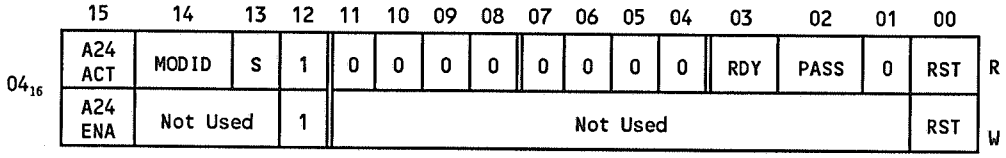
00_{16}

DEVICE TYPE REGISTER



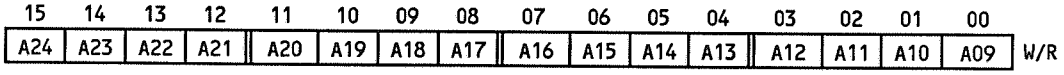
02_{16}

STATUS/CONTROL REGISTER



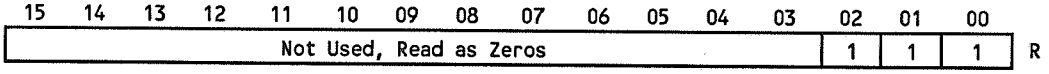
04_{16}

OFFSET REGISTER



06_{16}

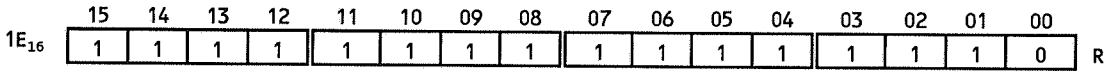
INTERRUPT ATTRIBUTE REGISTER



08_{16}

Model V305

SUBCLASS REGISTER

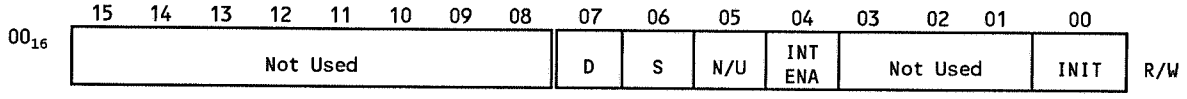


Operational Registers - Standard Address Space

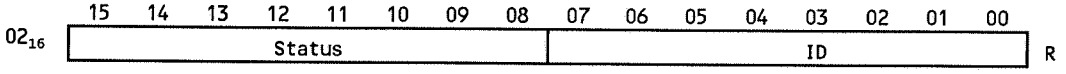
A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	Diagnostic Register
02_{16}	Read/Write	Interrupt Status/ID Register
12_{16}	Read	Input Register Low
14_{16}	Read	Input Register High
16_{16}	Read	Memory Register Low
18_{16}	Read	Memory Register High
$1A_{16}$	Read	Read Input Low / Update Memory / Clear COS Status
$1C_{16}$	Read	Read Input High (Read Register $1A_{16}$ first)
22_{16}	Read	Enable COS INT Status
26_{16}	Read	Disable COS INT Status
$2A_{16}$	Read	Clear COS Status
$2E_{16}$	Read	Test COS Status

Operational Register Formats

DIAGNOSTIC REGISTER



INTERRUPT STATUS/ID REGISTER



READ INPUT REGISTER LOW
READ INPUT REGISTER HIGH

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
12_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
14_{16}	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

READ MEMORY REGISTER LOW
READ MEMORY REGISTER HIGH

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
16_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
18_{16}	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

READ INPUT LOW/UPDATE MEMORY/CLEAR COS STATUS
READ INPUT HIGH

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1A_{16}$	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R
$1C_{16}$	Not Used								R24	R23	R22	R21	R20	R19	R18	R17	R

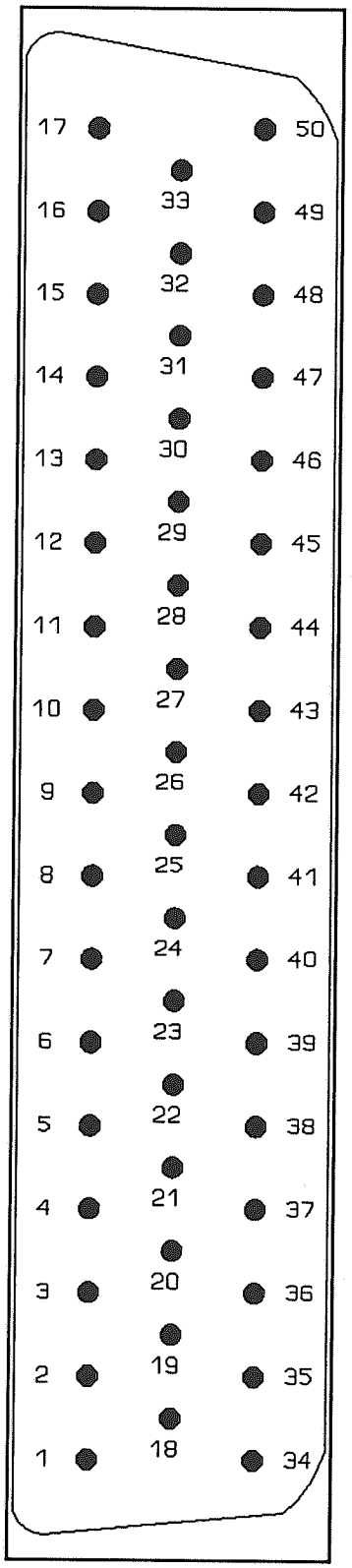


FIGURE 2 - V305 Connector Pinout

FIGURE 3 - V305 Connector Pinout Assignments

17	Channel 9 Signal	33	Channel 17 Signal	50	Unused
16	Channel 8 Return	32	Channel 16 Return	49	Unused
15	Channel 8 Signal	31	Channel 16 Signal	48	Channel 24 Return
14	Channel 7 Return	30	Channel 15 Return	47	Channel 24 Signal
13	Channel 7 Signal	29	Channel 15 Signal	46	Channel 23 Return
12	Channel 6 Return	28	Channel 14 Return	45	Channel 23 Signal
11	Channel 6 Signal	27	Channel 14 Signal	44	Channel 22 Return
10	Channel 5 Return	26	Channel 13 Return	43	Channel 22 Signal
9	Channel 5 Signal	25	Channel 13 Signal	42	Channel 21 Return
8	Channel 4 Return	24	Channel 12 Return	41	Channel 21 Signal
7	Channel 4 Signal	23	Channel 12 Signal	40	Channel 20 Return
6	Channel 3 Return	22	Channel 11 Return	39	Channel 20 Signal
5	Channel 3 Signal	21	Channel 11 Signal	38	Channel 19 Return
4	Channel 2 Return	20	Channel 10 Return	37	Channel 19 Signal
3	Channel 2 Signal	19	Channel 10 Signal	36	Channel 18 Return
2	Channel 1 Return	18	Channel 9 Return	35	Channel 18 Signal
1	Channel 1 Signal			34	Channel 17 Return

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2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com