Model V345-EA/EB/EC11

24-channel Isolated Output Register

INSTRUCTION MANUAL

March, 1998

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FIGURES

TABLES

24-channel Isolated Digital Output

Reed-relay, optical-isolator and ac-switch options are available

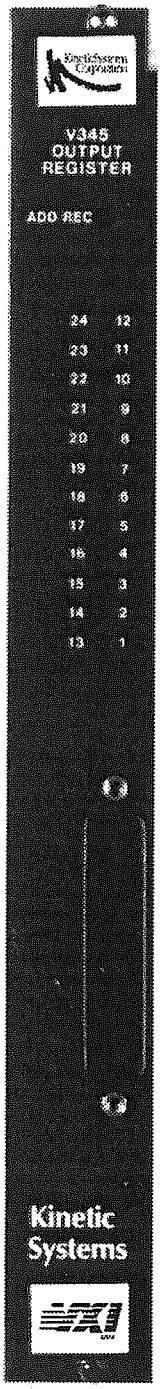
V345

Features

- **24 output circuits isolated from each other and ground**
- **Reed relay, optical isolator, and ac switch options available**
- **AC switch option includes zero-crossing network**
- **Front panel LEDs indicate state of all outputs**

Typical Applications

- **Test cells**
- **Driving relays, solenoids, lamps and other control devices**

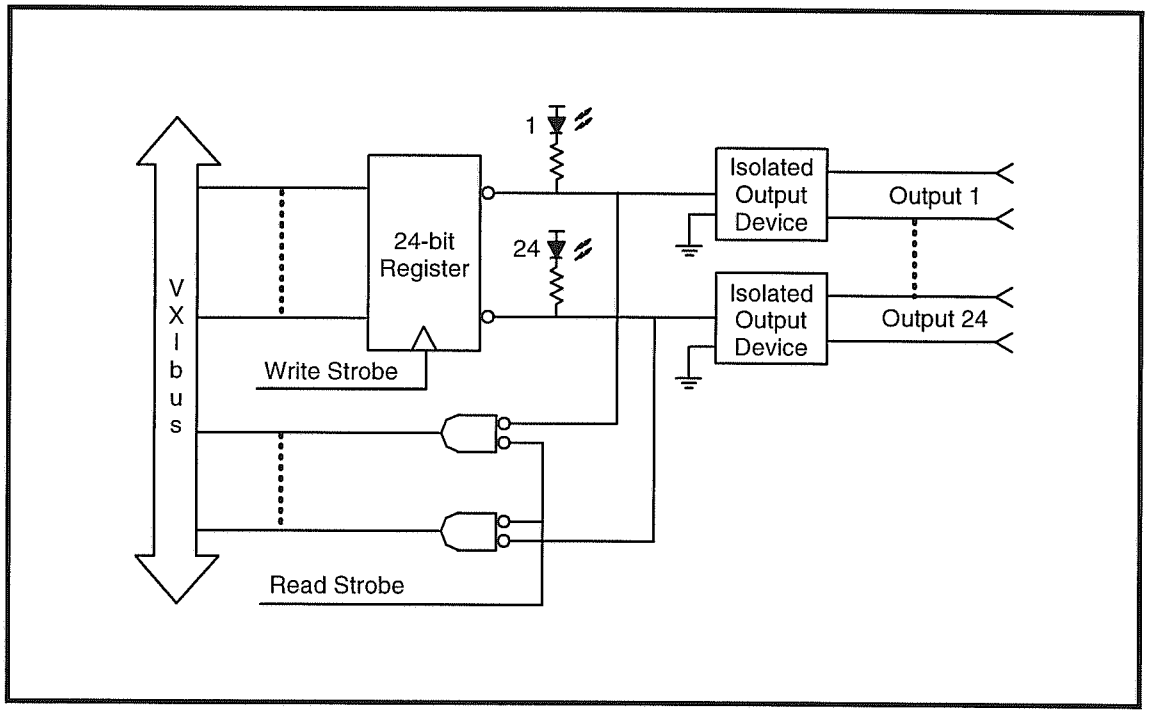


General Description *(Product specifications and descriptions subject to change without notice.)*

The V345 is a single-width, C-size, register-based, VXIbus module containing a 24-bit register that drives 24 output circuits. Module options are available with the output circuits composed of reed relays, optical isolators, or isolated ac switches. Each output option brings the output switches to a 50-contact "D" type connector on the module front panel. For all options, the maximum voltage, current, and (for the reed relay option) volt-ampere ratings must be observed. Appropriate external suppression must be provided for inductive loads.

Twenty-four light emitting diodes (LEDs) are provided on the front panel for visually monitoring the current state of all output circuits. Additionally, the output register can be read as well as written from software. With both read and write capabilities, "selective set" and "selective clear" functions can be performed by reading the register, performing the appropriate software sequence (logical AND, etc.) and then writing the output register.

The V345 supports both static and dynamic configuration. Access to the data is through memory locations indicated by the Offset Register within the VXIbus Configuration Register set, using A24/A16, D16 data transfers.



Item	Specification
Outputs	
Number of outputs	24, isolated
Output signal options	Reed relay, optical isolator, and ac switch
Output Ratings	
Reed Relay option	
Maximum open circuit voltage	100 V
Maximum current	0.5 A
Maximum switched load	10 VA
Output polarity	Either
Contact bounce	3 ms
Optical Isolator option	
Maximum open circuit voltage	30 V
Maximum ON current	10 mA
ON voltage drop	1 V
OFF current	Less than 1 μA
Output polarity	Collector positive with respect to emitter (Even I/O contacts positive, odd contacts negative)
AC Switch option	
Maximum open circuit voltage	200 V
Maximum On currect	0.5 A, 47-70 Hz
Minimum ON currect	0.01 A
On voltage drop	Less than 1.6 V
Output Connector Type	50P "D"
Mating Connector	KineticSystems Model 5934-Z1A
Power Requirements	
+ 5 V Reed Relay option	2.0 A, typical
+5 V All other options	1.9 A, typical
Environmental and Mechanical	
Temperature range	
Operational	0°C to 50 °C
Storage	-25 °C to +75 °C
Relative humidity	0 to 85%, non-condensing to +40 °C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V345-EA11 24-channel Isolated Digital Output; Reed relay outputs
Model V345-EB11 24-channel Isolated Digital Output; Optical isolator outputs
Model V345-EC11 24-channel Isolated Digital Output; AC switch outputs

Related Products

Model 5851-Bxyz Cable—50P "D" to Unterminated
Model 5851-Dxyz Cable—50S "D" to 50S "D"
Model 5851-Exyz Cable—50P "D" to 50S "D"
Model 5934-Z1A Connector—50S "D"

UNPACKING AND INSTALLATION

The Model V345 is shipped in a antistatic bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the operating environment.

UNPACKING AND INSTALLATION

The V345 represents one of 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device.) The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V345 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield. (Refer to FIGURE 1.)

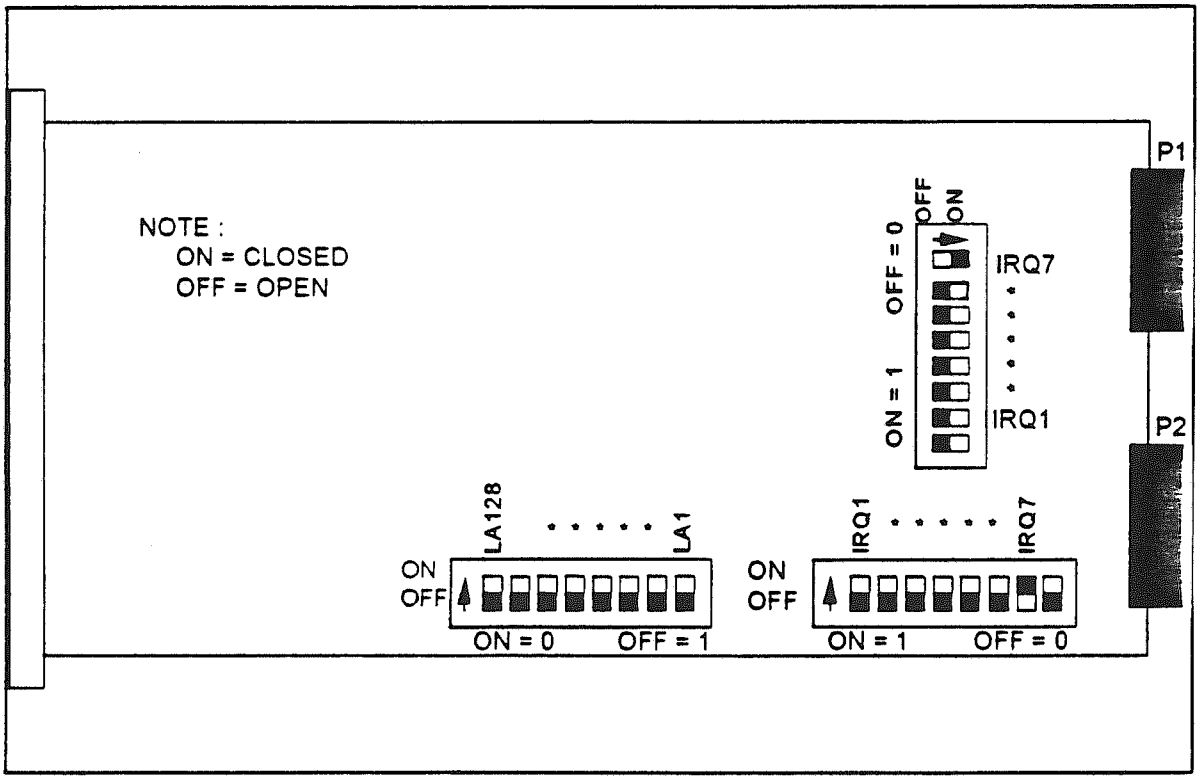


FIGURE 1 - V345 SWITCH LOCATIONS

The eight switches represent a binary combination of numbers that range from zero to 255. Use a scribe or other appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0	R

Bits 15 and 14 are set to "1" (VXI defined).
Bits 13 through 6 are user-selectable via the address switches LA128 - LA1.
Bits 5 through 0 are set to "0" to indicate a block of 64 bytes.

Module Insertion

The V345 is a C-sized, single width VXIbus module., It requires 1980 milliamperes of +5 volt power, and 10 cubic feet per minute of air flow to maintain stability. Except for Slot), it can be mounted in any unoccupied slot in a C-size VXIbus mainframe chassis.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE.

WARNING:
REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE.

To insure proper interrupt acknowledge cycles, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V345 and the Slot 0 Controller.

FRONT PANEL INFORMATION

LEDs

ADD_REC — This LED is illuminated when the Operational Registers are being accessed.

1 - 24 — These 24 LEDs indicate the state of each bit in the Output Register. If the LED is turned ON, then that bit is set to a "1."

CONNECTORS

The output signals of the V345 are available on a 50-pin "D" type subminiature connector (DD50P) on the module's front panel. The KineticSystems Model 5934-Z1A directly mates to this connector. Pin locations on the module's connector are detailed in Figure 2 on page ?, and the output pin assignments are defined in Table 1.

Table 1. Connector Pinout Assignments

17 Output Bit 9 (Neg)	33 Output Bit 17 (Neg)	50 Not Used
16 Output Bit 8 (Pos)	32 Output Bit 16 (Pos)	49 Not Used
15 Output Bit 8 (Neg)	31 Output Bit 16 (Neg)	48 Output Bit 24 (Pos)
14 Output Bit 7 (Pos)	30 Output Bit 15 (Pos)	47 Output Bit 24 (Neg)
13 Output Bit 7 (Neg)	29 Output Bit 15 (Neg)	46 Output Bit 23 (Pos)
12 Output Bit 6 (Pos)	28 Output Bit 14 (Pos)	45 Output Bit 23 (Neg)
11 Output Bit 6 (Neg)	27 Output Bit 14 (Neg)	44 Output Bit 22 (Pos)
10 Output Bit 5 (Pos)	26 Output Bit 13 (Pos)	43 Output Bit 22 (Neg)
9 Output Bit 5 (Neg)	25 Output Bit 13 (Neg)	42 Output Bit 21 (Pos)
8 Output Bit 4 (Pos)	24 Output Bit 12 (Pos)	41 Output Bit 21 (Neg)
7 Output Bit 4 (Neg)	23 Output Bit 12 (Neg)	40 Output Bit 20 (Pos)
6 Output Bit 3 (Pos)	22 Output Bit 11 (Pos)	39 Output Bit 20 (Neg)
5 Output Bit 3 (Neg)	21 Output Bit 11 (Neg)	38 Output Bit 19 (Pos)
4 Output Bit 2 (Pos)	20 Output Bit 10 (Pos)	37 Output Bit 19 (Neg)
3 Output Bit 2 (Neg)	19 Output Bit 10 (Neg)	36 Output Bit 18 (Pos)
2 Output Bit 1 (Pos)	18 Output Bit 9 (Pos)	35 Output Bit 18 (Neg)
1 Output Bit 1 (Neg)		34 Output Bit 17 (Pos)

PROGRAMMING INFORMATION

VMEbus/VXIbus Addressing

Of the defined VXIbus Configuration Registers, the V345 implements those required for register-based devices. The V345 also contains a set of Operational Registers to monitor and control the functional aspects of the device. Both register sets are described in this section.

Access to the Configuration Registers for all VXIbus modules is available through the VMEbus short (A16) address space. The register addresses are located in the upper 16 kilobytes of the A16 address range ($C000_{16}$ to $FFFF_{16}$). The setting of the Logical Address switch, or the contents of the Logical Address Register (see below) are mapped into Address Lines A6 through A13, thereby establishing a base address for the module somewhere in the range of $C000_{16}$ to $FFC0_{16}$.

VXIbus Configuration Registers

Configuration Registers are required by the VXIbus specification so that the appropriate levels of system configuration can be accomplished. The Configuration Registers in the V345 are offset from the base, or Logical Address. **Note: the V345 only responds to these**

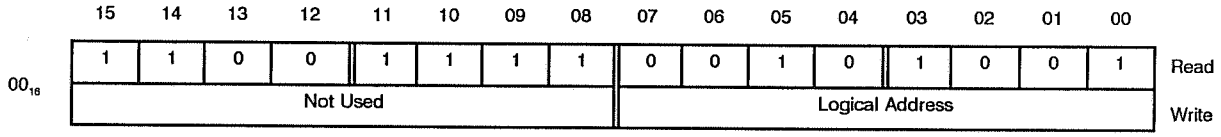
addresses if the Short Nonprivileged Access (29_{16}) or Short Supervisory Access ($2D_{16}$) Address Modifier Codes are set for the backplane bus cycle. Table 2 shows the applicable Configuration Registers present in the V345, their offset from the base address, and their Read/Write capabilities.

Table 2. Configuration Registers

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

ID/Logical Address Register

The format and bit assignments for the ID/Logical Address Register are as follows:



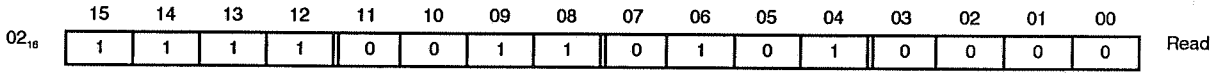
On READ transactions:

Bit(s)	Mnemonic	Meaning
15, 14	Device Class	This is a Register-Based device.
13, 12	Address Space Needs	This module requires the use of A16/A24 address space.
11 - 00	Manufacturer's ID	3881 ($F29_{16}$) for KineticSystems.

For WRITE transactions, bits 15 through eight are not used, and setting them has no effect on the V345. In Dynamically configured systems (i.e., the Logical Address switches were set to a value of 255), bits seven through zero are written with the new Logical Address value.

Device Type Register

The format and bit assignments for the Device Type Register are as follows:

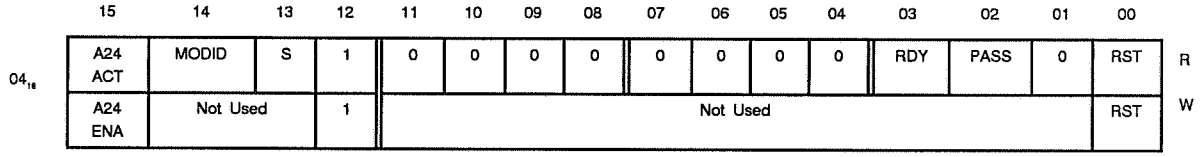


On READ transactions:

Bit(s)	Mnemonic	Meaning
15 - 12	Required Memory	The V345 requires 256 bytes of additional memory space.
11 - 00	Model Code	Identifies this device as Model V345 (345_{16}).

Status/Control Register

The format and bit assignments for the Status/Control Register are as follows:

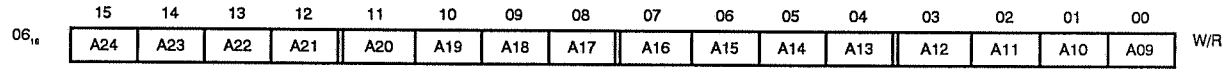


Bit(s)	Mnemonic	Meaning
15	A24 Enable	This bit is written with a "1" to enable A24 addressing and reset (to "0") to disable A24 addressing. **This bit must be set to "1" to allow access to the module's Operational Registers.** Reads of this bit indicate its current state. This bit is reset to "0" on power-up or the assertion of SYSRESET*.
14	MODID	This Read-Only bit is set to a "1" if the module is not selected with the MODID line on P2. A "0" indicates that the device is selected by a high state on the P2 MODID line.
13	Status	This Read-Only bit indicates the status of the last operational transaction to the V345. A "1" indicates the transaction completed successfully.
12	1	This Read/Write bit is included for compatibility with other KineticSystems VXIbus modules. It should always be written with a "1."
11 - 04	Not Used	When read, will return all "0s". These bits are ignored when written.
03	Ready	Along with Bit 02 (Passed), this Read-Only bit will appear as a "1" to indicate its readiness to accept operational commands.
02	Passed	See the Ready bit description.
01	Not Used	Read as "0" and ignored on write transactions.

00	Reset	This Read/Write bit controls the Soft Reset condition within the V345. While the Soft Reset condition is enabled (by writing a "1" to this bit position), any further access to the Operational Registers (see below) is inhibited. The output bit patterns from the module are maintained in the state they were in just prior to the Soft Reset being enabled. This bit can be reset by writing a "0", on power-up or the assertion of SYSRESET*.

Offset Register

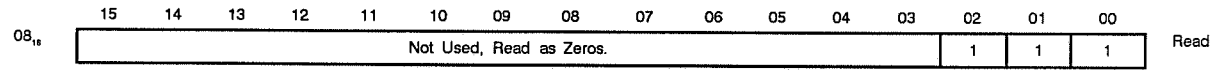
The format and bit assignments for the Offset Register are as follows:



This Read/Write register defines the base address of the V345's Operational Registers. These 16 bits contain the 16 most significant bits of the module's A24 space register addresses. The register is reset to an all "0" condition on power-up or the assertion of SYSRESET*, and is written with the appropriate value under program control.

Interrupt Attribute Register

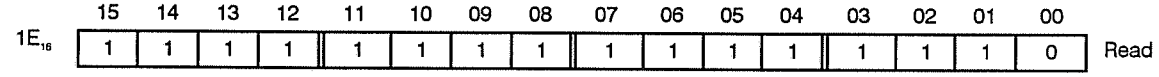
The format and bit assignments for the Interrupt Attribute Register are as follows:



Bit(s)	Mnemonic	Meaning
15 - 03	Not Used	These bits are not used by the V345, and are read as zeros.
02	Intr Control	The V345 does not have any Interrupt Control capabilities.
01	Intr Handler	The V345 does not have Interrupt Handler capabilities.
00	Intr Status	The V345 does not have an Interrupt Status register.

Subclass Register

The format and bit assignments for the Subclass Register are as follows:



Bit(s)	Mnemonic	Meaning
15	Extended Device	"1" indicates this to be a VXIbus defined Extended Device.

14-00 Register-Based — $7FFE_{16}$ indicates this to be an Extended register-based Device.

Operational Registers

The Operational Registers are the channels through which the output data patterns of the V345 are controlled. For compatibility with other KineticSystems VXIbus modules in this series, these registers are positioned in VMEbus Standard Address (A24) space. The base address for these registers is defined by the contents of the Offset Register within the Configuration Register set (see page 8).

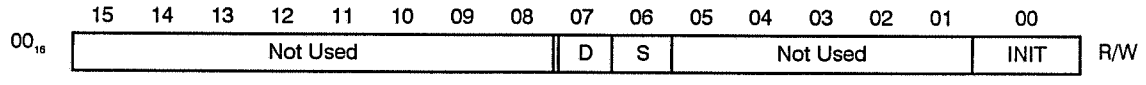
Prior to gaining access to the Operational Registers, the A24 Enable bit (bit 15) must be set in the Status/Control Register (see page 7). **Note: The V345 will only respond to these addresses if the Standard Nonprivileged Data Access (39_{16}), Standard Nonprivileged Program Access ($3A_{16}$), Standard Supervisory Data Access ($3D_{16}$), or Standard Supervisory Program Access ($3E_{16}$) Address Modifier Codes are set for the bus cycle(s).**

Of the 256 bytes requested by the setting of the Device Type register in the Configuration Register set, only ten bytes are used. (256 is the minimum number of bytes that can be requested through the Device Type register.) Table 3 shows the applicable Operational Registers present in the V345, their offset from the base A24 address, and their Read/Write capabilities.

Table 3. Operational Registers

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	Diagnostic Register
10_{16}	Write Only	Write Output Register (High)
12_{16}	Write Only	Write Output Register (Low)
16_{16}	Read Only	Read Output Register (Low)
18_{16}	Read Only	Read Output Register (High)

Diagnostic Register



Bit(s)	Mnemonic	Meaning
15 - 08	Not Used	On Read transactions, these bits return an all "0" pattern. On Write transactions, these bits are ignored by the module.
07	Diagnostic	When this bit is set to a "1", the last register access to the Operational Register (offsets 10_{16} through 18_{16}) was valid.

06	Status	When this bit is set to a "1", the last register access to the Operational Register (offsets 10_{16} through 18_{16}) was accepted.
05 - 01	Not Used	These bits are ignored on writes and read as "0".
00	Initialize	Setting this bit to a "1" will only reset the Operational Register (offsets 10_{16} through 18_{16}). The Configuration and Diagnostic registers are unaffected.

WRITE OUTPUT REGISTER (HIGH)
WRITE OUTPUT REGISTER (LOW)

To write all 24-bits of the Output Register, a write to the HIGH register must be executed before a write to the LOW register. A write to the LOW register will set the output state for bits 1-16, while the HIGH register will set the state of bits 17-24. Writing a "1" will turn on the corresponding bit in the output pattern while writing a "0" will reset the corresponding bit.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
10_{16}	Not Used.								W24	W23	W22	W21	W20	W19	W18	W17	W
12_{16}	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W

READ OUTPUT REGISTER (LOW)
READ OUTPUT REGISTER (HIGH)

To read all 24 bits of the output register, a read to the LOW register must be executed prior to a read from the HIGH register. The LOW register reads the output states for channels 1 through 16, while the HIGH register indicates the states of output channels 17 through 24.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
18_{16}	Not Used.								R24	R23	R22	R21	R20	R19	R18	R17	R
16_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R

Table of Configuration Registers

OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	ID/Logical Address Register
02_{16}	Read Only	Device Type Register
04_{16}	Read/Write	Status/Control Register
06_{16}	Read/Write	Offset Register
08_{16}	Read Only	Attribute Register
$1E_{16}$	Read Only	Subclass Register

ID/LOGICAL ADDRESS REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	1	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1	Read
	Not Used								Logical Address								Write

DEVICE TYPE REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
02_{16}	1	1	1	1	0	0	1	1	0	1	0	1	0	0	0	0	Read

STATUS/CONTROL REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
04_{16}	A24 ACT	MODID	S	1	0	0	0	0	0	0	0	0	RDY	PASS	0	RST	R
	A24 ENA	Not Used		1	Not Used											RST	W

OFFSET REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
06_{16}	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A0 9	W/R

INTERRUPT ATTRIBUTE REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
08_{16}	Not Used, Read as Zeros.													1	1	1	Read

VXIbus SUBCLASS REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
$1E_{16}$	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	Read

Table of Operational Registers

A24 OFFSET	READ/WRITE CAPABILITY	REGISTER NAME
00_{16}	Read/Write	Diagnostic Register
10_{16}	Write Only	Write Output Register (High)
12_{16}	Write Only	Write Output Register (Low)
16_{16}	Read Only	Read Output Register (Low)
18_{16}	Read Only	Read Output Register (High)

DIAGNOSTIC REGISTER

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
00_{16}	Not Used								D	S	Not Used					INIT	R/W

WRITE OUTPUT REGISTER (HIGH)
WRITE OUTPUT REGISTER (LOW)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
10_{16}	Not Used.								W24	W23	W22	W21	W20	W19	W18	W17	W
12_{16}	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	W2	W1	W

READ OUTPUT REGISTER (LOW)
READ OUTPUT REGISTER (HIGH)

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
18_{16}	Not Used.								R24	R23	R22	R21	R20	R19	R18	R17	R
16_{16}	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R